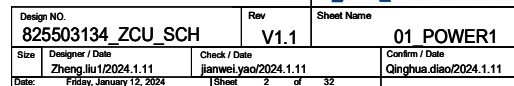
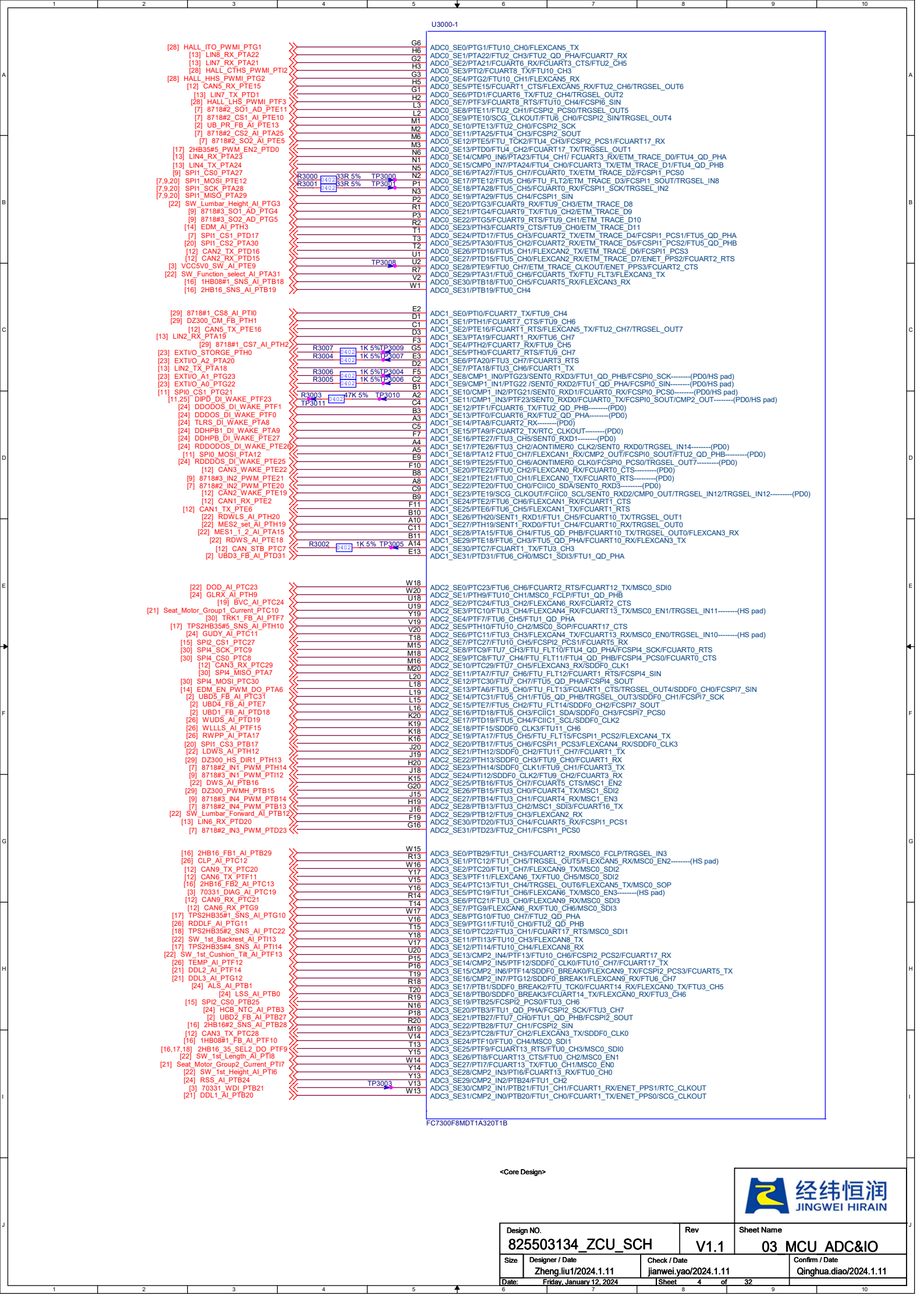


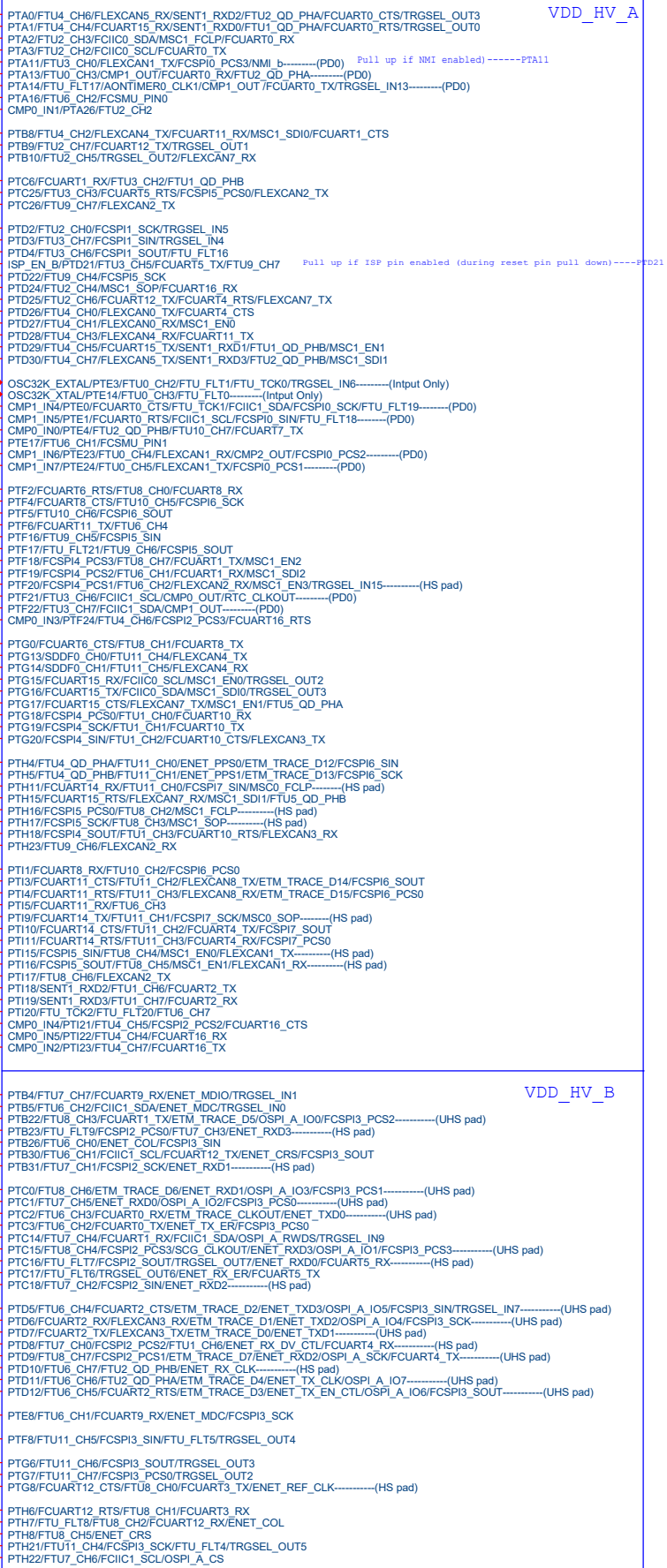
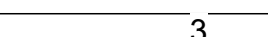
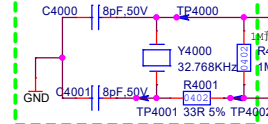
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项目编号:		AP238018		项目经理:		张红玲			
LAYOUT工程师:		付晶晶		应用工程师:		刘铮/冯成民			
输入信息:									
Input Information:									
输入时间:		2024-01-11		PCB ERP Number:		825503134			
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DXF文件名称:		825503134_BCM_DXF				DXF状态:			
PCB层数:		6 Layers		PCB基材:		FR4			
表面处理:		HASL		板厚:		1.6mm+/-0.14			
外层铜厚:		50um		1和2层间距:		0.16mm			
2和3层间距:		0.5mm		3和4层间距:		0.24mm			
其他要求:		-							
输出信息:									
Output Information:									
LAYOUT文件名称:		825503134_BCM_LAYOUT_brd				版本:		V1.1	
DXF文件名称:		825503134_BCM_DXF							
emp/emn文件名称:		NA							
Gerber文件名称:		TOP.art Soldermask_Top.art Drill_Dimention.art GND.art Soldermask_Bot.art Drill_Dimention.pdf PWR.art Silkscreen_Top.art BOT.art Silkscreen_Bot.art Assembly_Top.art Assembly_Bot.art							
Drill文件名称:		Ger_Con_Drill.drl							
Route文件名称:		Ger_Con_Route.rou							
其他输出:		-							
需要注意的问题:									
Need to Attention ! :									
敏感信号线:									
易干扰信号线:		LIN BUS							
射频信号线:		LF driver antenna terminal							
等长信号线:		-							
差分对:		CAN BUS							
大电流:									
其他:		NA							
其他:		NA							
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其他详见原理图内部信息。 如有未尽事宜, 请和应用工程师沟通。									
Design NO. 825503134_ZCU_SCH				Rev V1.1		Sheet Name 00_INFORMATION			
Size Zheng.liu1/2024.1.11		Check / Date jianwei.yao/2024.1.11		Confirm / Date Qinghua.diao/2024.1.11					
Date: Friday, January 12, 2024				Sheet 1 of 32					

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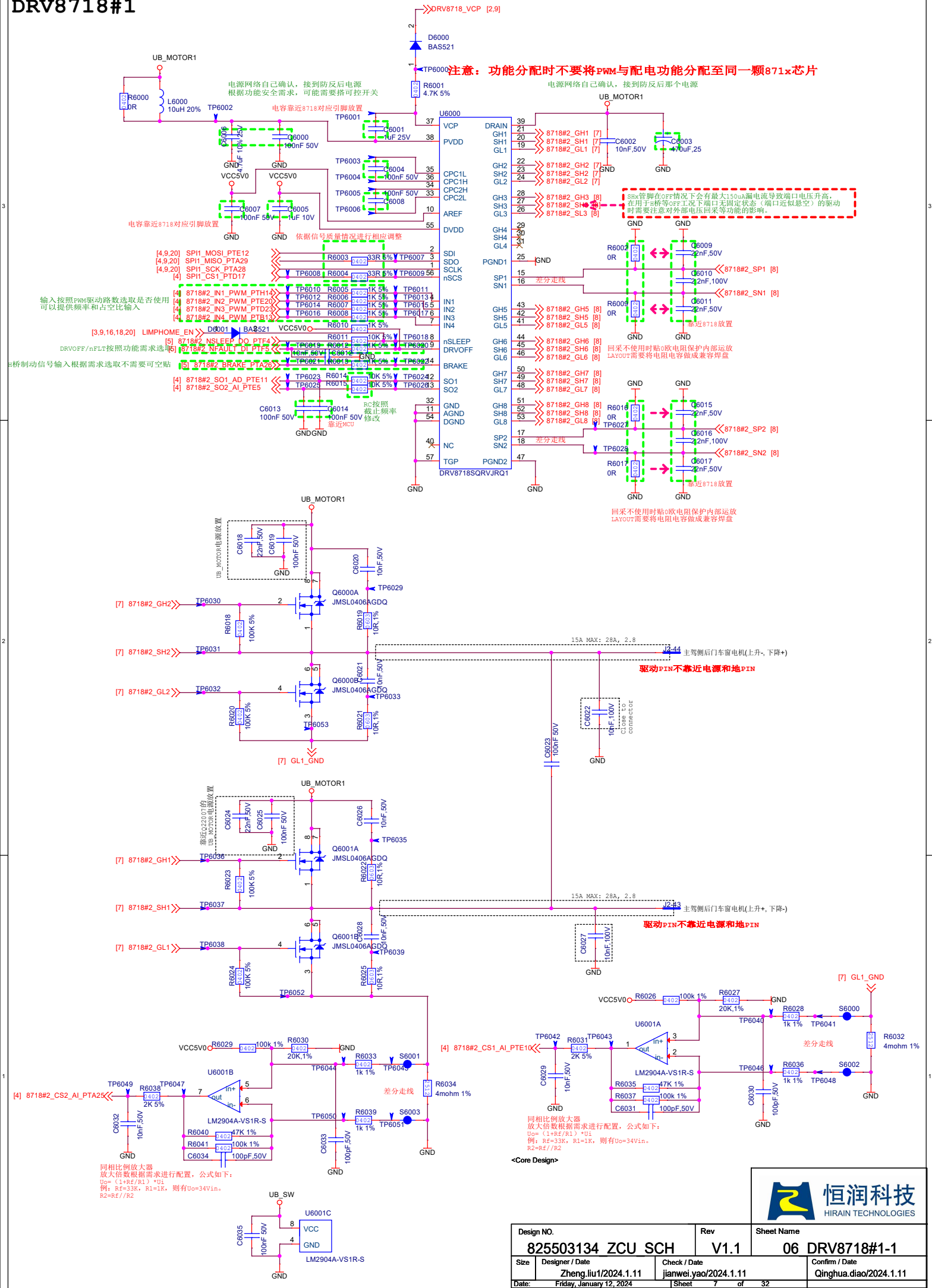
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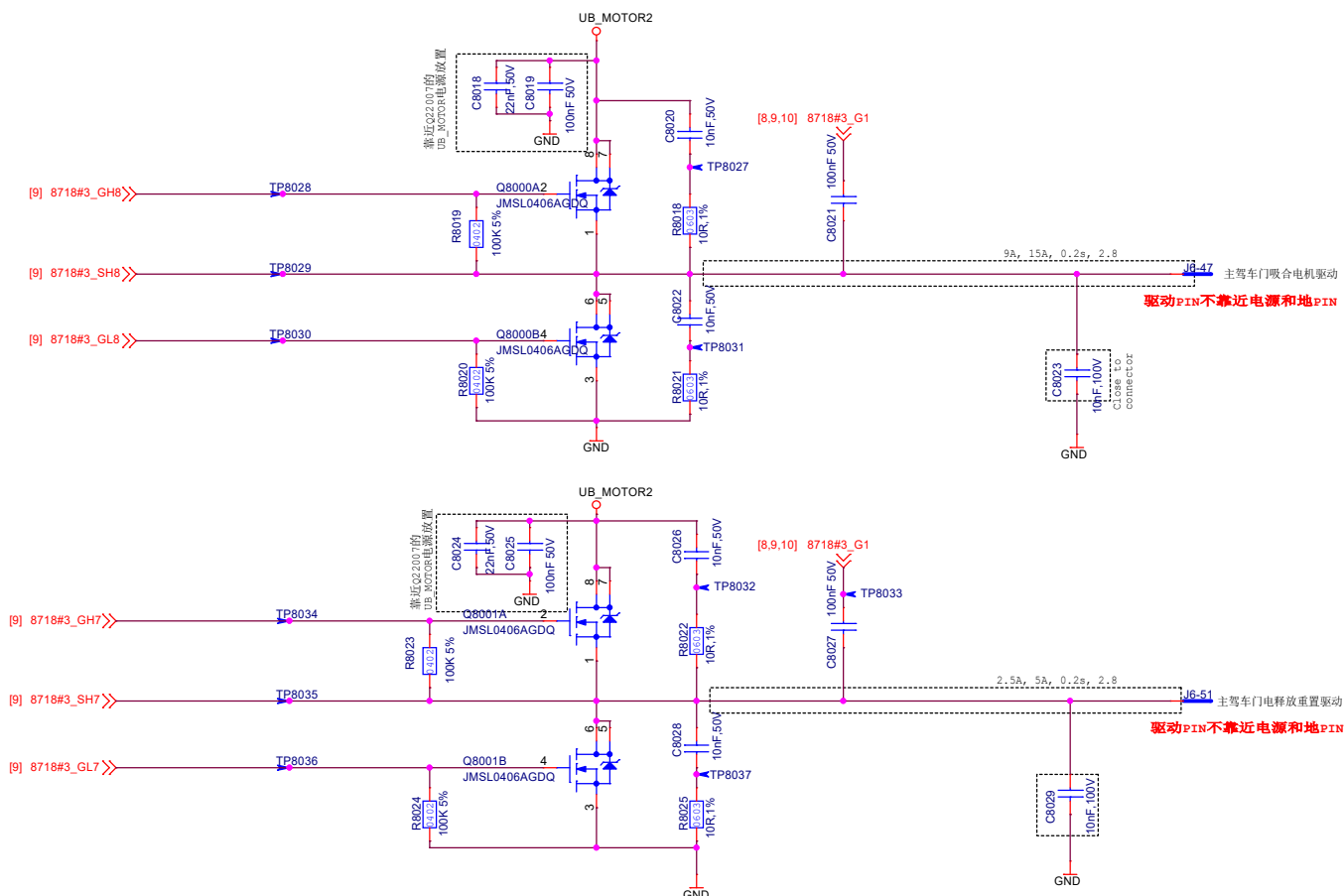
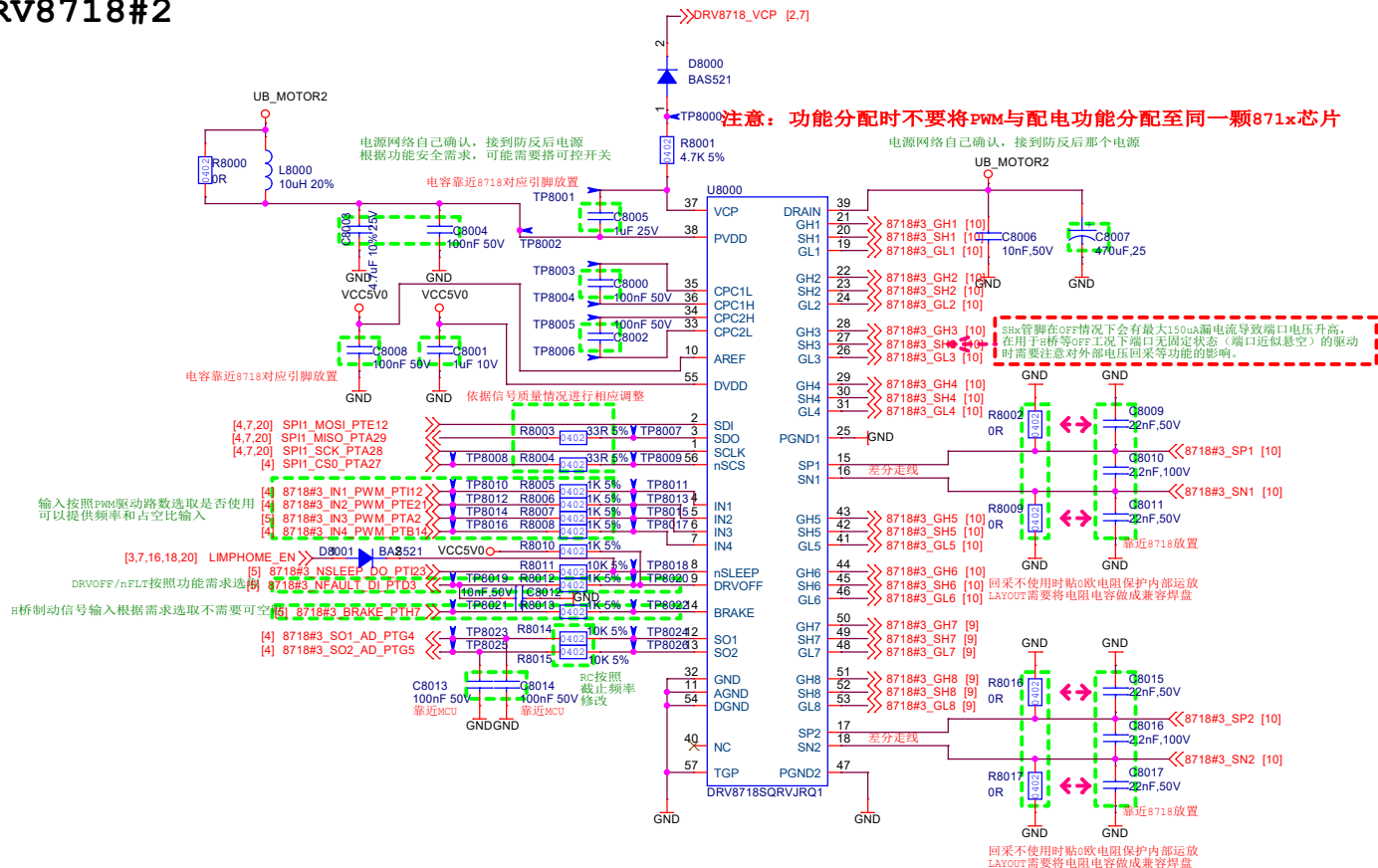


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Date:	Friday, January 12, 2024	Sheet	5	of 32

DRV8718#1



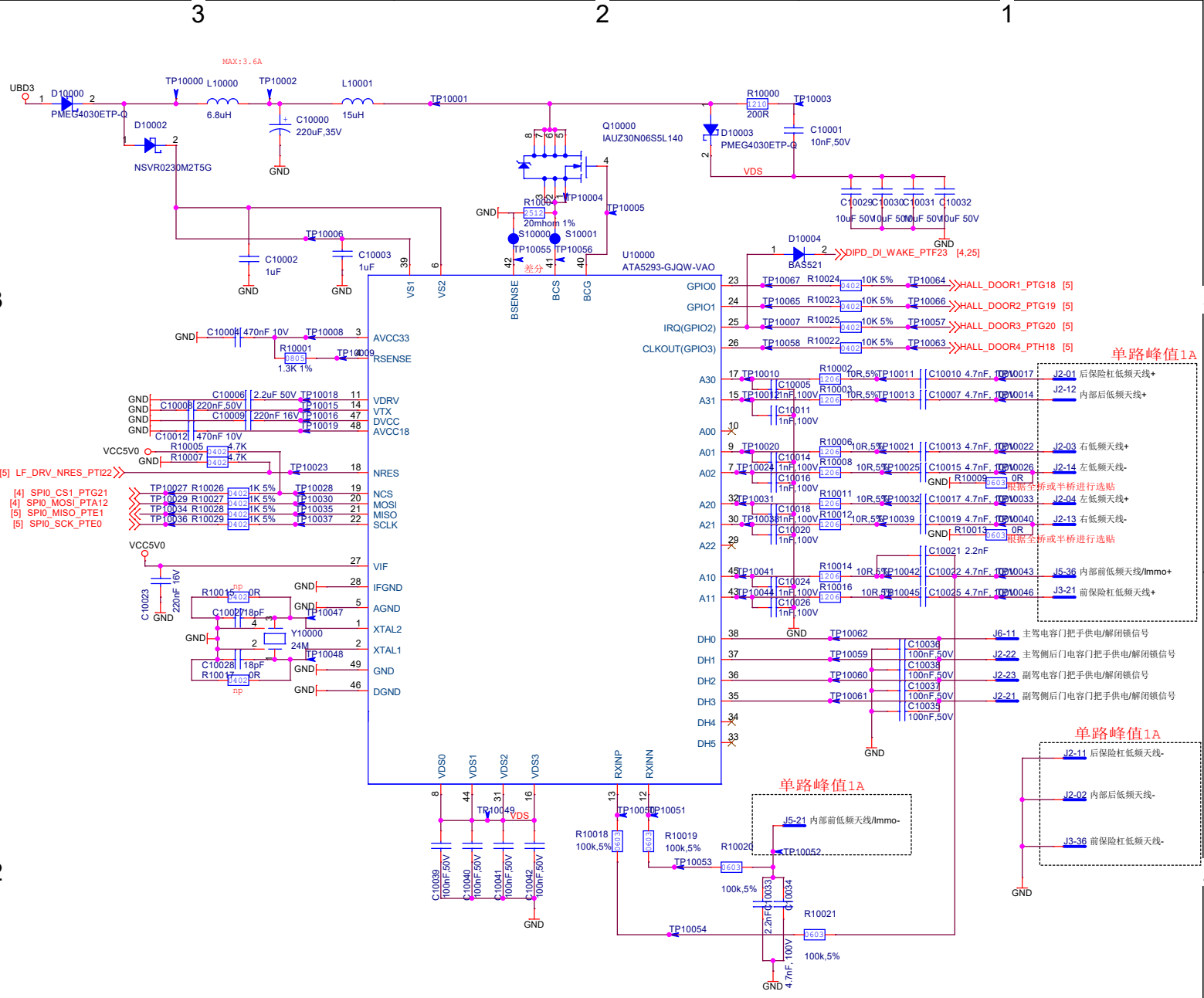
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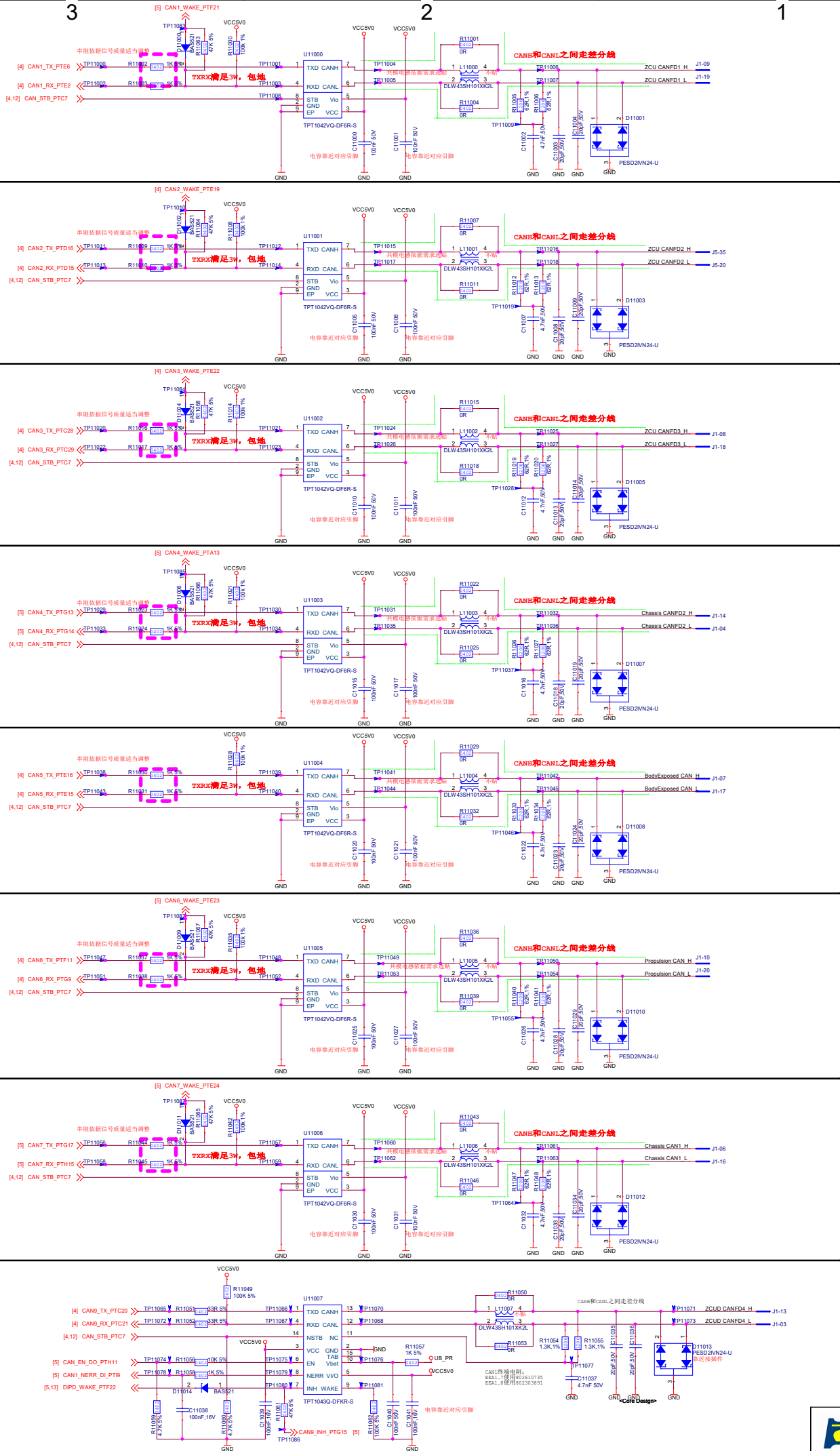
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825503134 ZCU SCH		V1.1		08 DRV8718#2-1	
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Custom	Zheng.liu/2024.1.11	jianwei.yao/2024.1.11		Qinghua.diao/2024.1.11	
Date:	Friday, January 12, 2024	Sheet	9 of 32		



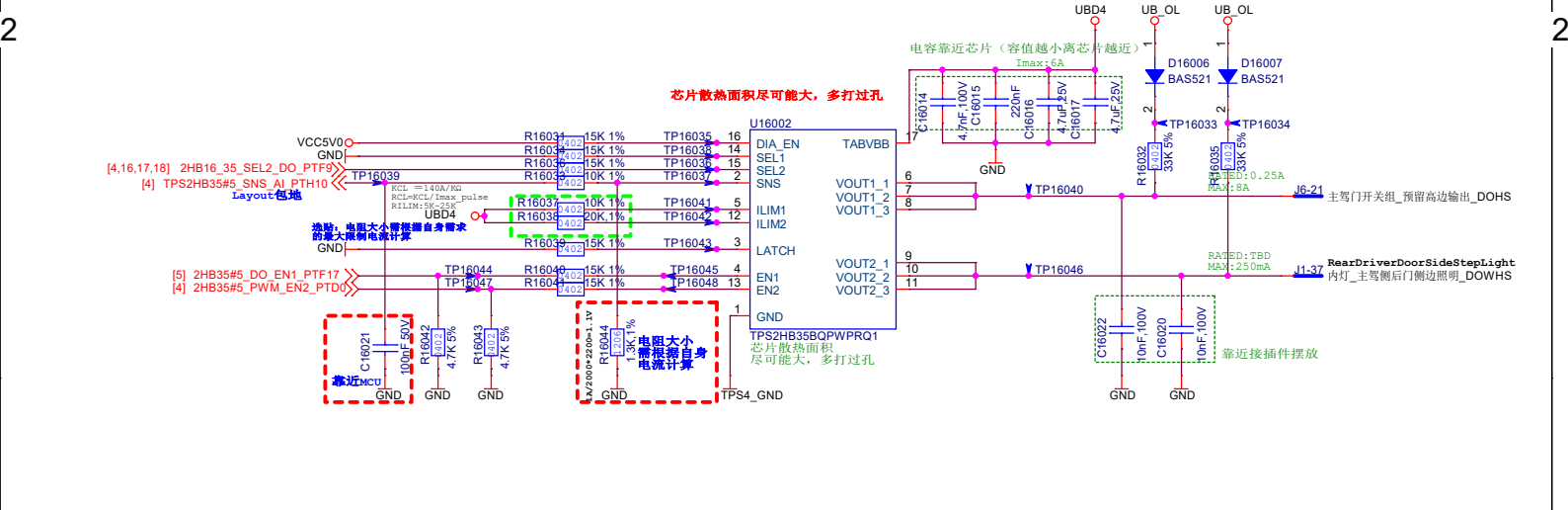
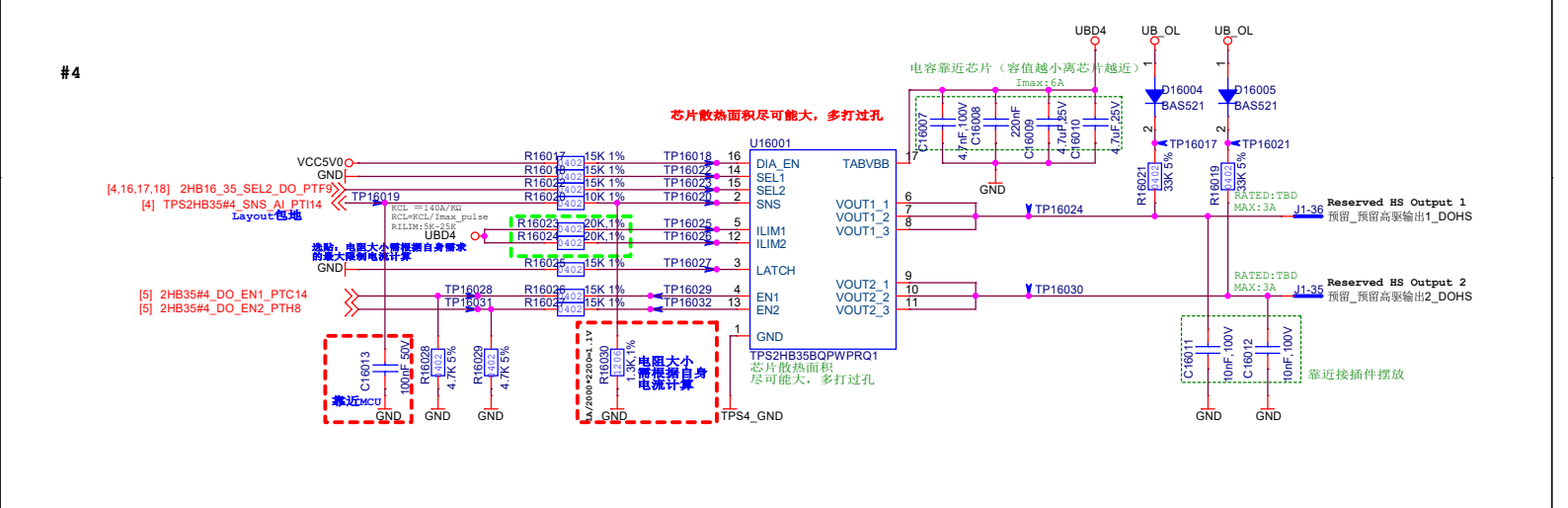
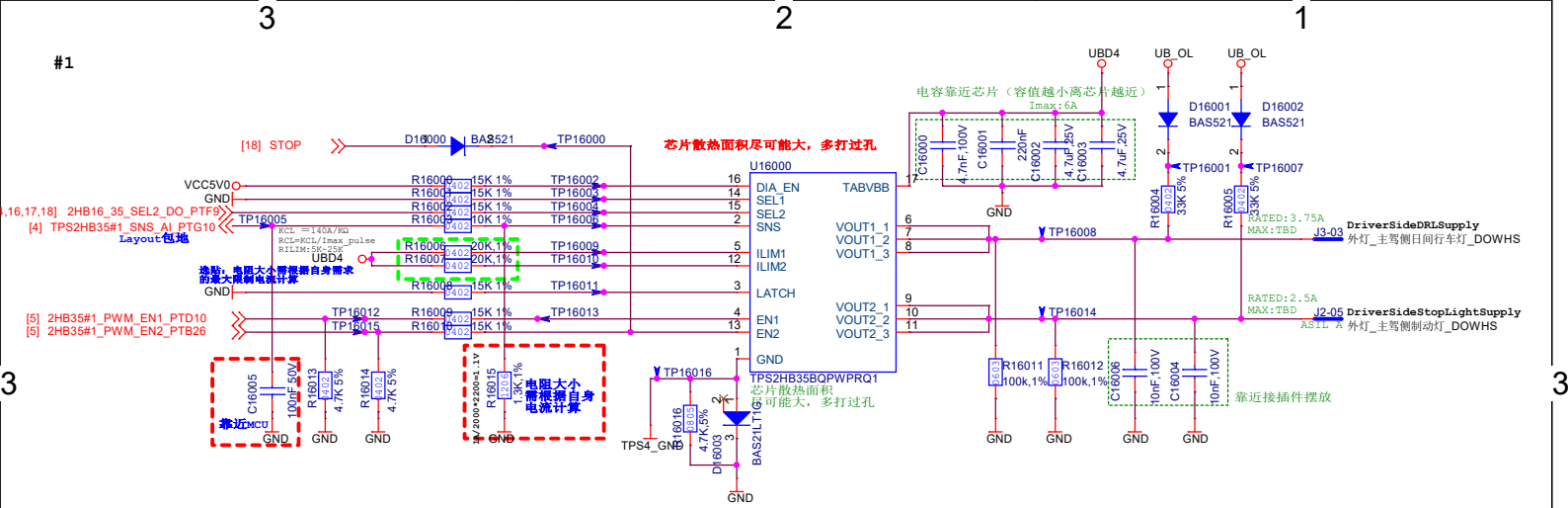
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Size	Designer / Date Zheng.liu/2024.1.11	Check / Date jianwei.yao/2024.1.11	Confirm / Date Qinghua.diao/2024.1.11	
Date: Friday, January 12, 2024	Sheet	14	of	32

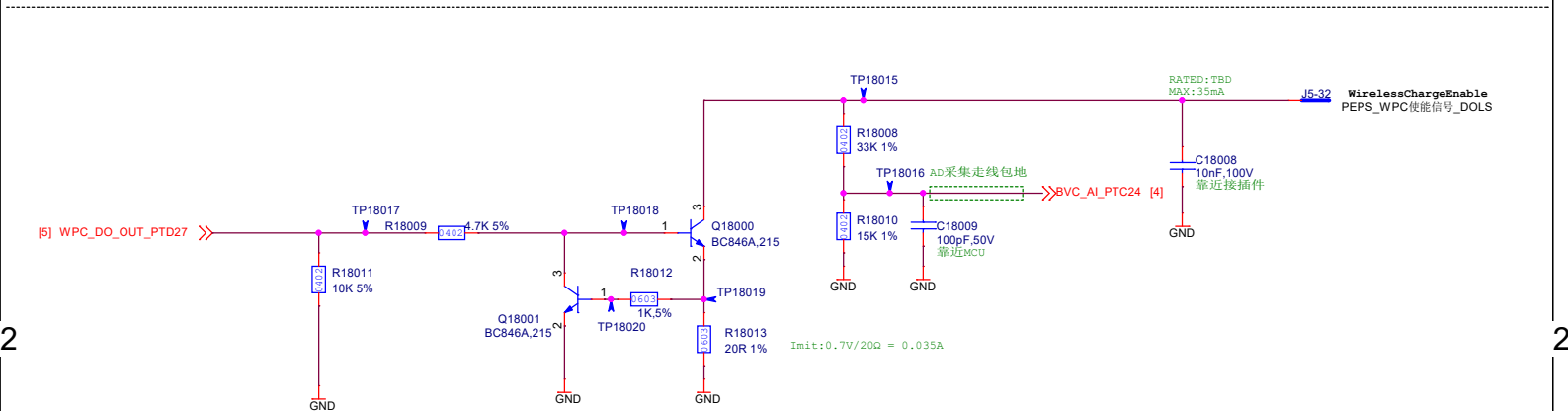


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Design NO. 825503134_ZCU_SCH		Rev V1.1	Sheet Name 16_HS_TPS2HB35
Size Zheng.liu1/2024.1.11	Check / Date jianwei.yao/2024.1.11	Confirm / Date Qinghua.diao/2024.1.11	
Date Monday, January 15, 2024	Sheet 17	of 32	

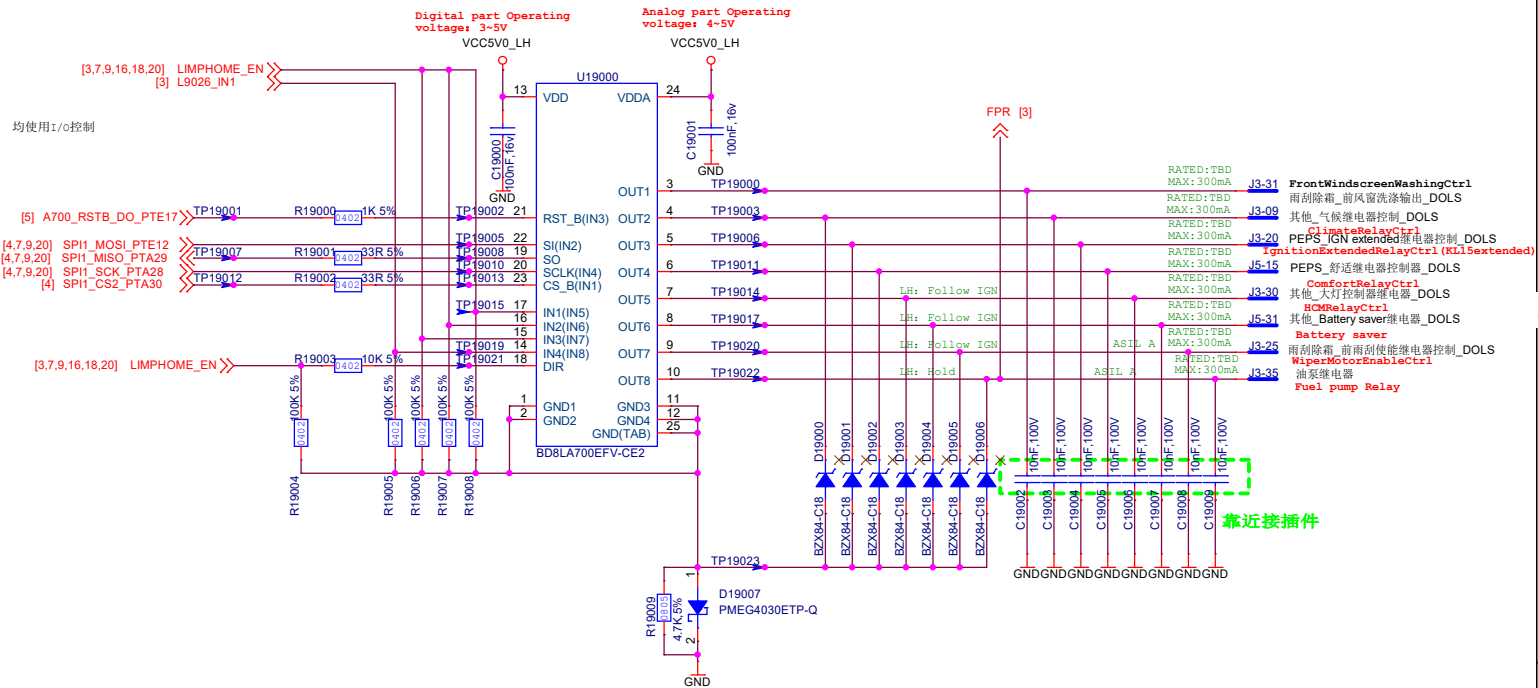
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825503134_ZCU_SCH		V1.1		17_HS_VNQ9025	
Size	Designer / Date	Check / Date			Confirm / Date
	Zheng.liu/2024.1.11	jianwei.yao/2024.1.11			Qinghua.diao/2024.1.11
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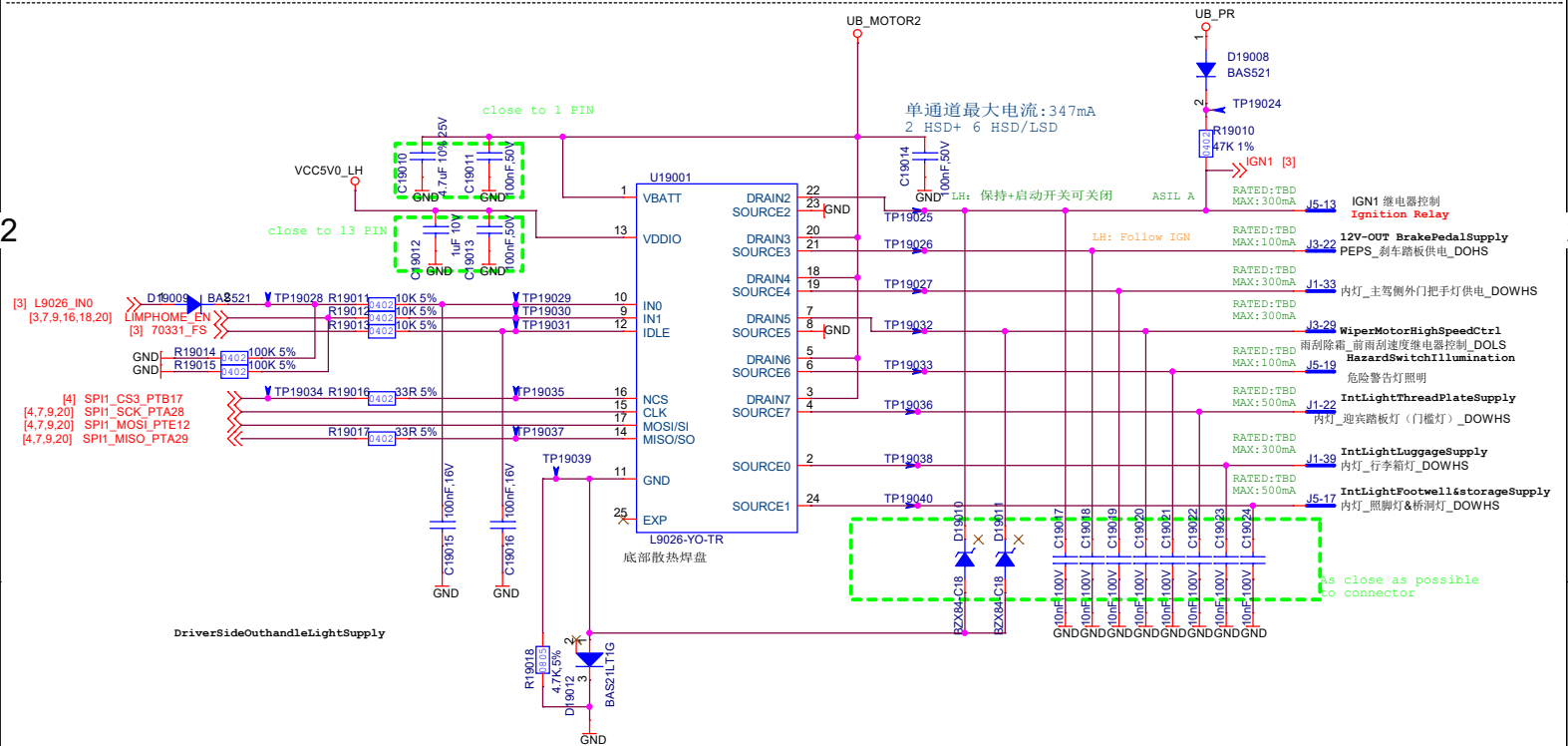
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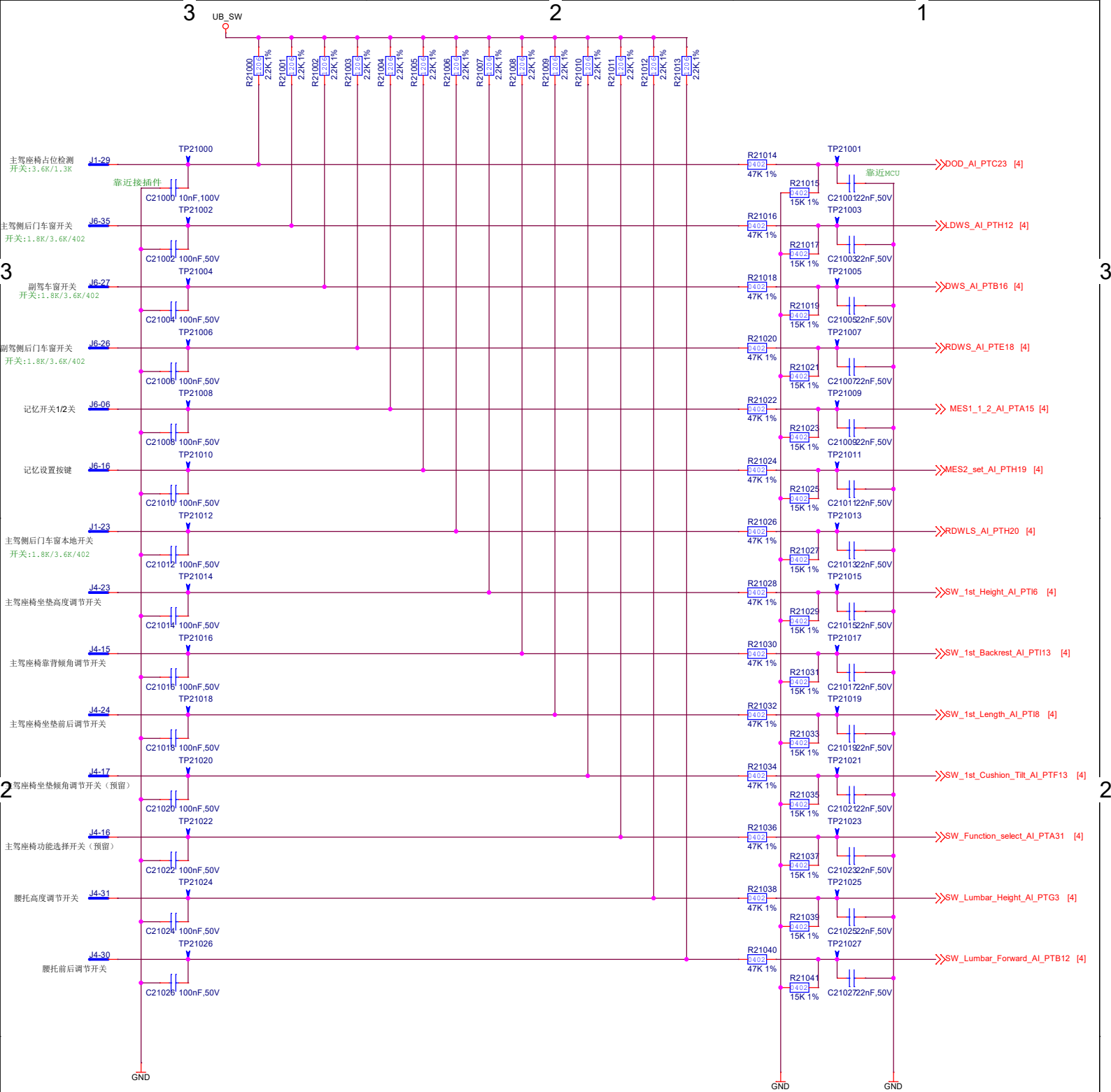


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Size	Designer / Date Zheng.liu/2024.1.11	Check / Date jianwei.yao/2024.1.11	Confirm / Date Qinghua.diao/2024.1.11	
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1. DIR管脚是低驱驱动模式选择管脚，拉低时是SPI控制，此时要给RST_B管脚一个高信号（或者直接拉高），DIR管脚拉高时候是直驱模式，symbol中括号里的输入对应相应的输出，高有效。
2. 使用SPI模式时候，可以直接控制8个通道的输出，14~17PIN脚（IN1~IN4）管脚可以不用。



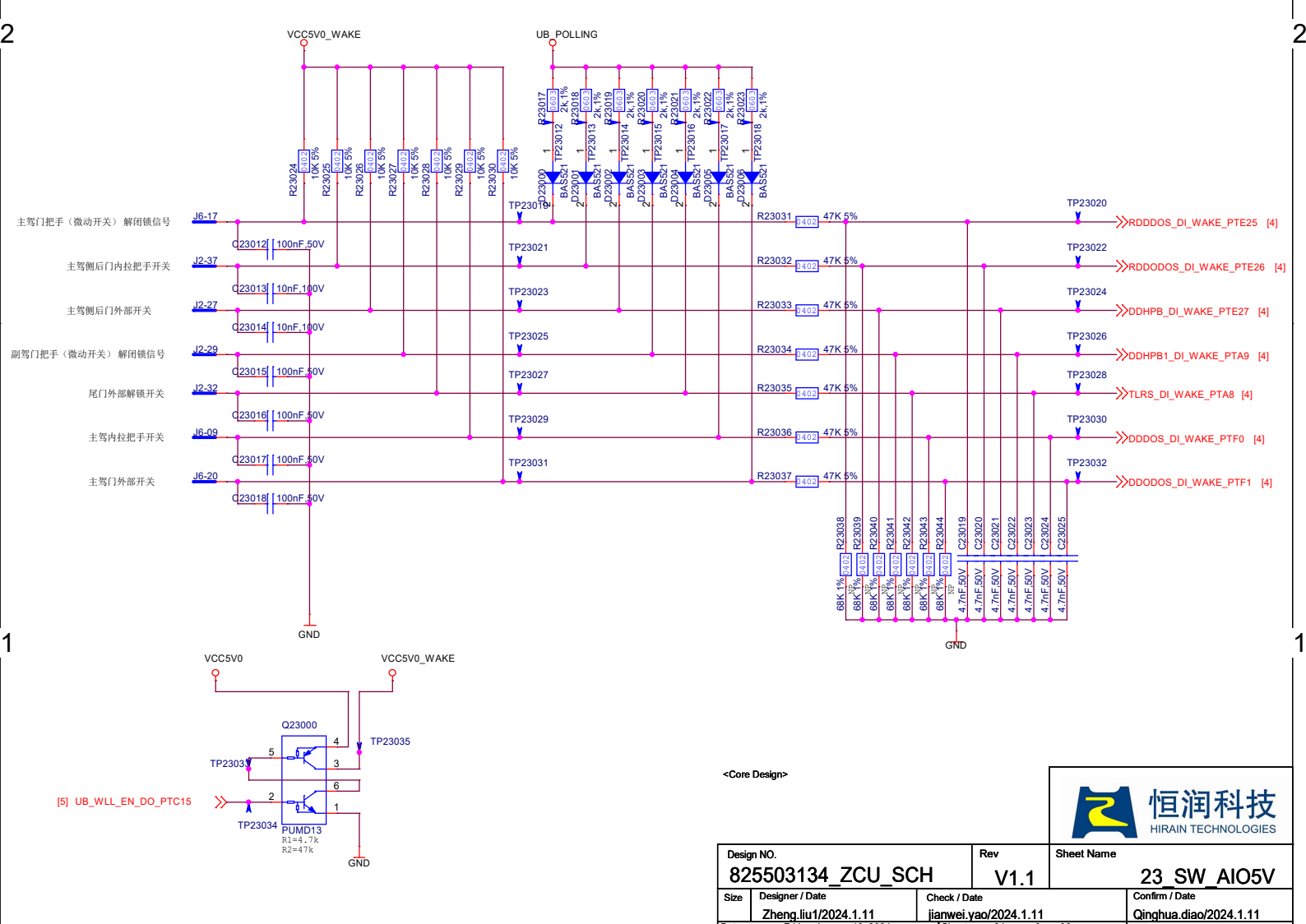
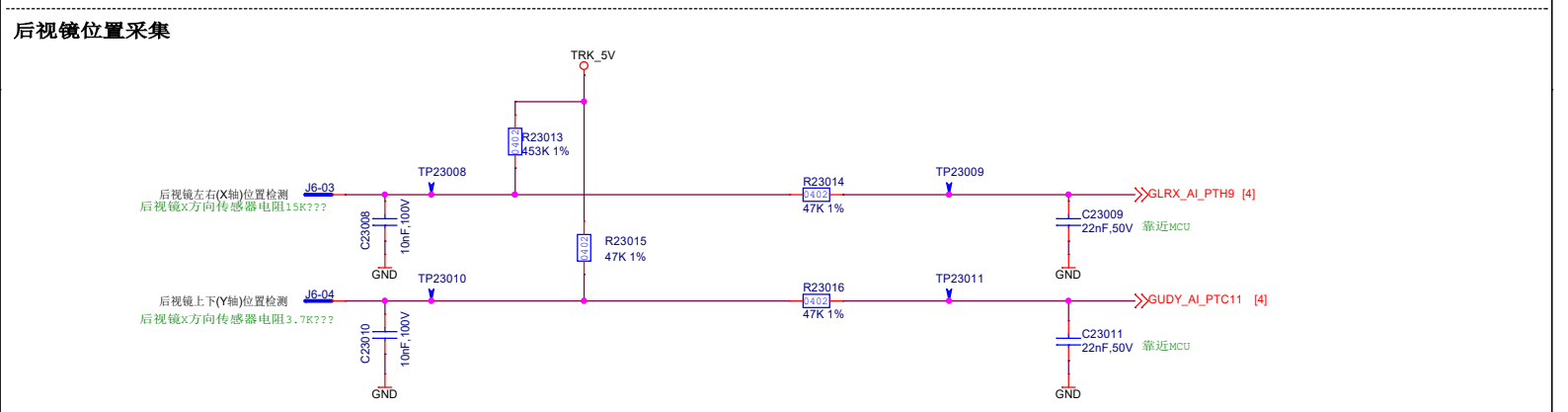
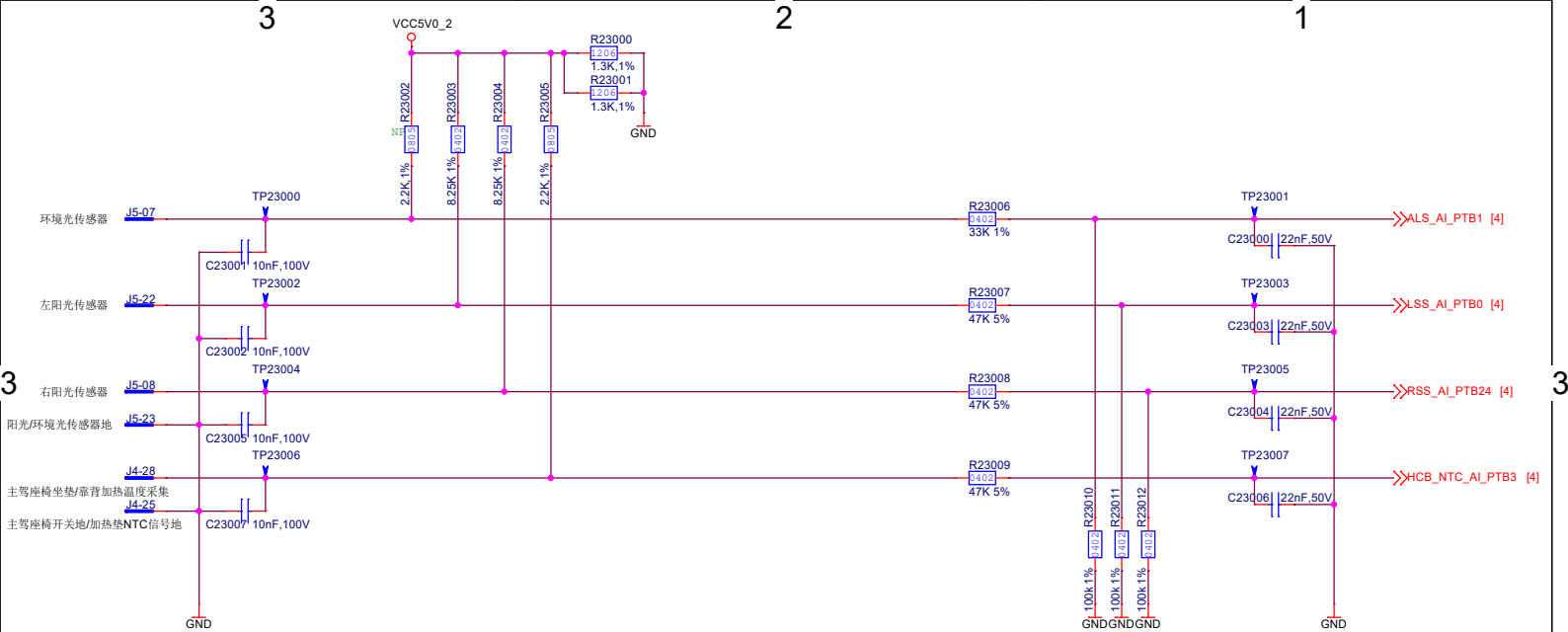


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Design NO. 825503134_ZCU_SCH		Rev V1.1	Sheet Name 21_SW_AI12V#1
Size Custom	Designer / Date Zheng.liu1/2024.1.11	Check / Date jianwei.yao/2024.1.11	Confirm / Date Qinghua.diao/2024.1.11
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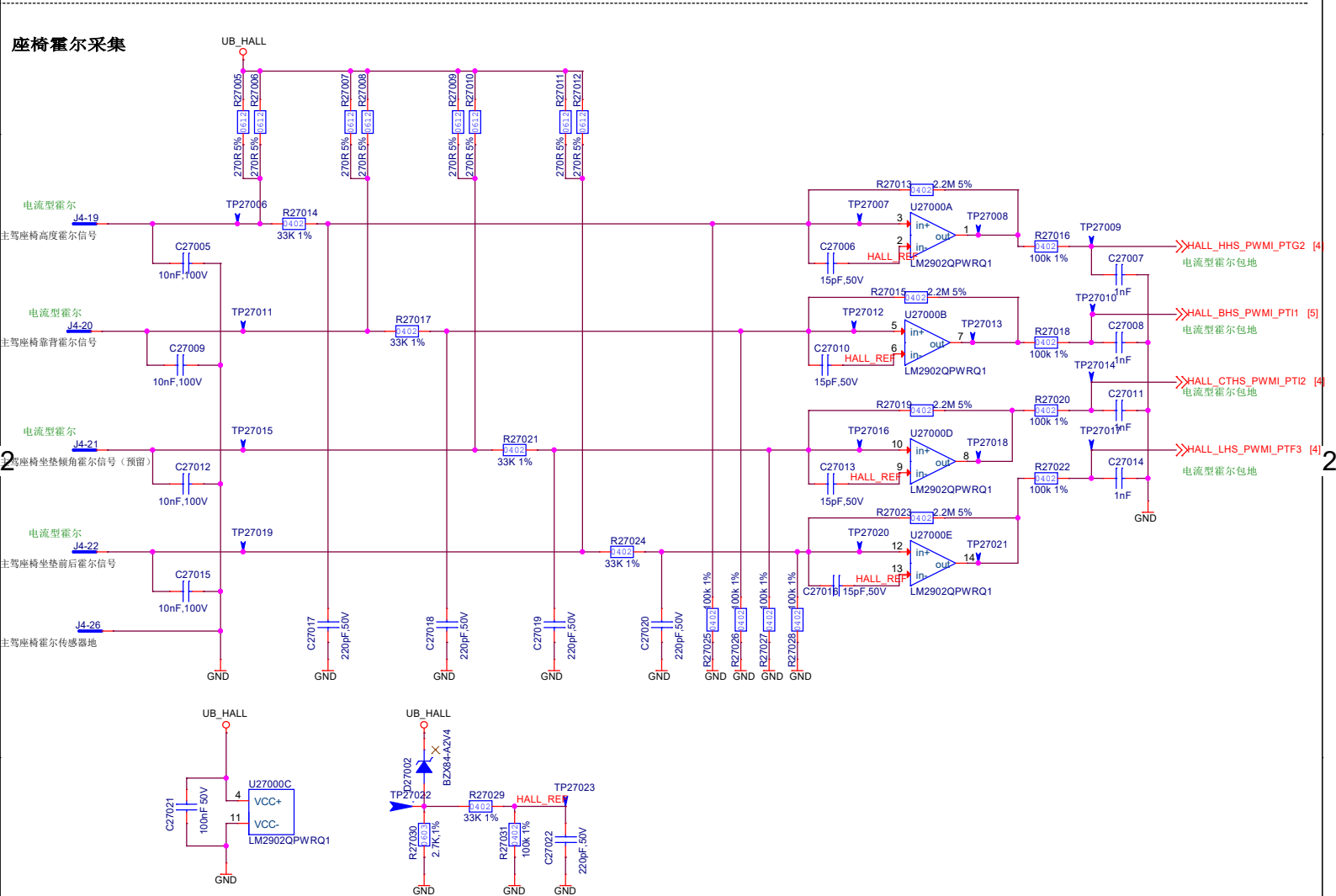
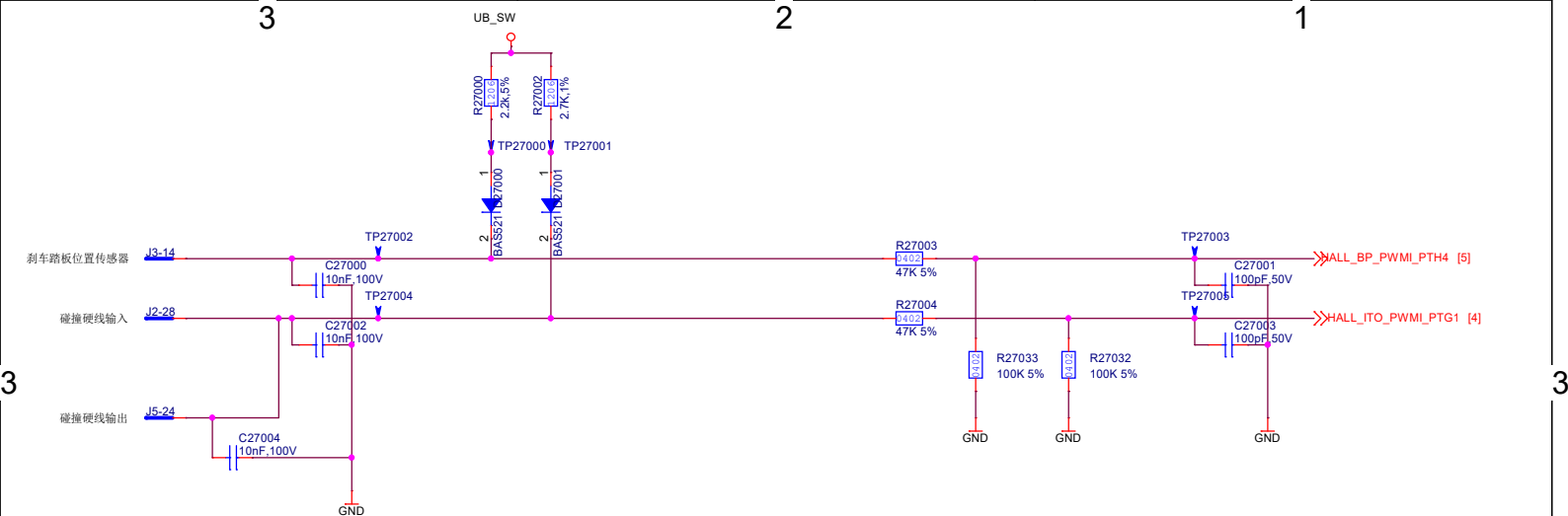
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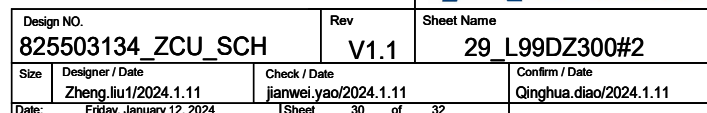
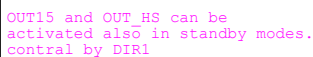
恒润科技
HIRAIN TECHNOLOGIES

Design NO. 825503134_ZCU_SCH			Rev V1.1	Sheet Name 26_NA	
Size	Designer / Date Zheng.liu1/2024.1.11	Check / Date jianwei.yao/2024.1.11		Confirm / Date Qinghua.diao/2024.1.11	
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Size	Designer / Date Zheng.liu/2024.1.11	Check / Date jianwei.yao/2024.1.11	Confirm / Date Qinghua.diao/2024.1.11	
Date:	Friday, January 12, 2024	Sheet	29	of 32



[illegible]

12345678910											
A	Debug Information									A	
	位号	网络名称	描述								
B	TP1000	UBD1	Power_Window							B	
	TP1001	UBD2	Power_Lock								
C	DP2000	UBD3	Power_Exterior Light1							C	
	TP1003	UBD4	Power_Exterior Light2								
D	TP1004	UBD5	Power_Seat							D	
	DP2001	GND	GND								
E	DP2002	GND	GND							E	
	TP2000	UB_PR	12V Logic Power								
F	TP2010	VCC5V0	5V Logic Power							F	
	TP2016	VCC1V5	1.5V Logic Power								
G										G	
H										H	
I										I	
J										J	
K										K	
L										L	
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R	R										
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Size	Designer / Date Zheng.liu1/2024.1.11	Check / Date jianwei.yao/2024.1.11	Confirm / Date Qinghua.diao/2024.1.11	
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