

PCB Layout Information

项目名称:	吉利ZCU_L技术研发项目		
项目编号:	AP238018	项目经理:	张红玲
LAYOUT工程师:	付晶晶	应用工程师:	刘铮/冯成民

输入信息:
Input Information:

输入时间:	2024-05-11	PCB ERP Number:	825503134
原理图名称:	825503134_ZCU_SCH	版本:	V1.2
Shematics Name :		Version:	
DXF文件名称:	825503134_BCM_DXF	DXF状态:	
DXF File Name:		DXF State:	
PCB层数:	6 Layers	PCB基材:	FR4
PCB Layer Number:		PCB Base Material:	
表面处理:	HASL	板厚:	1.6mm+/-0.14
Surface Handing:		Thickness:	
外层铜厚:	50um	1和2层间距:	0.16mm
Finished Copper Thickness:		Layer1 to Layer2 :	
2和3层间距:	0.5mm	3和4层间距:	0.24mm
Layer2 to Layer3 :		Layer3 to Layer4 :	
其他要求:	-		
Other :			

输出信息:
Output Information:

LAYOUT文件名称:	825503134_BCM_LAYOUT_brd	版本:	V1.2
LAYOUT File Name:		Version:	
DXF文件名称:	825503134_BCM_DXF		
DXF File Name:			
emp/emn文件名称:	注意: 导出三维信息时, 输入和输出文件		
emp/emn File Name:	都为英文字符, 否则不能正确生成。		
Gerber文件名称:	TOP.art Soldermask_Top.art Drill_Dimention.art GND.art Soldermask_Bot.art Drill_Dimention.pdf PWR.art Silkscreen_Top.art Gerber File Name: BOT.art Silkscreen_Bot.art Assembly_Top.art Assembly_Bot.art		
Drill文件名称:	Ger_Con_Drill.drl		
Drill File Name:			
Route文件名称:	Ger_Con_Route.rou		
Route File Name:	注意: 如果PCB上有异形孔, 请生成ROUTE文件。		
其他输出:	-		
Other :			

需要注意的问题:
Need to Attention ! :

敏感信号线: Sensitive Signal Line:	
易干扰信号线: Interference Signal Line:	LIN BUS
射频信号线: RF Signal Line:	LF driver antenna terminal
等长信号线: Same Delay Signal Line :	-
差分对: Differetial Signal Line:	CAN BUS
大电流: High Current:	
其他: Other :	NA
其他: Other :	NA

DV BOM

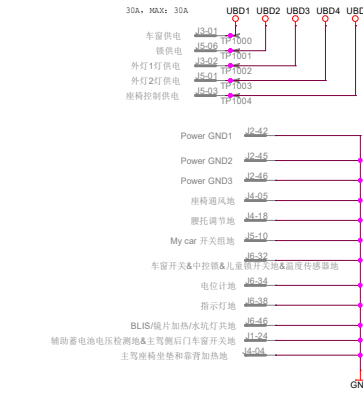


其他详见原理图内部信息。
如有未尽事宜，请和应用工程师沟通。

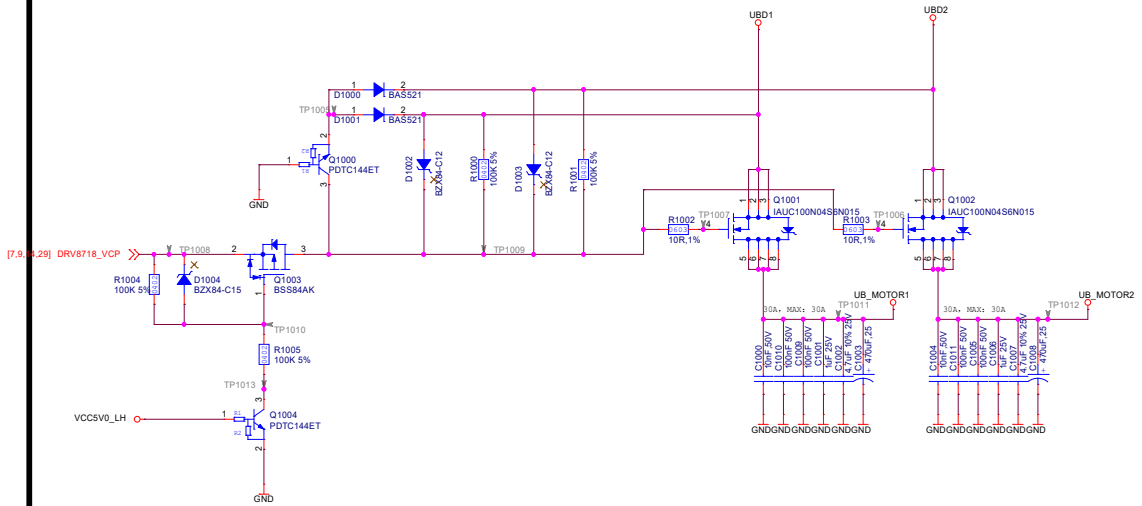
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Size	Designer / Date Zheng.liu/2024.5.11	Check / Date jianwei.yao/2024.5.11	Confirm / Date Qinghua.diao/2024.5.11
Date:	Monday, June 17, 2024	Sheet	1 of 32

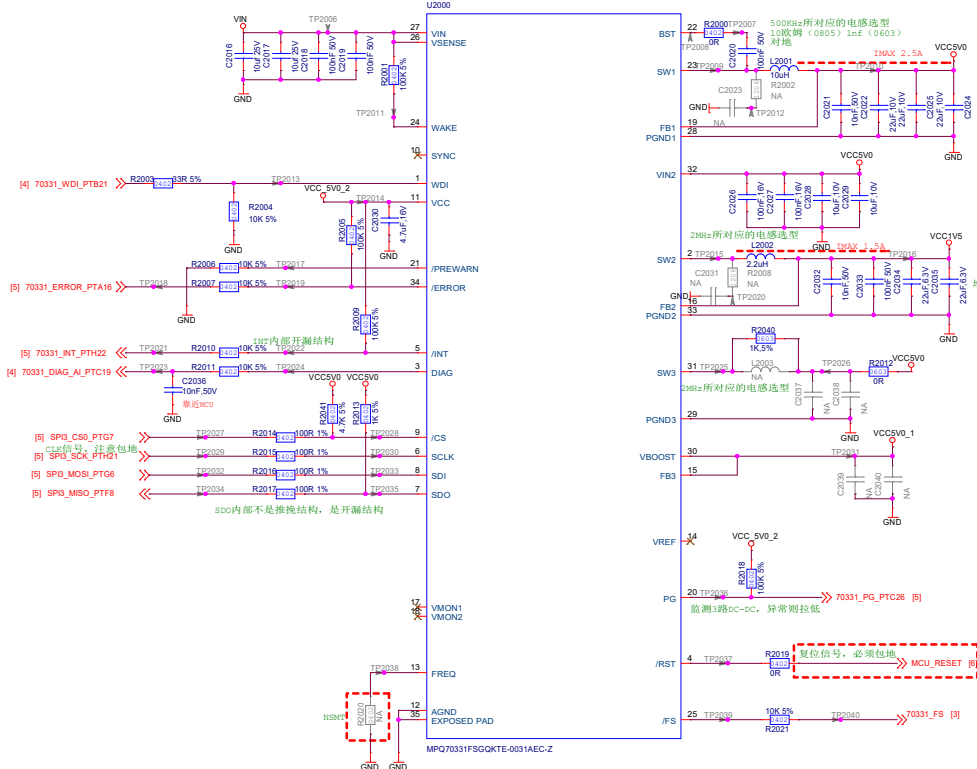
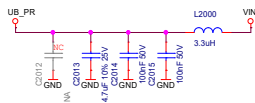
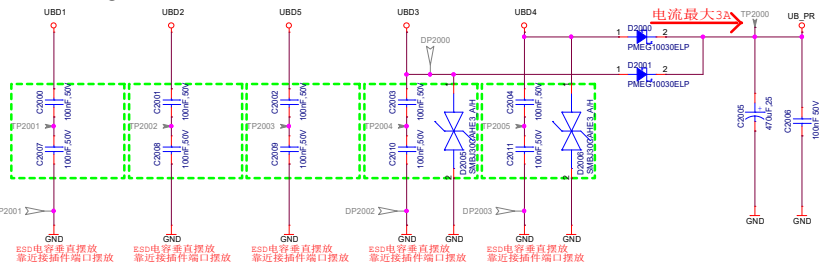
电源&地

PCB
825503134

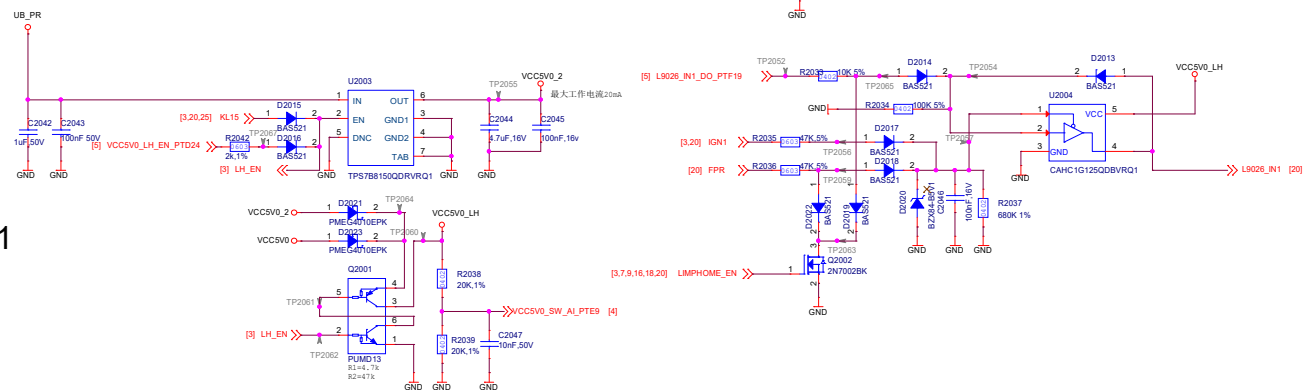
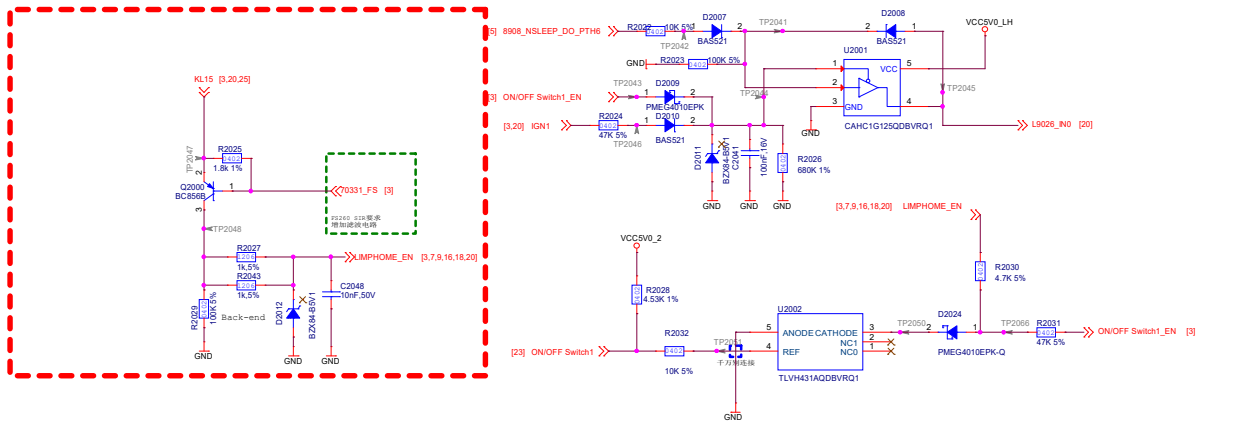


功率防反





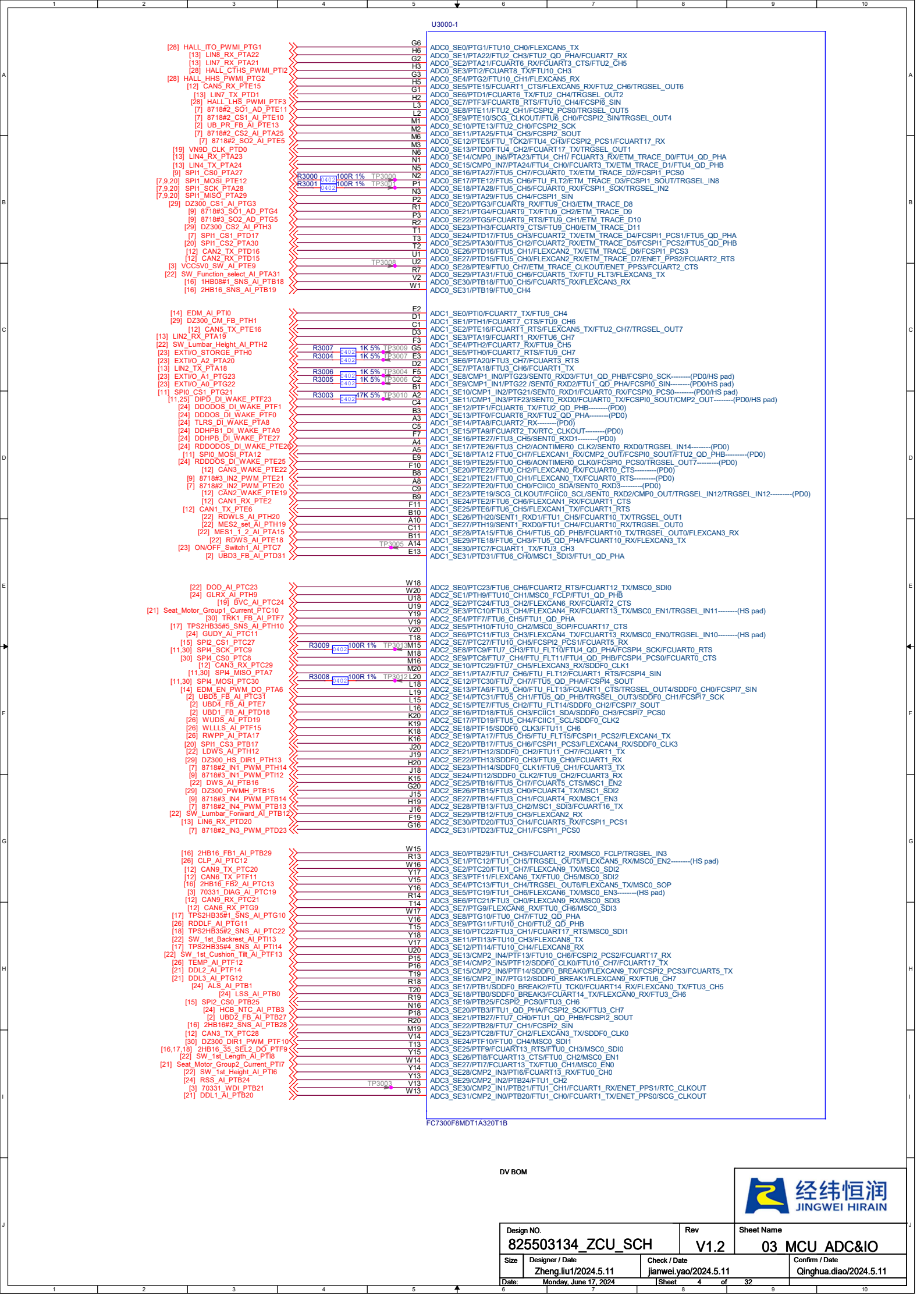
Limpome使能电路

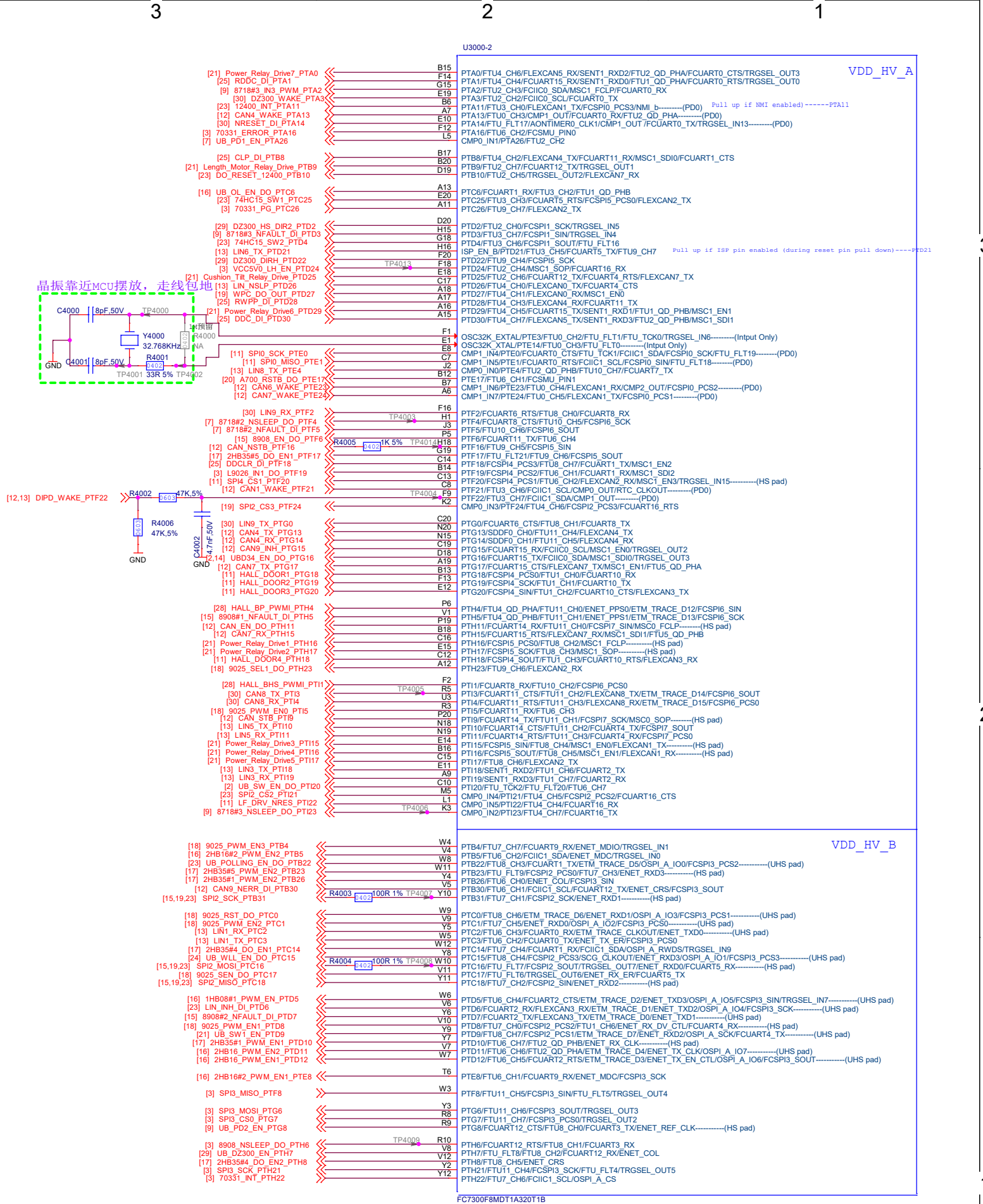


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Date:	Monday, June 17, 2024	Sheet	3	of	32

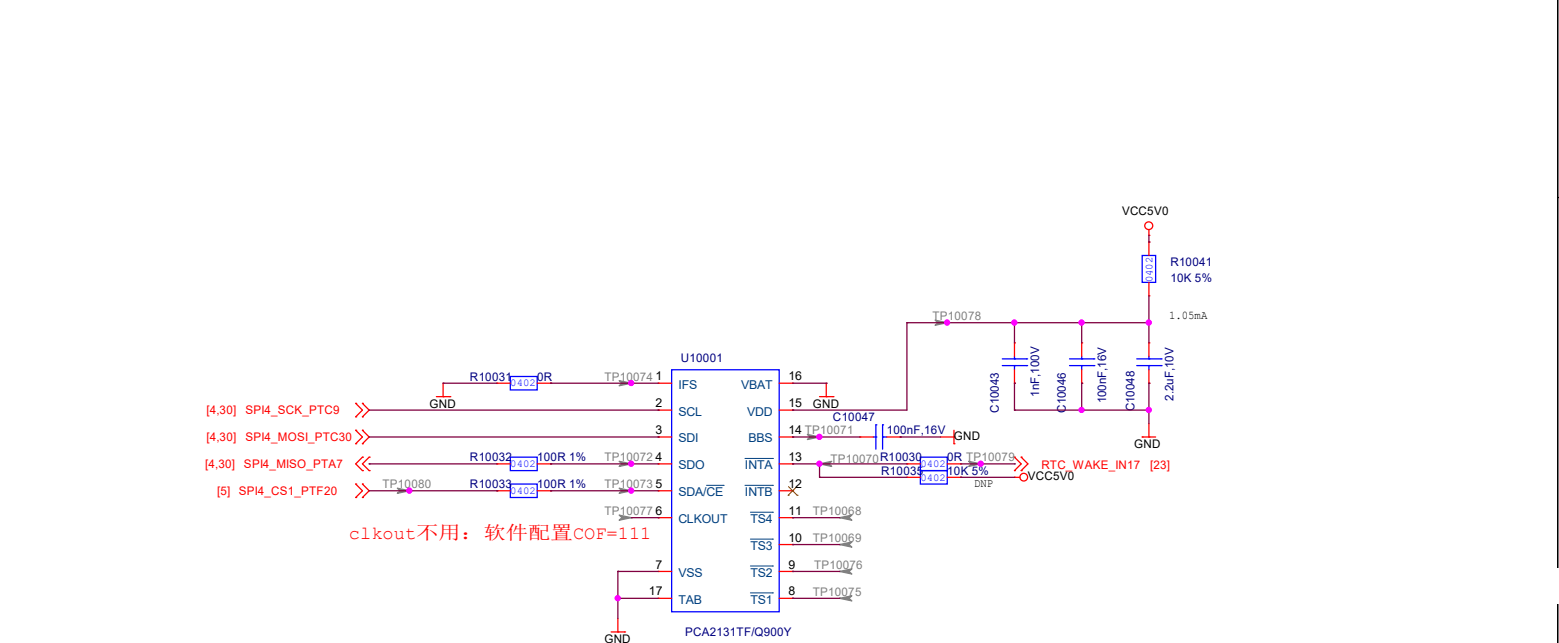
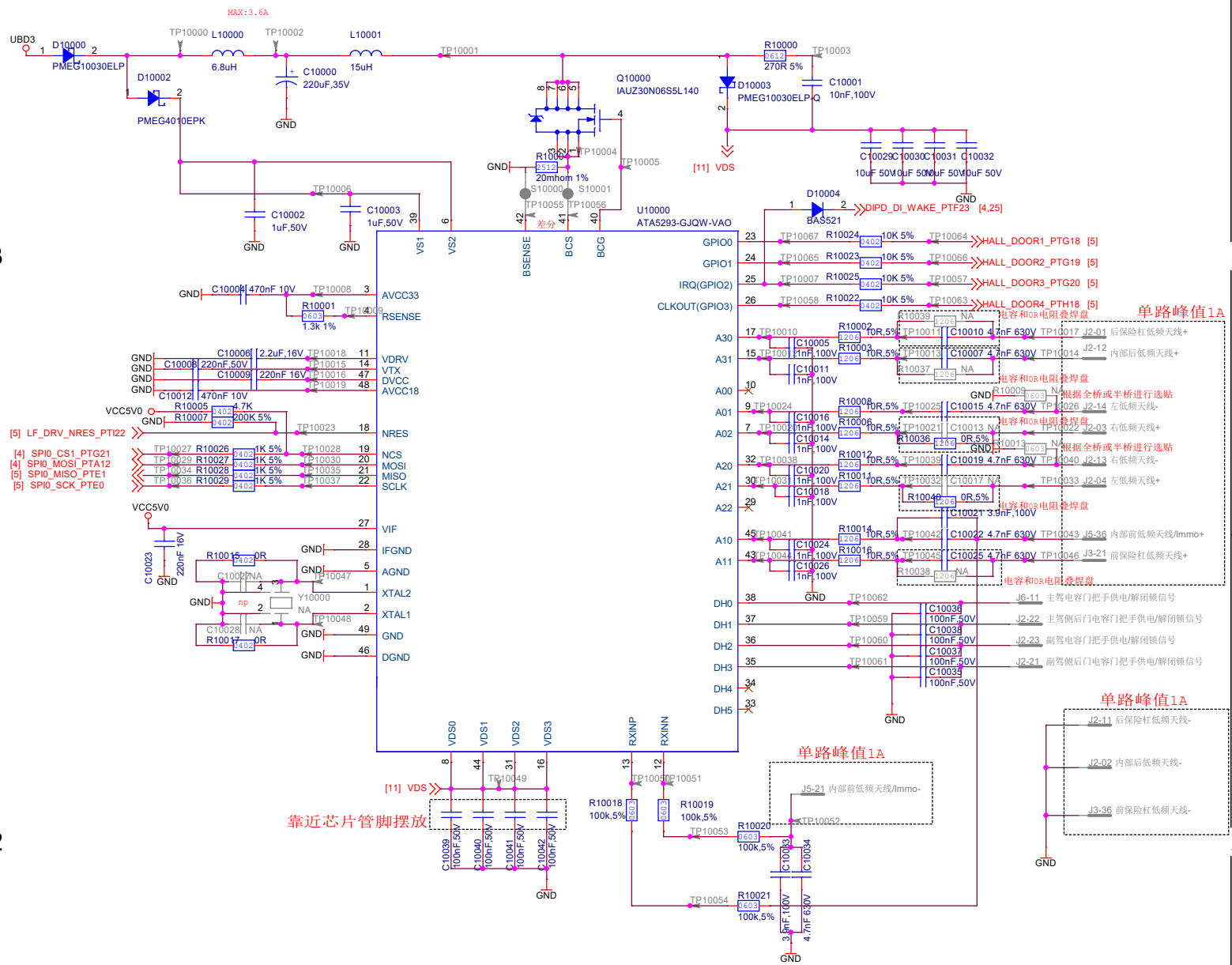




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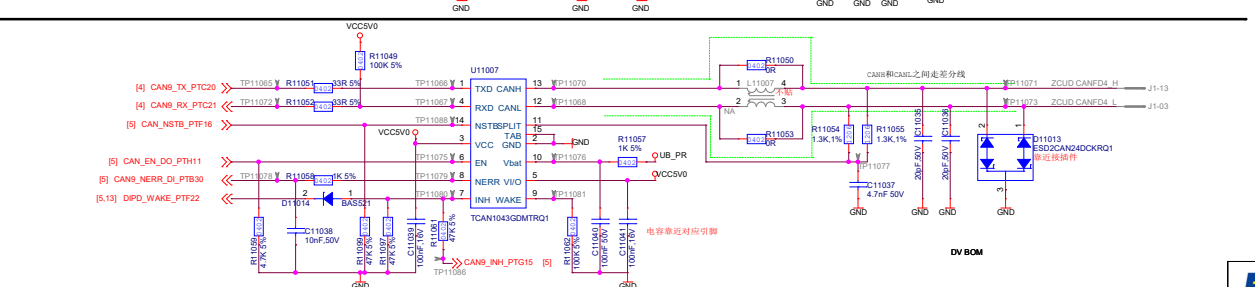
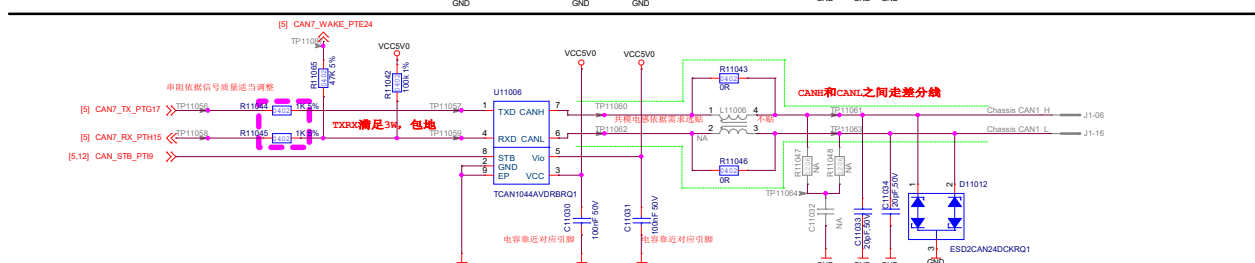
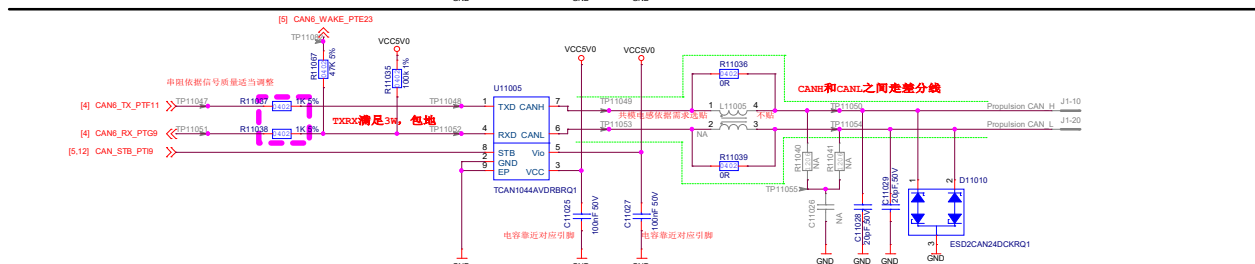
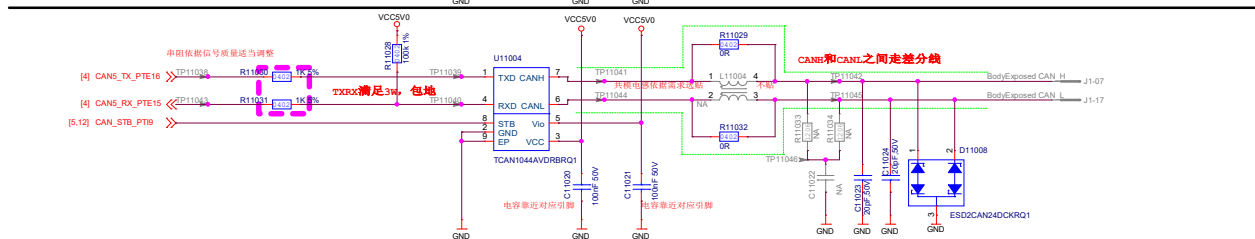
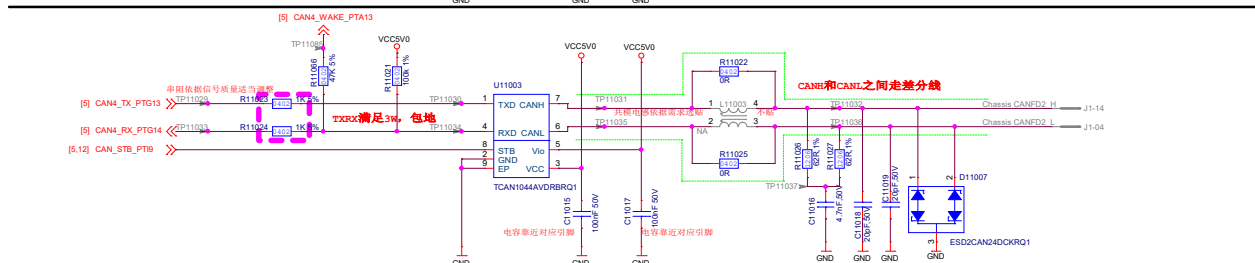
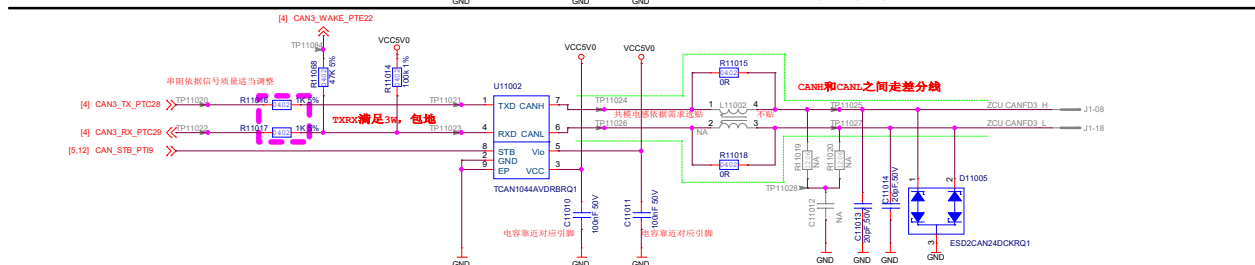
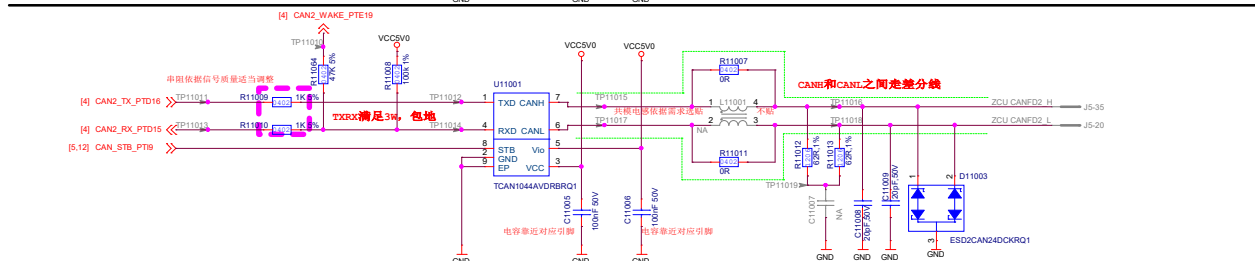
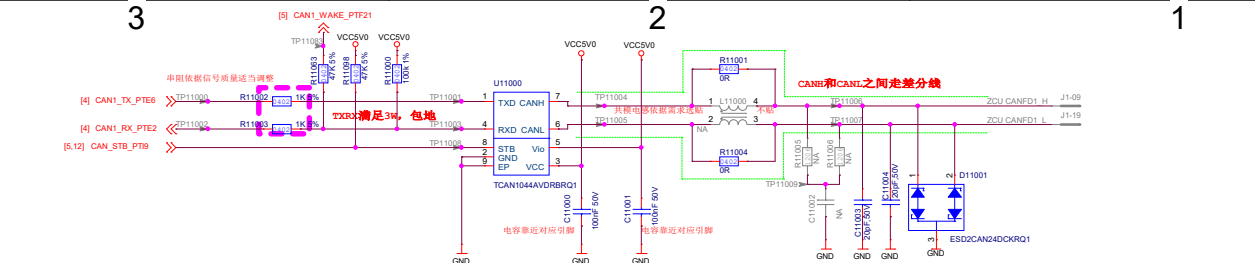
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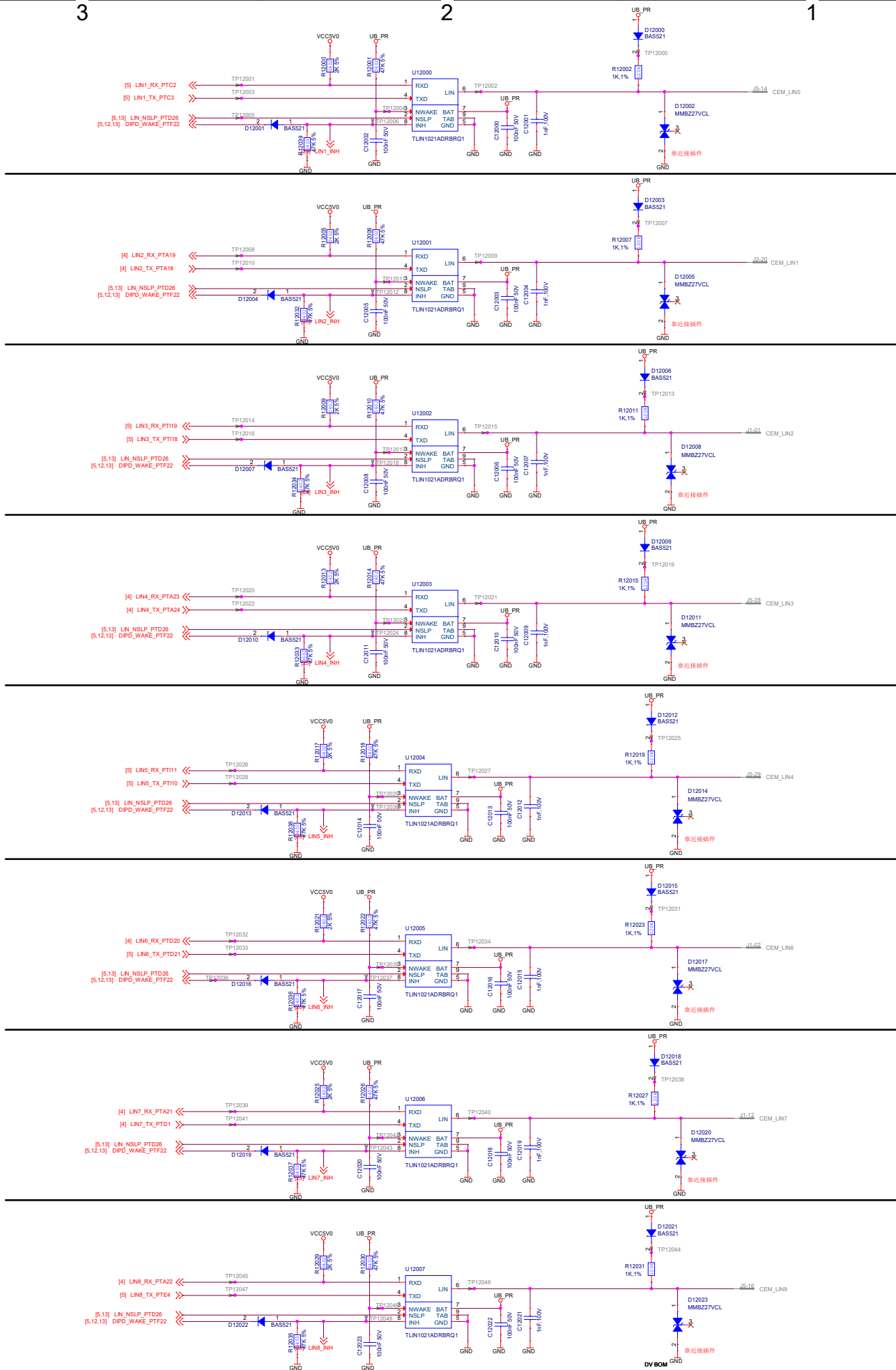


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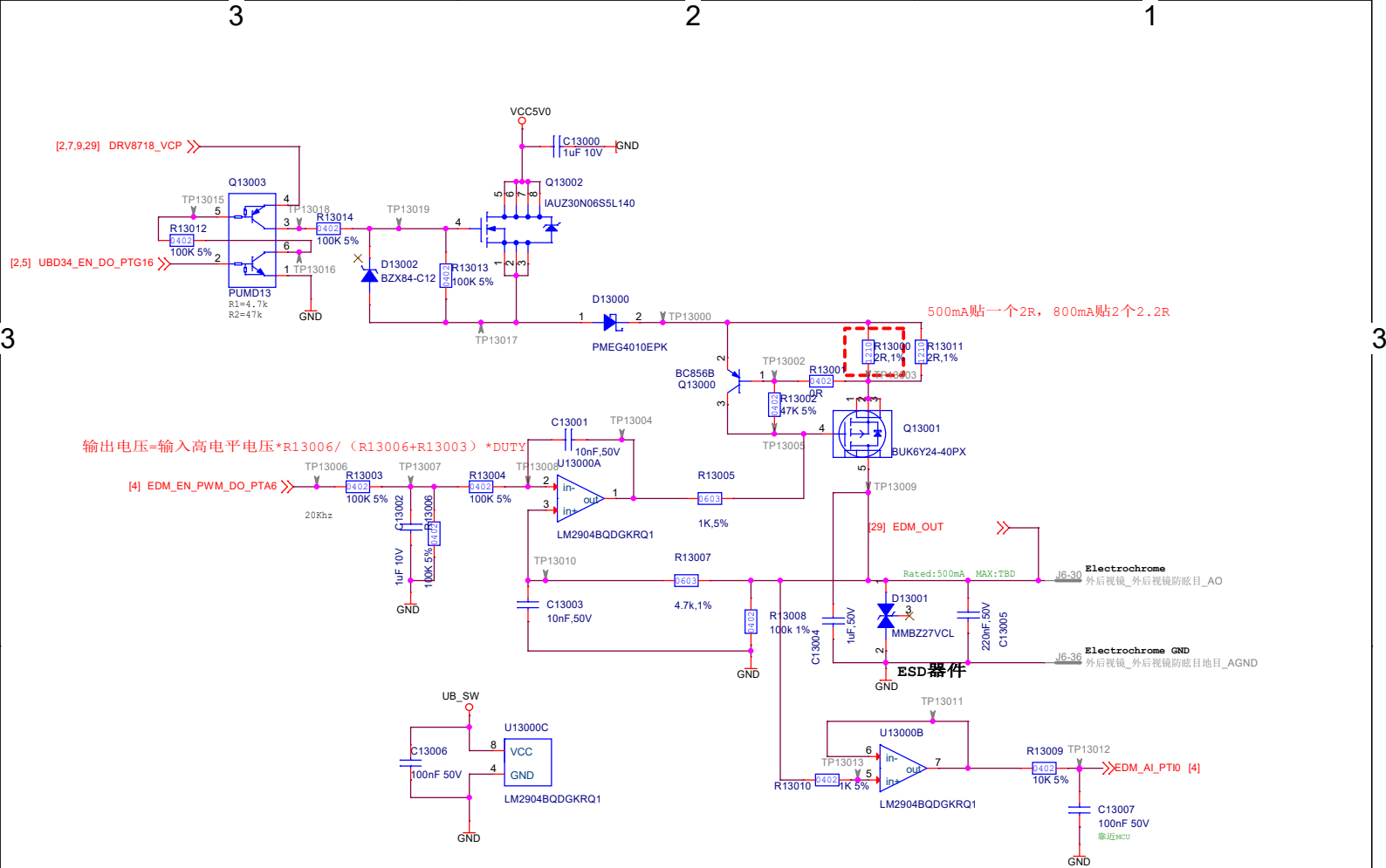


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Date Wednesday, July 03, 2024	Sheet 11	of 32	





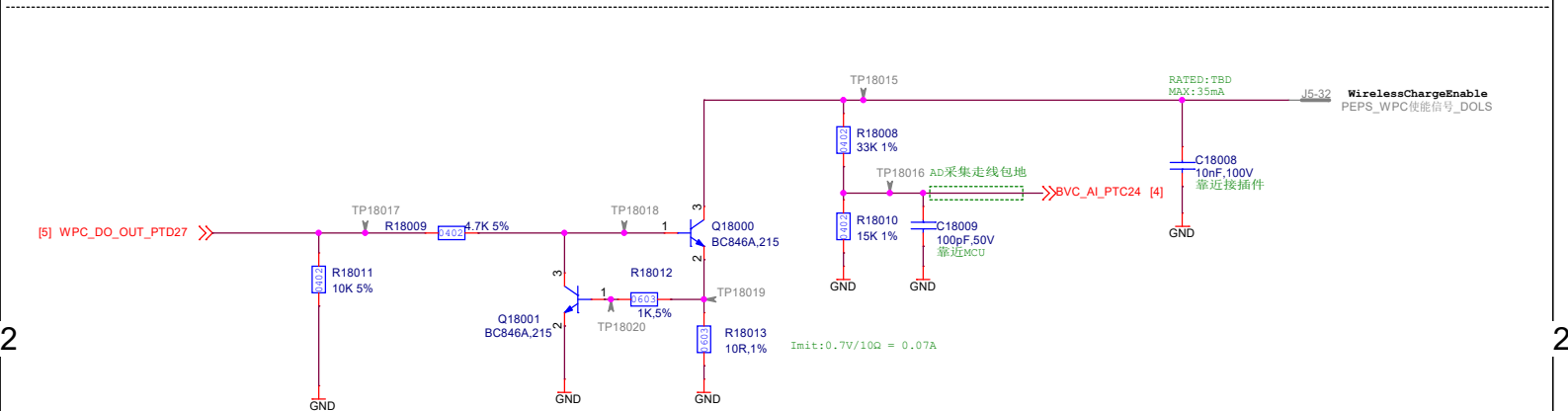
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Size Zheng lu/2024.5.11	Check / Date jianwei.yao/2024.5.11	Confirm / Date Qinghua.diao/2024.5.11	
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经纬恒润
JINGWEI HIRAIN

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2

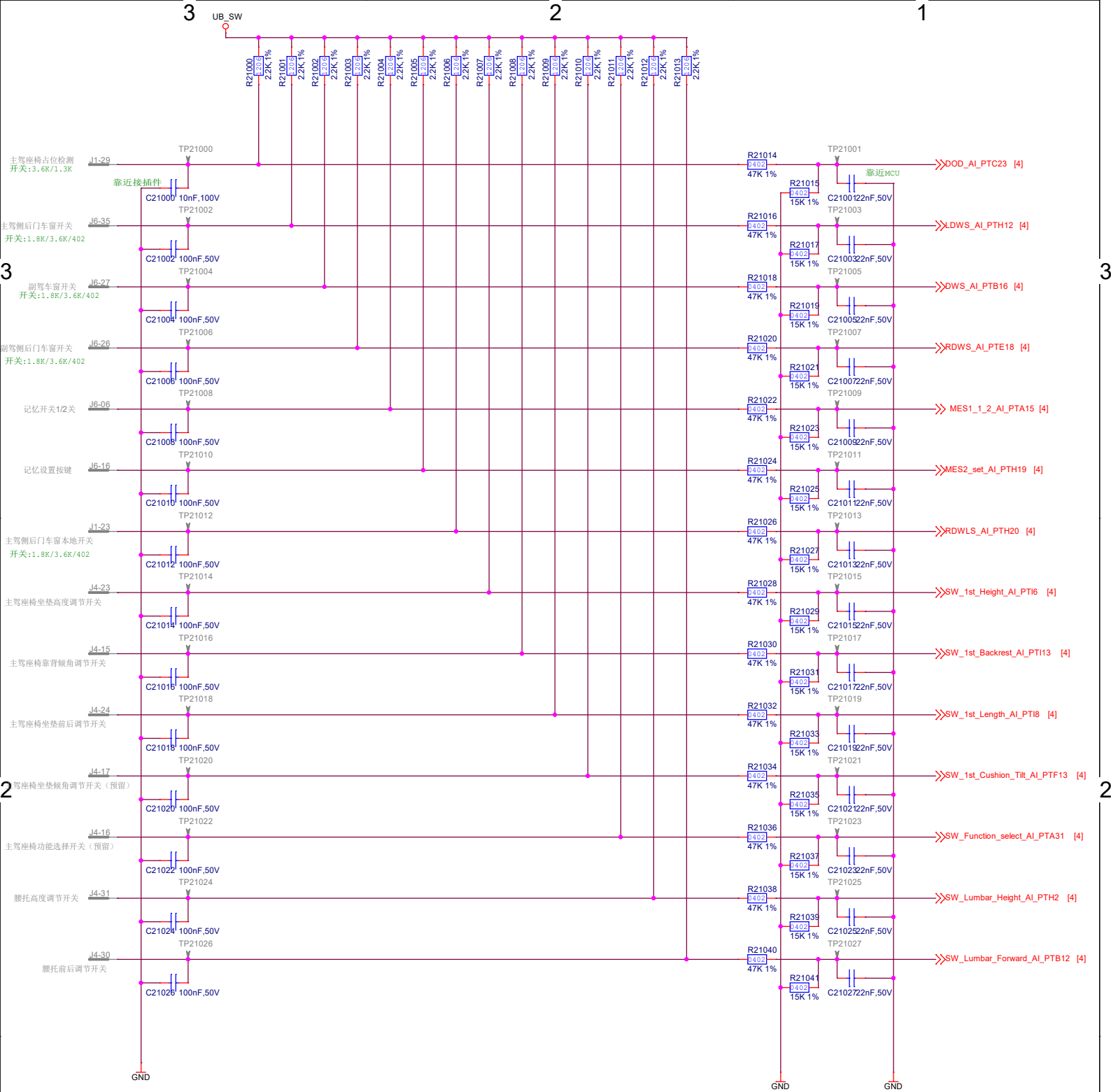


3



经纬恒润
JINGWEI HIRAIN

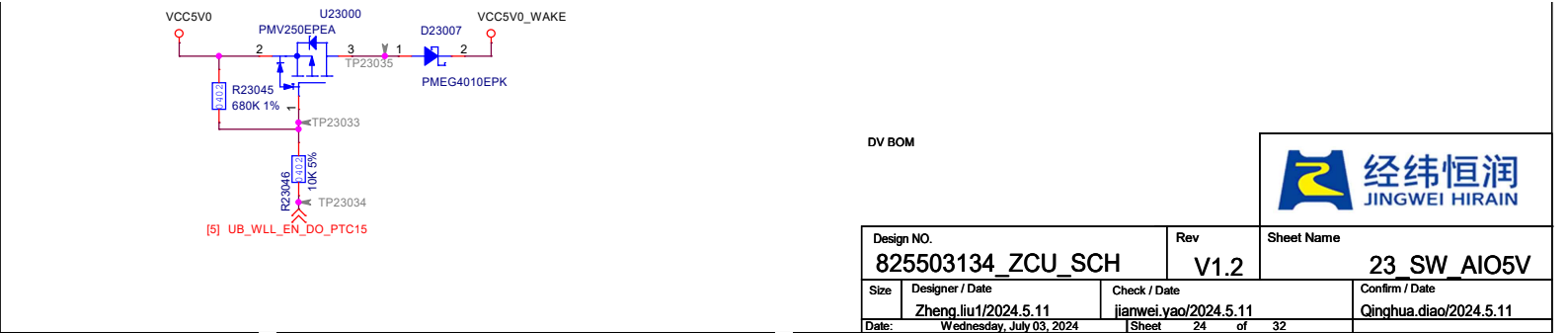
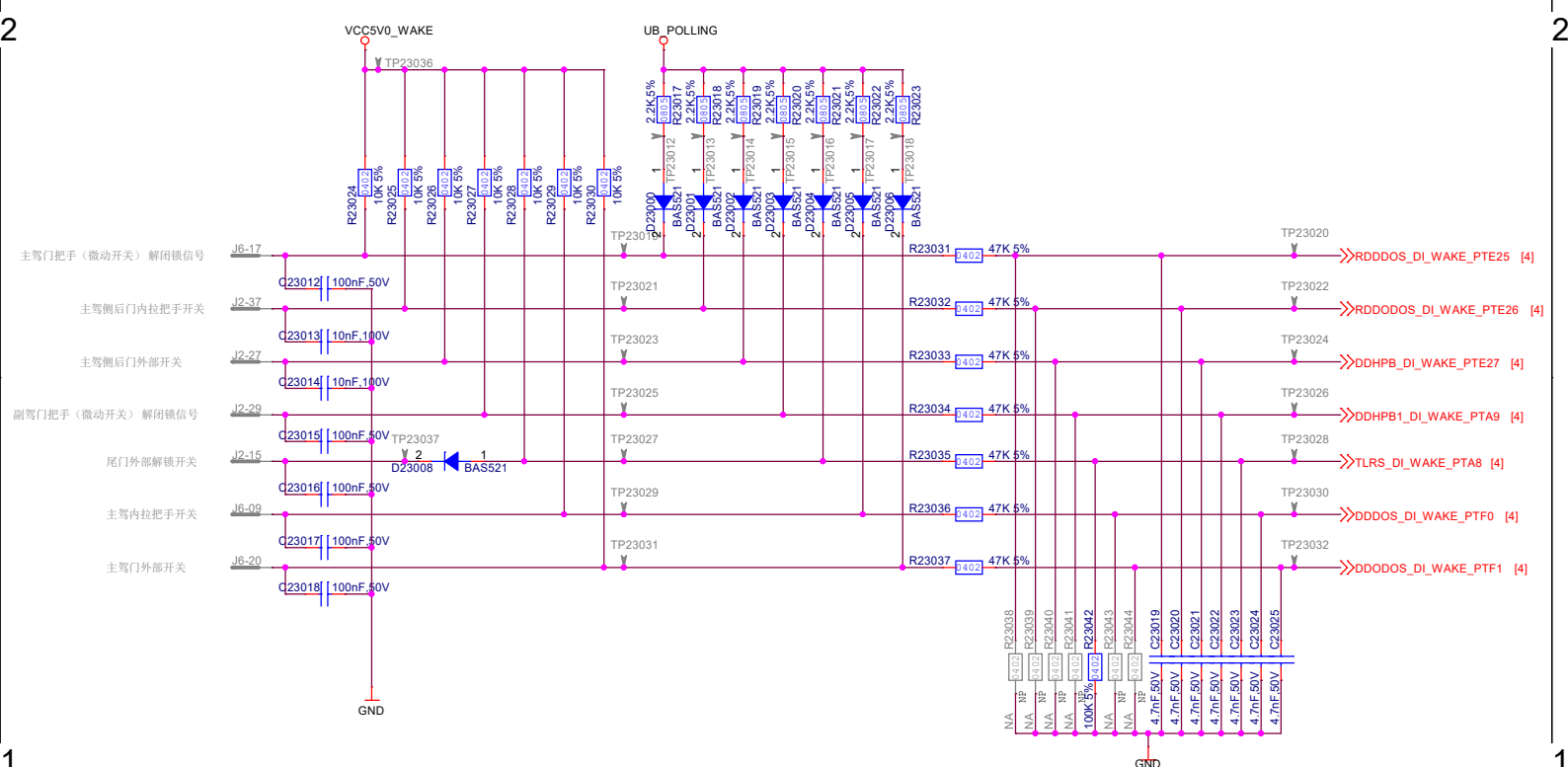
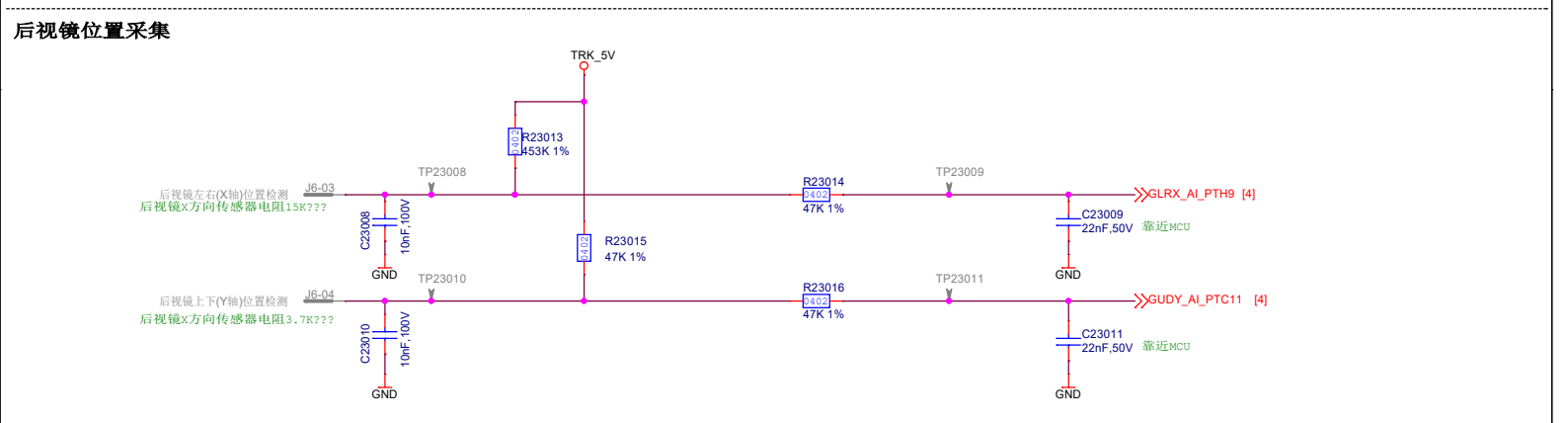
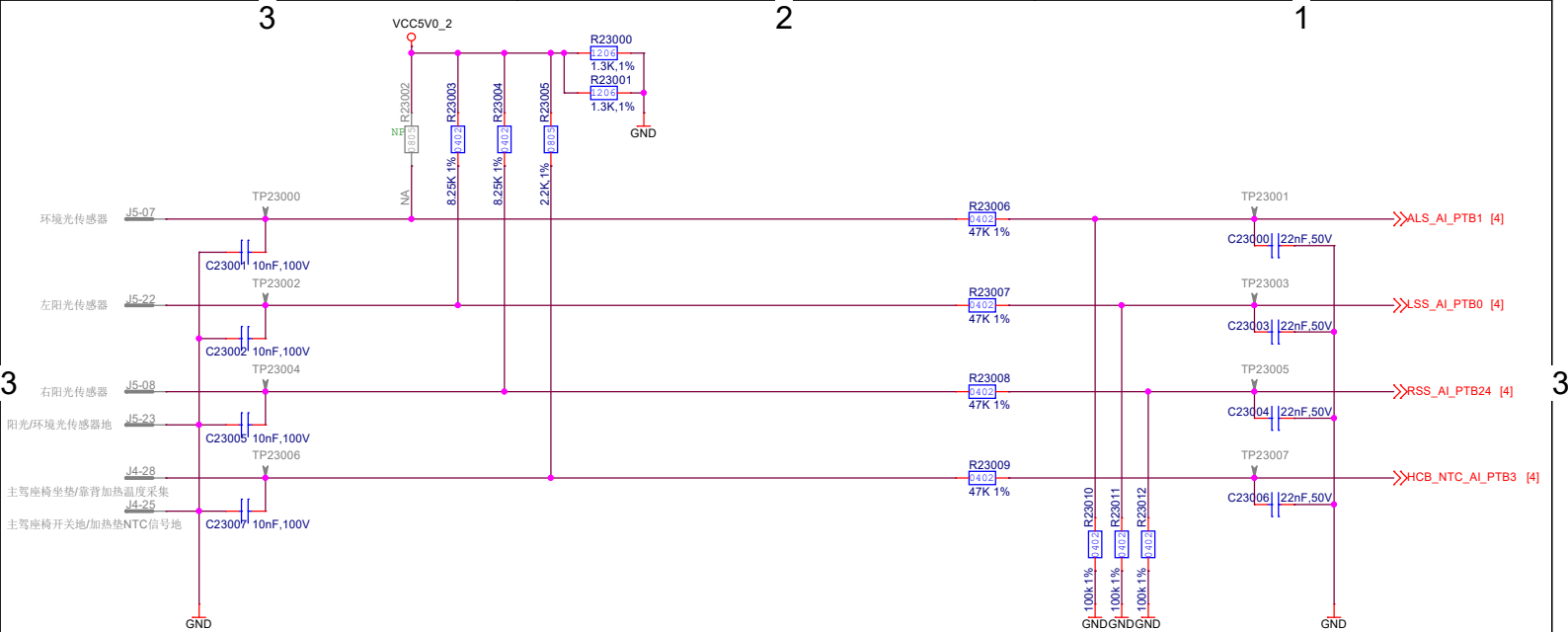
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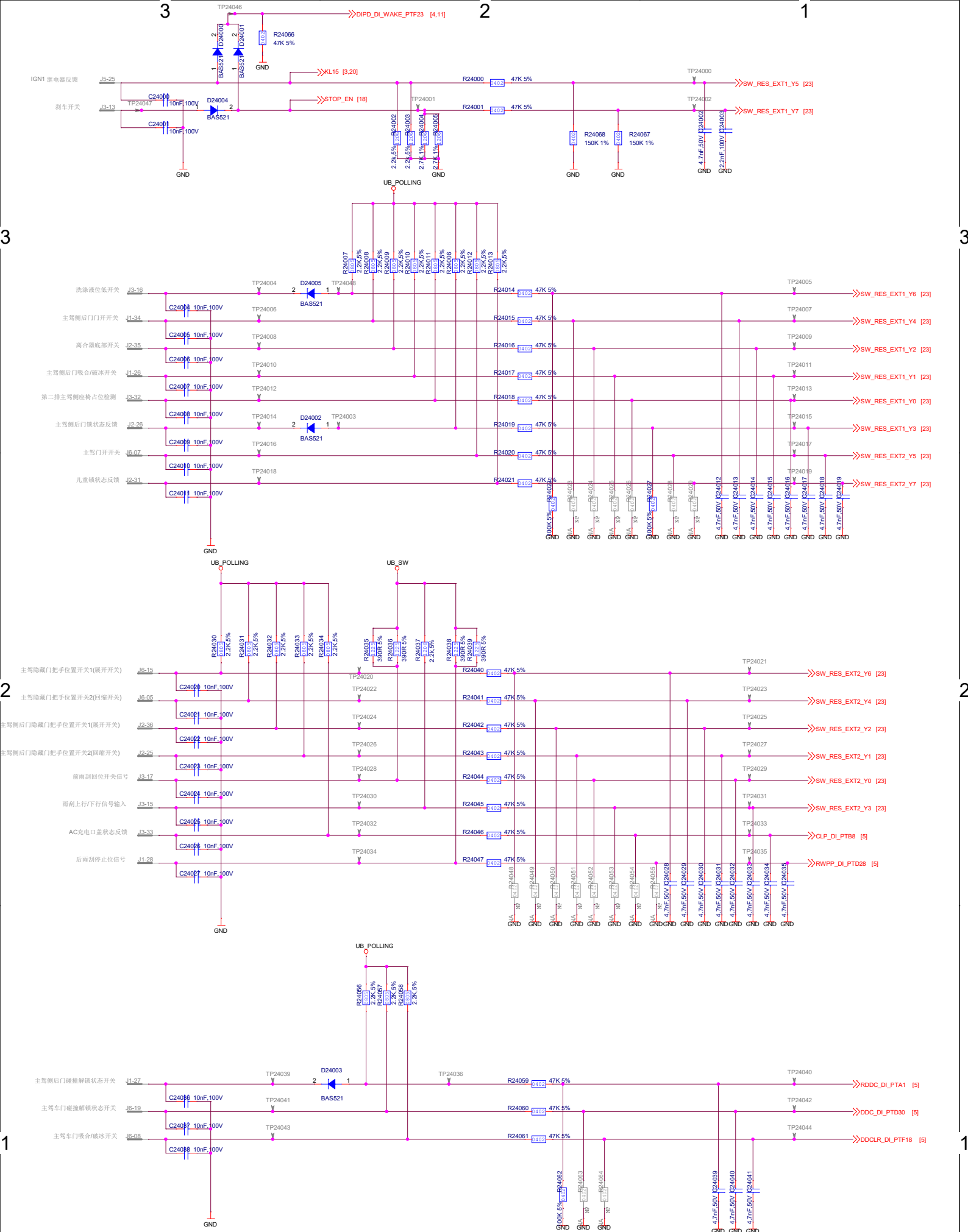


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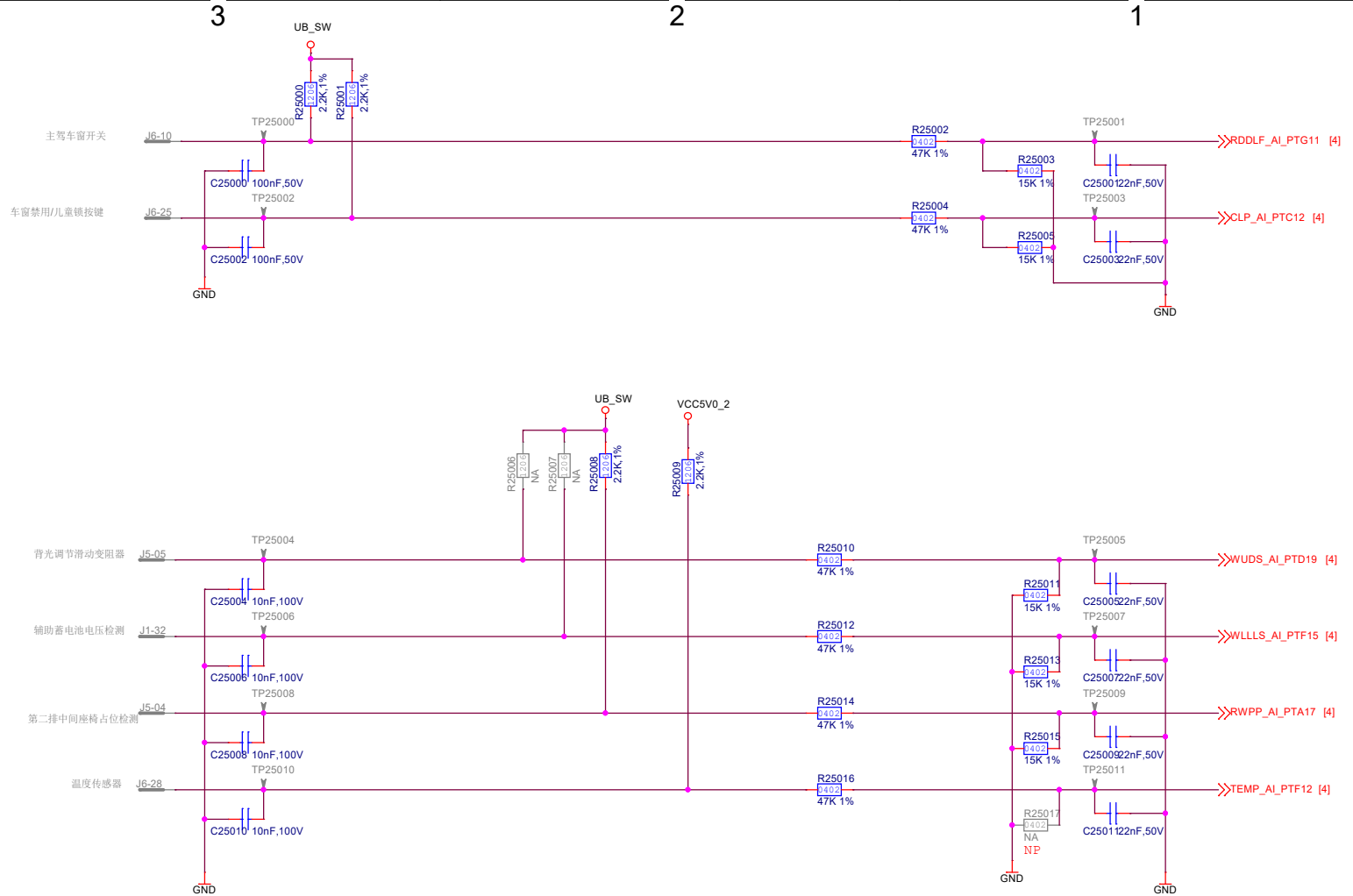




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Design NO. 825503134 ZCU SCH		Rev V1.2	Sheet Name 24 SW DIPD
Size	Designer / Date Zheng.liu1/2024.5.11	Check / Date jianwei.yao/2024.5.11	Confirm / Date Qinghua.diao/2024.5.11
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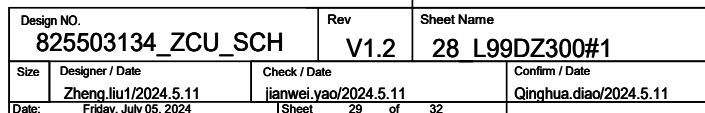


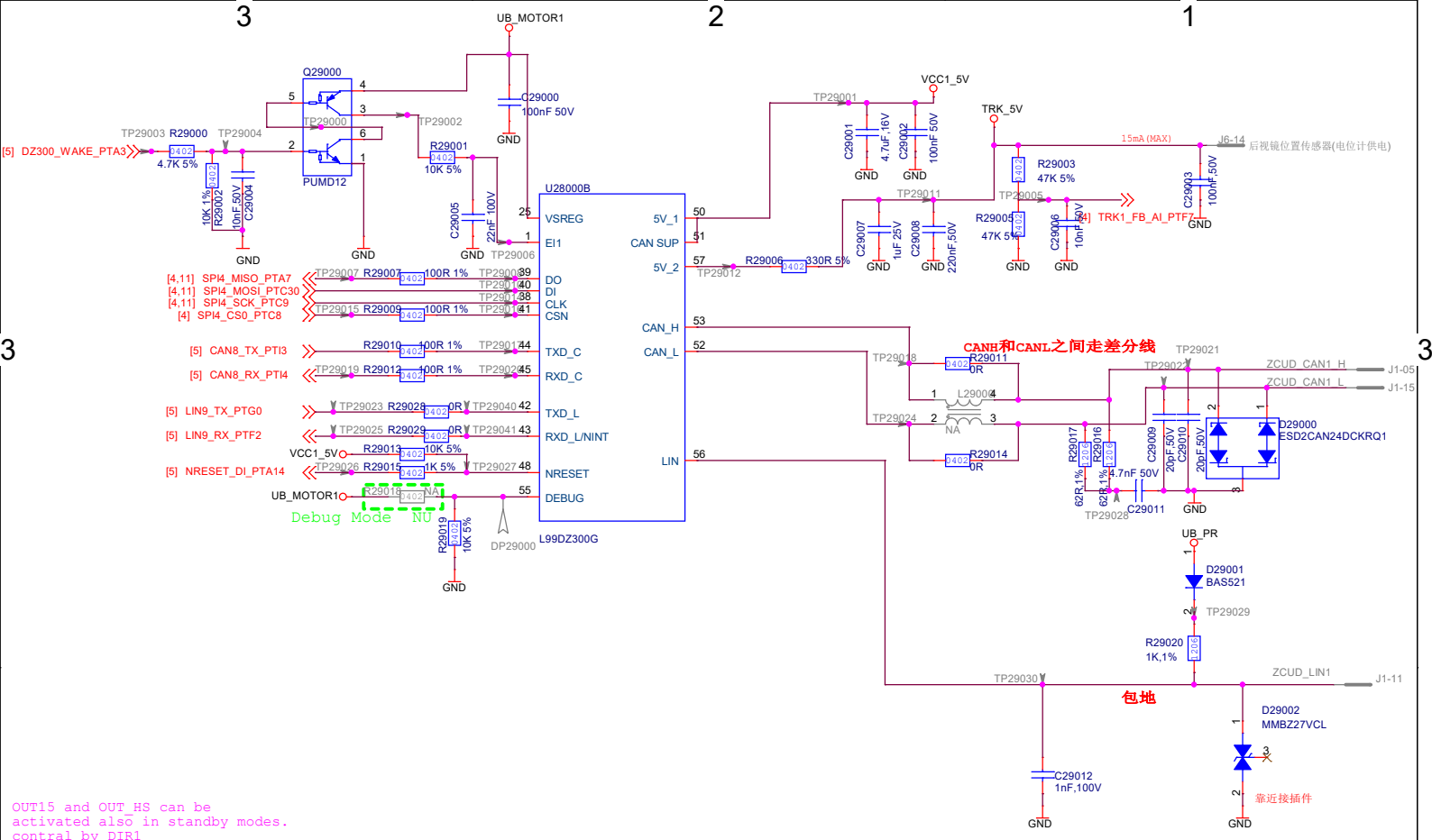
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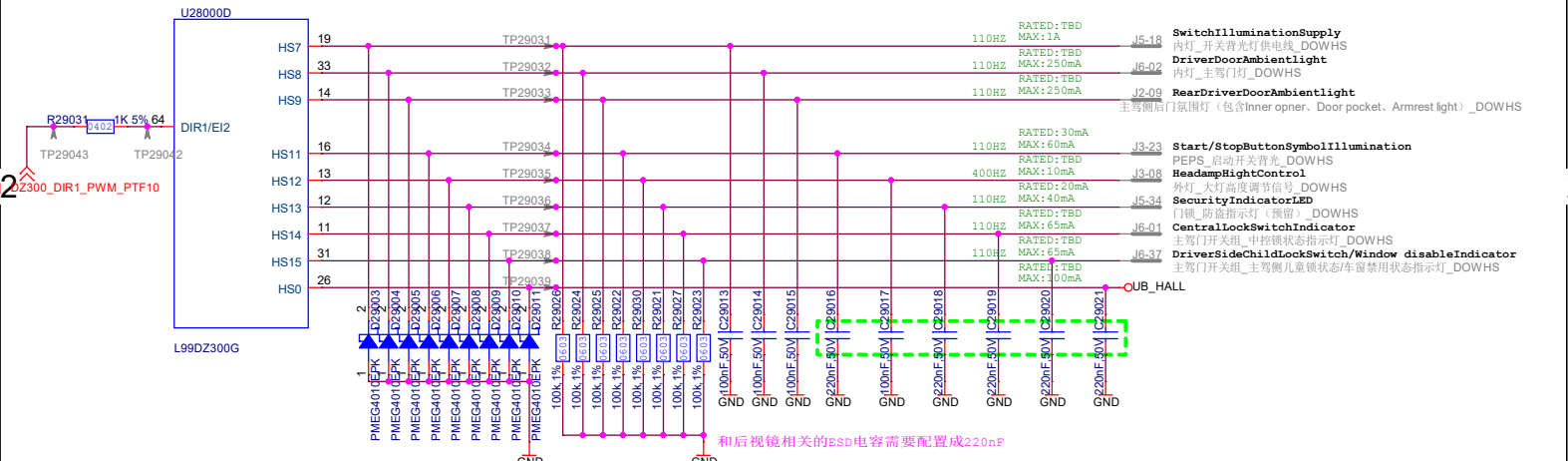


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	Zheng.liu/2024.5.11	jianwei.yao/2024.5.11	Qinghua.diao/2024.5.11
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OUT15 and OUT_HS can be activated also in standby modes. contral by DIR1



DV BOM



Design NO. 825503134_ZCU_SCH		Rev V1.2	Sheet Name 29_L99DZ300#2
Size	Designer / Date Zheng.liu/2024.5.11	Check / Date jianwei.yao/2024.5.11	Confirm / Date Qinghua.diao/2024.5.11
Date	Wednesday, July 03, 2024		Sheet 30 of 32

Debug Information									
位号	网络名称	描述							
TP1000	UBD1	Power_Window							
TP1001	UBD2	Power_Lock							
DP2000	UBD3	Power_Exterior Light1							
TP1003	UBD4	Power_Exterior Light2							
TP1004	UBD5	Power_Seat							
DP2001	GND	GND							
DP2002	GND	GND							
DP2003	GND	GND							
TP2000	UB_PR	12V Logic Power							
TP2010	VCC5V0	5V Logic Power							
TP2016	VCC1V5	1.5V Logic Power							

DV BOM



Design NO. 825503134_ZCU_SCH			Rev V1.2	Sheet Name 31_DEBUG	
Size	Designer / Date Zheng.liu1/2024.5.11		Check / Date jianwei.yao/2024.5.11		Confirm / Date Qinghua.diao/2024.5.11
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