

Digital Design and Computer Organisation Laboratory

UE22CS251A

3rd Semester, Academic Year 2023

Date: 10-08-2023

Name: Gurram Shreya	SRN: PES2UG22CS209	Section: D
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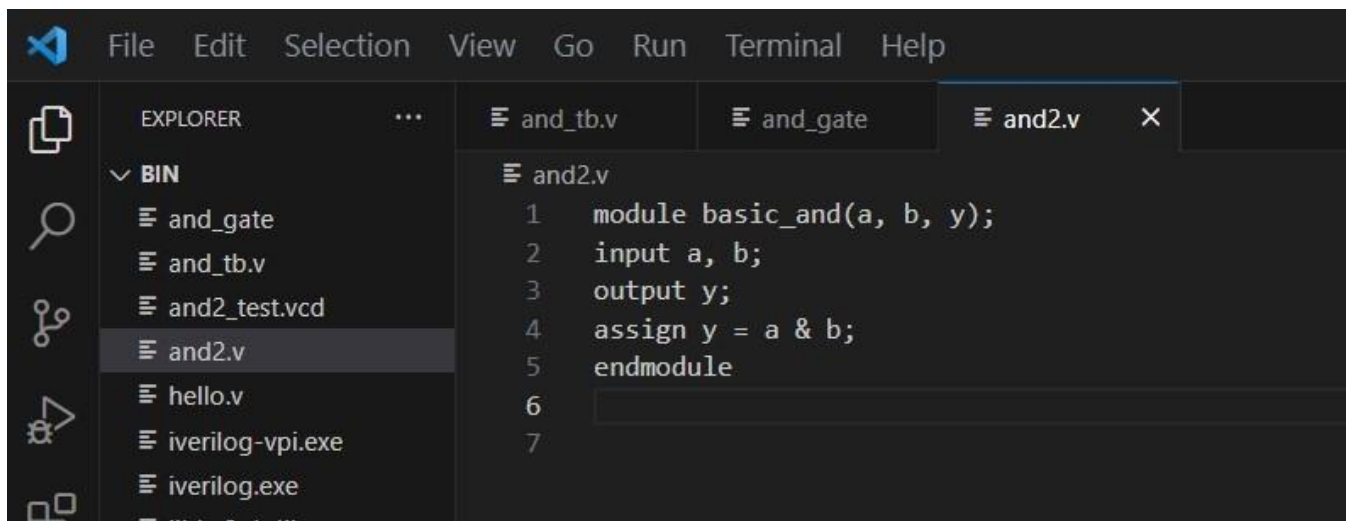
Week# ____1____

Program Number: ____1____

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT AND GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE

I. Verilog Code Screenshot



The screenshot shows the Icarus Verilog IDE interface. The Explorer panel on the left lists files under the 'BIN' directory: and_gate, and_tb.v, and2_test.vcd, and2.v (selected), hello.v, iverilog-vpi.exe, and iverilog.exe. The main editor window displays the Verilog code for 'and2.v'.

```
and2.v
1  module basic_and(a, b, y);
2  input a, b;
3  output y;
4  assign y = a & b;
5  endmodule
6
7
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>iverilog -o test1 and2.v and_tb.v

C:\iverilog\bin>vvp test1
VCD info: dumpfile and2_test.vcd opened for output.
      0a=0, b=0, y=0
      5a=0, b=1, y=0
     15a=1, b=0, y=0
     30a=1, b=1, y=1

C:\iverilog\bin>gtkwave and2_test.vcd

GTKWave Analyzer v3.3.100 (w)1999-2019 BSI

[0] start time.
[30] end time.
```

III. GTKWAVE Screenshot

```
C:\iverilog\bin>iverilog -o test1 and2.v and_tb.v

C:\iverilog\bin>vvp test1
VCD info: dumpfile and2_test.vcd opened for output.
      0a=0, b=0, y=0
      5a=0, b=1, y=0
     15a=1, b=0, y=0
     30a=1, b=1, y=1

C:\iverilog\bin>gtkwave and2_test.vcd

GTKWave Analyzer v3.3.100 (w)1999-2019 BSI

[0] start time.
[30] end time.
```

IV. Output Table to be completed and included

a	b	y
0	0	0
0	1	0
1	0	0
1	1	1

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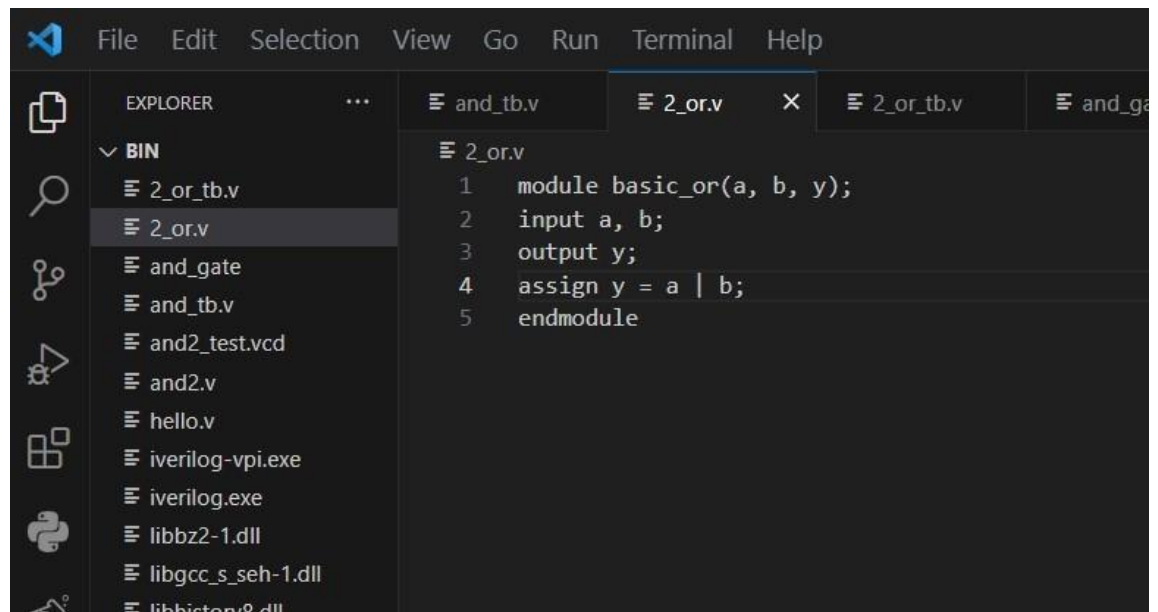
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Week# ____1____ Program Number: ____2____

TITLE :

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT OR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE OR GATE TRUTH TABLE

I. Verilog Code Screenshot



The screenshot shows an IDE with a dark theme. The Explorer panel on the left lists files in a 'BIN' directory, including '2_or_tb.v', '2_or.v' (selected), 'and_gate', 'and_tb.v', 'and2_test.vcd', 'and2.v', 'hello.v', 'iverilog-vpi.exe', 'iverilog.exe', 'libbz2-1.dll', 'libgcc_s_seh-1.dll', and 'libhistory8.dll'. The main editor window displays the Verilog code for '2_or.v'.

```
1 module basic_or(a, b, y);  
2   input a, b;  
3   output y;  
4   assign y = a | b;  
5 endmodule
```

II. Verilog VVP Output Screen Shot

```
^C
C:\iverilog\bin>iverilog -o test2 2_or.v 2_or_tb.v

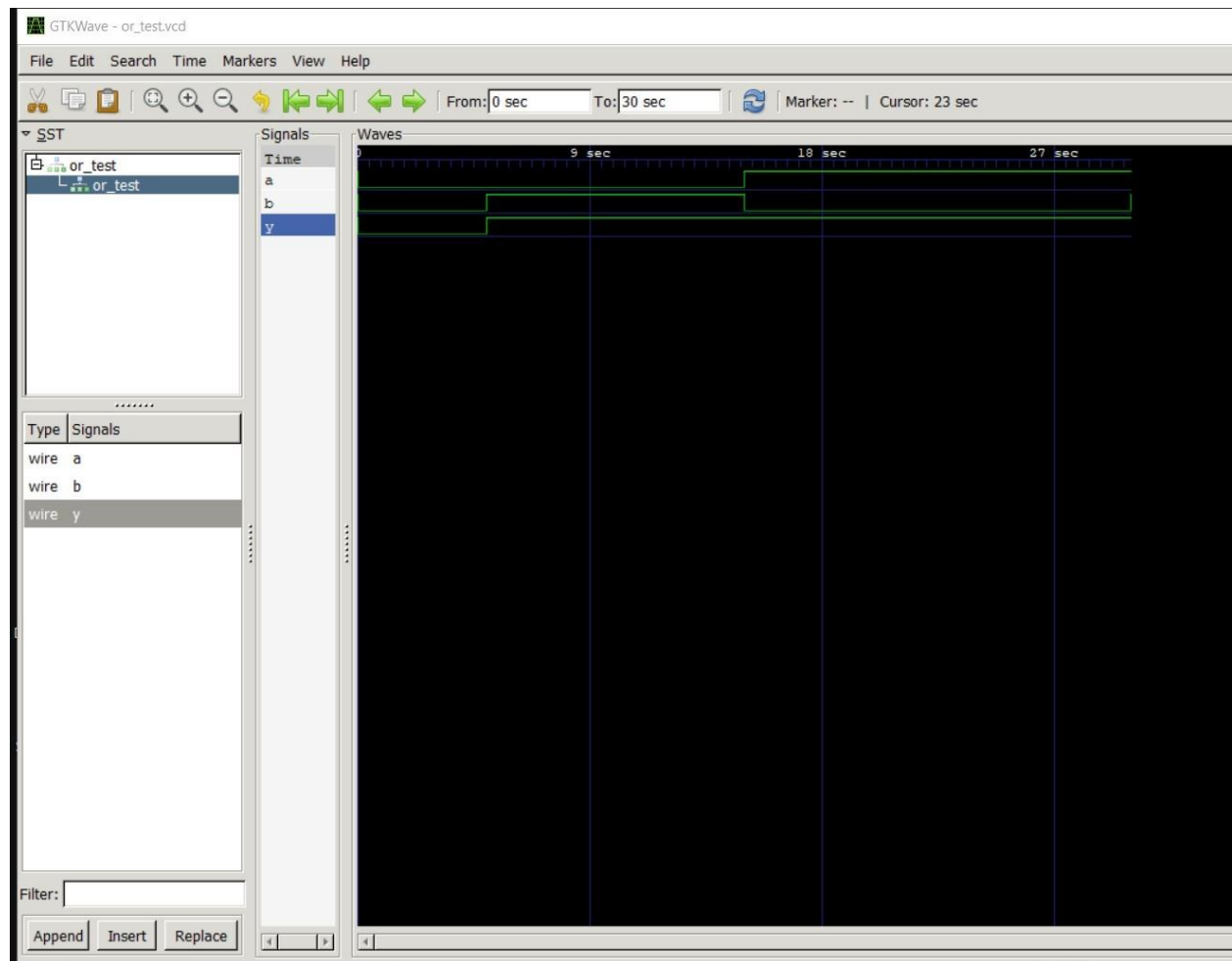
C:\iverilog\bin>vvp test2
VCD info: dumpfile or_test.vcd opened for output.
          0a=0, b=0, y=0
          5a=0, b=1, y=1
          15a=1, b=0, y=1
          30a=1, b=1, y=1

C:\iverilog\bin>gtkwave or_test.vcd

GTKWave Analyzer v3.3.100 (w)1999-2019 BSI

[0] start time.
[30] end time.
```

III. GTKWAVE Screenshot



IV. Output Table to be completed and included

a	b	y
0	0	0
0	1	1
1	0	1
1	1	1

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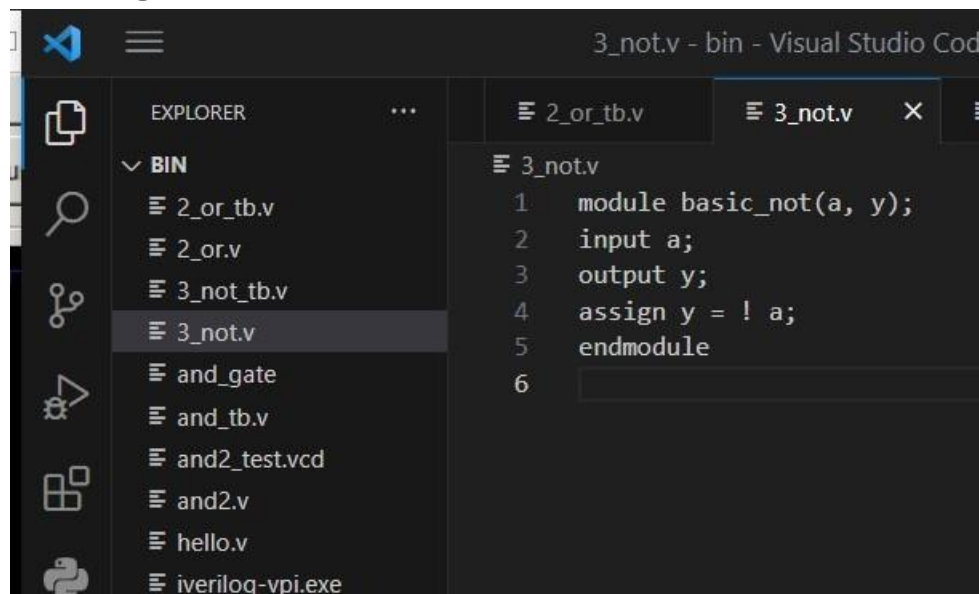
Week# ____1____

Program Number: ____3____

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A NOT GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE NOT GATE TRUTH TABLE

I. Verilog Code Screenshot



The screenshot shows the Visual Studio Code interface with a Verilog file named 3_not.v open. The Explorer panel on the left shows a project structure with a BIN folder containing several files, including 3_not.v which is selected. The main editor area displays the Verilog code for a module named basic_not.

```
1 module basic_not(a, y);  
2   input a;  
3   output y;  
4   assign y = ! a;  
5 endmodule  
6
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>iverilog -o test3 3_not.v 2_not_tb.v
2_not_tb.v: No such file or directory
Preprocessor failed with 1 errors.

C:\iverilog\bin>iverilog -o test3 3_not.v 3_not_tb.v

C:\iverilog\bin>vvp test3
test: Unable to open input file.

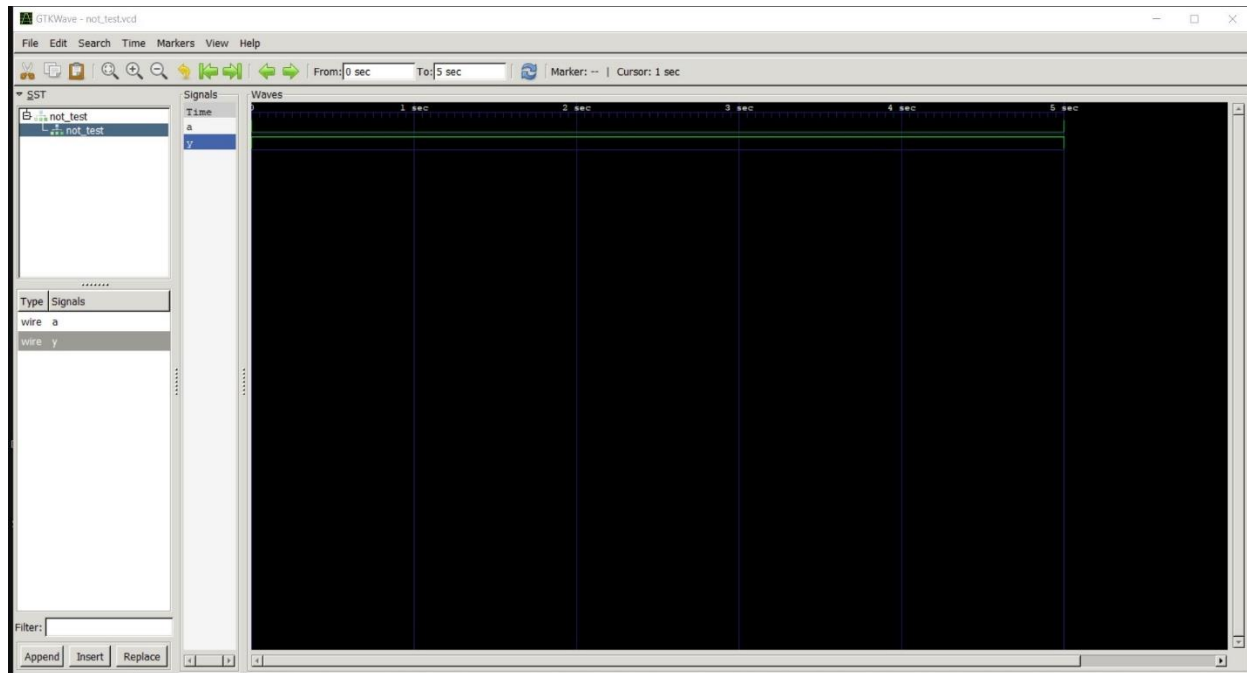
C:\iverilog\bin>vvp test3
VCD info: dumpfile not_test.vcd opened for output.
          0a=0, y=1
          5a=1, y=0

C:\iverilog\bin>gtkwave not_test.vcd

GTKWave Analyzer v3.3.100 (w)1999-2019 BSI

[0] start time.
[5] end time.
```

III. GTKWAVE Screenshot



IV. Output Table to be completed and included

a	y
0	1
1	0

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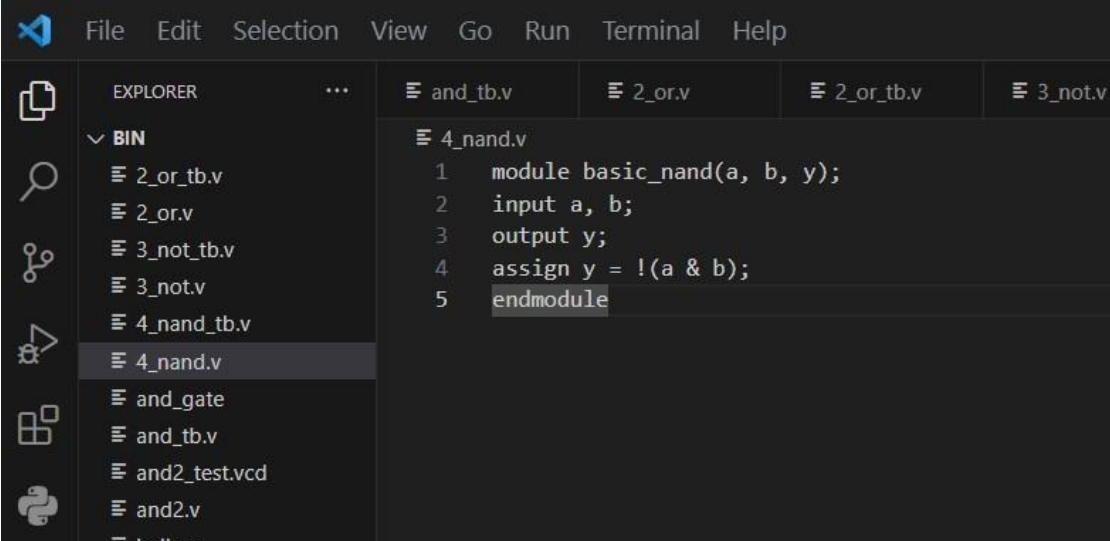
Week# ____1____

Program Number: ____4____

TITLE :

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT NAND GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE NAND GATE TRUTH TABLE

I. Verilog Code Screenshot



The screenshot shows a Verilog code editor with a dark theme. The Explorer panel on the left lists files in a directory named 'BIN', including testbenches and modules for OR, NOT, and NAND gates. The main editor window displays the code for '4_nand.v', which defines a 'basic_nand' module with two inputs (a, b) and one output (y). The logic is implemented using an 'assign' statement: `assign y = !(a & b);`. The code is as follows:

```
1 module basic_nand(a, b, y);
2   input a, b;
3   output y;
4   assign y = !(a & b);
5 endmodule
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>iverilog -o test4 4_nand.v 4_nand_tb.v

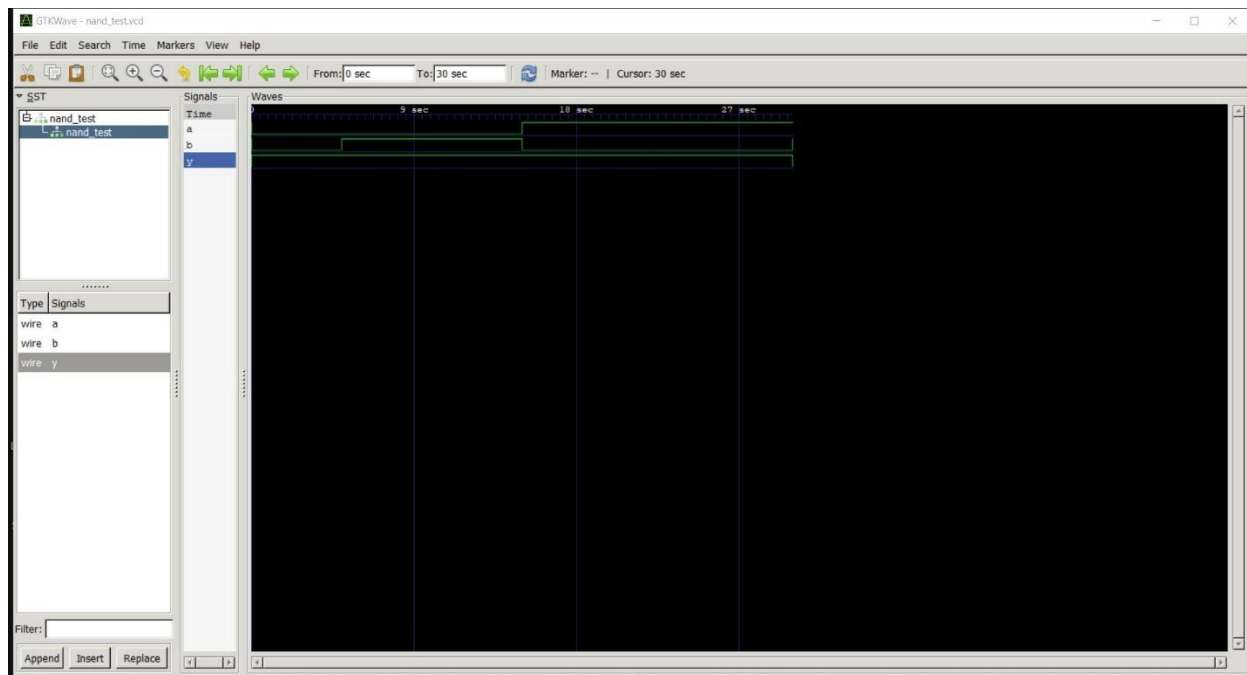
C:\iverilog\bin>vvp test4
VCD info: dumpfile nand_test.vcd opened for output.
      0a=0, b=0, y=1
      5a=0, b=1, y=1
     15a=1, b=0, y=1
     30a=1, b=1, y=0

C:\iverilog\bin>gtkwave nand_test.vcd

GTKWave Analyzer v3.3.100 (w)1999-2019 BSI

[0] start time.
[30] end time.
```

III. GTKWAVE Screenshot



IV. Output Table to be completed and included

a	b	y
0	0	1
0	1	1
1	0	1
1	1	0

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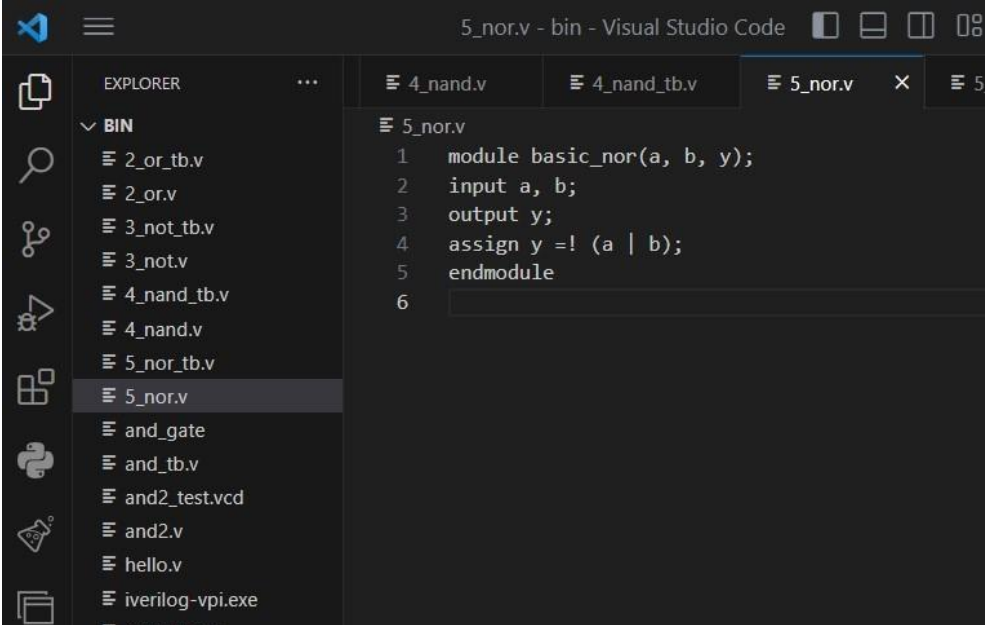
Week# ____1____

Program Number: ____5____

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT NOR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE NOR GATE TRUTH TABLE

I. Verilog Code Screenshot



The screenshot shows the Visual Studio Code editor with a file explorer on the left and a code editor on the right. The file explorer shows a directory named 'BIN' containing several files, including '5_nor.v' which is selected. The code editor displays the Verilog code for '5_nor.v'.

```
5_nor.v
1  module basic_nor(a, b, y);
2  input a, b;
3  output y;
4  assign y =! (a | b);
5  endmodule
6
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>iverilog -o test5 5_nor.v 5_nor_tb.v

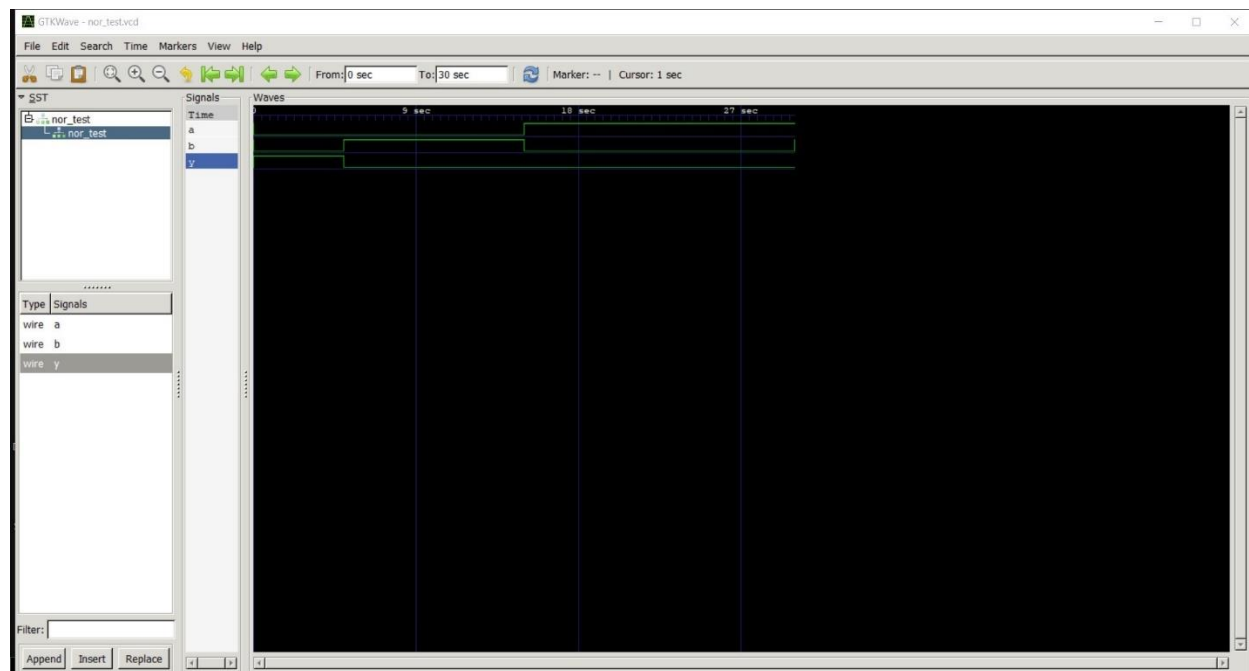
C:\iverilog\bin>vvp test5
VCD info: dumpfile nor_test.vcd opened for output.
      0a=0, b=0, y=1
      5a=0, b=1, y=0
     15a=1, b=0, y=0
     30a=1, b=1, y=0

C:\iverilog\bin>gtkwave nor_test.vcd

GTKWave Analyzer v3.3.100 (w)1999-2019 BSI

[0] start time.
[30] end time.
```

III. GTKWAVE Screenshot



IV. Output Table to be completed and included

a	b	y
0	0	1
0	1	0
1	0	0
1	1	0

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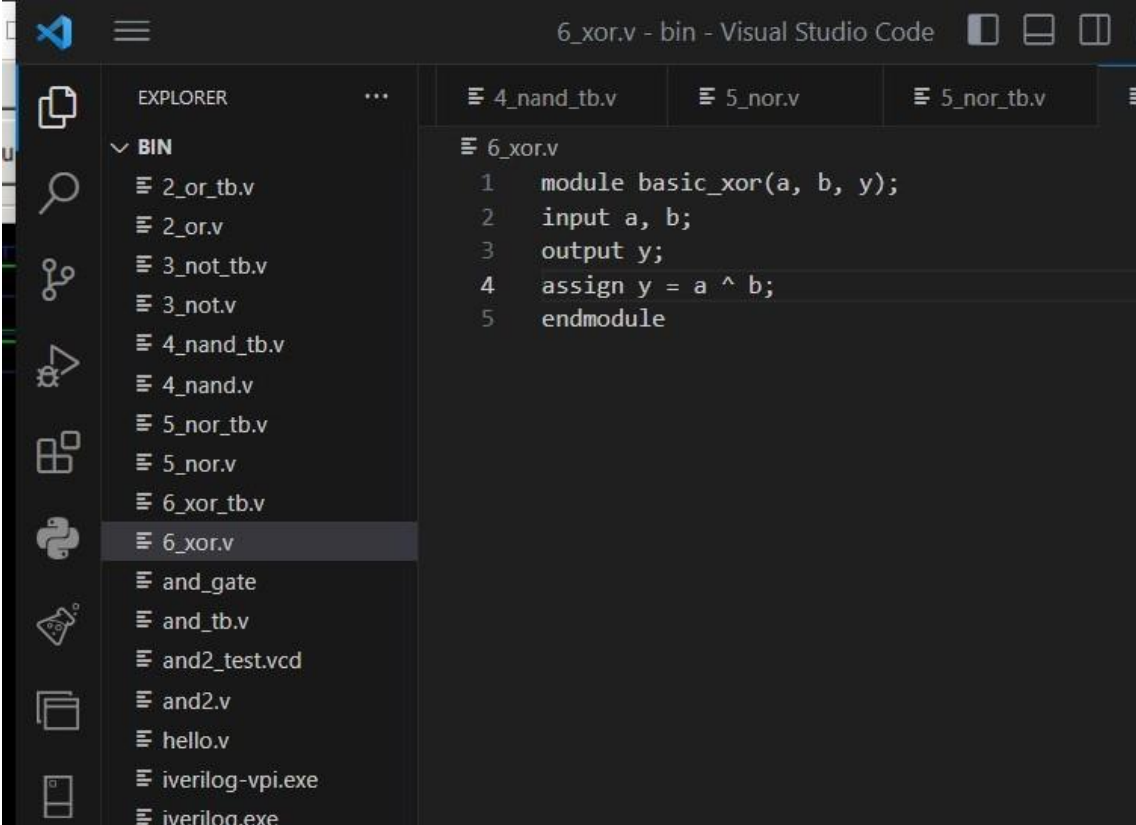
Week# ____1____

Program Number: ____6__

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT XOR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE

I. Verilog Code Screenshot



The screenshot shows the Visual Studio Code interface with a Verilog file named `6_xor.v` open. The Explorer sidebar on the left lists files in a directory named `BIN`, including `2_or_tb.v`, `2_or.v`, `3_not_tb.v`, `3_not.v`, `4_nand_tb.v`, `4_nand.v`, `5_nor_tb.v`, `5_nor.v`, `6_xor_tb.v`, `6_xor.v` (selected), `and_gate`, `and_tb.v`, `and2_test.vcd`, `and2.v`, `hello.v`, `iverilog-vpi.exe`, and `iverilog.exe`. The main editor area displays the Verilog code for `6_xor.v`:

```
1 module basic_xor(a, b, y);  
2   input a, b;  
3   output y;  
4   assign y = a ^ b;  
5 endmodule
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>iverilog -o test6 6_xor.v 6_xor_tb.v

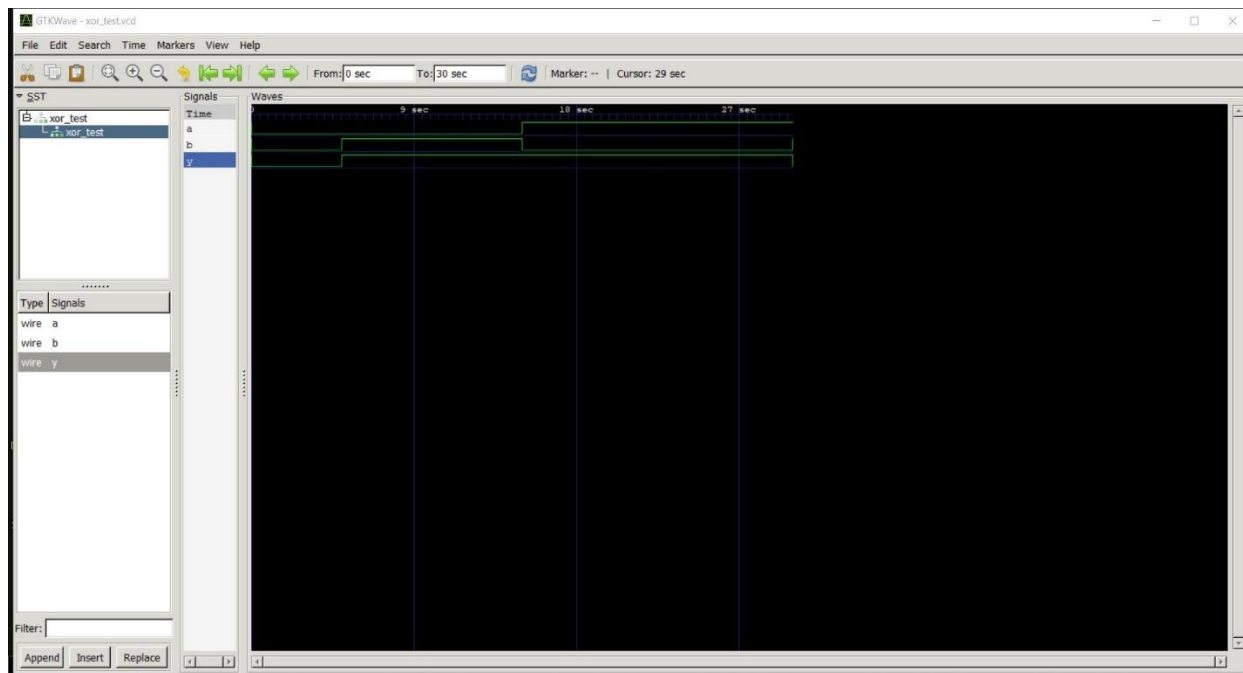
C:\iverilog\bin>vvp test6
VCD info: dumpfile xor_test.vcd opened for output.
      0a=0, b=0, y=0
      5a=0, b=1, y=1
     15a=1, b=0, y=1
     30a=1, b=1, y=0

C:\iverilog\bin>gtkwave xor_test.vcd

GTKWave Analyzer v3.3.100 (w)1999-2019 BSI

[0] start time.
[30] end time.
```

III. GTKWAVE Screenshot



IV. Output Table to be completed and included

a	b	y
0	0	0
0	1	1
1	0	1
1	1	0

Date: 10-08-2023

Name: Gurram Shreya	SRN: PES2UG22CS209	Section: D
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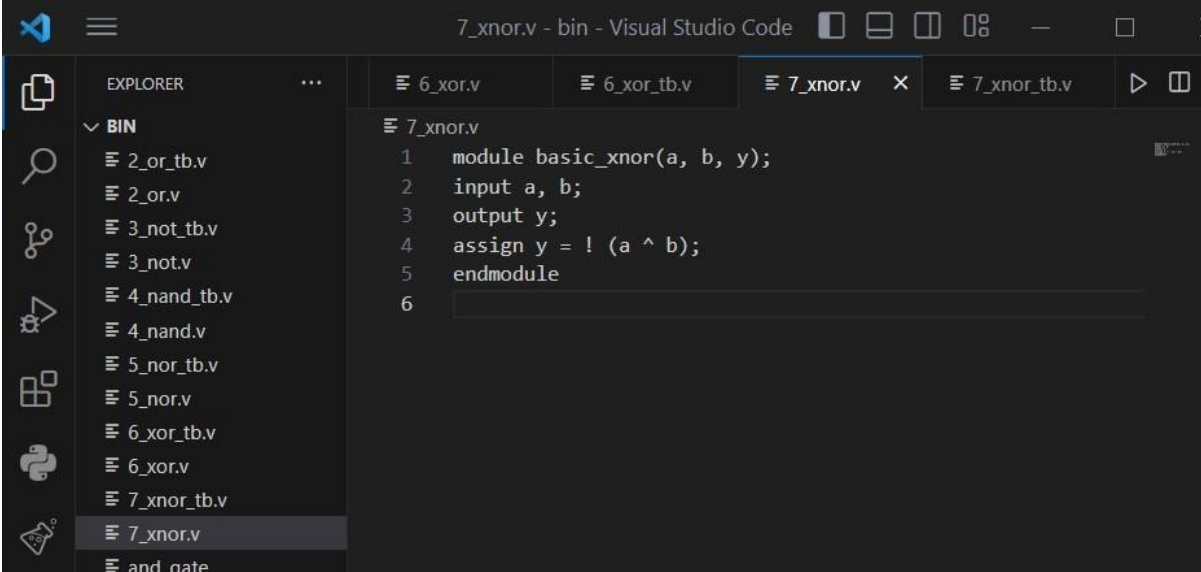
Week# 1

Program Number: 7

TITLE :

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT XNOR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE

I. Verilog Code Screenshot



The screenshot shows the Visual Studio Code interface with a Verilog file named 7_xnor.v open. The Explorer panel on the left shows a file tree with a 'BIN' folder containing various Verilog files, including 7_xnor.v which is currently selected. The main editor area displays the Verilog code for the basic_xnor module.

```
1 module basic_xnor(a, b, y);  
2   input a, b;  
3   output y;  
4   assign y = ! (a ^ b);  
5 endmodule  
6
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>iverilog -o test7 7_xnor.v 7_xnor_tb.v

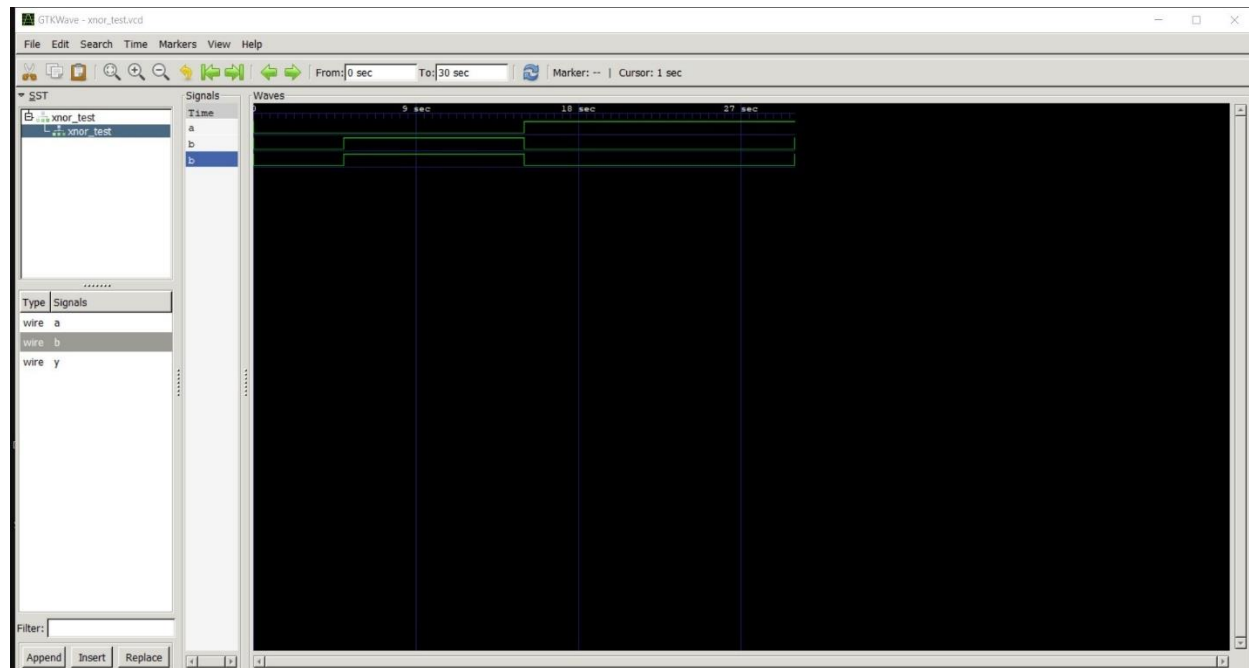
C:\iverilog\bin>vvp test7
VCD info: dumpfile xnor_test.vcd opened for output.
      0a=0, b=0, y=1
      5a=0, b=1, y=0
     15a=1, b=0, y=0
     30a=1, b=1, y=1

C:\iverilog\bin>gtkwave xnor_test.vcd

GTKWave Analyzer v3.3.100 (w)1999-2019 BSI

[0] start time.
[30] end time.
```

III. GTKWAVE Screenshot



IV. Output Table to be completed and included

a	b	y
0	0	1
0	1	0
1	0	0
1	1	1

Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature:

Name: Gurram Shreya

SRN: PES2UG22CS209

Section: D

Date: 10-08-2023