Digital Design and Computer Organisation Laboratory

UE22CS251A

3rd Semester, Academic Year 2023

Date: 16-08-2023

Name: K. Haripriya	SRN: PES2UG22CS243	Section: D

Week#____1_____ Program Number: ____1___

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT AND GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE

I. Verilog Code Screenshot

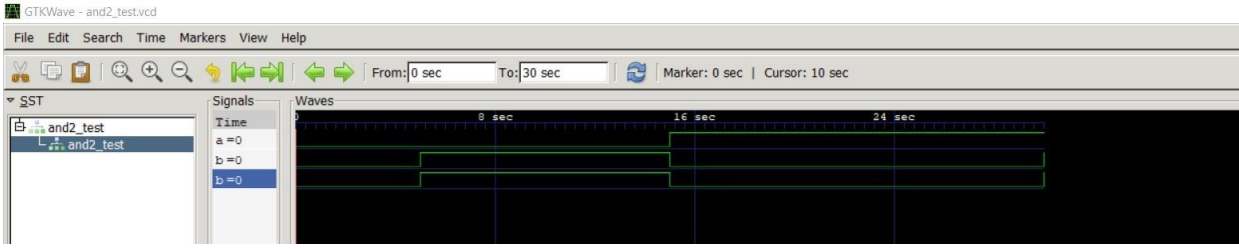
and2.v

```
1  module basic_and(a, b, y);
2  input a, b;
3  output y;
4  assign y = a & b;
5  endmodule
6
7
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>iverilog -o test1 and2.v and_tb.v

C:\iverilog\bin>vvp test1
VCD info: dumpfile and2_test.vcd opened for output.
                   0a=0, b=0, y=0
                   5a=0, b=1, y=0
                  15a=1, b=0, y=0
                  30a=1, b=1, y=1

C:\iverilog\bin>gtkwave and2_test.vcd
```

III. GTKWAVE Screenshot



IV. Output Table to be completed and included

a	b	y
0	0	0
0	1	0
1	0	0
1	1	1

Date: 16-08-2023

Name: K. Haripriya	SRN: PES2UG22CS243	Section: D

Week#____1_____ Program Number: ____2___

TITLE :

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT OR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE OR GATE TRUTH TABLE

I. Verilog Code Screenshot

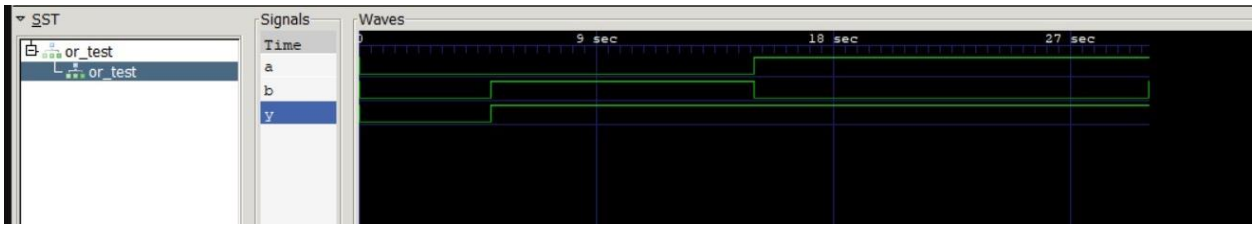
2_or.v

```
1  module basic_or(a, b, y);
2  input a, b;
3  output y;
4  assign y = a | b;
5  endmodule
```

II. Verilog VVP Output Screen Shot

```
^C
C:\iverilog\bin>iverilog -o test2 2_or.v 2_or_tb.v

C:\iverilog\bin>vvp test2
VCD info: dumpfile or_test.vcd opened for output.
                   0a=0, b=0, y=0
                   5a=0, b=1, y=1
                  15a=1, b=0, y=1
                  30a=1, b=1, y=1

C:\iverilog\bin>gtkwave or_test.vcd
```

III. GTKWAVE Screenshot



IV. Output Table to be completed and included

a	b	y
0	0	0
0	1	1
1	0	1
1	1	1

Date: 16-08-2023

Name: K. Haripriya	SRN: PES2UG22CS243	Section: D

Week#____1_____ Program Number: ____3___

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A NOT GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE NOT GATE TRUTH TABLE

I. Verilog Code Screenshot

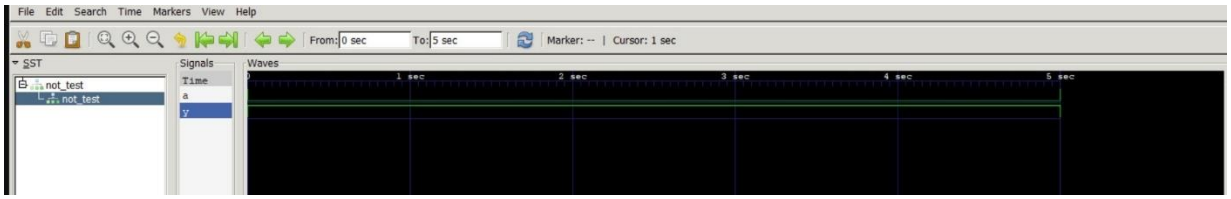
```
1   module basic_not(a, y);
2   input a;
3   output y;
4   assign y = ! a;
5   endmodule
```

II.

III. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>iverilog -o test3 3_not.v 3_not_tb.v

C:\iverilog\bin>vvp test 3
test: Unable to open input file.

C:\iverilog\bin>vvp test3
VCD info: dumpfile not_test.vcd opened for output.
                  0a=0, y=1
                  5a=1, y=0

C:\iverilog\bin>gtkwave not_test.vcd

GTKWave Analyzer v3.3.100 (w)1999-2019 BSI

[0] start time.
[5] end time.
```

IV. GTKWAVE Screenshot



V. Output Table to be completed and included

a	y
0	1
1	0

Date: 16-08-2023

Name: K. Haripriya	SRN: PES2UG22CS243	Section: D

Week#____1_____ Program Number: ____4___

TITLE :

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT NAND GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE NAND GATE TRUTH TABLE

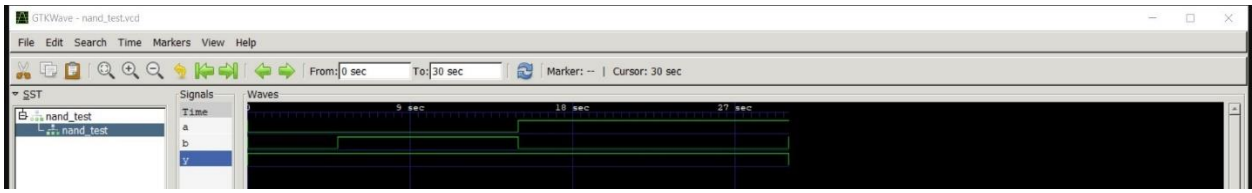
I. Verilog Code Screenshot

```
1   module basic_nand(a, b, y);
2   input a, b;
3   output y;
4   assign y = !(a & b);
5   endmodule
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>iverilog -o test4 4_nand.v 4_nand_tb.v

C:\iverilog\bin>vvp test4
VCD info: dumpfile nand_test.vcd opened for output.
                   0a=0, b=0, y=1
                   5a=0, b=1, y=1
                  15a=1, b=0, y=1
                  30a=1, b=1, y=0

C:\iverilog\bin>gtkwave nand_test.vcd
```

III. GTKWAVE Screenshot



IV. Output Table to be completed and included

a	b	y
0	0	1
0	1	1
1	0	1
1	1	0

Date: 16-08-2023

Name: K. Haripriya	SRN: PES2UG22CS243	Section: D

Week#____1_____ Program Number: ____5___

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT NOR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE NOR GATE TRUTH TABLE

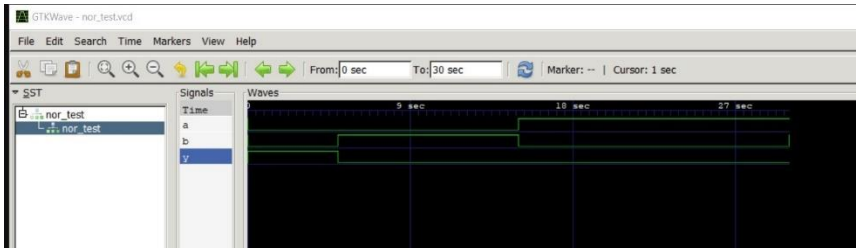
I. Verilog Code Screenshot

```
1  module basic_nor(a, b, y);
2  input a, b;
3  output y;
4  assign y =! (a | b);
5  endmodule
6
```

II. Verilog VVP Output Screen Shot

```
^C
C:\iverilog\bin>iverilog -o test5 5_nor.v 5_nor_tb.v

C:\iverilog\bin>vvp test5
VCD info: dumpfile nor_test.vcd opened for output.
                   0a=0, b=0, y=1
                   5a=0, b=1, y=0
                  15a=1, b=0, y=0
                  30a=1, b=1, y=0

C:\iverilog\bin>gtkwave nor_test.vcd
```

III. GTKWAVE Screenshot



IV. Output Table to be completed and included

a	b	y
0	0	1
0	1	0
1	0	0
1	1	0

Date: 16-08-2023

Name: K. Haripriya	SRN: PES2UG22CS243	Section: D

Week#____1_____ Program Number: ____6__

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT XOR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE

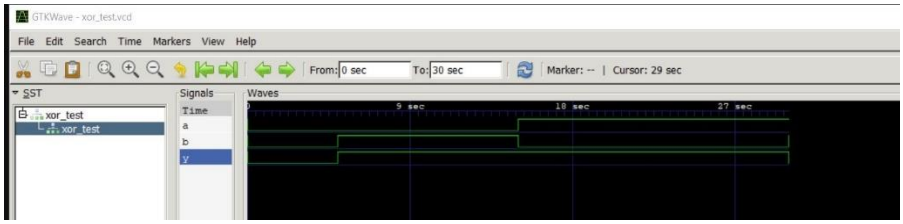
I. Verilog Code Screenshot

```
1   module basic_xor(a, b, y);
2   input a, b;
3   output y;
4   assign y = a ^ b;
5   endmodule
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>iverilog -o test6 6_xor.v 6_xor_tb.v

C:\iverilog\bin>vvp test6
VCD info: dumpfile xor_test.vcd opened for output.
                   0a=0, b=0, y=0
                   5a=0, b=1, y=1
                  15a=1, b=0, y=1
                  30a=1, b=1, y=0

C:\iverilog\bin>gtkwave xor_test.vcd
```

III. GTKWAVE Screenshot



IV. Output Table to be completed and included

a	b	y
0	0	0
0	1	1
1	0	1
1	1	0

Date: 16-08-2023

Name: K. Haripriya	SRN: PES2UG22CS243	Section: D

Week#____1_____ Program Number: ____7___

TITLE :

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT XNOR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE

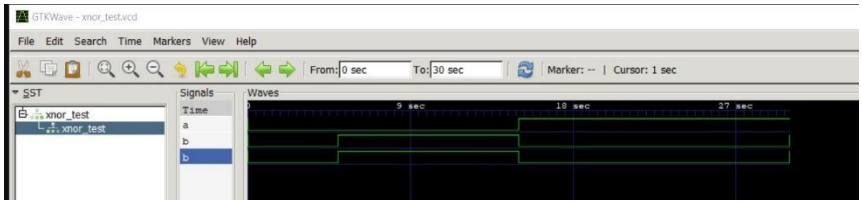
I. Verilog Code Screenshot

```
module basic_xnor(a, b, y);
input a, b;
output y;
assign y = ! (a ^ b);
endmodule
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>iverilog -o test7 7_xnor.v 7_xnor_tb.v

C:\iverilog\bin>vvp test7
VCD info: dumpfile xnor_test.vcd opened for output.
                   0a=0, b=0, y=1
                   5a=0, b=1, y=0
                  15a=1, b=0, y=0
                  30a=1, b=1, y=1

C:\iverilog\bin>gtkwave xnor_test.vcd
```

III. GTKWAVE Screenshot



IV. Output Table to be completed and included

a	b	y
0	0	1
0	1	0
1	0	0
1	1	1

Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature:

Name:

SRN:

Section: D

Date: 16-08-2023