

Digital Design and Computer Organization Laboratory

UE22CS251A

3rd Semester, Academic Year 2023-24

Date:

Name: Gurram Shreya	SRN: PES2UG22CS209	Section: D
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Week#__2_____

Program Number :__1_____

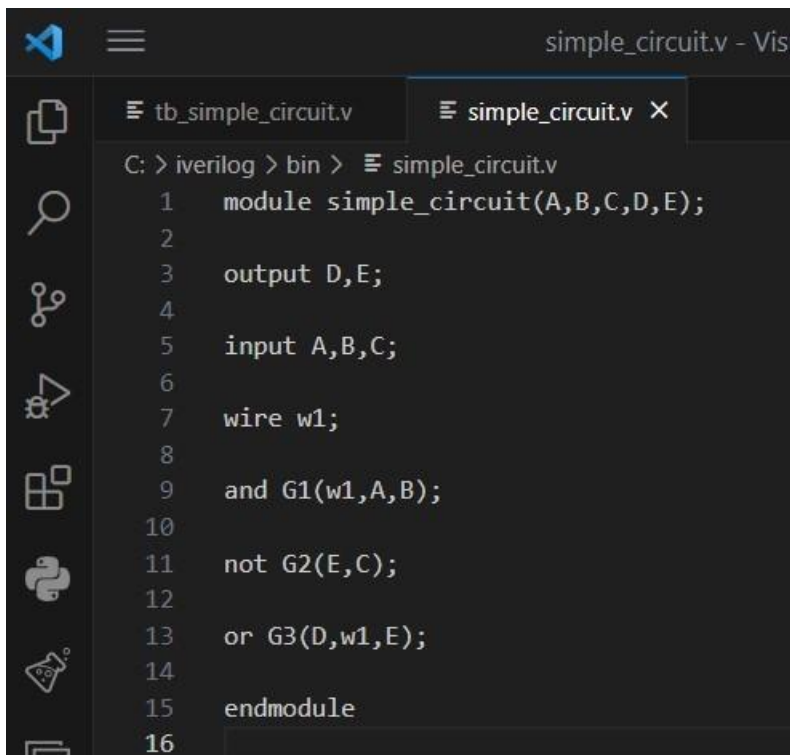
Title of the Program

SIMPLE_CIRCUIT

Aim:

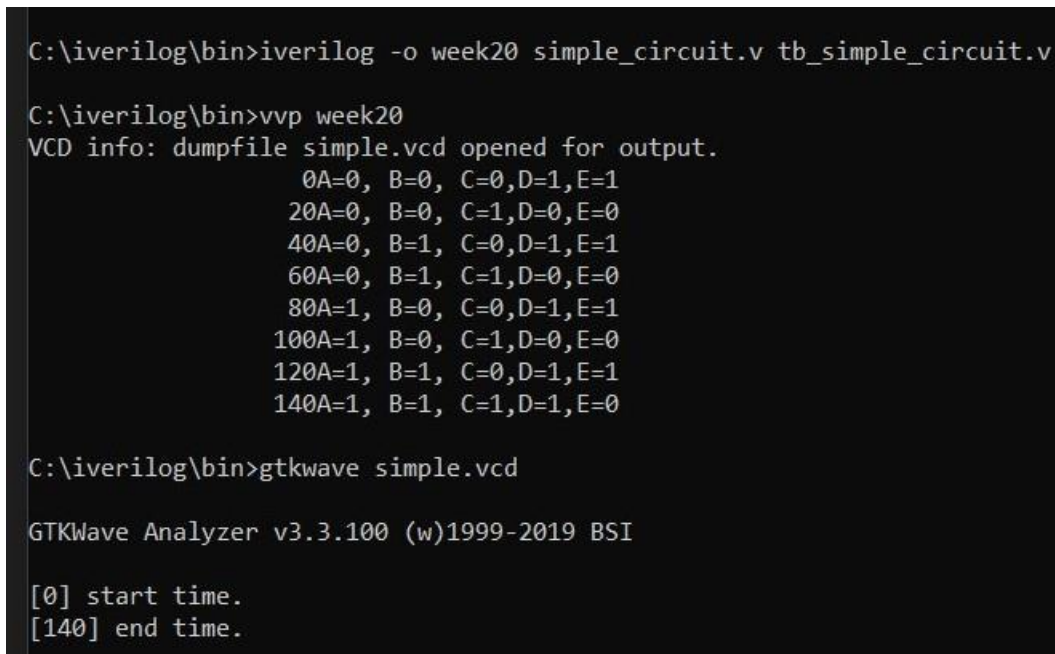
WRITE A VERILOG PROGRAM TO MODEL THE GIVEN SIMPLE CIRCUIT.GENERATE THE VVP OUTPUT AND VIEW THE SIMULATION WAVEFORM USING GTKWAVE.VERIFY THE OUTPUT AND WAVEFORM WITH THE RELEVANT TRUTH TABLE

1. Paste the Screen Shot of the source code

A screenshot of a Verilog code editor window titled 'simple_circuit.v - Vis'. The editor shows the source code for a Verilog module named 'simple_circuit'. The code includes input declarations for A, B, and C; output declarations for D and E; a wire declaration for w1; and logic gates: an AND gate G1, a NOT gate G2, and an OR gate G3. The code is as follows:

```
1  module simple_circuit(A,B,C,D,E);
2
3  output D,E;
4
5  input A,B,C;
6
7  wire w1;
8
9  and G1(w1,A,B);
10
11 not G2(E,C);
12
13 or G3(D,w1,E);
14
15 endmodule
16
```

2. Paste the Screen Shot of the VVP command output

A screenshot of a terminal window showing the execution of VVP and GTKWave commands. The terminal output is as follows:

```
C:\iverilog\bin>iverilog -o week20 simple_circuit.v tb_simple_circuit.v

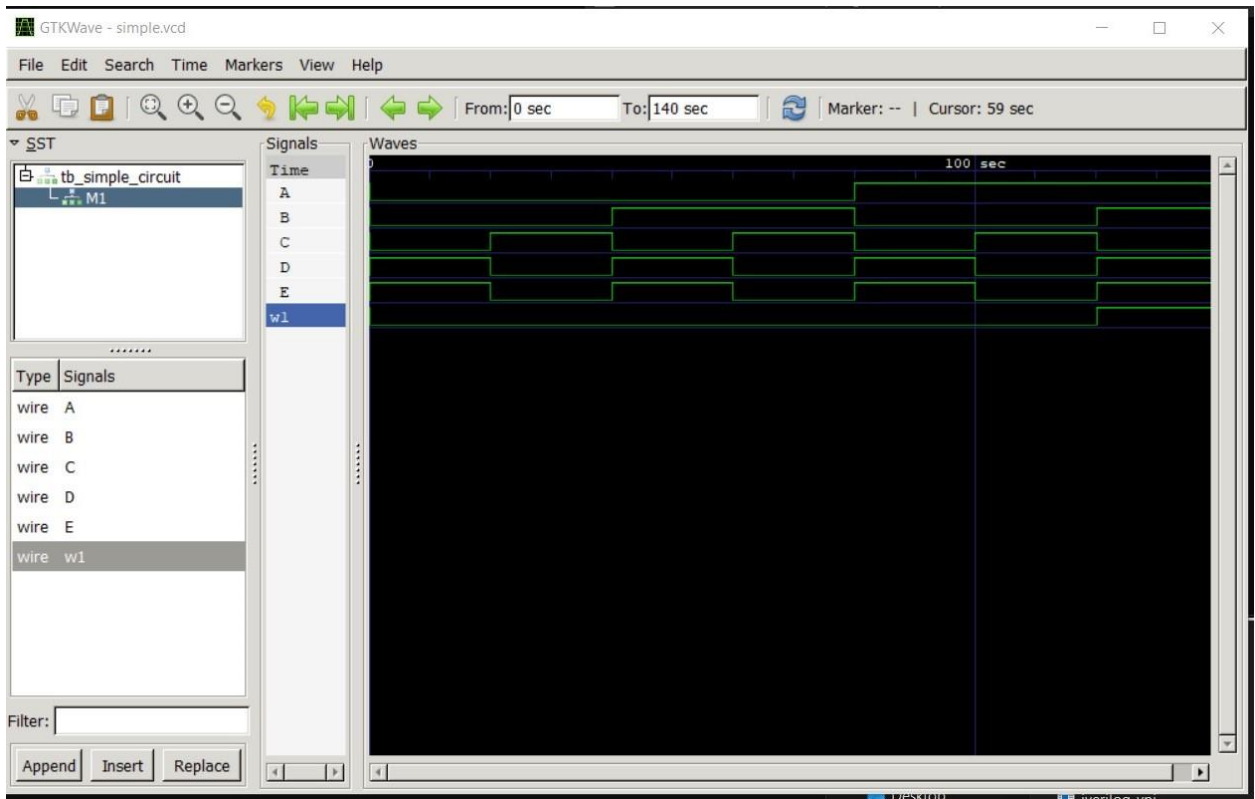
C:\iverilog\bin>vvp week20
VCD info: dumpfile simple.vcd opened for output.
      0A=0, B=0, C=0,D=1,E=1
      20A=0, B=0, C=1,D=0,E=0
      40A=0, B=1, C=0,D=1,E=1
      60A=0, B=1, C=1,D=0,E=0
      80A=1, B=0, C=0,D=1,E=1
     100A=1, B=0, C=1,D=0,E=0
     120A=1, B=1, C=0,D=1,E=1
     140A=1, B=1, C=1,D=1,E=0

C:\iverilog\bin>gtkwave simple.vcd

GTKWave Analyzer v3.3.100 (w)1999-2019 BSI

[0] start time.
[140] end time.
```

3. Paste the Screen shot of the GTKWave form



4. Include relevant Truth Table

A	B	C	D	E
0	0	0	1	1
0	0	1	0	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	1	1
1	1	1	1	0

Week#__2_____

Program Number: __2_____

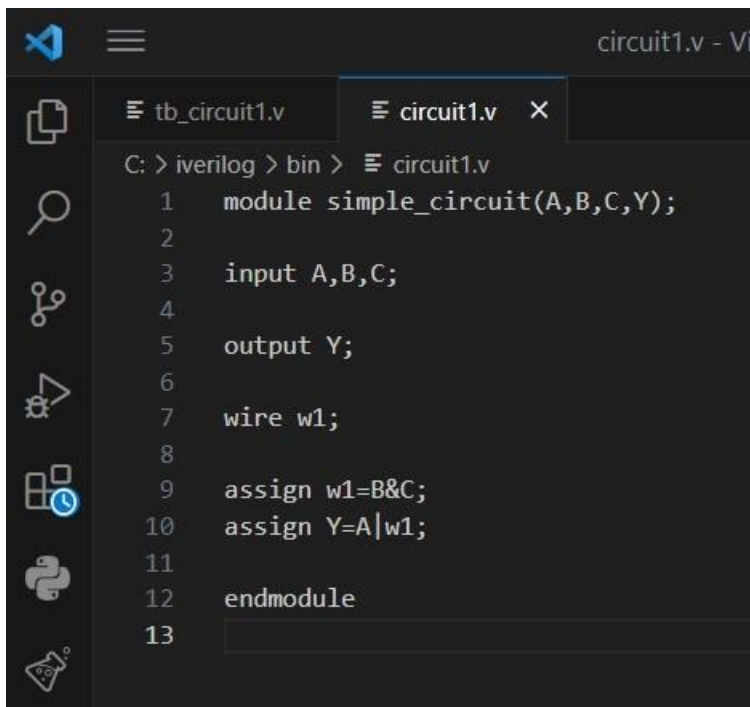
Title of the Program

CIRCUIT1

Aim:

**WRITE A VERILOG PROGRAM TO MODEL THE GIVEN CIRCUIT1.
GENERATE THE VVP OUTPUT AND VIEW THE SIMULATION
WAVEFORM USING GTKWAVE.VERIFY THE OUTPUT AND
WAVEFORM WITH THE RELEVANT TRUTH TABLE**

1. Paste the Screen Shot of the source code

A screenshot of a text editor window titled 'circuit1.v - Vi'. The editor shows a Verilog module named 'simple_circuit' with inputs A, B, C and output Y. The code is as follows:

```
1  module simple_circuit(A,B,C,Y);  
2  
3  input A,B,C;  
4  
5  output Y;  
6  
7  wire w1;  
8  
9  assign w1=B&C;  
10 assign Y=A|w1;  
11  
12 endmodule  
13
```

The left sidebar of the editor shows various icons for file operations, search, and simulation. The top of the window has a menu bar and a tab for 'circuit1.v'.

2. Paste the Screen Shot of the VVP command output

```

C:\iverilog\bin>iverilog -o week21 circuit1.v tb_circuit1.v

C:\iverilog\bin>vvp week21
VCD info: dumpfile circuit1.vcd opened for output.
      0A=0, B=0, C=0,Y=0
     20A=0, B=0, C=1,Y=0
     40A=0, B=1, C=0,Y=0
     60A=0, B=1, C=1,Y=1
     80A=1, B=0, C=0,Y=1
    100A=1, B=0, C=1,Y=1
    120A=1, B=1, C=0,Y=1
    140A=1, B=1, C=1,Y=1

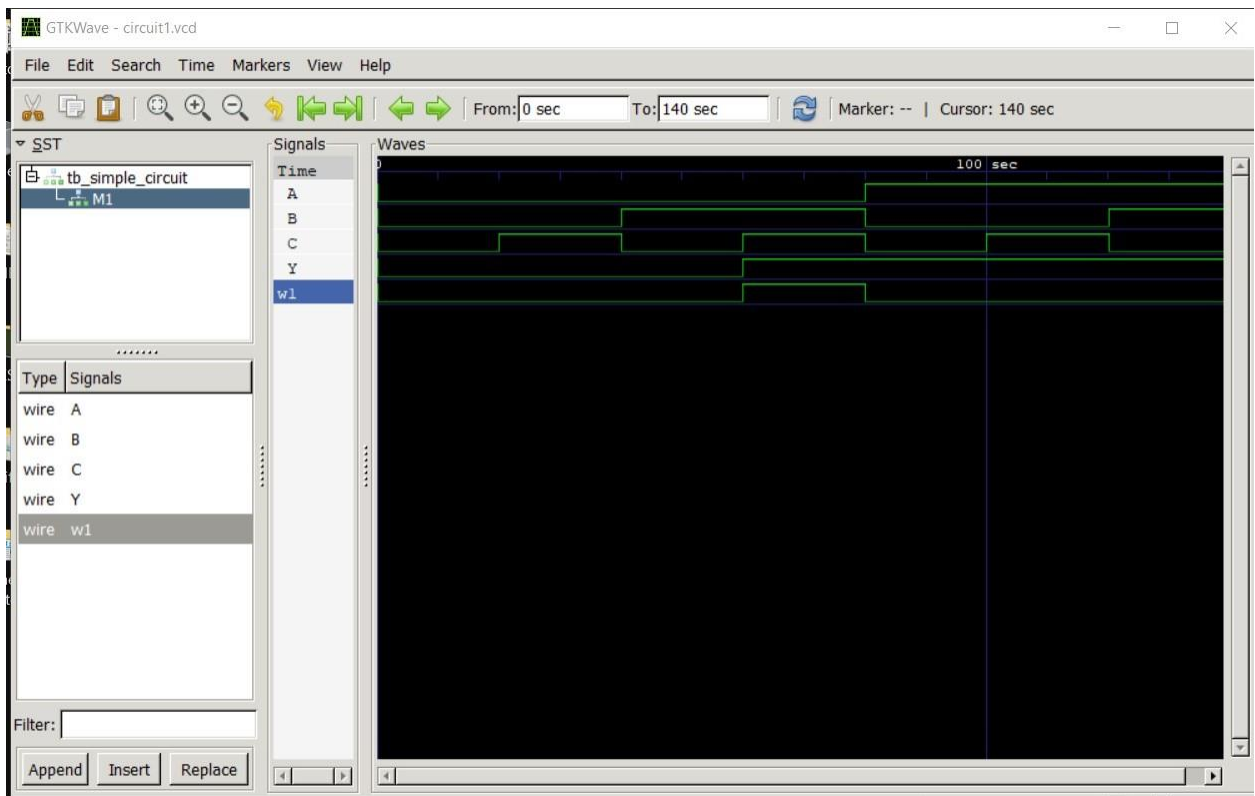
C:\iverilog\bin>gtkwave circuit1.vcd

GTKWave Analyzer v3.3.100 (w)1999-2019 BSI

[0] start time.
[140] end time.

```

3. Paste the Screen shot of the GTKWave form



4. Include relevant Truth Table

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Week# __2__

Program Number: __3__

Title of the Program

CIRCUIT2

Aim:

**WRITE A VERILOG PROGRAM TO MODEL THE GIVEN CIRCUIT2.
GENERATE THE VVP OUTPUT AND VIEW THE SIMULATION
WAVEFORM USING GTKWAVE.VERIFY THE OUTPUT AND
WAVEFORM WITH THE RELEVANT TRUTH TABLE**

1. Paste the Screen Shot of the source code

```
circuit2.v X
C: > iverilog > bin > circuit2.v
1  module simple_circuit(A,B,C,Y);
2
3  output Y;
4
5  input A,B,C;
6
7  wire w1,w2,w3;
8
9  assign w1=B&C ;
10 assign w2=A|w1;
11 assign w3=A&B ;
12 assign Y= w2|w3 ;
13
14 endmodule
15
```

2. Paste the Screen Shot of the VVP command output

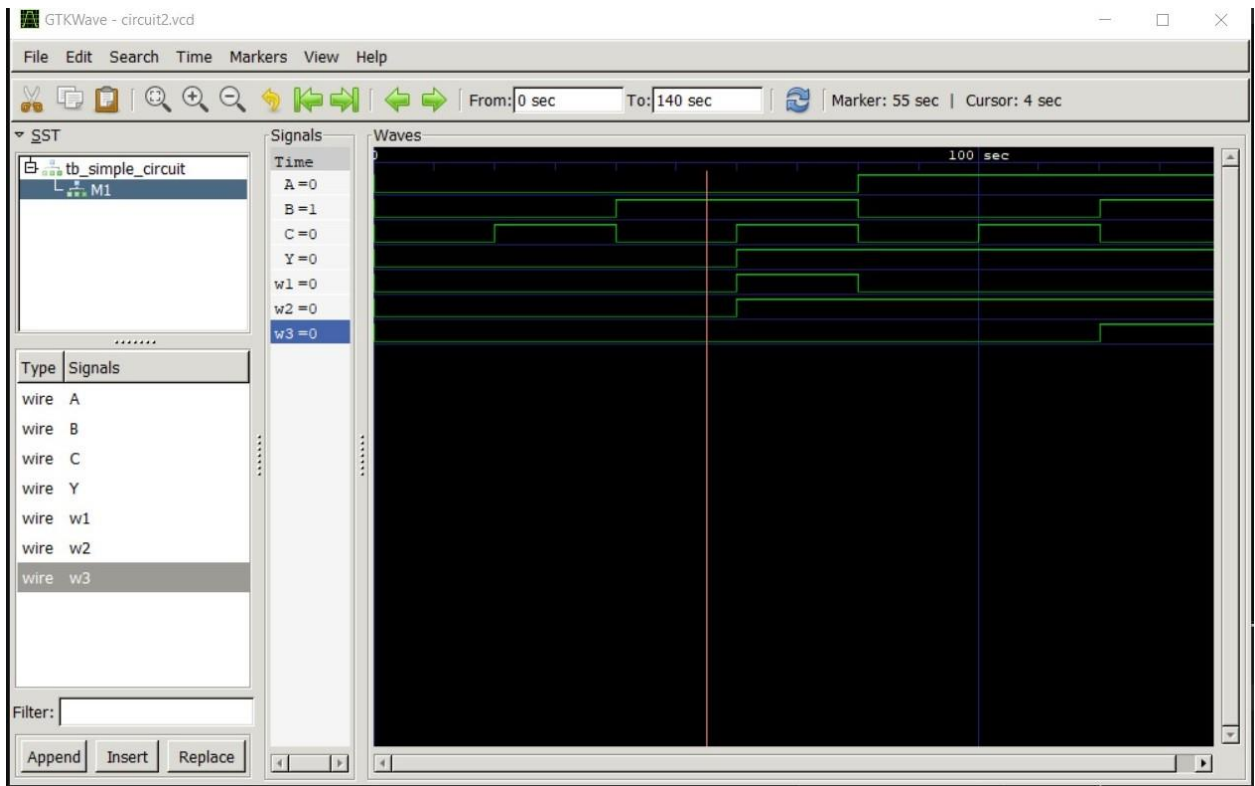
```
C:\iverilog\bin>iverilog -o week22 circuit2.v tb_circuit2.v
C:\iverilog\bin>vvp week22
VCD info: dumpfile circuit2.vcd opened for output.
      0A2=0, B2=0, C2=0,Y=0
     20A2=0, B2=0, C2=1,Y=0
     40A2=0, B2=1, C2=0,Y=0
     60A2=0, B2=1, C2=1,Y=1
     80A2=1, B2=0, C2=0,Y=1
    100A2=1, B2=0, C2=1,Y=1
    120A2=1, B2=1, C2=0,Y=1
    140A2=1, B2=1, C2=1,Y=1

C:\iverilog\bin>gtkwave circuit2.vcd

GTKWave Analyzer v3.3.100 (w)1999-2019 BSI

[0] start time.
[140] end time.
```

3. Paste the Screen shot of the GTKWave form



4. Include relevant Truth Table

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature:

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Section: D:

Date: 17-08-2023