普 誠 科 技
Princeton Technology Corp.

DESCRIPTION

PT6955 is an LED Controller driven on a 1/4 to 1/7 duty factor. Twelve/nine segment output lines, 4 to 7 grid output lines, one display memory, control circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip microcomputer. Serial data is fed to PT6955 via a three-line serial interface. Housed in a 24-pin SOP, PT6955's pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.
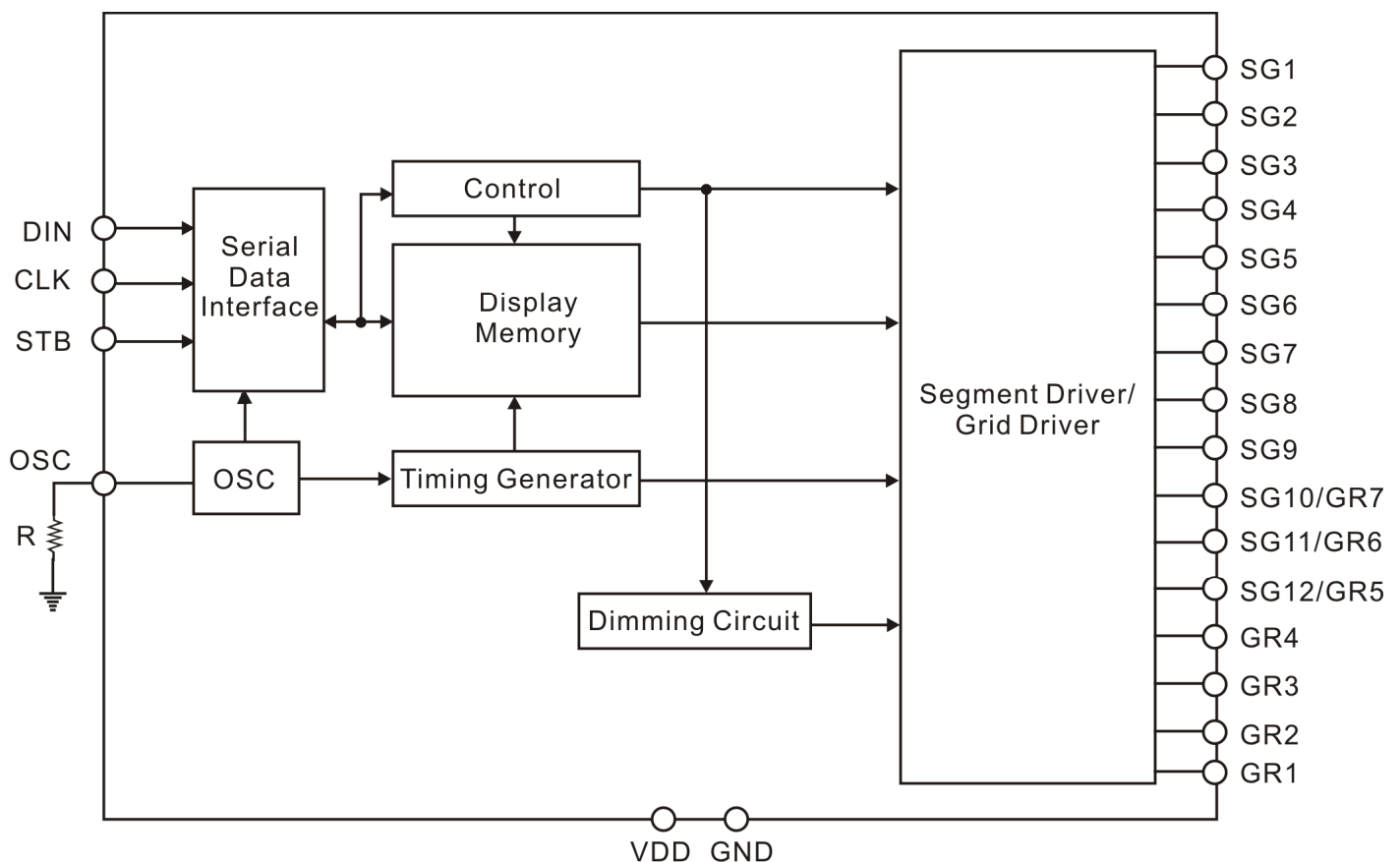
FEATURES

- CMOS Technology
- Low Power Consumption
- 8-Step Dimming Circuitry
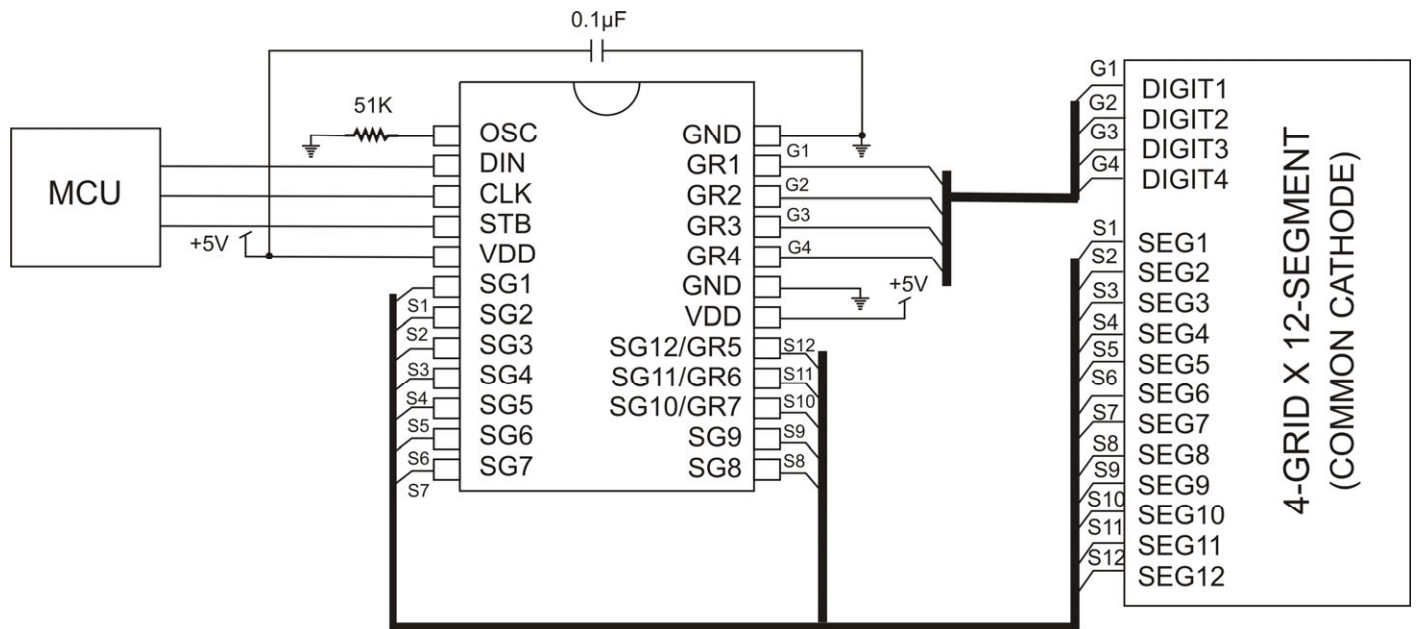- Serial Interface for Clock, Data Input, Strobe Pins
- Available in 24-pin, SOP

APPLICATION
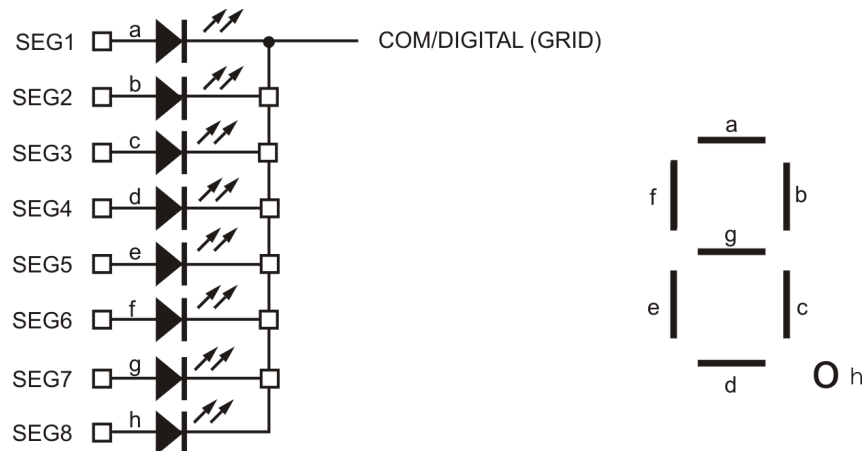
- Micro-computer Peripheral Device

BLOCK DIAGRAM

APPLICATION CIRCUIT

Notes:
1. The capacitor (0.1μF) connected between the GND and VDD Pins must be located as near as possible to the PT6955 chip.
2. The PT6955 power supply is separate from the application system power supply.
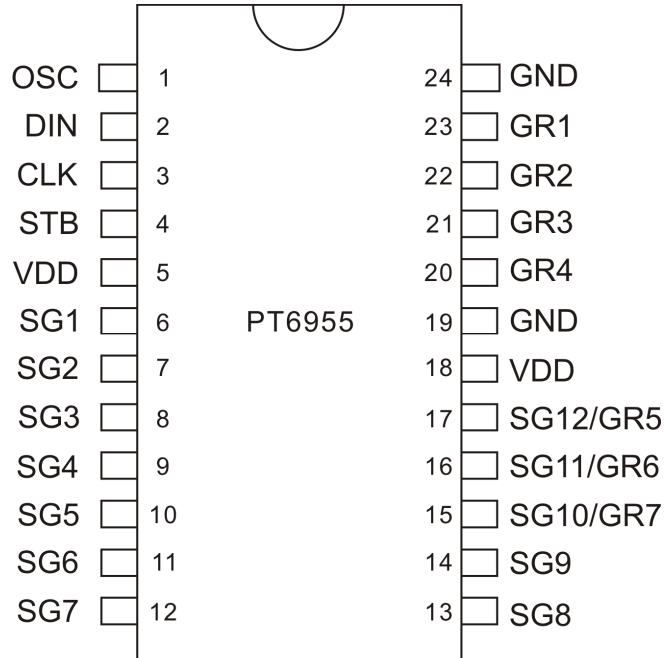
COMMON CATHODE TYPE LED PANEL

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6955	24pins, SOP, 300mil	PT6955

PIN CONFIGURATION

```
           ┌───────⌒───────┐
   OSC  ─□ │ 1          24 │ □─  GND
   DIN  ─□ │ 2          23 │ □─  GR1
   CLK  ─□ │ 3          22 │ □─  GR2
   STB  ─□ │ 4          21 │ □─  GR3
   VDD  ─□ │ 5          20 │ □─  GR4
   SG1  ─□ │ 6   PT6955 19 │ □─  GND
   SG2  ─□ │ 7          18 │ □─  VDD
   SG3  ─□ │ 8          17 │ □─  SG12/GR5
   SG4  ─□ │ 9          16 │ □─  SG11/GR6
   SG5  ─□ │ 10         15 │ □─  SG10/GR7
   SG6  ─□ │ 11         14 │ □─  SG9
   SG7  ─□ │ 12         13 │ □─  SG8
           └───────────────┘
```

PIN DESCRIPTION

| Pin Name	I/O	Description	Pin No.
OSC	I	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation frequency	1
DIN	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit)	2
CLK	I	Clock Input Pin This pin reads serial data at the rising edge.	3
STB	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this pin is "HIGH", CLK is ignored.	4
VDD	-	Power Supply	5, 18
SG1 ~ SG9	O	Segment Output Pins (p-channel, open drain)	6 ~ 14
SG10/GR7 ~ SG12/GR5	O	Segment Output Pin/Grid Output Pin (CMOS Output)	15 ~ 17
GND	-	Ground Pin	19, 24
GR4 ~ GR1	O	Grid Output Pins (n-channel, open drain)	20 ~ 23

INPUT/OUTPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below.
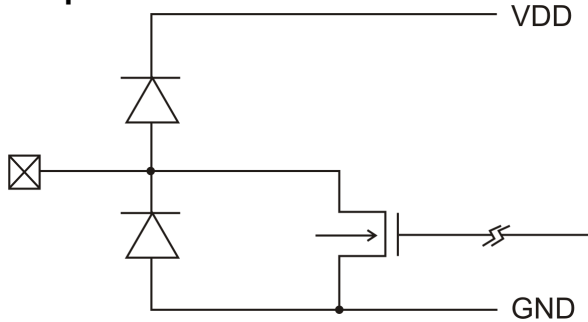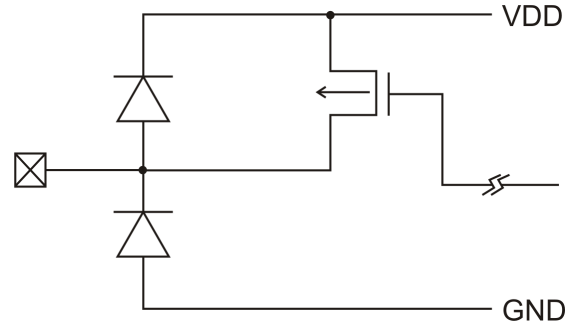
Input Pins: CLK, STB & DIN

GND
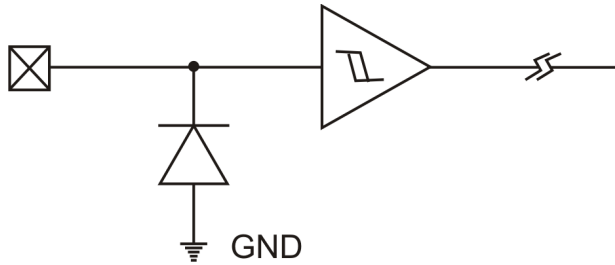
Output Pins: SG10/GR7, SG11/GR6, SG12/GR5

VDD

GND
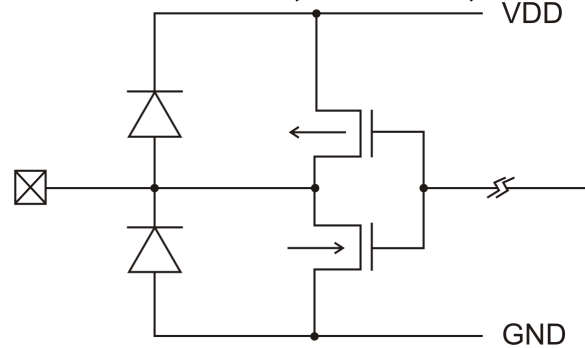
Output Pins: GR1 to GR4

VDD

GND

Output Pins: SG1 to SG9

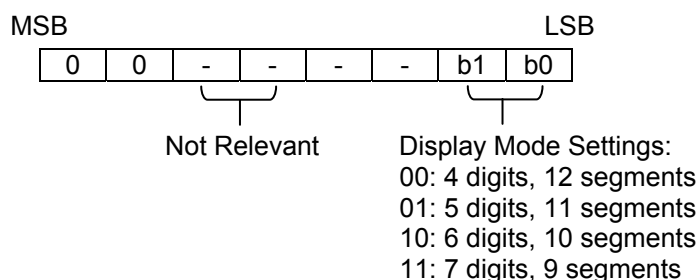VDD

GND

FUNCTION DESCRIPTION

COMMANDS

A command is the first byte (b0 to b7) inputted to PT6955 via the DIN Pin after STB Pin has changed from "HIGH" to "LOW" State. If for some reason the STB Pin is set to "HIGH" while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

COMMAND 1: DISPLAY MODE SETTING COMMANDS

PT6955 provides 4 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to PT6955 via the DIN Pin when STB is "LOW". However, for these commands, Bit No. 3 to Bit No.6 (b2 to b5) are ignored, Bit No.7 & Bit No.8 (b6 to b7) are given a value of "0".

The Display Mode Setting Commands determine the number of segments and grids to be used (1/4 to 1/7 duty, 12 to 9 segments). When these commands are executed, the display is forcibly turned off. A display command "ON" must be executed in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.
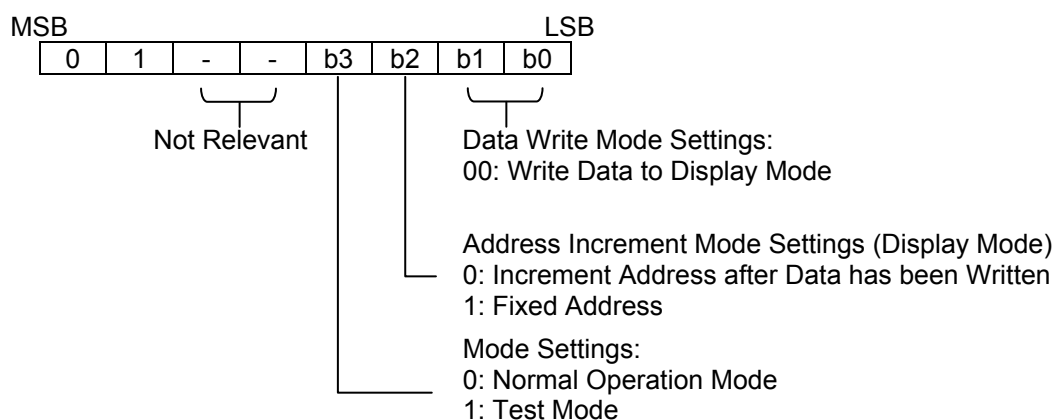
When Power is turned "ON", the 7-Grid, 9-Segment Mode is selected.

MSB   LSB

0	0	-	-	-	-	b1	b0

Not Relevant   Display Mode Settings:
                      00: 4 digits, 12 segments
                      01: 5 digits, 11 segments
                      10: 6 digits, 10 segments
                      11: 7 digits, 9 segments

COMMAND 2: DATA SETTING COMMANDS

The Data Setting Commands executes the Data Write Mode for PT6955. The Data Setting Command, the bits 5 and 6 (b4, b5) are ignored, bit 7 (b6) is given the value of "1" while bit 8 (b7) is given the value of "0". Please refer to the diagram below.

When power is turned ON, bit 4 to bit 1 (b3 to b0) are given the value of "0".

MSB   LSB

0	1	-	-	b3	b2	b1	b0

Not Relevant   Data Write Mode Settings:
                            00: Write Data to Display Mode

                            Address Increment Mode Settings (Display Mode)
                            0: Increment Address after Data has been Written
                            1: Fixed Address

                            Mode Settings:
                            0: Normal Operation Mode
                            1: Test Mode

COMMAND 3: ADDRESS SETTING COMMANDS

Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of "00H" to 0DH". If the address is set to 0EH or higher, the data is
ignored until a valid address is set. When power is turned ON, the address is set at "00H".

Please refer to the diagram below.

MSB							LSB
1	1	-	-	b3	b2	b1	b0

Not Relevant

Address: 00H to 0DH
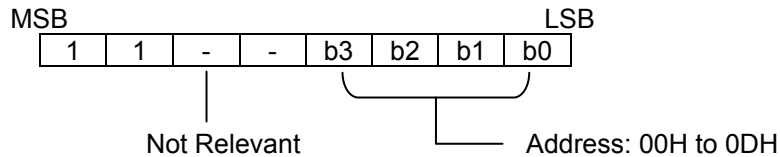
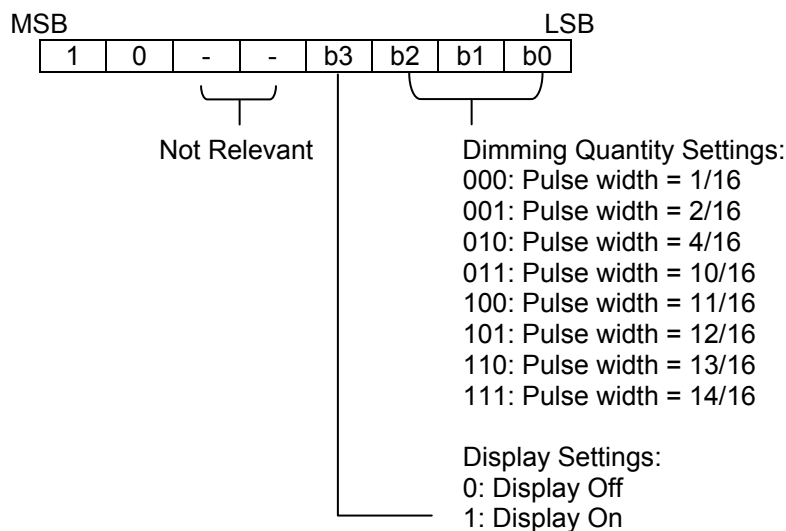## *DISPLAY MODE AND RAM ADDRESS*

Data transmitted from an external device to PT6955 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM Addresses of PT6955 are given below in 8 bits unit.

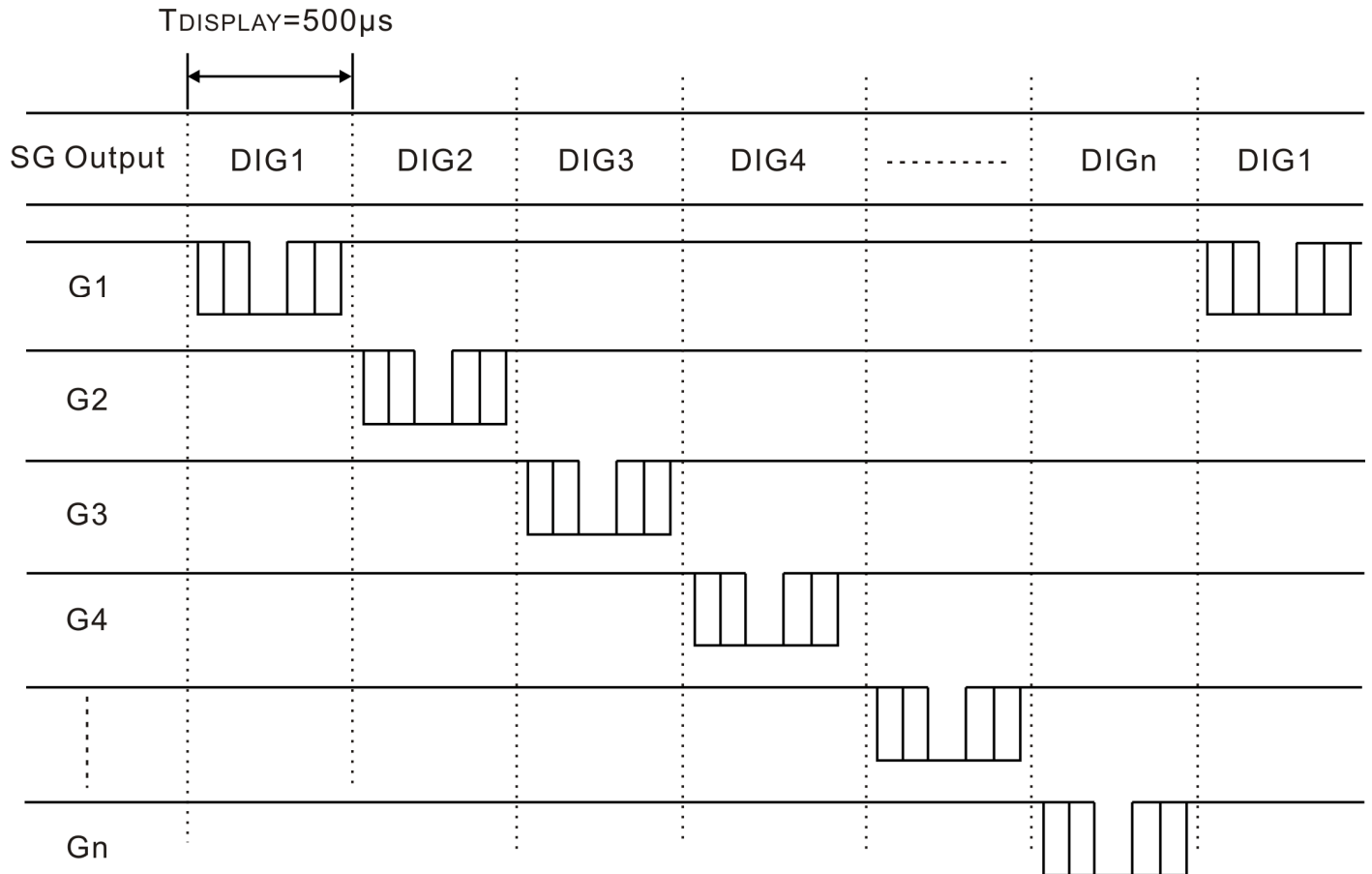| SG1	SG4	SG5	SG8	SG9	SG12	
00HL		00HU		01HL		DIG1
02HL		02HU		03HL		DIG2
04HL		04HU		05HL		DIG3
06HL		06HU		07HL		DIG4
08HL		08HU		09HL		DIG5
0AHL		0AHU		0BHL		DIG6
0CHL		0CHU		0DHL		DIG7

b0	b3	b4	b7
xxHL		xxHU	
Lower 4 bits		Higher 4 bits	

COMMAND 4: DISPLAY CONTROL COMMANDS

The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF.

MSB							LSB
1	0	-	-	b3	b2	b1	b0

Not Relevant

Dimming Quantity Settings:
000: Pulse width = 1/16
001: Pulse width = 2/16
010: Pulse width = 4/16
011: Pulse width = 10/16
100: Pulse width = 11/16
101: Pulse width = 12/16
110: Pulse width = 13/16
111: Pulse width = 14/16

Display Settings:
0: Display Off
1: Display On

DISPLAY TIMING WAVEFORM

TDISPLAY=500μs

| SG Output | DIG1 | DIG2 | DIG3 | DIG4 | .... | DIGn | DIG1 |

G1

G2

G3

G4

Gn

SERIAL COMMUNICATION FORMAT

The following diagram shows the PT6955 serial communication format.

RECEPTION (DATA/COMMAND WRITE)

If data continues

STB

DIN   b0   b1   b2   ....   b6   b7

CLK   1   2   3   7   8
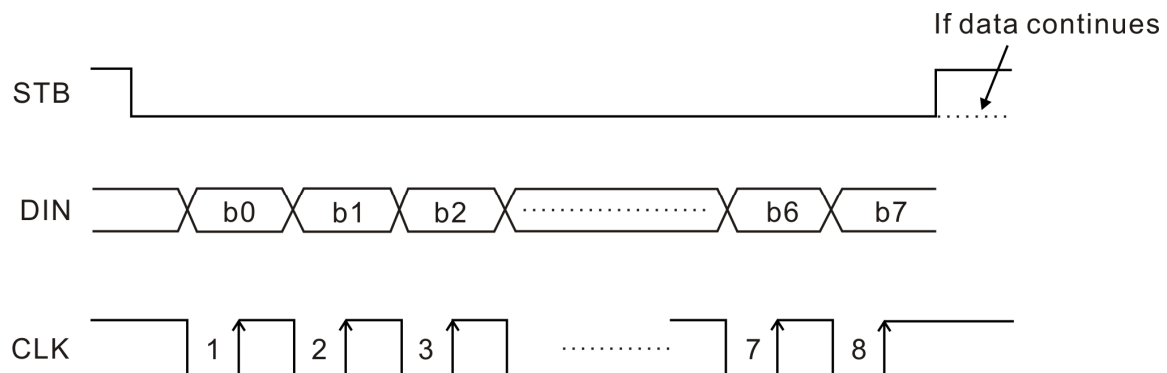
SWITCHING CHARACTERISTICS WAVEFORM
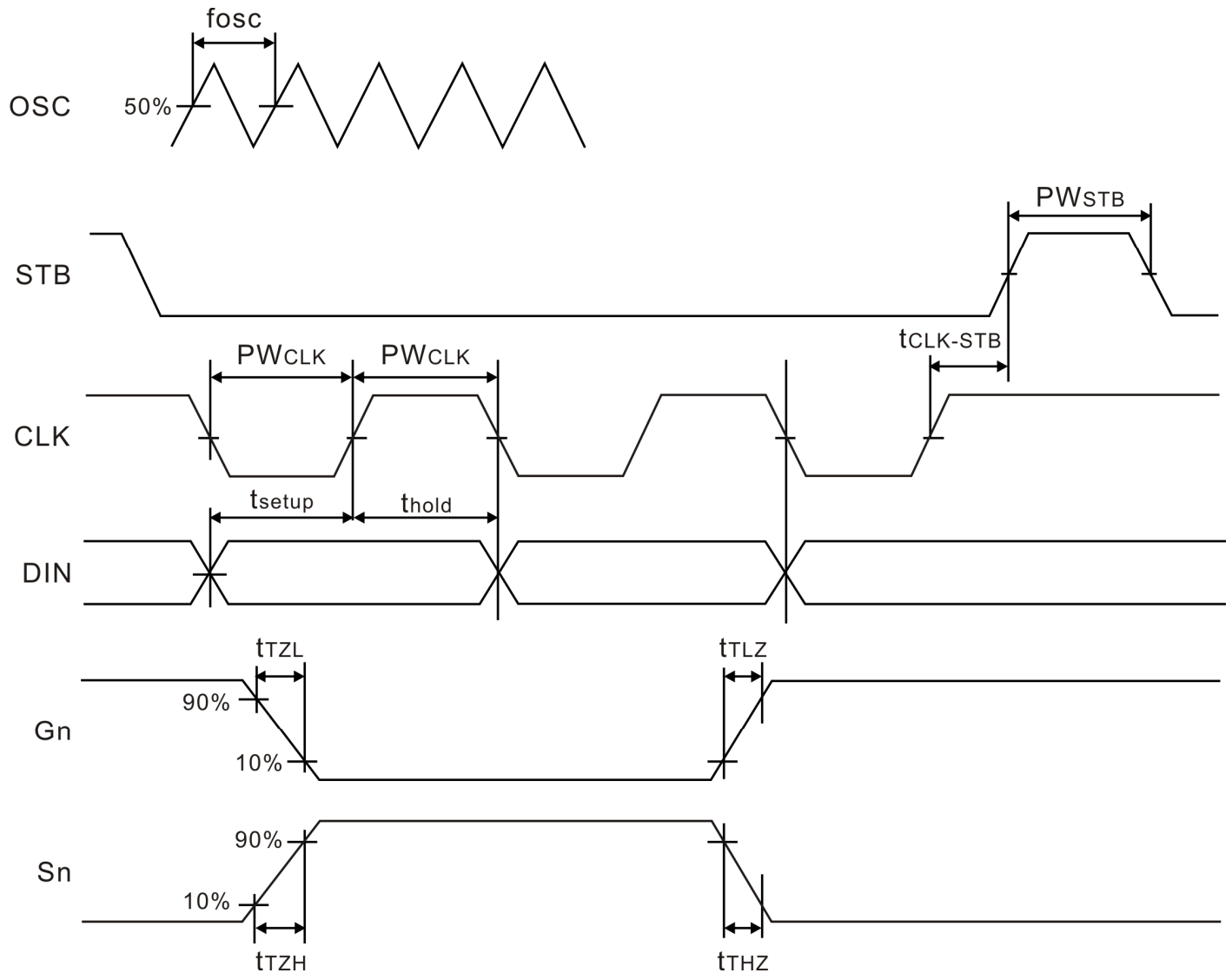
where:

PW$_{CLK}$ (Clock Pulse Width) ≥ 400ns

t$_{setup}$ (Data Setup Time) ≥100ns

t$_{CLK-STB}$ (Clock - Strobe Time) ≥ 1μs

t$_{TZH}$ (Rise Time) ≤ 1 μs

t$_{TZL}$ ≤ 1μs

PW$_{STB}$ (Strobe Pulse Width) ≥ 1μs

t$_{hold}$ (Data Hold Time) ≥ 100ns

t$_{THZ}$ (Fall Time) ≤ 10μs
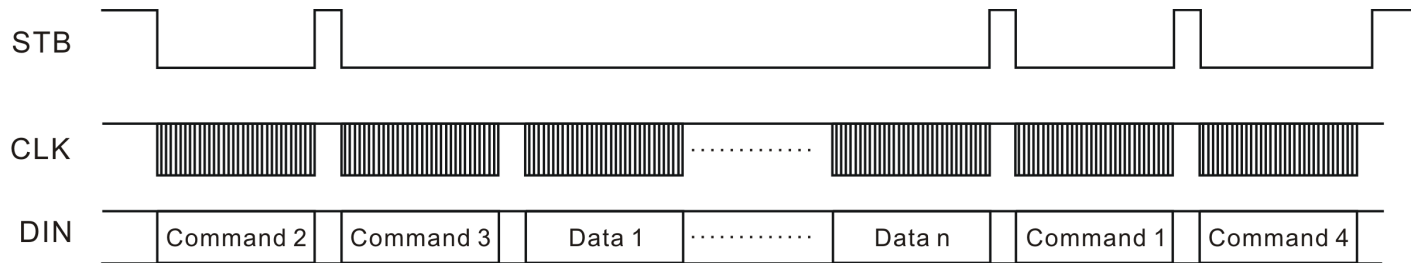
fosc = Oscillation Frequency

t$_{TLZ}$ ≤ 10μs

APPLICATIONS

Display memory is updates by incrementing addresses. Please refer to the following diagram.

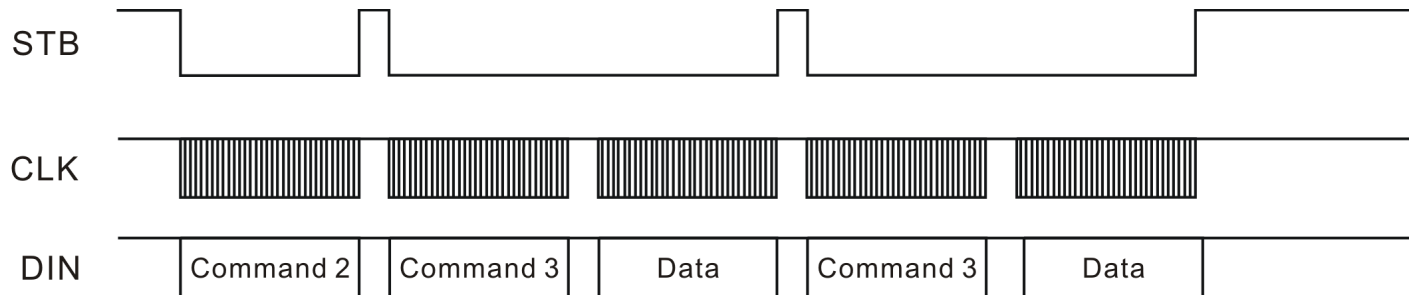where:
Command 1: Display Mode Setting Command
Command 2: Data Setting Command
Command 3: Address Setting Command
Data 1 to n: Transfer Display Data (14 Byte max.)
Command 4: Display Control Command

The following diagram shows the waveforms when updating specific addresses.
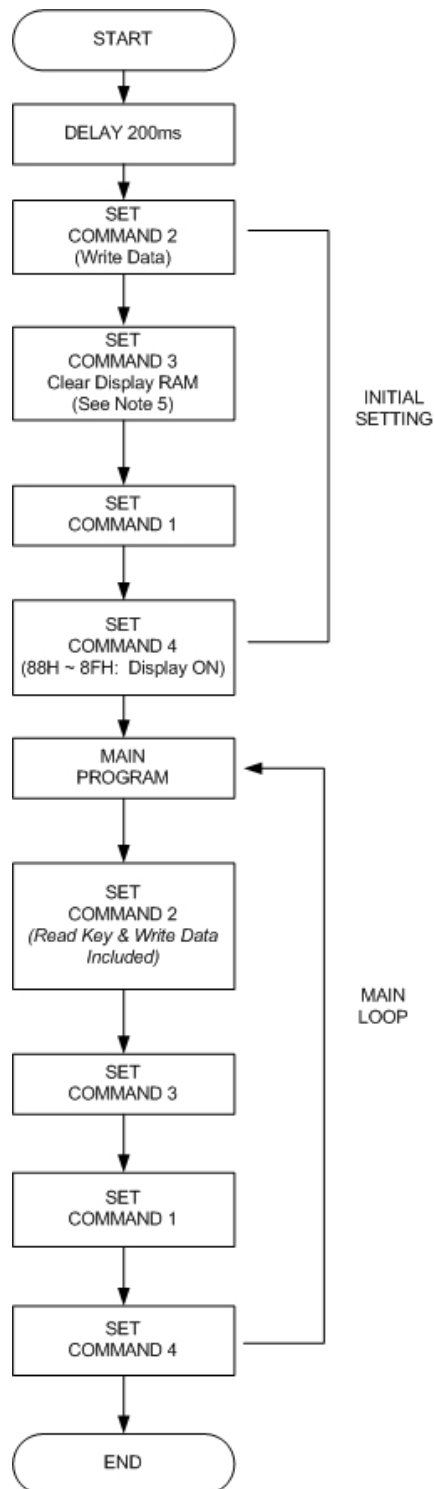

where:
Command 2: Data Setting Command
Command 3: Address Setting Command
Data: Display Data

RECOMMENDED SOFTWARE FOLWCHART

Notes:
1. Command 1: Display Mode Commands
2. Command 2: Data Setting Commands
3. Command 3: Address Setting Commands
4. Command 4: Display Control Commands
5. When IC power is applied for the first time, the contents of the Display RAM are not defined; thus, it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

SOP 24L (300MIL) THERMAL PERFORMANCE IN STILL AIR

JUNCTION TEMPERATURE: 100℃
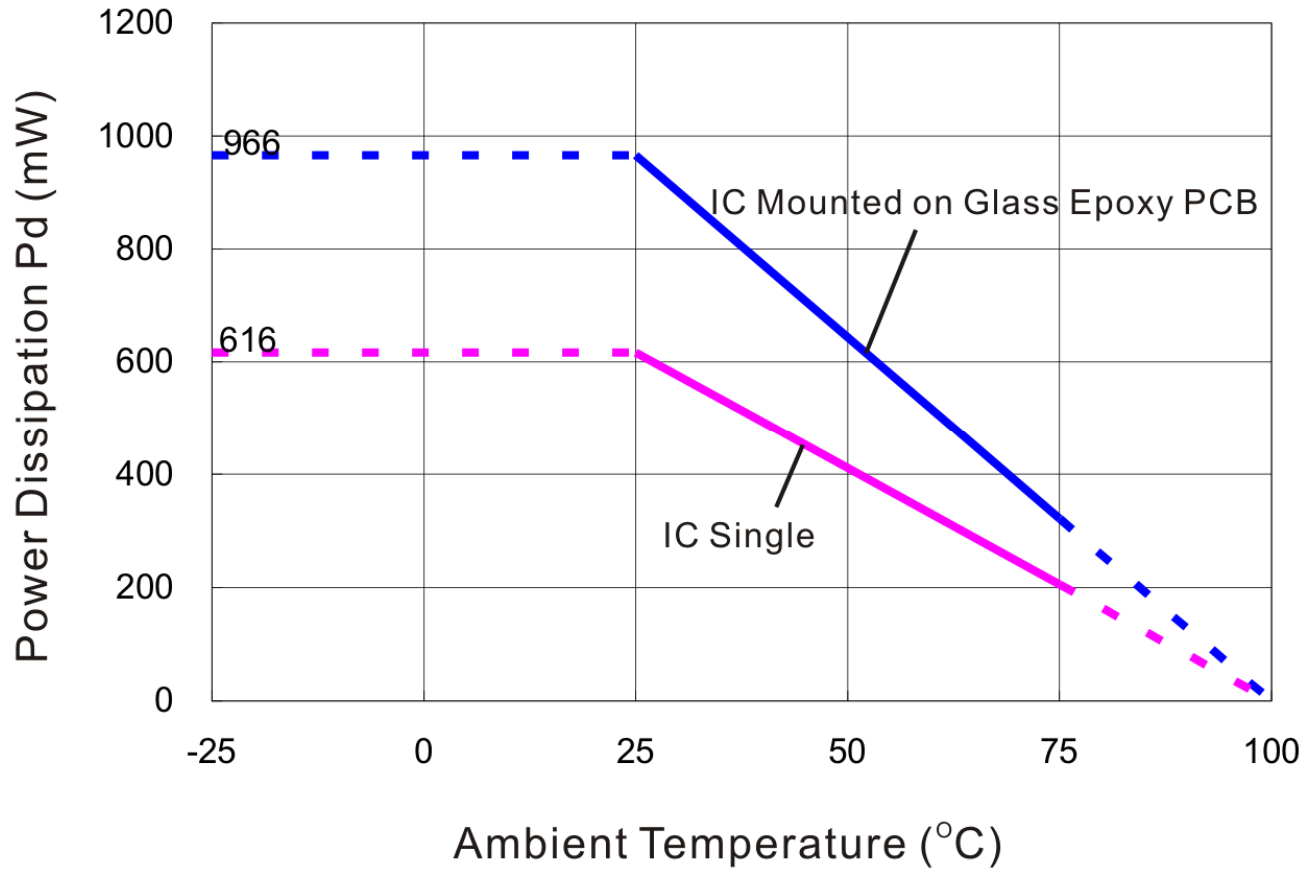
ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta=25℃, GND=0V)

Parameter	Symbol	Rating	Units
Supply Voltage	VDD	-0.3 to +7.0	V
Logic Input Voltage	VI	-0.3 to VDD+0.3	V
Driver Output Current/Pin	IOLGR	+250	mA
	IOHSG	-50	mA
Maximum Driver Output Current/Total	ITOTAL	400	mA
Operating Temperature	Topr	-40 ~ +85	℃
Storage Temperature	Tstg	-40 ~ +150	℃

RECOMMANDED OPERATING RANGE

(Unless otherwise stated, Topr=-40 to +85℃, GND=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic Supply Voltage	VDD	4.5	5	5.5	V
Dynamic Current (see note)	IDDdyn	-	-	5	mA
High-Level Input Voltage	VIH	0.8VDD	-	VDD	V
Low-Level Input Voltage	VIL	0	-	0.3VDD	V

Note: Test Condition: Set Display Control Commands=80H (Display Turn Off State)

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, VDD=5V, GND=0V, Ta=25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-Level Output Current	IOHSG(1)	VO=VDD-1V SG1 to SG9, SG10/GR7 to SG12/GR5	-10	-14	-30	mA
	IOHSG(2)	VO=VDD-2V SG1 to SG9, SG10/GR7 to SG12/GR5	-20	-25	-50	mA
Low-Level Output Current	IOLGR	VO=0.3V GR1 to GR4, SG10/GR7 to SG12/GR5	100	140	-	mA
Segment High-Level Output Current Tolerance	ITOLSG	VO=VDD-1V SG1 to SG9, SG10/GR7 to SG12/GR5	-	-	±5	%
High-Level Input Voltage	VIH	-	0.8VDD	-	-	V
Low-Level Input Voltage	VIL	-	-	-	0.3VDD	V
Oscillation Frequency	fosc	R=51KΩ	350	500	650	KHz

PACKAGE INFORMATION

24-PIN, SOP, 300MIL

PIN 1 INDENT
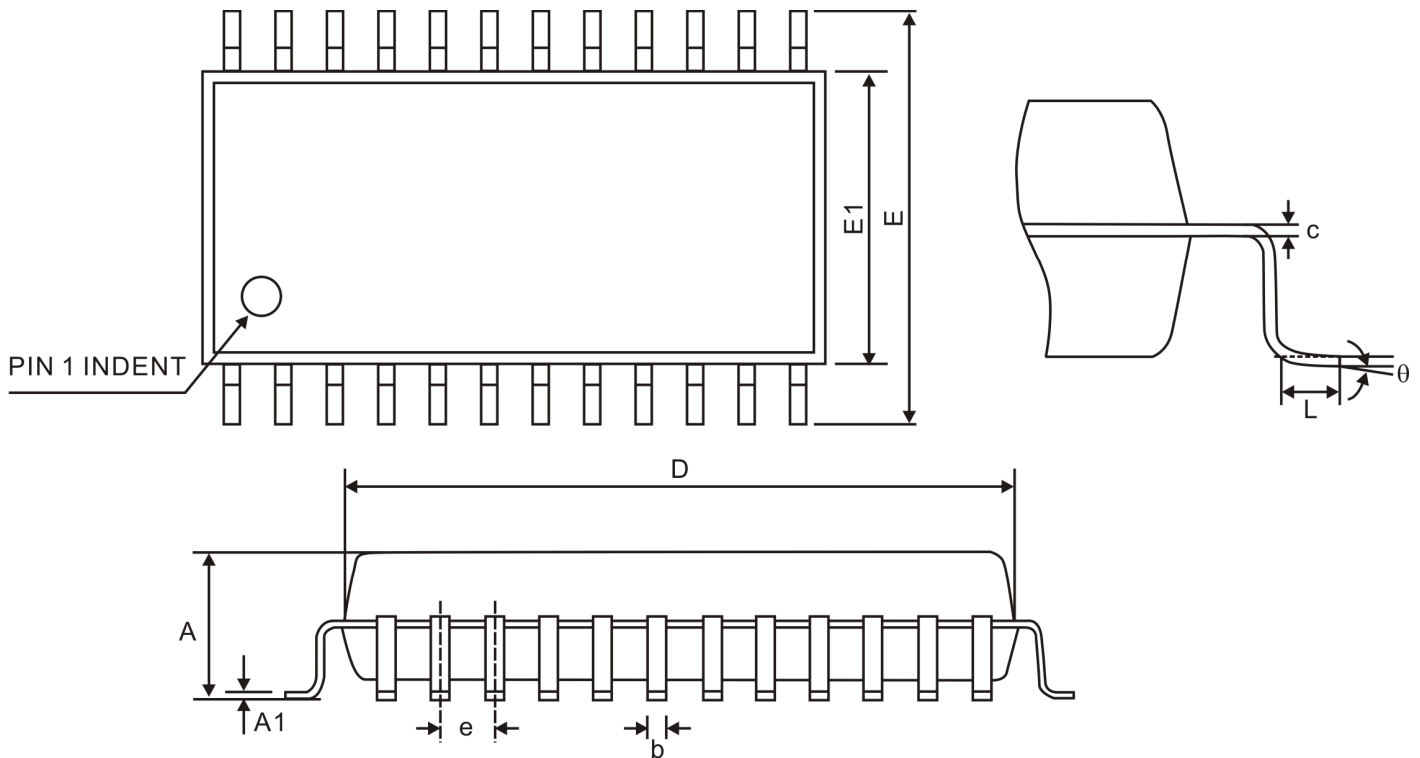
Symbol	Min.	Nom.	Max.
A	2.35	-	2.65
A1	0.10	-	0.30
b	0.33	-	0.51
c	0.23	-	0.32
D	15.20	-	15.60
E	10.00	-	10.65
E1	7.40	-	7.60
e	1.27 BSC.		
L	0.40	-	1.27
θ	0°	-	8°

Notes:
1. All controlling dimensions are in millimeters.
2. Refer to JEDEC MS-013 AD.

IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.

PTC cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a PTC product. No circuit patent licenses are implied.

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