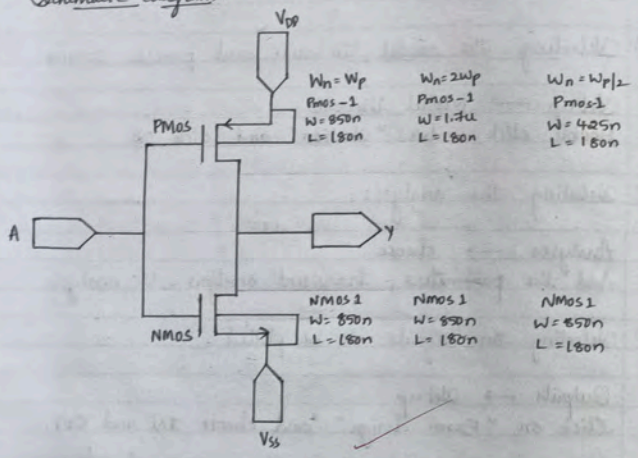
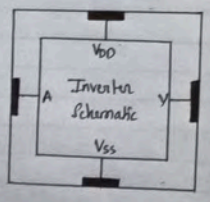
Schematic diagram :-




Symbol




Name of Experiment : CMOS Inverter  Date : 18/10/2022

Experiment No : 01  Experiment Result : Verified  Page No. 06

## Experiment – 01
## CMOS INVERTER

Aim :- Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the width of the inverter with $W_N = W_P$.

Length and width of NMOS and PMOS Transistors for the condition $W_N = W_P$.

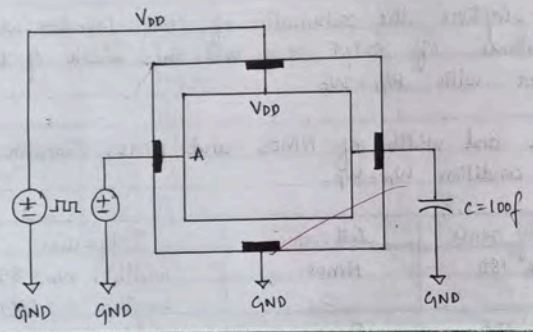
| Library name | Cell name | Properties |
|---|---|---|
| gpdk 180 | Nmos | width, $W_N$ = 850n |
| | | length, L = 180n |
| gpdk 180 | Pmos | width, $W_P$ = 850n |
| | | length, L = 180n |

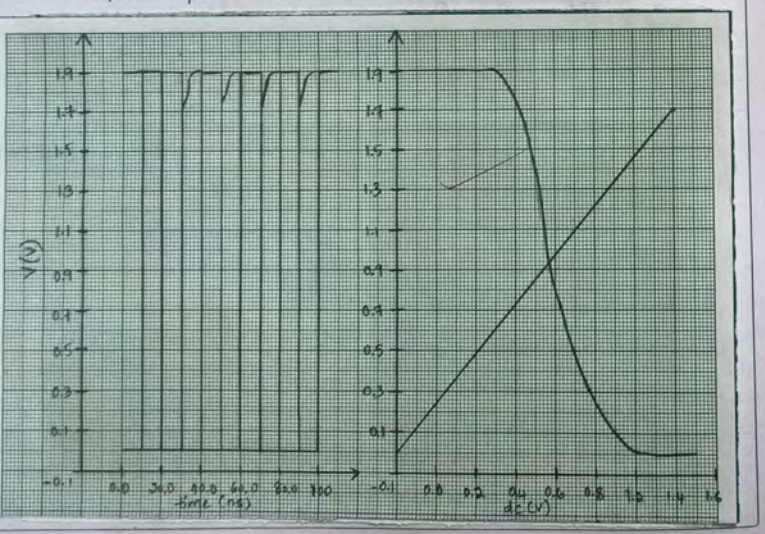
Properties of Vdc, Vpulse, cap and gnd

| Library name | Cell name | Properties |
|---|---|---|
| Analog lib | Vdc | DC voltage = 1.8V |
| Analog lib | Vpulse | Voltage 1 = 0V |
| | | Voltage 2 = 1.8V |
| | | period = 20nS |
| | | Delay time=10ns, Rise time = 1ps |
| | | Pulse = 10ns |
| Analog lib | cap | Capacitance = 100PF |
| Analog lib | gnd | |

Teacher's Signature :

Test bench diagram




Name of Experiment : CMOS Inverter Date : 18/10/2022 Page No. 04

Experiment No : 01 Experiment Result : Verified

CMOS Inverter :-

A CMOS inverter is a field effect transistor that is composed of a metal gate that lies on top of an insulating layer of oxygen, which lies on top of semiconductor. CMOS inverter's are found in most electronic devices and are responsible for producing data within small circuit.

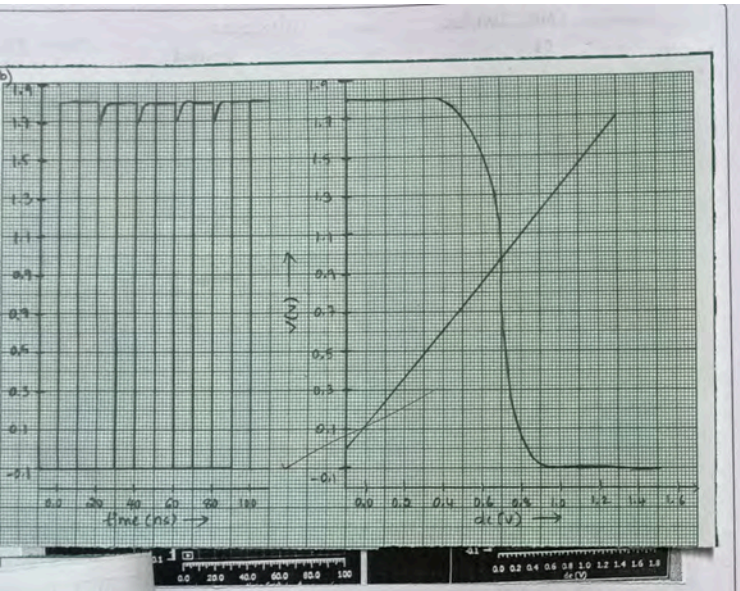
Result :

$T_{PHL}$ → 326.08psec

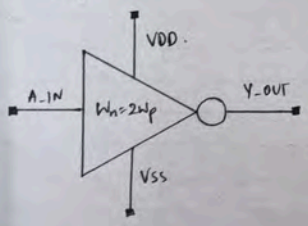
$T_{PLH}$ → 784.56psec

$T_{pd}$ → 555.32psec

Teacher's Signature :




Symbol




Name of Experiment : CMOS inverter Date : 16/10/2022

Experiment No : 01 Experiment Result : Verified



## CMOS Inverter [$W_n = 2W_p$]

Aim :- Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the width of the inverter with $W_n = 2W_p$.

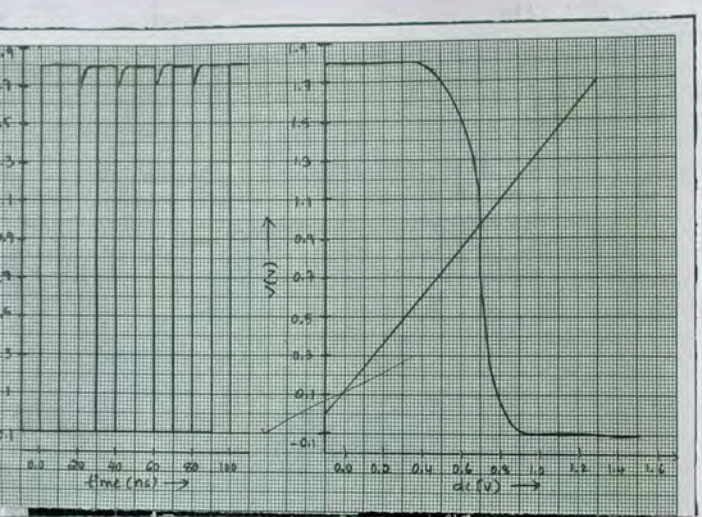
CMOS Inverter :-

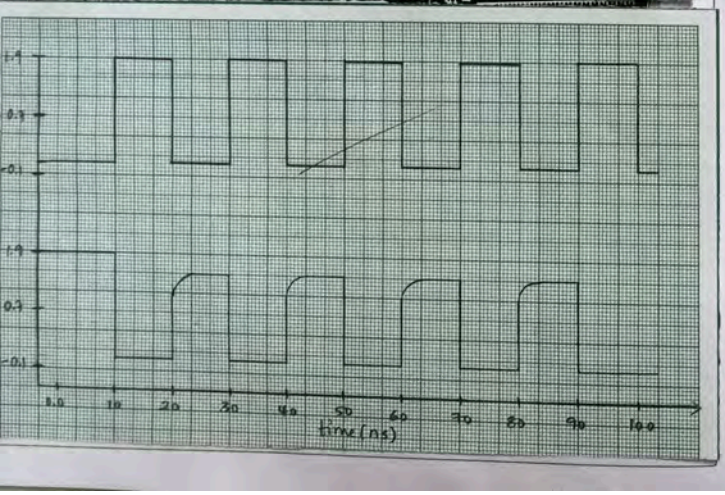
A CMOS inverter is a field-effect transistor that is composed of a metal gate that lies on top of a semiconductor. CMOS inverters are found in most electronic devices and are responsible for producing data within small circuit.

Length and width of NMOS and PMOS transistor for the condition $W_n = 2W_p$

| Library name | Cell name | Properties |
|---|---|---|
| gpdk 180 | NMOS | width, $W_N$ = 850n<br>length, L = 180n |
| gpdk 180 | PMOS | width, $W_p$ = 850n<br>length, L = 180n |

Teacher's Signature : _____




Name of Experiment: ..... Date: 15/10/2022

Experiment No: 01 Experiment Result: Verified Page No. 08

## CMOS Inverter [$W_n = 2W_p$]

Aim:- Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the width of the inverter with $W_n = 2W_p$.

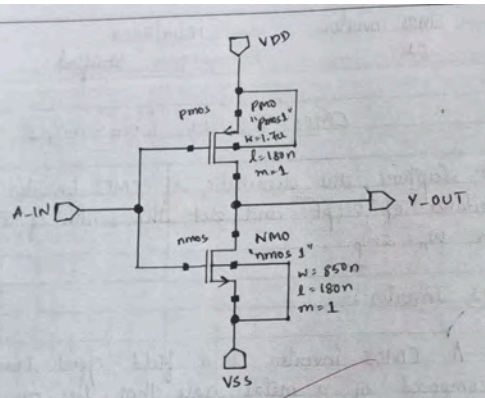
CMOS Inverter :-

A CMOS inverter is a field-effect transistor that is composed of a metal gate that lies on top of a semiconductor. CMOS inverters are found in most electronic devices and are responsible for producing data within small circuit.

Length and width of NMOS and PMOS transistor for the condition $W_n = 2W_p$

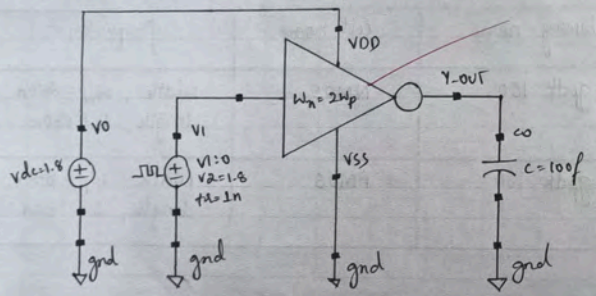
| Library name | Cell name | Properties |
|---|---|---|
| gpdk 180 | NMOS | width, $W_N = 850n$<br>length, $L = 180n$ |
| gpdk 180 | PMOS | width, $W_p = 850n$<br>length, $L = 180n$ |

Teacher's Signature: _____




Schematic diagram

Test bench Schematic




Name of Experiment : CMOS Inverter Date : 16/10/2022 Page No. 09

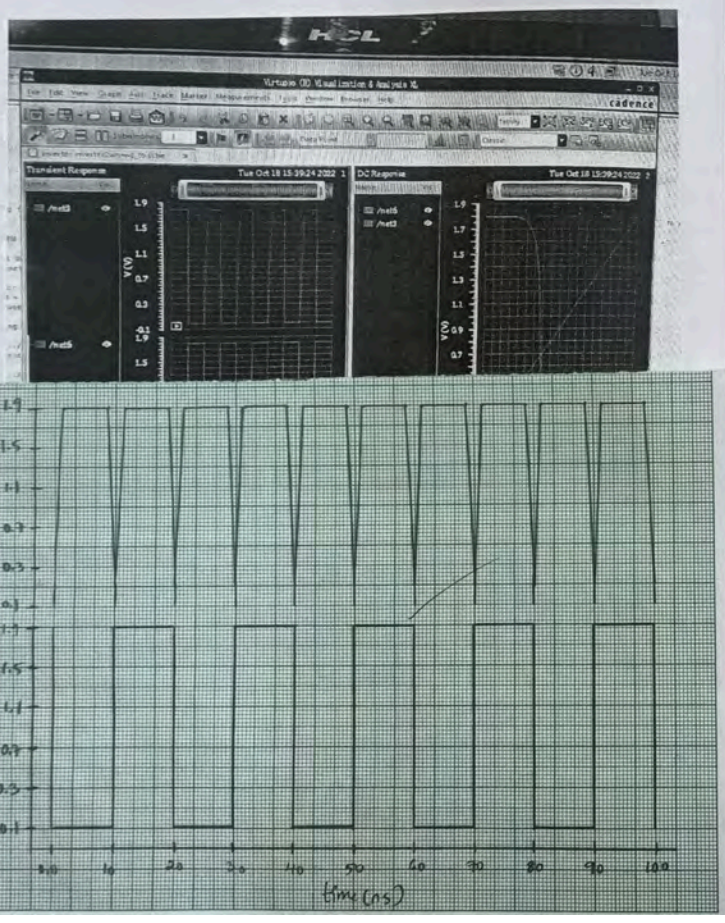
Experiment No : 01 Experiment Result : Verified

Properties of Vdc, Vpulse, cap and gnd

| Library name | Cell name | Properties |
|---|---|---|
| Analog lib | Vdc | DC voltage = 1.8V |
| Analog lib | Vpulse | $V_1$ = 0V, V2 = 1.8V<br>period = 20ns<br>Delay time = 10ns<br>Rise time = 1ps<br>fall time = 1ps<br>pulse = 10ns |
| Analog lib | cap | Capacitance = 100fF |
| Analog lib | gnd | |

Result :-

$T_{PLH}$ → 530.9psec
$T_{PHL}$ → 430.0psec
$T_{pd}$ → 480.45psec




Name of Experiment : CMOS Inverter  Date : 18/10/2022

Experiment No : 01  Experiment Result : Verified  Page No. 10

## CMOS Inverter [$W_n = W_p/2$]

Aim :- Capture the schematic of CMOS Inverter with load capacitor of 0.1pf and set the width of the inverter with $W_n = W_p/2$.

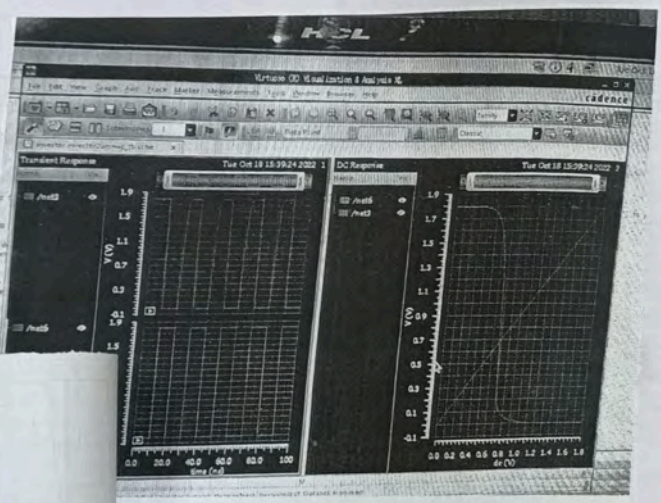
CMOS Inverter :-

A CMOS Inverter is a field-effect transistor that is composed of a metal gate that lies on top of an insulting layer of oxygen which lies on top of a semiconductor.

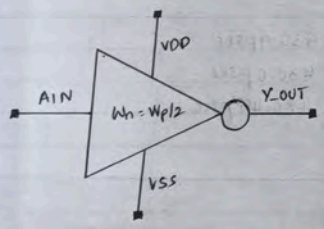
Length and width of NMOS and PMOS transistor for the conductor $W_n = W_p/2$

| Library name | Cell name | Properties |
|---|---|---|
| gpdk 180 | NMOS | width, $W_n$ = 850n<br>length, L = 180n |
| gpdk 180 | PMOS | width, $W_p$ = 850n<br>length, L = 180n |

Teacher's Signature :




Symbol




Name of Experiment : CMOS Inverter  Date : 18/10/2022

Experiment No : 01  Experiment Result : Verified  Page No. 10

## CMOS Inverter [$W_n = W_p/2$]

Aim :- Capture the schematic of CMOS Inverter with load capacitor of 0.1pf and set the width of the inverter with $W_n = W_p/2$.

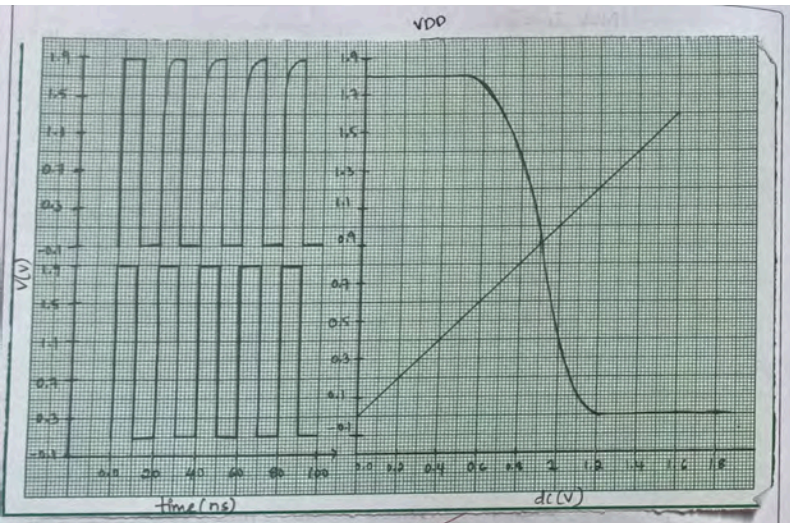
CMOS Inverter :-

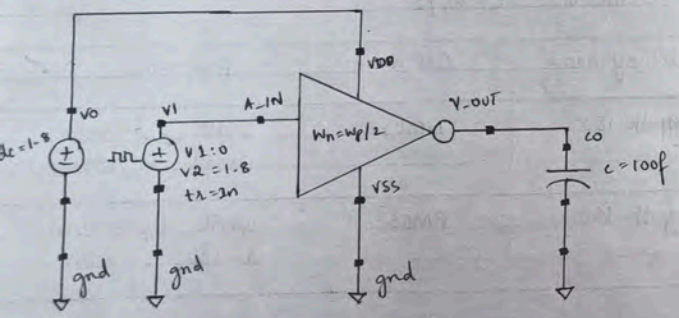
A CMOS Inverter is a field-effect transistor that is composed of a metal gate that lies on top of an insulting layer of oxygen which lies on top of a semiconductor.

Length and width of NMOS and PMOS transistor for the conduction $W_n = W_p/2$

| Library name | Cell name | Properties |
|---|---|---|
| gpdk 180 | NMOS | width, $W_n$ = 850n<br>length, L = 180n |
| gpdk 180 | PMOS | width, $W_p$ = 850n<br>length, L = 180n |

Teacher's Signature : _____




Test bench schematic

Name of Experiment : CMOS Inverter  Date : 18/10/2022
Experiment No : 01  Experiment Result : Verified  Page No. 11

Properties of $V_{dc}$, $V_{pulse}$, cap and gnd.

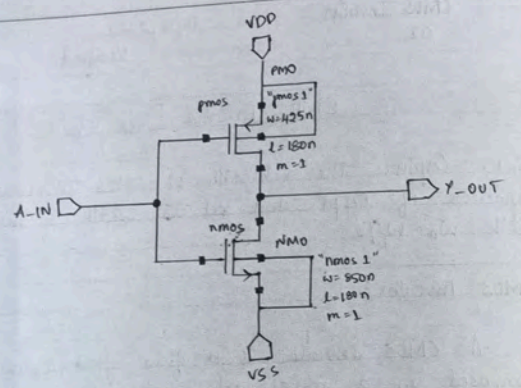
| Library name | Cell name | properties |
|---|---|---|
| Analog lib | $V_{dc}$ | DC voltage = 1.8V |
| Analog lib | $V_{pulse}$ | Voltage1 = 0V, $V_2$ = 1.8V<br>Period = 2ns<br>Rise = 1ps |
| Analog lib | cap | Cap = 100fF |
| Analog lib | gnd | |

Result :-

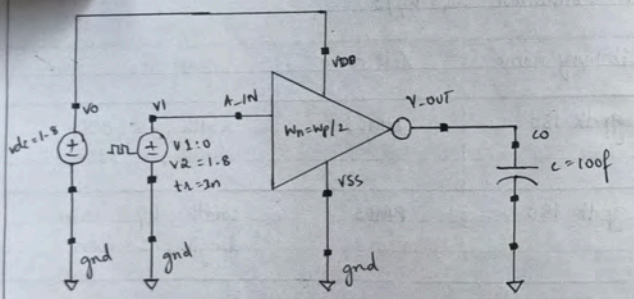
$T_{PLH}$ = 1.03E-09 sec
$T_{PHL}$ = 3.23E-10 sec
$T_{pd}$ = 7.183E-10 sec

From the design we can conclude that $W_n = 2W_p$ is best design, because it has less delay.

Teacher's Signature :




Schematic diagram




Test bench Schematic

Name of Experiment : CMOS Inverter  Date : 18/10/2022  Page No. 11

Experiment No : 01  Experiment Result : Verified

Properties of $V_{dc}$, $V_{pulse}$, cap and gnd.

| Library name | Cell name | properties |
|---|---|---|
| Analog lib | $V_{dc}$ | DC voltage = 1.8V |
| Analog lib | $V_{pulse}$ | Voltage1 = 0V, $V_2$ = 1.8V<br>Period = 2ns<br>Rise = 1ps |
| Analog lib | cap | cap = 100fF |
| Analog lib | gnd | |

Result :-

$T_{PLH}$ = 1.03E-09 sec
$T_{PHL}$ = 3.23E-10 sec
$T_{pd}$ = 7.183E-10 sec

From the design we can conclude that $W_n = 2W_p$ is best design, because it has less delay.

Teacher's Signature : _____

ame of Experiment : CMOS Inverter  Date : 18/10/2022  Page No. 12

xperiment No : 01  Experiment Result : Verified.

Table : Values of $t_{pHL}$, $t_{pLH}$ and $t_{pD}$ for different geometries

| Width settings | MOSFET | Width | $t_{pLH}$ | $t_{pHL}$ | $t_{pd}$ |
|---|---|---|---|---|---|
| $W_p = W_n$ | PMOS<br>NMOS | 850n<br>850n | 784.56p | 326.08p | 555.32p |
| $W_n = 2W_p$ | PMOS<br>NMOS | 850n<br>1.7u | 530.9p | 430.0p | 480.45p |
| $W_n = W_p/2$ | PMOS<br>NMOS | 425n<br>850n | 103E-09 | 3.23E-10 | 7.183E-10 |

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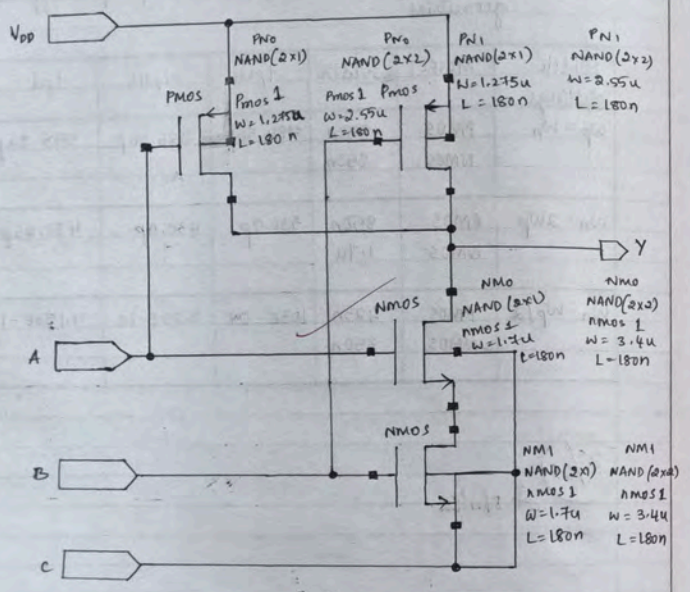
Schematic Diagram:-




Name of Experiment : 2/p CMOS NAND  Date : 8/11/2022

Experiment No : 02  Experiment Result : Verified  Page No. 13

## Experiment-02

## INPUT CMOS NAND

Aim:- Capture the schematic of a 2-input CMOS NAND gate, verify the functionality of the NAND gate.

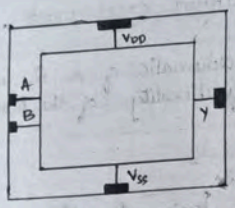
NAND Gate:-

NAND gate is a logic gate which produces an output which is taken only if all inputs are true, thus its output is complement to that of an AND gate. A low output result only if all the inputs to gate is high, if any input is low, a high output result.

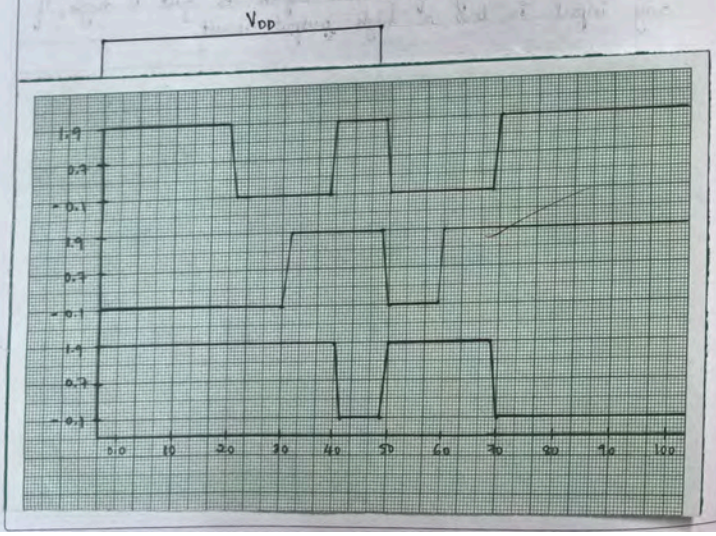
Width and length of NMOS and PMOS transistors for CMOS NAND gate

| Library Name | Cell name | Properties |
|---|---|---|
| gpdk 180 | NMOS | width $W_n = 1.7u$<br>length $L = 180n$ |
| gpdk 180 | PMOS | width $W_p = 1.275u$<br>length $L = 180n$ |

Symbol




Test Bench circuit




Name of Experiment P/F CMOS NAND Date 8/11/2022

Experiment No. 02 Experiment Result Verified Page No. 14

Setup Analog stimuli

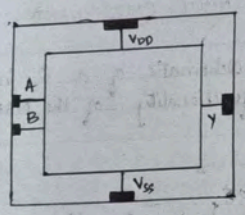
One value to zero
Zero value to 0
Rise time and fall time to 1n
period 10n
Bit pattern for A = 11001001
Bit pattern for B = 10100110

Properties of Vdc, Cap and gnd

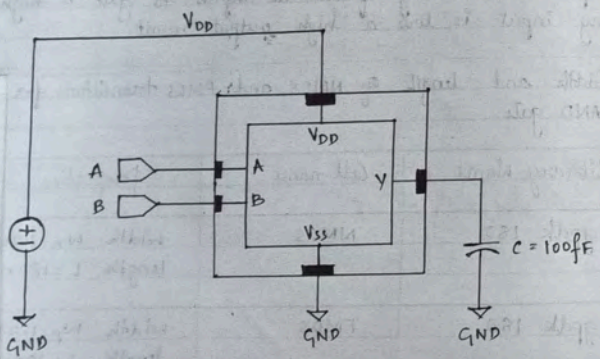
| Library name | Cell name | Properties |
|---|---|---|
| Analog lib | Vdc | DC voltage = 1.8V |
| Analog lib | Cap | Capacitance = 100fF |
| Analog lib | Gnd | |

Result :- TPLH = 372.0PSec
TPHL = 343.1PSec
TPd = 357.55psec

Symbol




Test Bench circuit




Name of Experiment: I/p CMOS NAND  Date: 8/11/2022

Experiment No.: 02  Experiment Result: Verified  Page No. 14

Setup Analog stimuli

One value to zero
Zero value to 0
Rise time and fall time to 1n
period 10n
Bit pattern for A = 11001001
Bit pattern for B = 10100110

Properties of Vdc, Cap and gnd

| Library name | Cell name | Properties |
|---|---|---|
| Analog lib | Vdc | DC voltage = 1.8V |
| Analog lib | Cap | Capacitance = 100fF |
| Analog lib | Gnd | |

Result :- TPLH = 372.0PSec
TPHL = 343.1PSec
TPd = 357.55psec

Name of Experiment : I/P CMOS NAND  Date : 8/11/2022  Page No. 15

Experiment No : 02  Experiment Result : Verified

# Input CMOS NAND Gate (2x2)

Aim:- Capture the schematic of a 2-input CMOS NAND gate verify the functionality of NAND gate.

## NAND Gate

NAND gate is a logic gate which produces an output which is false only if all inputs are true thus its output is complement to that of an AND gate

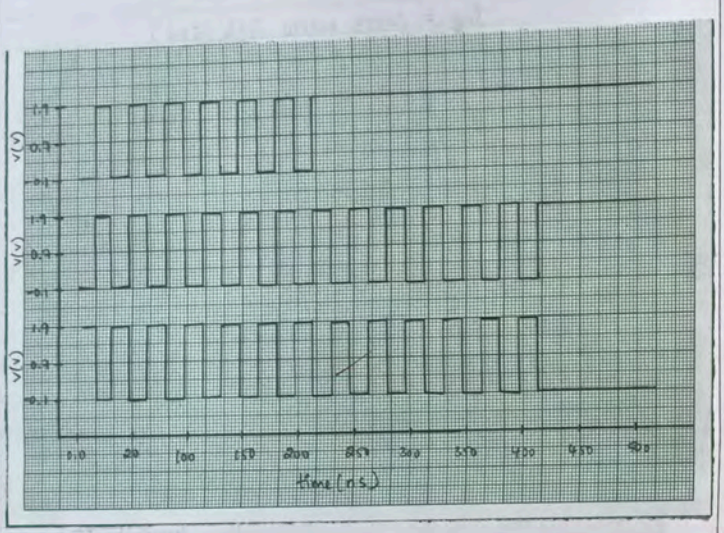
Width and length of NMOS and PMOS Transistor for CMOS NAND gate

| Library Name | Cell Name | properties |
|---|---|---|
| gpdk 180 | NMOS | width Wn = <br> length L = 180n |
| gpdk 180 | PMOS | width Wp = <br> length L = 180n |

Properties of Vdc, Cap and Gnd

| Library Name | Cell Name | Properties |
|---|---|---|
| Analog lib | Vdc | DC voltage = 1.8V |
| Analog lib | Vpulse | Capacitance = 100fF |
| Analog lib | Gnd | |

Teacher's Signature :




Name of Experiment : i/p CMOS NAND Date : 8/11/2022

Experiment No : 02 Experiment Result : Verified Page No. 16

## Setup Analog stimuli

One value to zero
Zero value to 0
Rise time and fall time to 1n
period 10n
Bit pattern for A = 11001001
Bit pattern for B = 10000110

Result :-

TpLH = 224.3 psec
TPHL = 216.0 psec
Tpd = 220.15 psec

From the design we can conclude that NAND 2X2 having less delay than 2X1 it is best suited for the design purpose.

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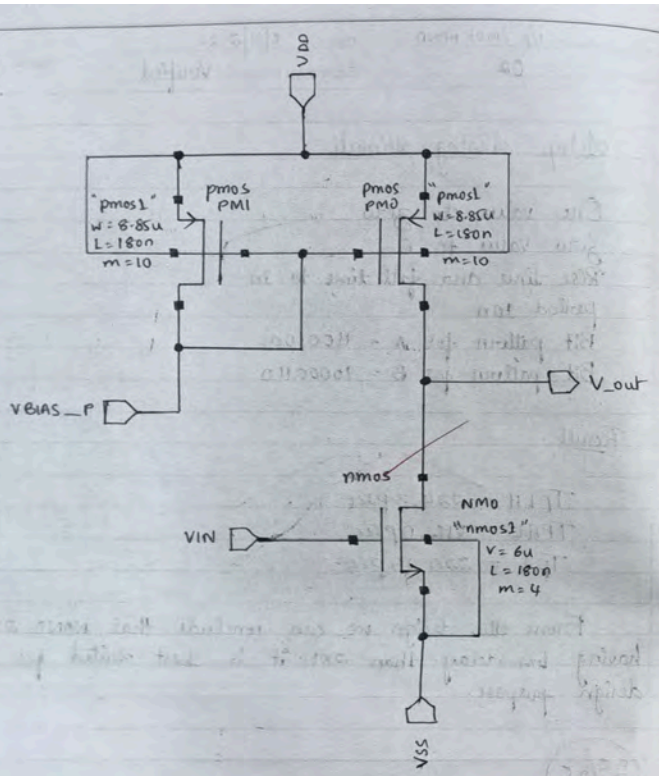



Schematic of Common Source Amplifier with PMOS Current Mirror load.

Name of Experiment : Common Source amplifier  Date : 6/12/2022

Experiment No : 03  Experiment Result : Verified  Page No. 17

## Experiment -03

## Common Source Amplifier with PMOS current mirror load

**Objective:**

Capture the schematic of a common source amplifier with PMOS current mirror load and find its transient response and AC response. Measure the UGB and amplification factor by varying transistor geometries, study the impact of variation in width to UGB.

**Solution:**

Schematic capture:

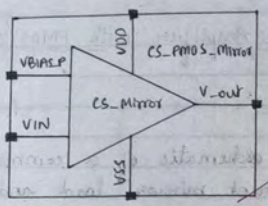
Create a new library using the option File → New → library, create a new cell view upon selecting the newly created library using the option File → new → cell view created library using and instantiate the required devices using the option create → Instance.

Width and length of NMOS and PMOS transistor

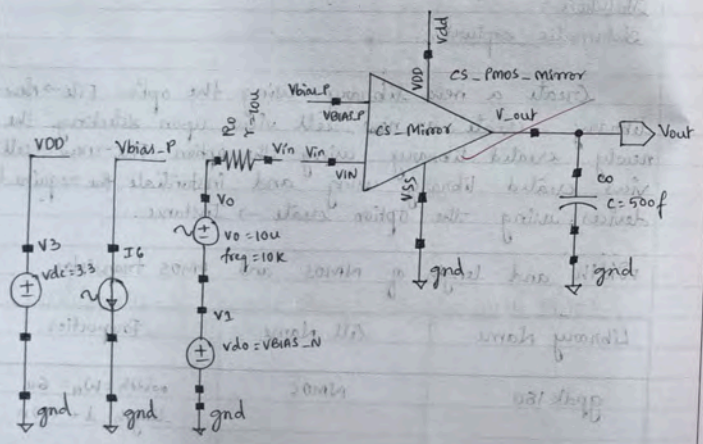
| Library Name | Cell Name | Properties |
|---|---|---|
| gpdk180 | NMOS | width = $W_N$ = 6u<br>length, l = 180n |

Teacher's Signature : _____

Symbol




Test schematic for 2-input CMOS Nand gate




Name of Experiment : Common source amplifier  Date : 6/12/2022  Page No. 18

Experiment No : 03  Experiment Result : Verified

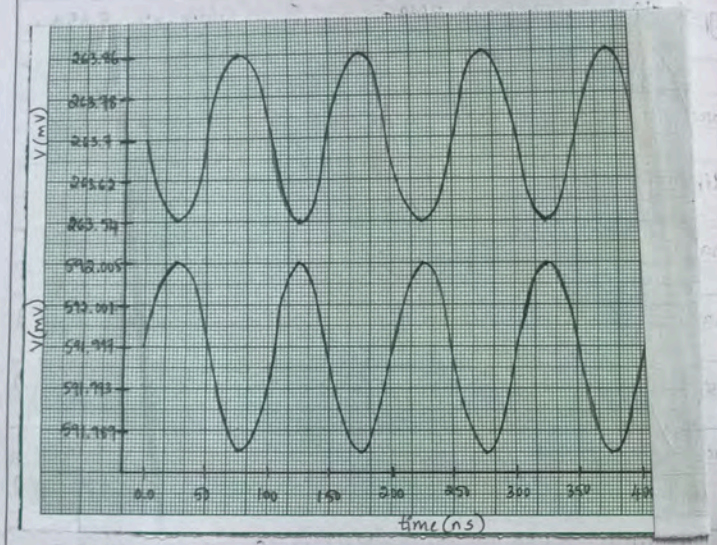
| | | |
|---|---|---|
| gpdk 180 | PMOS | width, Wp = 8.85u<br>length, L = 180n |

Parameters for the devices used in test schematic

| Library name | Cell name | Properties |
|---|---|---|
| Analog lib | Vdc | DC voltage = 3.3V ($V_{DD}$) |
| Analog lib | Vdc | DC voltage = $V_{BIAS\_NV}$ ($V_{in}$) |
| Analog lib | isin | DC current = 100A ($V_{bias\_P}$) |
| Analog lib | vsin | Ac magnitude = 1V, Amplitude = 10u V, frequency = 10KHz ($V_{in}$) |
| Analog lib | cap | Capacitance = 500f F |
| Analog lib | res | Resistance = 10u ohms |
| Analog lib | gnd | |

Launch, ADEL, import the design variables, mention the values and select the transistent analysis 500 moderate DC analysis 0-10 linear step size start-step-10m/V,

Teacher's Signature : _____




Name of Experiment : Common source amplifier
Experiment No : 03
Date : 6/12/2022
Experiment Result : Verified
Page No. 19

AC analysis 1-10G logarithmic points per decode start stop 10

To measure the gain and unity gain BW, go back to the ADEL window select Results → Direct plot → AC magnitude and phase

Result :

Gain, A = 23.56 dB

Unity gain bandwidth, UGB = 869.4 MHz

Conclusion :-

Gain and USB for common source amplifier is verified.

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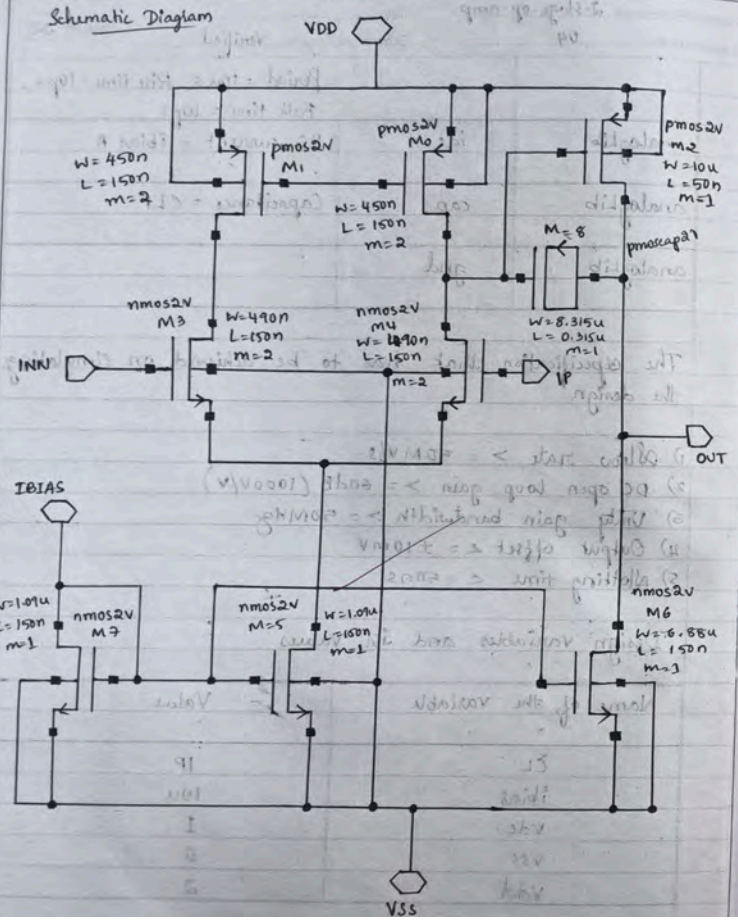
10/12/22

Teacher's Signature :

Schematic Diagram




Name of Experiment : 2-stage op-amp  Date : 10/12/2022

Experiment No : 04  Experiment Result : Verified  Page No. 20

## Experiment No: 04

## 2-Stage Operational Amplifier

Objective:-

Capture the schematic of a 2-stage operational amplifier and measure the following:

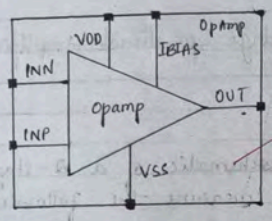
1. UGB
2. dB Bandwidth
3. Gain margin and phase margin with and without coupling capacitance.
4. Use the op-amp in the inverting and non-inverting configuration and verify its functionality.
5. Study the USB, 3dB Bandwidth, gain and power requirement in op-amp by varying the stage wise transistor geometry and record the observations.

Solutions:-

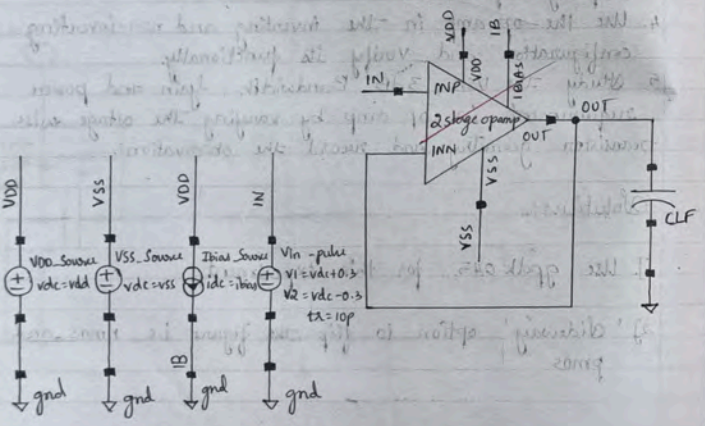
1] Use gpdk 045 for this experiment.

2] 'Sideway' option to flip the figure i.e, nmos and pmos

Symbol




Test bench circuit




Name of Experiment : 2-stage op-amp Date : 10/12/2022 Page No. 21

Experiment No : 04 Experiment Result : Verified

Device parameters for 2-stage operational amplifier

| Library name | Transistor | Cell name | Components / properties |
|---|---|---|---|
| gpdk 045 | M0, M1 | pmos 2V | Width, W = 465n<br>Length, L = 150n |
| gpdk 045 | M3, M4 | nmos2V | Width, W = 490n<br>Length, L = 150n |
| gpdk 045 | M5, M7 | nmos2V | Width, W = 1.09u<br>Length, L = 150n |
| gpdk 045 | M2 | pmos2V | Width, W = 10u<br>Length, L = 150n |
| gpdk 045 | M6 | nmos2V | Width, W = 6.88u<br>Length, L = 150n |
| gpdk 045 | M8 | pmoscap2V | Calculated parameter = Capacitance<br>Capacitance = 250.043f |

Device parameters for 2-stage operational amplifier test schematic

| Library Name | Cell Name | Comments / Properties |
|---|---|---|
| analog lib | Vdc | DC voltage = vdd V |
| analog lib | vdc | DC voltage = vss V |
| analog lib | vpulse | Voltage 1 = vdc + 0.3 V,<br>Voltage 2 = vdc - 0.3V, |

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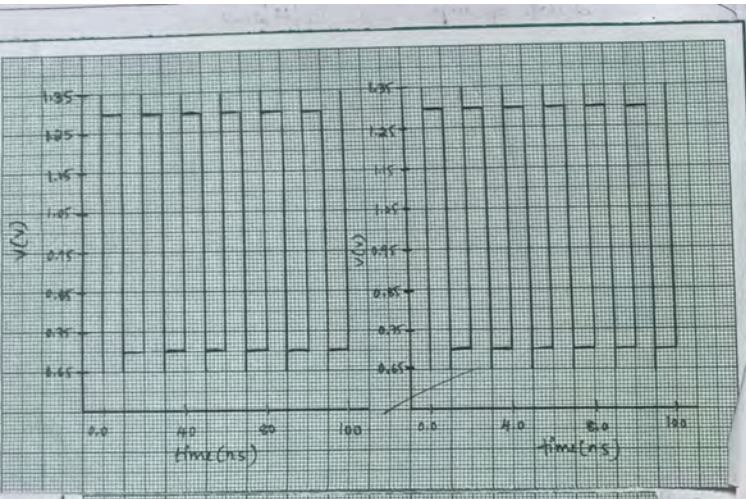


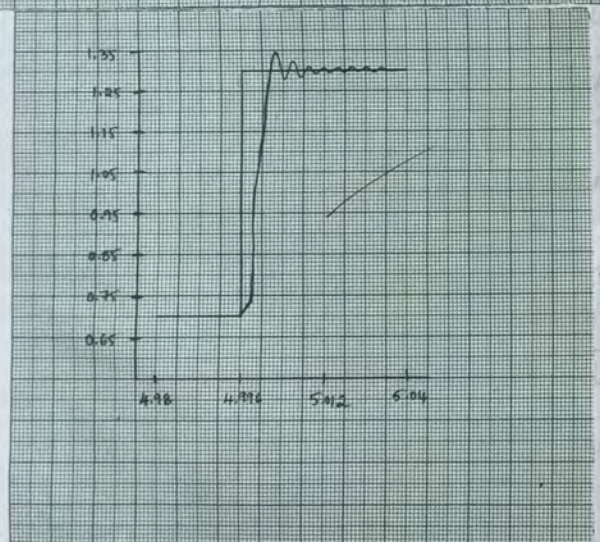

Name of Experiment : 2-stage op-amp  Date : 10/12/2022
Experiment No : 04  Experiment Result : Verified  Page No. 22

| | | |
|---|---|---|
| | | Period = 10us, Rise time = 10ps, Fall time = 10ps |
| analog Lib | idc | DC current = ibias A |
| analogLib | cap | Capacitance = CLF |
| analogLib | gnd | |

The specification that has to be achieved on simulating the design.

1) Slew rate >= 50M V/s
2) DC open loop gain >= 60dB (1000V/V)
3) Unity gain bandwidth >= 50MHg
4) Output offset <= ± 10mV
5) Slotting time <= 50ns

Design variables and its values

| Name of the variable | Value |
|---|---|
| CL | 1P |
| ibias | 10u |
| vdc | 1 |
| vss | 0 |
| vdd | 2 |

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Name of Experiment : 2-stage opamp  Date : 10/12/2022  Page No. 23

Experiment No : 04  Experiment Result : Verified

Result :- $V_{out\_dc} = 1.298\,V$

$V_{in\_dc} = 1.3\,V$

Conclusion :-

The schematic of a 2-stage operational amplifier is verified and measured the values.

25/25 A
10/12/22