FLASH_/HOLD/IO3

1

VBAT 2 J?

3

J1

1 — FLASH_/WP/IO2
2 — MISO
3 — RAM_/CS
4 — VBAT
5 — Vcc

RAM: 2.5 – 5V
Flash: 2.7 – 3.6V

J2

1 — GND
2 — FLASH_/CS
3 — FLASH_/HOLD/IO3
4 — CLK
5 — MOSI

23LCV1024   U1   Vcc

RAM_/CS 1 /CS   VCC 8
MISO   2 SO/SIO1 VBAT 7 — VBAT
         3 NC   SCK 6 — CLK
         4 VSS   SI/SIO0 5 — MOSI
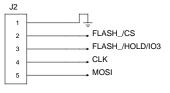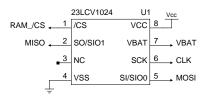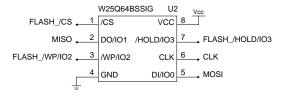
23LCV1024 notes

when /CS is high, SO is hi–z
tie VBAT to VSS if not in use
MCU should check the mode first (SPI/SDI)

23LC1024 diffs

NC –> SIO2
VBAT –> /HOLD/SIO3

pin 3 should not be left floating in SPI and SDI mode
–let MCU pull it high so the bus can recover if SQI is exited by accident

W25Q64BSSIG   U2   Vcc

FLASH_/CS   1 /CS   VCC   8
MISO   2 DO/IO1   /HOLD/IO3 7 — FLASH_/HOLD/IO3
FLASH_/WP/IO2 3 /WP/IO2 CLK   6 — CLK
              4 GND   DI/IO0   5 — MOSI

W25Q64BSSIG notes

when /CS is high, DO or SI0–3 are hi–z
when /HOLD is low, DO is hi–z and signals on CLK and DI are ignored

clk, miso, mosi, hold/io3, wp/io2, cs1, cs2, pwr, bat, gnd