M02: Basic Programming for TM4C123

2.1. Timer & Interrupt

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Ref: www.geeksforgeeks.org

TI, TivaWare C workshop slides

J. Valvano, Embedded Systems: Shape the World.

Project 2 Contents

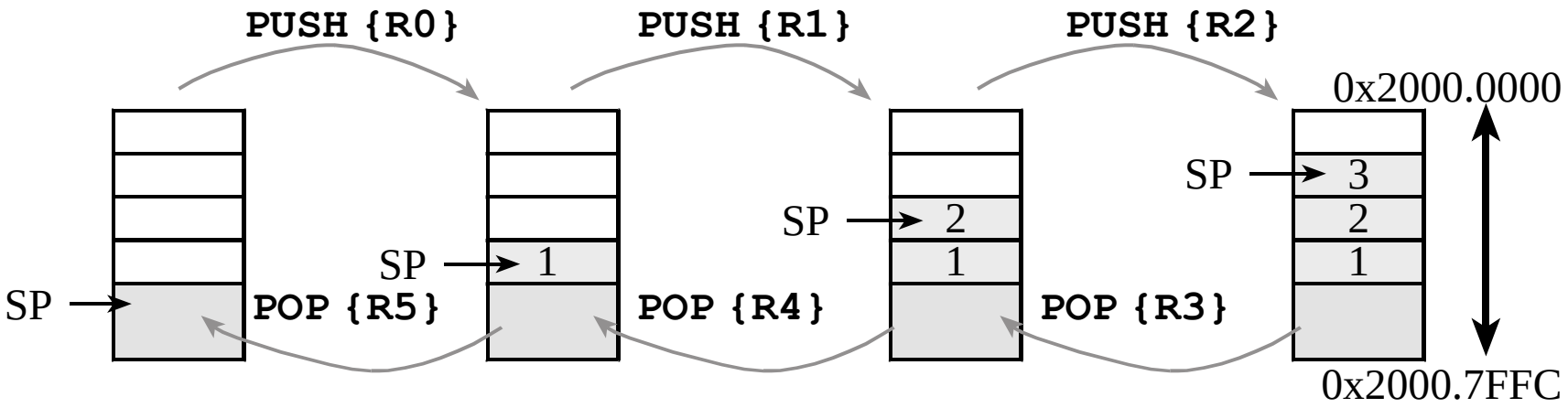
- **Part 2.1: Tiva C workshop lab 4**
  - Import/export projects
  - Interrupts and timers
  - PWM (Pulse Width Modulation)
- **Part 2.2: Tiva C workshop lab 5**
  - Analog to Digital Converter (ADC)
    - Nyquist Sampling Theorem & Quantization
- **Part 2.3: Tiva C workshop lab 9**
  - Floating-Point Processor Unit (FPU)

Interrupts

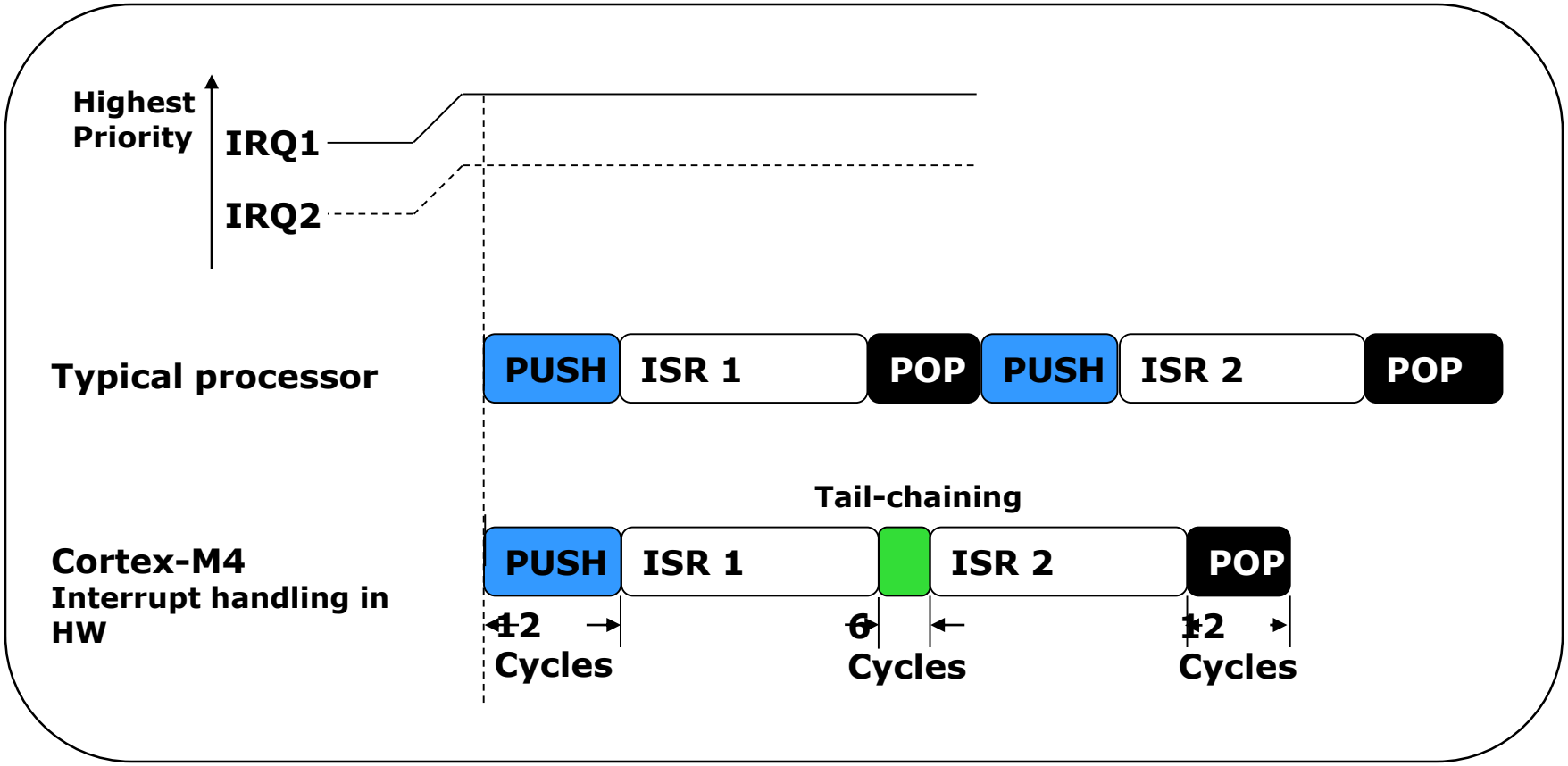
- **Interrupts vs Polling**
- **Interrupts vs. Exceptions**
- **TM4C Nested Vectored Interrupt Controller (NVIC)**
  - Handles exceptions and interrupts
  - 8 programmable priority levels, priority grouping
  - 7 exceptions and 71 Interrupts
  - Automatic state saving and restoring
  - Automatic reading of the vector table entry
  - Pre-emptive/Nested Interrupts
  - Tail-chaining
  - Deterministic: always 12 cycles or 6 with tail-chaining

The Stack

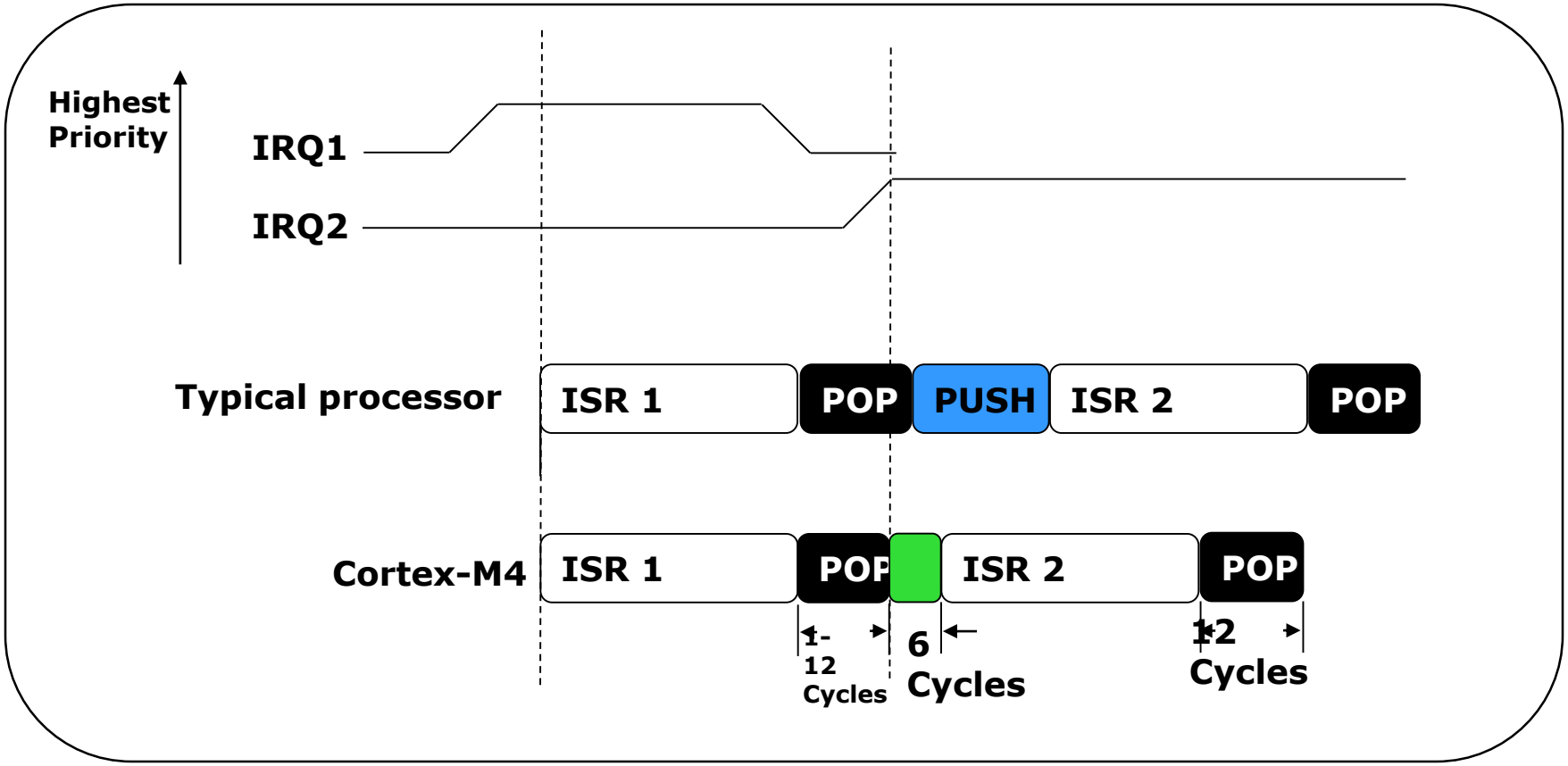
- Stack is last-in-first-out (LIFO) storage
  - 32-bit data
- Stack pointer, SP or R13, points to top element of stack
- Stack pointer *decremented* as data placed on stack
- `PUSH` and `POP` instructions used to load and retrieve data



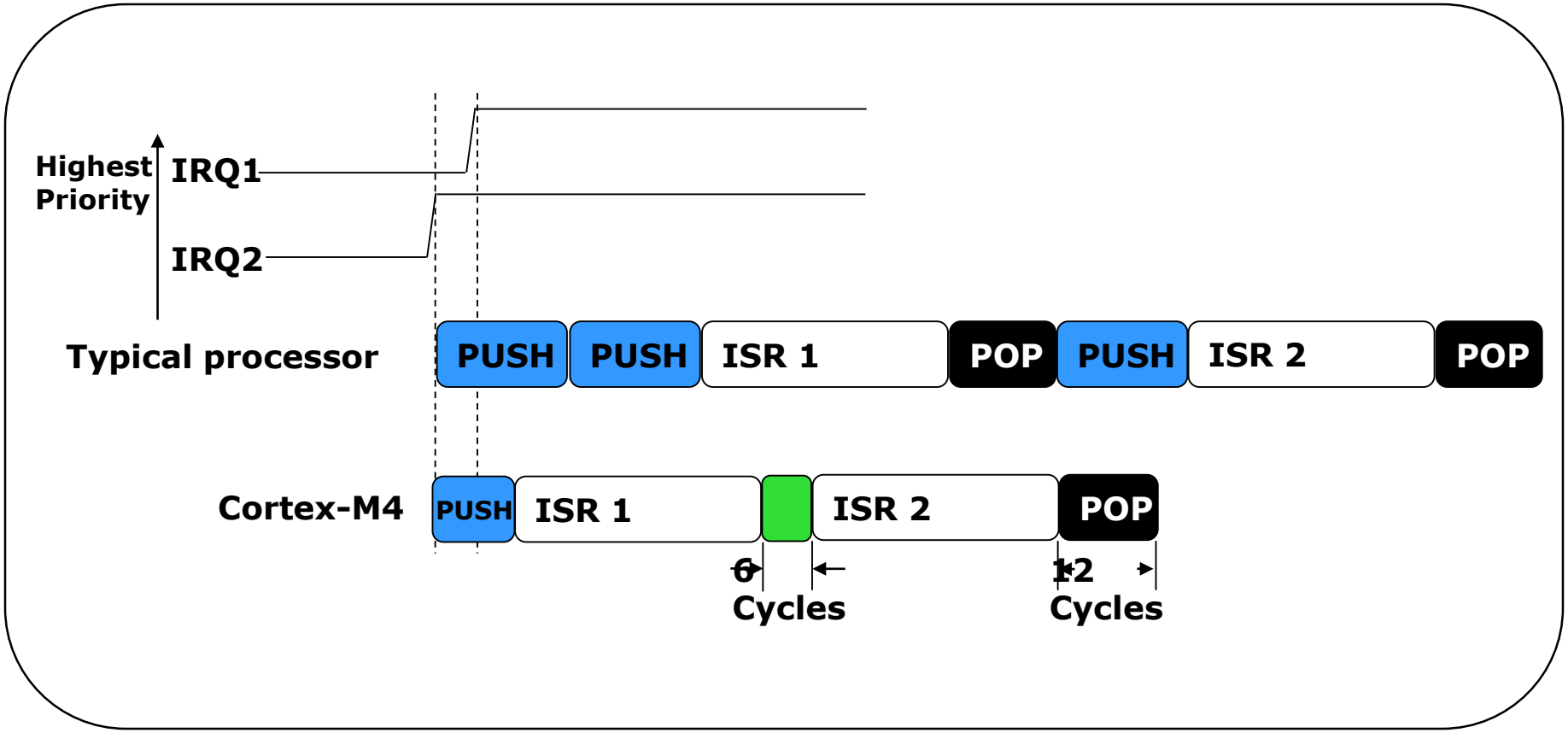
Interrupt Latency - Tail Chaining



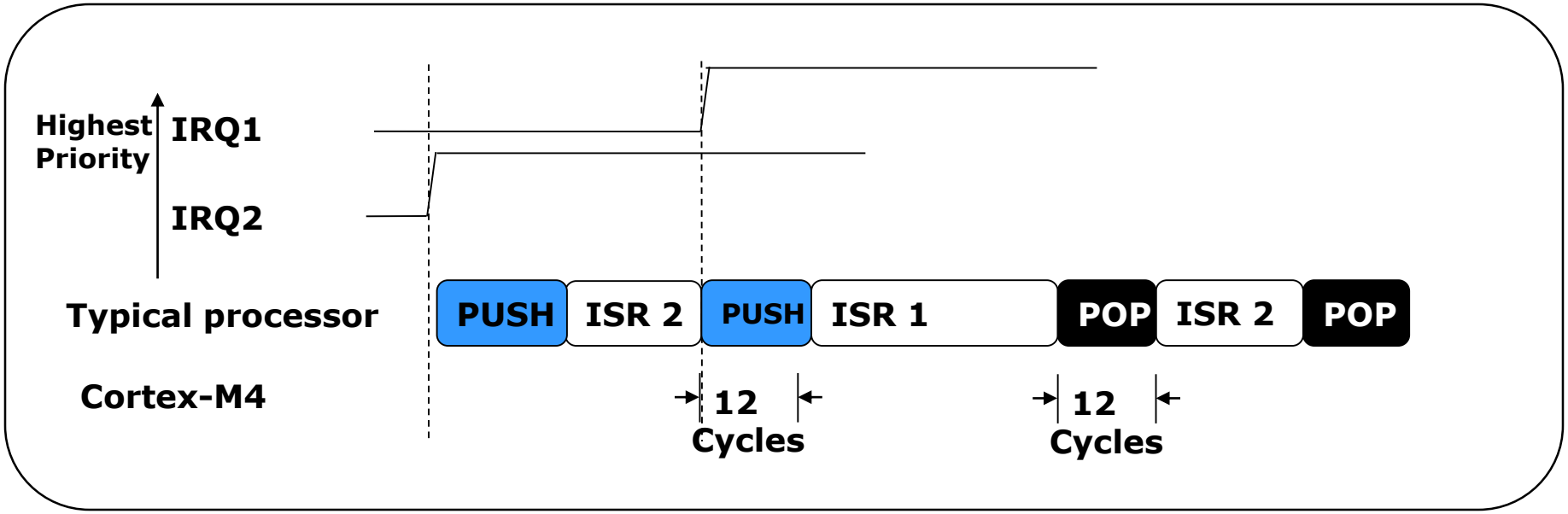
Interrupt Latency – Pre-emption



Interrupt Latency – Late Arrival



Interrupt Latency – Normal Case



- **Interrupt handling is automatic. No instruction overhead.**
- **Entry:** Automatically pushes registers R0–R3, R12, LR, PSR, and PC onto the stack. In parallel, ISR is pre-fetched on the instruction bus. ISR ready to start executing as soon as stack PUSH complete
- **Exit:** Processor state is automatically restored from the stack. In parallel, interrupted instruction is pre-fetched ready for execution upon completion of stack POP

Cortex-M4® Vector Table

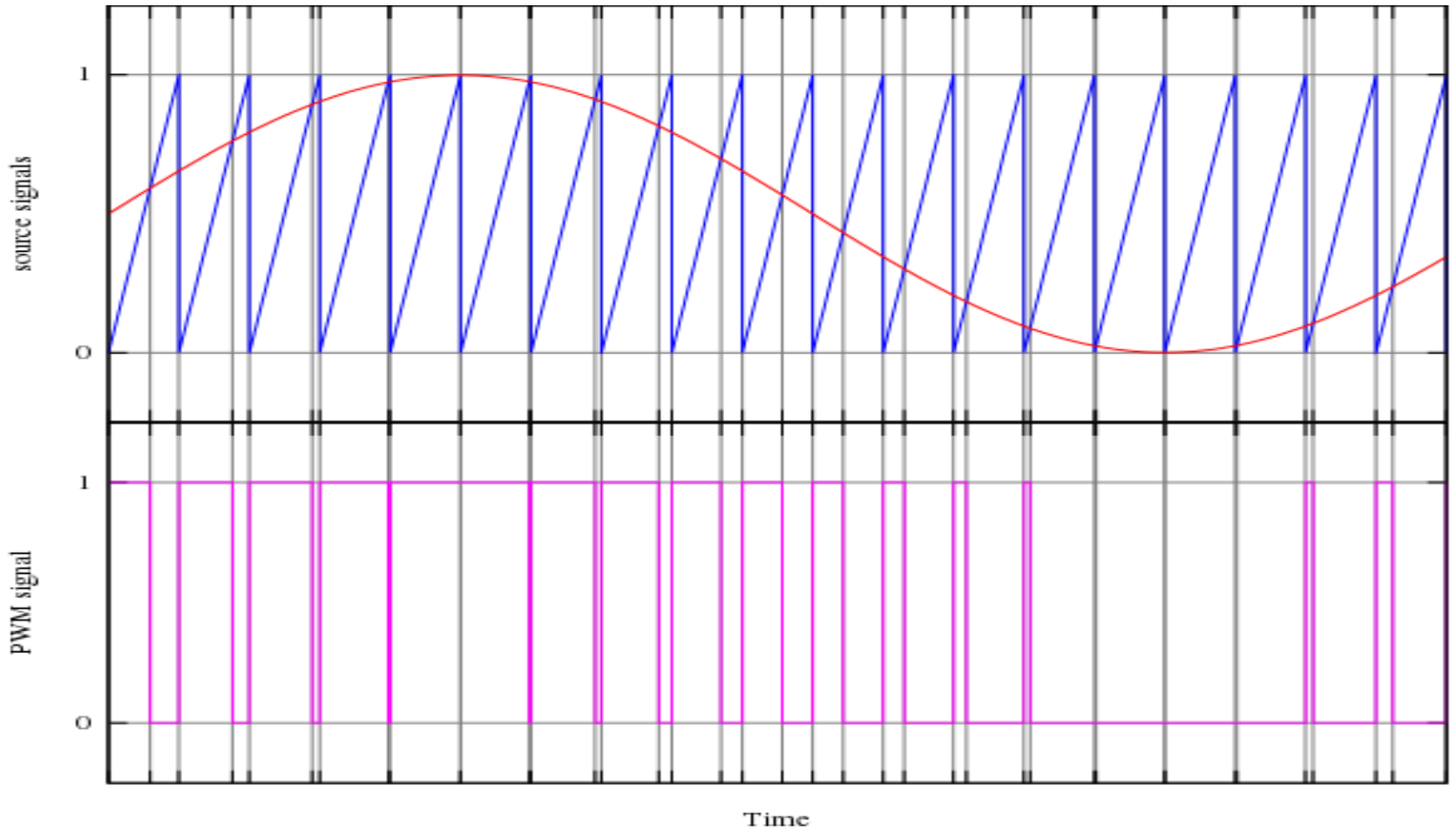
- After reset, vector table is located at address 0
- Each entry contains the address of the function to be executed
- The value in address 0x00 is used as starting address of the Main Stack Pointer (MSP)
- Vector table can be relocated by writing to the VTABLE register (must be aligned on a 1KB boundary)
- Open startup_ccs.c to see vector table coding

Exception number	IRQ number	Offset	Vector
154	138	0x0268	IRQ131
.		.	.
.		.	.
.		.	.
		0x004C	
18	2	0x0048	IRQ2
17	1	0x0044	IRQ1
16	0	0x0040	IRQ0
15	-1	0x003C	Systick
14	-2	0x0038	PendSV
13			Reserved
12			Reserved for Debug
11	-5	0x002C	SVCall
10			Reserved
9			
8			
7			
6	-10	0x0018	Usage fault
5	-11	0x0014	Bus fault
4	-12	0x0010	Memory management fault
3	-13	0x000C	Hard fault
2	-14	0x0008	NMI
1		0x0004	Reset
		0x0000	Initial SP value

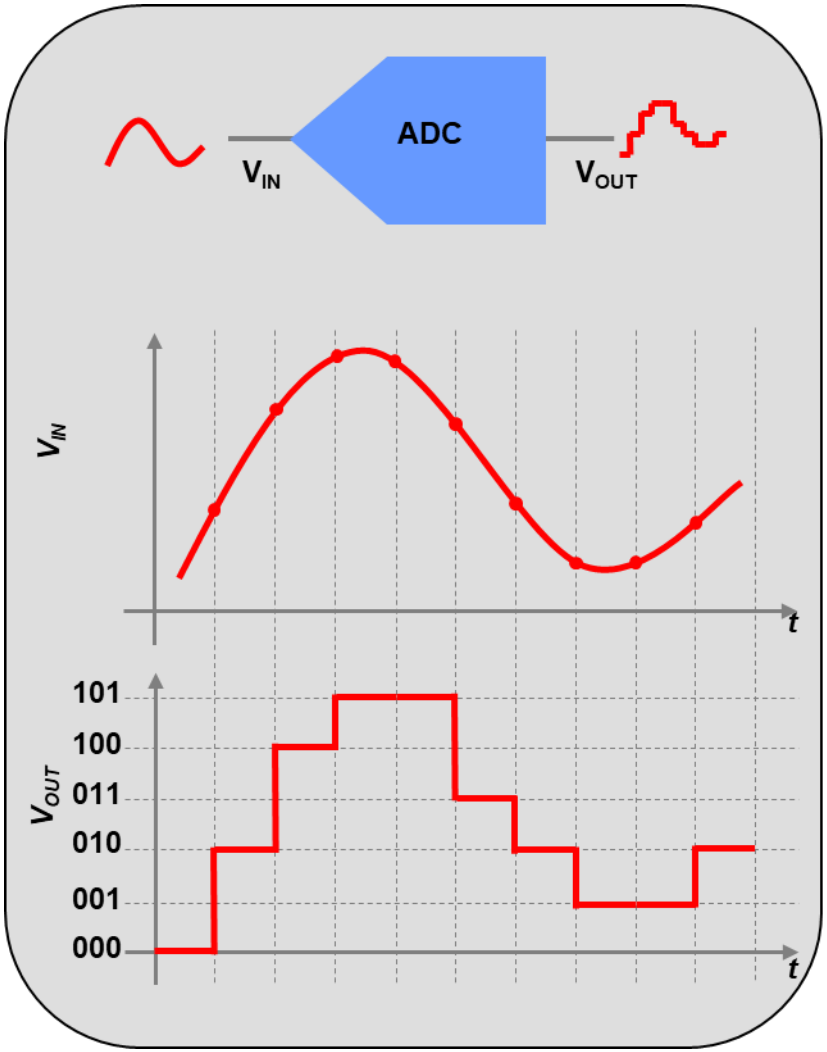
General Purpose Timer Module

- Six 16/32-bit and Six 32/64-bit general purpose (wide) timers
- Twelve 16/32-bit and Twelve 32/64-bit capture / compare / PWM pins
- Timer modes:
  - One-shot or Periodic
  - Input edge count or time capture with 16-bit prescaler
  - PWM generation (separated only)
  - Real-Time Clock (concatenated only)
- Count up or down
- Simple PWM (no deadband generation)
- Support for timer synchronization, daisy-chains, and stalling during debugging
- May trigger ADC samples or DMA transfers

Pulse Width Modulation



ADC ~ PAM



- Tiva TM4C MCUs feature two ADC modules (ADC0 and ADC1) that can be used to convert continuous analog voltages to discrete digital values
- Each ADC module has 12-bit resolution
- Each ADC module operates independently and can:
  - Execute different sample sequences
  - Sample any of the shared analog input channels
  - Generate interrupts & triggers