M03: Memory& uDMA

3.2. uDMA

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References:

1.TM4C123GH6PM data sheet (**spms376e.pdf**) Chapter 9.

2. TM4C123 Workshop Lab 13 slides

3. Tivaware example: udma_demo.c - uDMA example

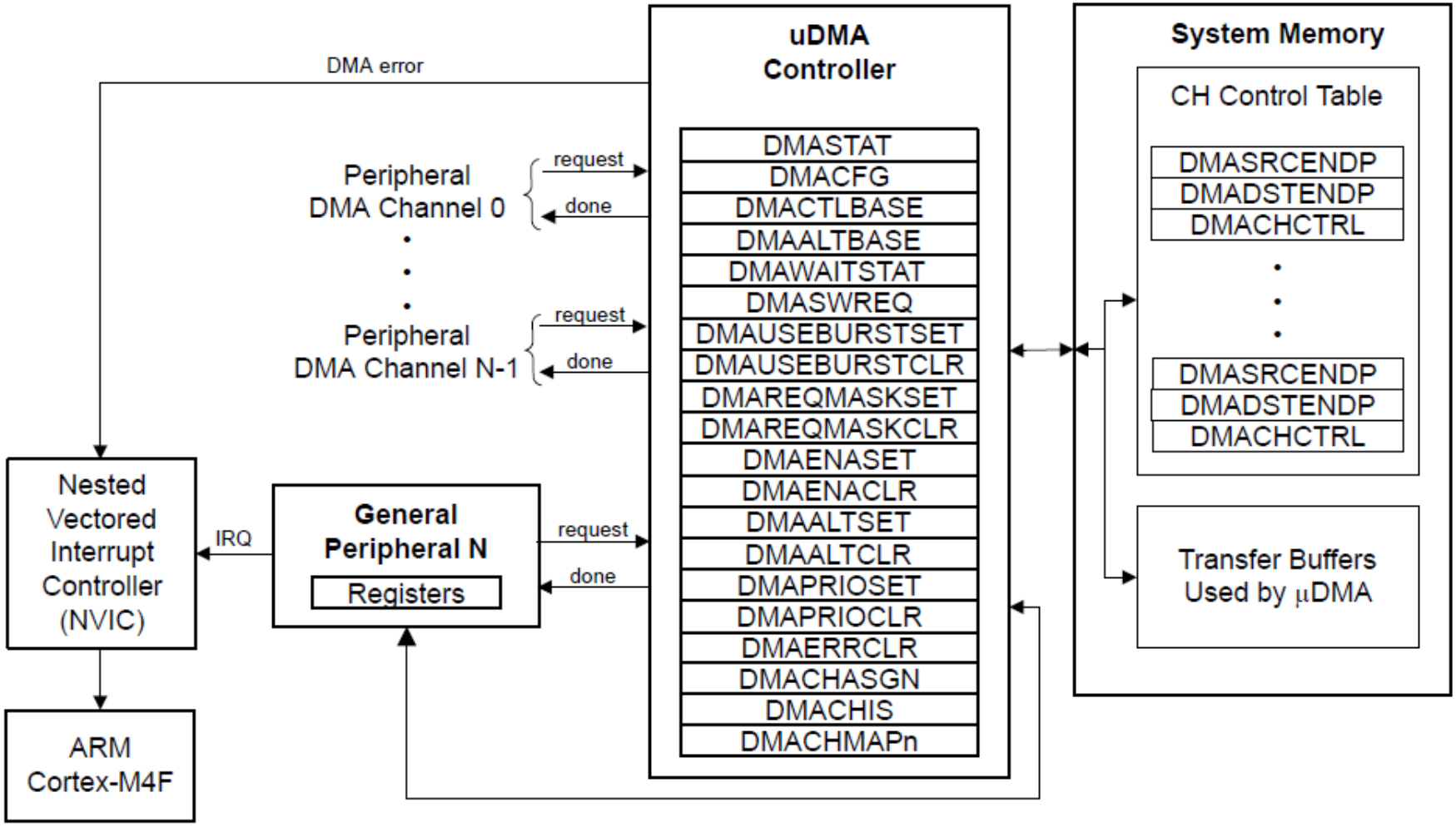
µDMA Features

- **Basic features:**
  - 32 channels, 2 priority levels, 8, 16 and 32-bit data element sizes
  - Transfer sizes of 1 to 1024 elements (in binary steps)
  - CPU bus accesses outrank DMA controller
- **Source – Destination:**
  - SRAM to SRAM , SRAM to peripheral and;
  - peripheral to SRAM transfers
  - no Flash or ROM transfers are possible
  - Source and destination address increment sizes: size of element, half-word, word, no increment
- **DMA Modes:**
  - Basic, Auto (transfer completes even if request is removed),
  - Ping-Pong and Scatter-gather (via a task list)
  - Interrupt on transfer completion (per channel)
  - Hardware and software triggers
  - Single and Burst requests

Transfer Types

- **Basic**
  - Single to Single; Single to Array; Array to Single; Array to Array
- **Auto**
  - Same as Basic but the transfer completes even if the request is removed
- **Ping-Pong**
  - Single to Array (and vice-versa). Normally used to stream data from a peripheral to memory. When the PING array is full the µDMA switches to the PONG array, freeing the PING array for use by the program.
- **Scatter-Gather**
  - Many Singles to an Array (and vice-versa). May be used to read elements from a data stream or move objects in a graphics memory frame.

SRAM & uDMA


DMA error
uDMA Controller
System Memory
CH Control Table
DMASRCENDP
DMADSTENDP
DMACHCTRL
Peripheral DMA Channel 0
request
done
Peripheral DMA Channel N-1
request
done
DMASTAT
DMACFG
DMACTLBASE
DMAALTBASE
DMAWAITSTAT
DMASWREQ
DMAUSEBURSTSET
DMAUSEBURSTCLR
DMAREQMASKSET
DMAREQMASKCLR
DMAENASET
DMAENACLR
DMAALTSET
DMAALTCLR
DMAPRIOSET
DMAPRIOCLR
DMAERRCLR
DMACHASGN
DMACHIS
DMACHMAPn
Nested Vectored Interrupt Controller (NVIC)
IRQ
General Peripheral N
Registers
request
done
ARM Cortex-M4F
Transfer Buffers Used by µDMA

µDMA Channels

- Each channel has 5 possible assignments made in the DMACHMAPn register

Enc.	0		1		2		3		4	
Ch #	Peripheral	Type	Peripheral	Type	Peripheral	Type	Peripheral	Type	Peripheral	Type
0	USB0 EP1 RX	SB	UART2 RX	SB	Software	B	GPTimer 4A	B	Software	B
1	USB0 EP1 TX	B	UART2 TX	SB	Software	B	GPTimer 4B	B	Software	B
2	USB0 EP2 RX	B	GPTimer 3A	B	Software	B	Software	B	Software	B
3	USB0 EP2 TX	B	GPTimer 3B	B	Software	B	Software	B	Software	B
4	USB0 EP3 RX	B	GPTimer 2A	B	Software	B	GPIO A	B	Software	B
5	USB0 EP3 TX	B	GPTimer 2B	B	Software	B	GPIO B	B	Software	B
6	Software	B	GPTimer 2A	B	UART5 RX	SB	GPIO C	B	Software	B
7	Software	B	GPTimer 2B	B	UART5 TX	SB	GPIO D	B	Software	B
8	UART0 RX	SB	UART1 RX	SB	Software	B	GPTimer 5A	B	Software	B
9	UART0 TX	SB	UART1 TX	SB	Software	B	GPTimer 5B	B	Software	B
10	SSI0 RX	SB	SSI1 RX	SB	UART6 RX	SB	GPTimer 6A	B	Software	B
11	SSI0 TX	SB	SSI1 TX	SB	UART6 TX	SB	GPTimer 6B	B	Software	B
12	Software	B	UART2 RX	SB	SSI2 RX	SB	GPTimer 7A	B	Software	B
13	Software	B	UART2 TX	SB	SSI2 TX	SB	GPTimer 7B	B	Software	B
14	ADC0 SS0	B	GPTimer 2A	B	SSI3 RX	SB	GPIO E	B	Software	B
15	ADC0 SS1	B	GPTimer 2B	B	SSI3 TX	SB	GPIO F	B	Software	B
16	ADC0 SS2	B	Software	B	UART3 RX	SB	GPTimer 8A	B	Software	B
17	ADC0 SS3	B	Software	B	UART3 TX	SB	GPTimer 8B	B	Software	B
18	GPTimer 0A	B	GPTimer 1A	B	UART4 RX	SB	GPIO B	B	Software	B
19	GPTimer 0B	B	GPTimer 1B	B	UART4 TX	SB	Software	B	Software	B
20	GPTimer 1A	B	Software	B	UART7 RX	SB	Software	B	Software	B

Channel Configuration

- Channel control is done via a set of control structures in a table
- The table must be located on a 1024-byte boundary
- Each channel can have one or two control structures; a primary and an alternate
- The primary structure is for BASIC and AUTO transfers. Alternate is for Ping-Pong and Scatter-gather

Control Structure Memory Map

Offset	Channel
0x0	0, Primary
0x10	1, Primary
...	...
0x1F0	31, Primary
0x200	0, Alternate
0x210	1, Alternate
...	...
0x3F0	31, Alternate

Channel Control Structure

Offset	Description
0x000	Source End Pointer
0x004	Destination End Pointer
0x008	Control Word
0x00C	Unused

Control word contains:

- Source and Dest data sizes
- Source and Dest addr increment size
- # of transfers before bus arbitration
- Total elements to transfer
- Useburst flag
- Transfer mode