M01: Embedded Systems Architecture

1.1. Overview: Computer Architecture

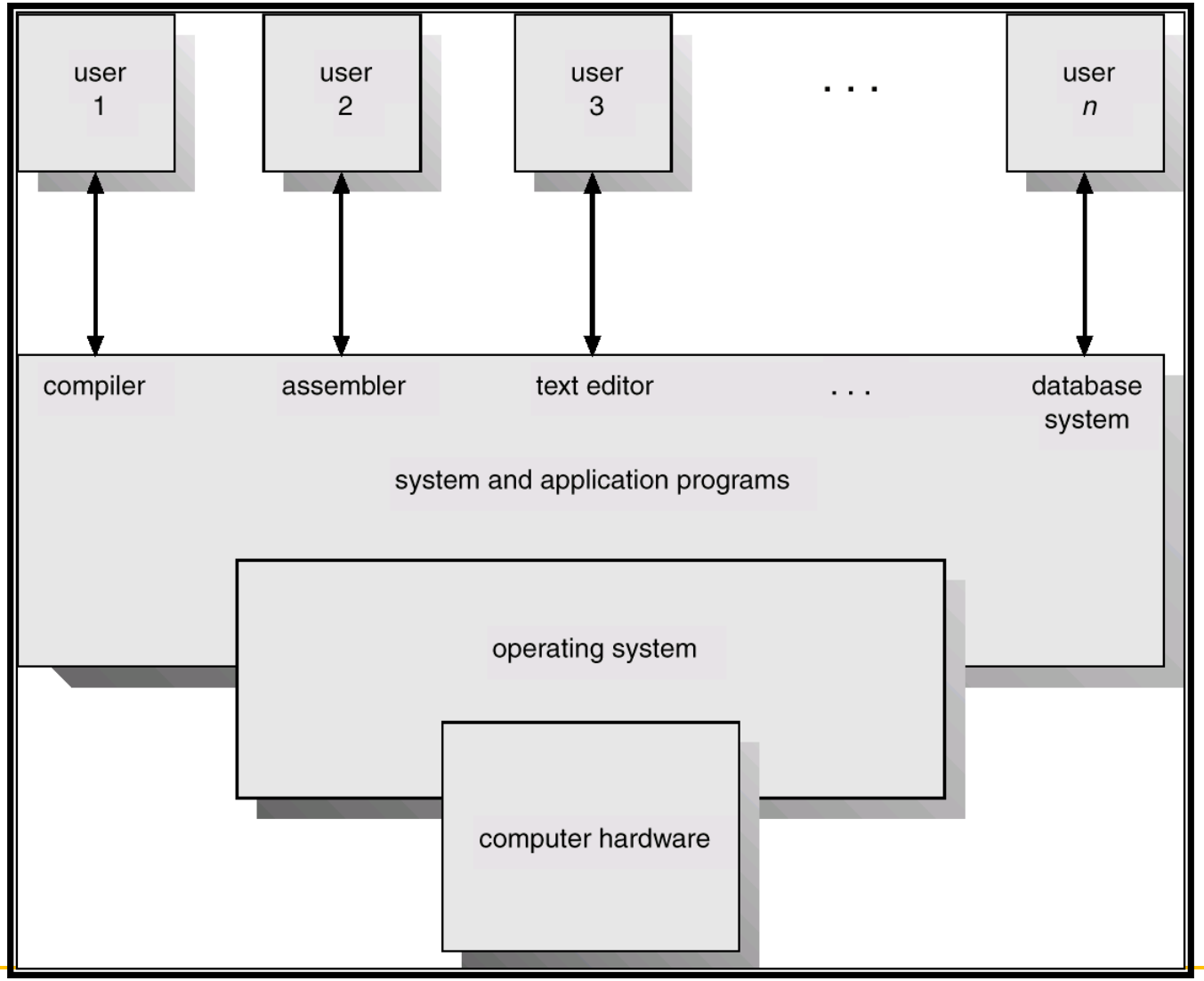
Ref: A. Silberschatz, P. B. Galvin, and G. Gagne, Operating System Concepts, Wiley, 2012

J. Valvano, Embedded Systems: Shape the World.

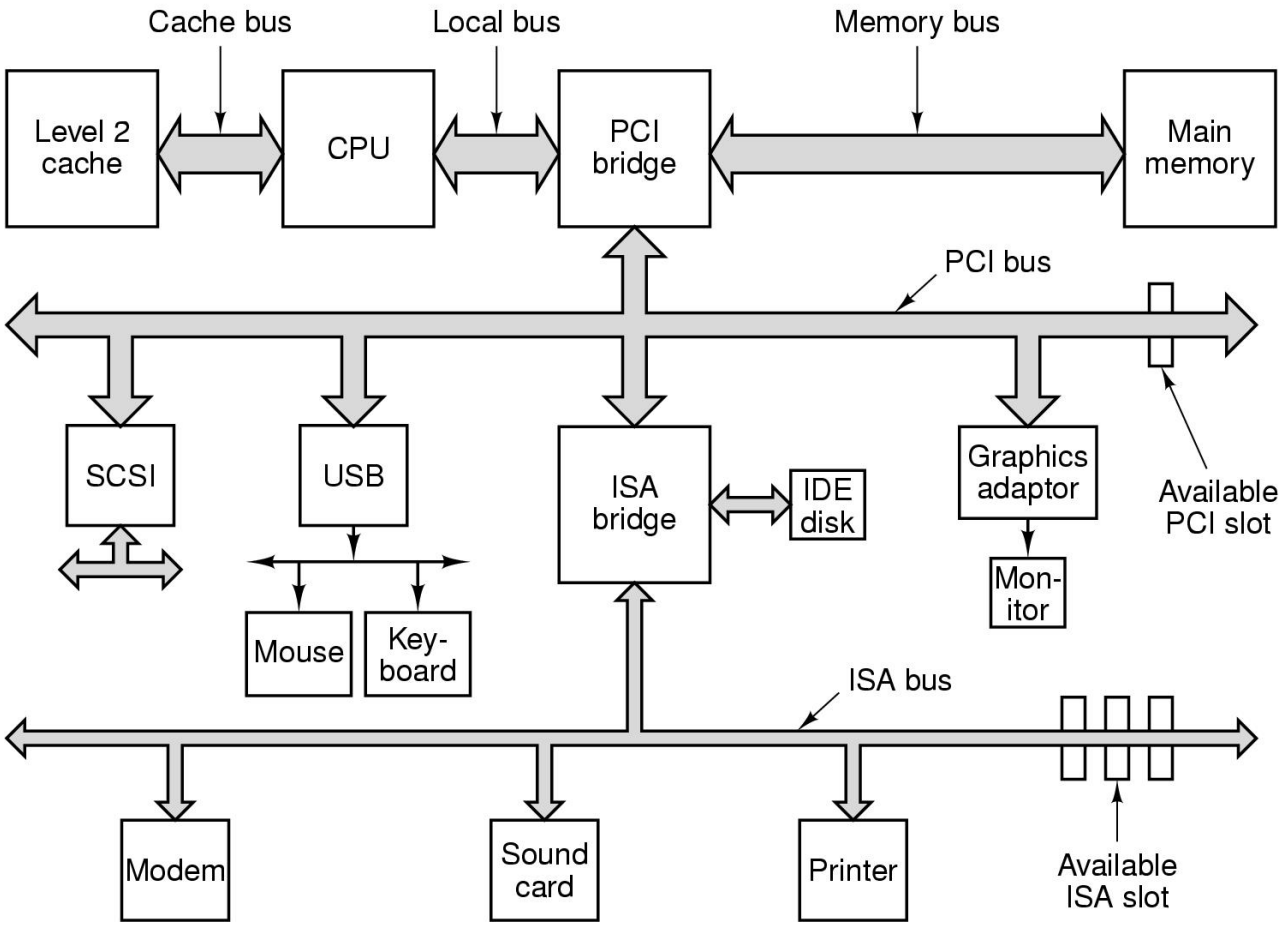
Computer System

- **Hardware** – provides basic computing resources (CPU, memory, I/O devices).
- **Operating system** – controls and coordinates the use of the hardware among the various application programs for the various users.
- **Applications programs** – define the ways in which the system resources are used to solve the computing problems of the users (compilers, database systems, video games, business programs).
- **Users** - people, machines, other computers.

Computer System



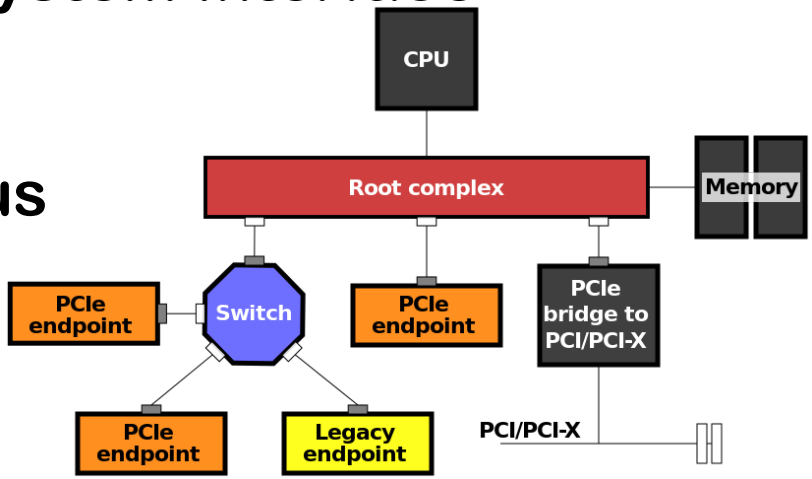
Computer Hardware Review



Structure of a large Pentium system

Buses: parallel or serial

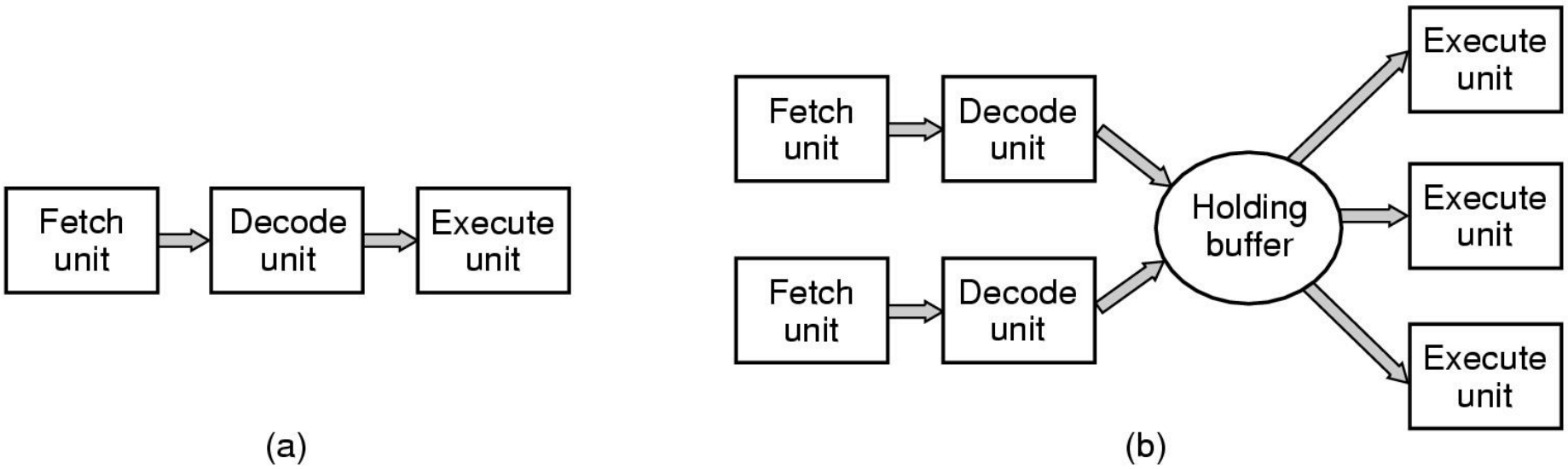
- Parallel buses:
  - ISA – Industry Standard Architecture
  - PCI – Peripheral Component Interconnect
  - IDE – Independent Drive Electronics (hard disk) or parallel ATA (AT Attachment)
  - SCSI – Small Computer System Interface
- Serial buses
  - USB – Universal Serial Bus
  - PCI Express - PCIe
  - IEEE 1394 -- FireWire
  - SATA -- Serial ATA



Types of CPU and Systems

- General purpose CPU:
  - good at handling user interface
- Digital Signal Processers (DSP):
  - strong at computing large amount of data
- Microcontrollers:
  - processors +memory+ I/O ports
- Embedded Systems: (System on a Chip):
  - microcontroller + peripherals

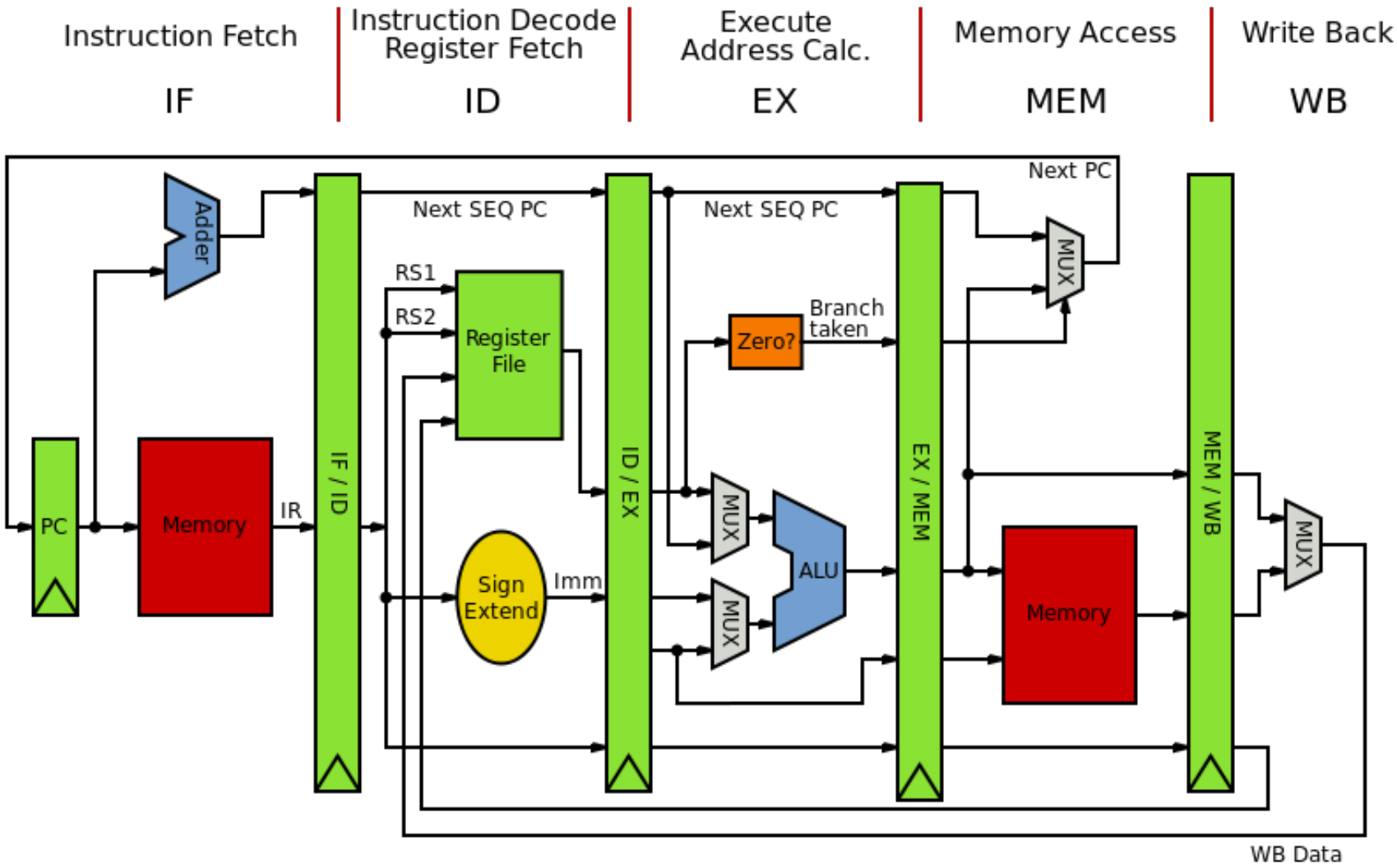
Central Processing Unit



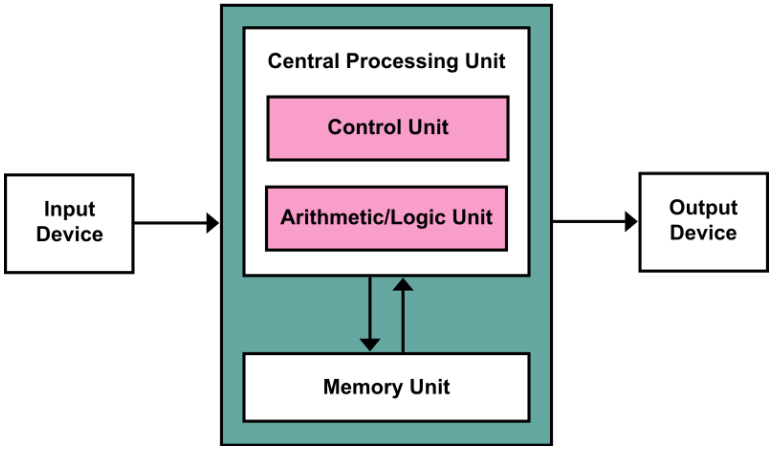
(a) A three-stage pipeline

(b) A superscalar CPU

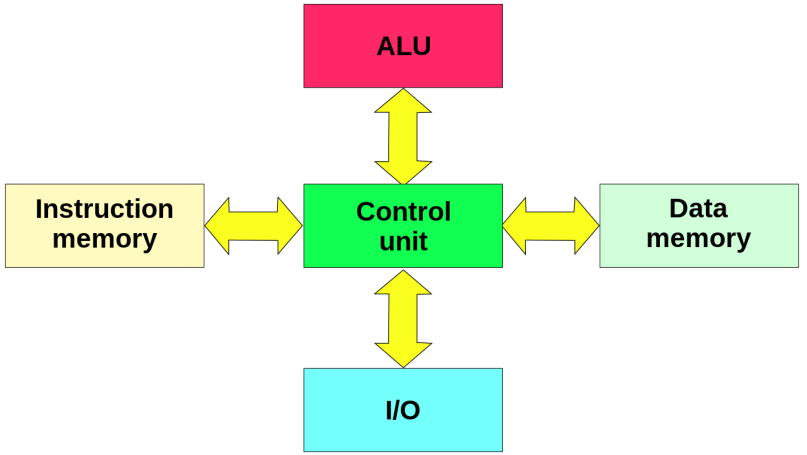
Von Neumann Architecture



Von Neumann vs. Harvard Architectures



Von Neumann (Princeton) architecture

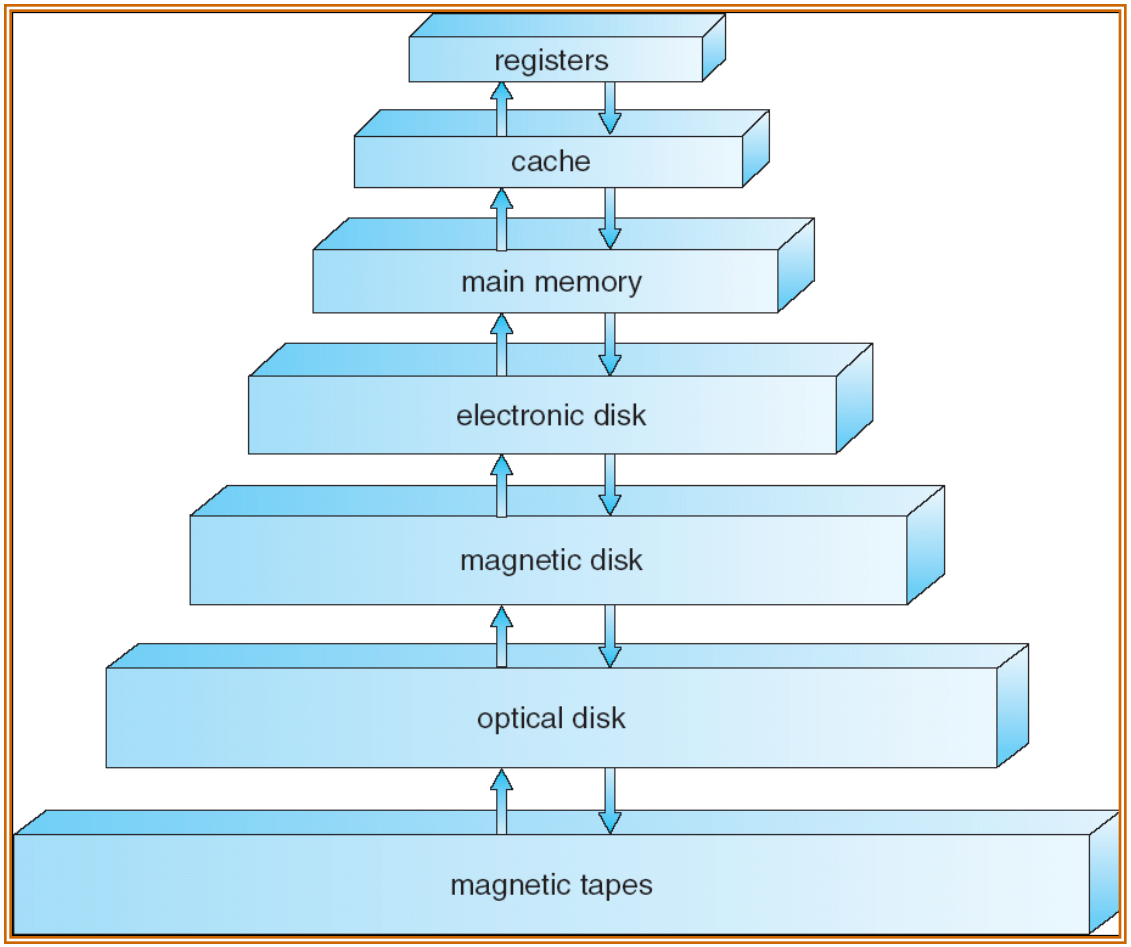


Harvard architecture

Storage Hierarchy

- Storage systems organized in hierarchy.
  - Speed and Cost
  - Volatility
    - Non-volatile: ROM, EPROM, EEPROM, FLASH
    - Volatile: RAM (DRAM, SRAM)
- *Primary (main) vs. Secondary.*
- *Caching* – copying information into faster storage system; main memory can be viewed as a last *cache* for secondary storage.

Storage-Device Hierarchy



Various Levels of Storage

Level	1	2	3	4
Name	registers	cache	main memory	disk storage
Typical size	< 1 KB	> 16 MB	> 16 GB	> 100 GB
Implementation technology	custom memory with multiple ports, CMOS	on-chip or off-chip CMOS SRAM	CMOS DRAM	magnetic disk
Access time (ns)	0.25 – 0.5	0.5 – 25	80 – 250	5,000.000
Bandwidth (MB/sec)	20,000 – 100,000	5000 – 10,000	1000 – 5000	20 – 150
Managed by	compiler	hardware	operating system	operating system
Backed by	cache	main memory	disk	CD or tape

I/O Structure

- Memory-mapped or Instruction-mapped
  - Memory-mapped I/O: like a memory and takes a block of memory
  - Instruction (Port)-mapped I/O: Each device connected to a controller
    - Some controllers provide a bus for one or more devices (i.e. SCSI)
    - Device driver for each device controller
      - Knows details of controller
      - Provides uniform interface to kernel

Computer Startup and Execution

- Bootstrap program is loaded at power-up or reboot
  - Typically stored in ROM or EEPROM, generally known as firmware
  - Initializes all aspects of system
  - Loads operating system kernel and starts execution
- Kernel runs, waits for event to occur
  - Interrupt from either hardware or software

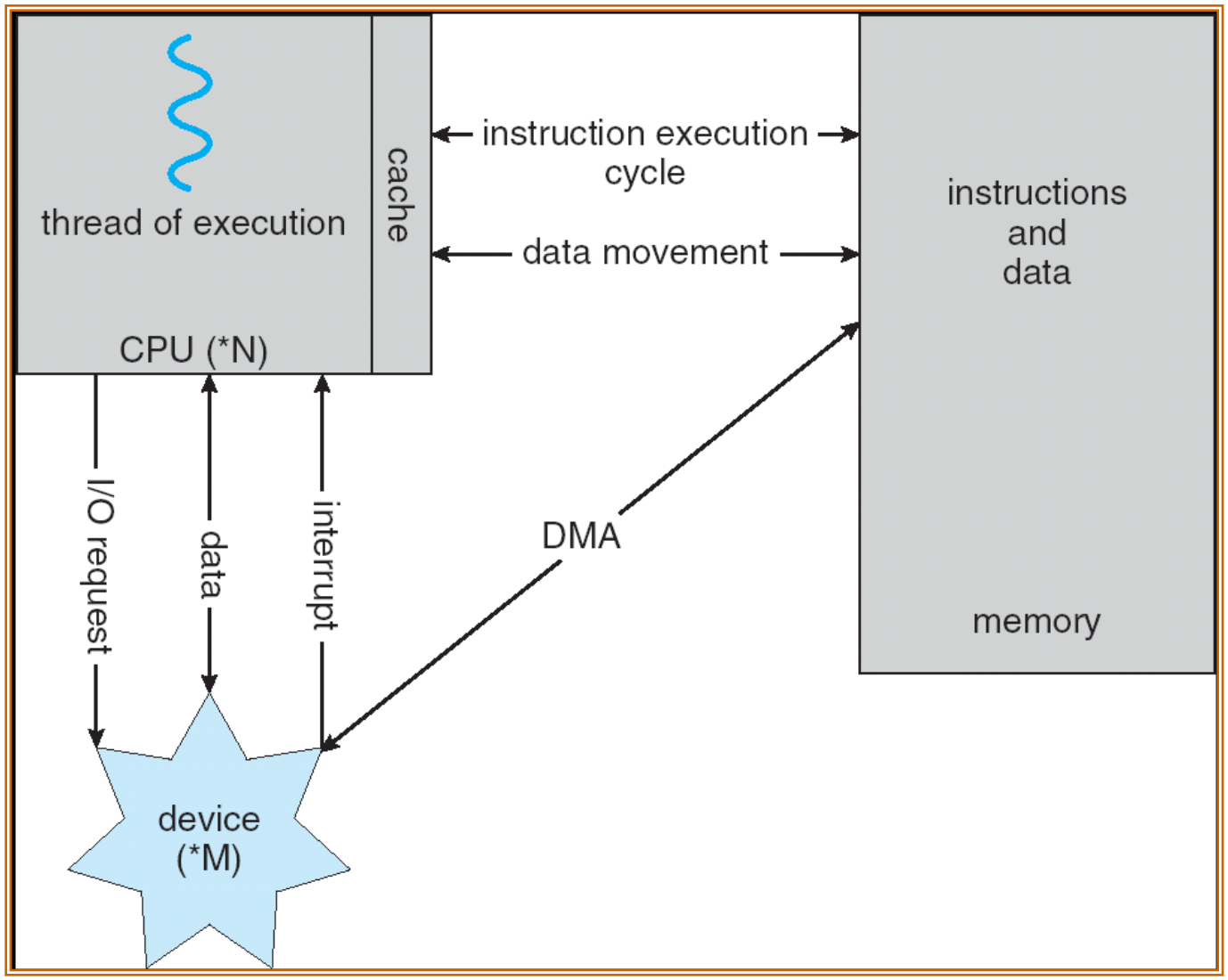
Computer-System Operation

- I/O devices and the CPU can execute concurrently
- Each device controller is in charge of a particular device type
- Each device controller has a local buffer

System Operation (2)

- CPU moves data from/to main memory to/from the local buffers.
- I/O: data transfer between the device to local buffer of controller.
- Device controller informs CPU that it has finished its operation by causing an interrupt.
- Direct Memory Access (DMA)

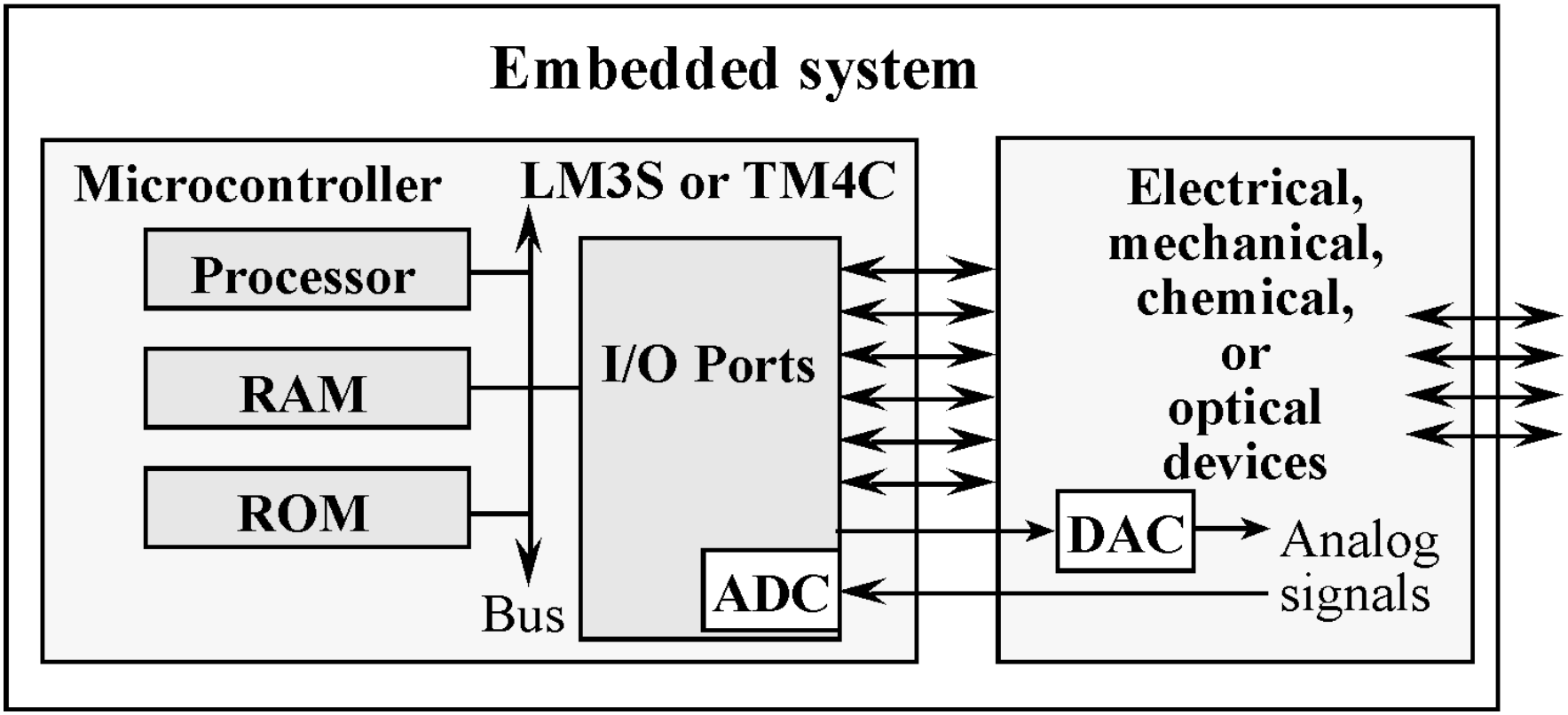
Interrupt and DMA



Interrupt and Trap

- Interrupt
  - hardware-generated interruption
  - an interrupt handler is called to deal with the cause; deal with I/O, etc
- A trap is a software-generated interrupt
  - used to make System Call
  - catch arithmetic errors, etc.
- Interrupt has higher priority than trap

Embedded Systems



- Hardware: processor, memory, I/O, ADC/DAC, power
- Software: Instruction set, firmware, middleware, API (Application Programming Interface), RTOS, DSP.

Instruction Set Architecture

- complex instruction set computer (CISC)
- reduced instruction set computer (RISC)
- minimal instruction set computer (MISC)
- one instruction set computer (OISC).

- *long instruction word* (LIW)
- very long instruction word (VLIW)
- *explicitly parallel instruction computing* (EPIC)