#define XAXIVDMA\_WRITE 1 /\*\*< DMA transfer into memory \*/

#define XAXIVDMA\_READ 2 /\*\*< DMA transfer from memory \*/

XPAR\_PS7\_DDR\_0\_S\_AXI\_BASEADDR 0x0010\_0000

#define FRAMEBUFFER\_GUI\_START\_ADDR XPAR\_PS7\_DDR\_0\_S\_AXI\_BASEADDR + 0x30000000 //0x3010\_0000

#define FRAMEBUFFER\_CAMERA\_START\_ADDR XPAR\_PS7\_DDR\_0\_S\_AXI\_BASEADDR + 0x3200\_0000 // shift by 32MB //0x3210\_0000

#define FRAMEBUFFER\_CAMERA\_FREEZE\_START\_ADDR XPAR\_PS7\_DDR\_0\_S\_AXI\_BASEADDR + 0x3240\_0000 // Shift by 4MB //0x3250\_0000

Start addr base fr base addr(外給) Read/Write皆為相同位址

VSIZE HSIZE Frame\_buffer Frame(相差2048x480=0xF0000)

Camera VDMA Read Channel 0x4300\_0050 0x4300\_0054 0x3210\_0000 0x3210\_0000(0x5c) MM2S\_START\_ADDR0

左小圖 (ChanBase: 0x4300\_0000) 0x321F\_0000(0x60) MM2S\_START\_ADDR1

Base: 0x4300\_0000 0x322E\_0000(0x64) MM2S\_START\_ADDR2

High: 0x4300\_ffff Write Channel 0x4300\_00A0 0x4300\_00A4 0x3210\_0000(0xAC) S2MM\_START\_ADDR0

VDMA (ChanBase: 0x4300\_0030) 0x321F\_0000(0xB0) S2MM\_START\_ADDR1

0x322E\_0000(0xB4) S2MM\_START\_ADDR2

Camera Freeze VDMA Read Channel 0x4303\_0050 0x4303\_0054 0x3250\_0000 0x3250\_0000(0x0c) MM2S\_START\_ADDR0

右大圖 (ChanBase: 0x4303\_0000) 0x325F\_0000(0x10) MM2S\_START\_ADDR1

Base: 0x4303\_0000 0x326E\_0000(0x14) MM2S\_START\_ADDR2

High: 0x4303\_ffff Write Channel 0x4303\_00A0 0x4303\_00A4 0x3250\_0000(0xAC) S2MM\_START\_ADDR0

(ChanBase: 0x4303\_0030) 0x325F\_0000(0xB0) S2MM\_START\_ADDR1

0x326E\_0000(0xB4) S2MM\_START\_ADDR2

MM2S: Memory Map to Stream S2MM: Stream to Memory Map

0x00 MM2S\_VDMACR MM2S VDMA Control Register 0x30 S2MM\_VDMACR S2MM VDMA Control Register

0x04 MM2S\_VDMASR MM2S VDMA Status Register 0x34 S2MM\_VDMASR S2MM VDMA Status Register

0x50 MM2S\_VSIZE MM2S V Size Register 0xA0 S2MM\_VSIZE S2MM V Size Register

0x54 MM2S\_HSIZE MM2S H Size Register 0xA4 S2MM\_HSIZE S2MM H Size Register

0x5C~98 MM2S\_START\_ADDR MM2S Start Address 0xAC~E8 S2MM\_START\_ADDR S2MM Start Address

0x28 PARK\_PRT\_REG MM2S/S2MM Park指針寄存器

DMA啟動 WRITE(S2MM) READ(MM2S)

Camera VDMA start hw 0x4300\_0030填bit0 0x4300\_0000填bit0

start tf 0x4300\_00A0填v 0x4300\_0050填v

Camera freeze VDMA start hw 0x4303\_0030填bit0 0x4303\_0000填bit0

start tf 0x4303\_00A0填v 0x4303\_0050填v

PS7\_DDR\_0 0010\_0000~3fff\_ffff

LOCK\_MONITOR 4120\_0000~4120\_ffff xgpio

Camera vdma 4300\_0000~4300\_ffff Xilinx\_VDMA\_v6.2\_PG020.pdf

Camera freeze vdma 4303\_0000~4303\_ffff 同上

Mixer 43cc\_0000~43cf\_ffff Xilinx\_VideoMixer\_v1.0\_PG243.pdf

VTG\_1(CH7038, 其他) 43c8\_0000~43c8\_ffff Xilinx\_VTC\_v6.1\_PG016.pdf

VTG\_0(TFP410, DVI上) 43c9\_0000~43c9\_ffff 同上

Camera\_freeze scaler 43d0\_0000~43d3\_ffff ??

xvprocss 43d1\_0000 xilinx video processing subsystem

xvprocss 43d2\_0000

Test Pattern Gen 43d4\_0000~43d4\_ffff Xilinx\_VTPG\_PG103.pdf

scaler

input stream output stream

VidStreamIn VidStreamOut

(17) (147)

640X480 1216X912

0~0xffff\_ffff 4G 0~(0x0200\_0000-1) 32MB 0~(0x0040\_0000-1) 4MB

(X\_st, Y\_st, W, H) Offset Alpha X\_st Y\_st W H BufferAddr

0x0000\_0100 0x0000\_0108 0x0000\_0110 0x0000\_0118 0x0000\_0128 0x0000\_0140

Layer0 0, 0, 1920, 1080 0x0000\_0000 0x43cc\_0100 0x43cc\_0108 0x43cc\_0110 0x43cc\_0118 0x43cc\_0128

Layer1 688, 16, 1216, 912 0x0000\_0100 0x43cc\_0200 0x43cc\_0208 0x43cc\_0210 0x43cc\_0218 0x43cc\_0228

Layer2 16, 584, 640, 480 0x0000\_0200 0x43cc\_0300 0x43cc\_0308 0x43cc\_0310 0x43cc\_0318 0x43cc\_0328

Layer3 0, 0, 1920, 1080 0x0000\_0300 0x43cc\_0400 0x43cc\_0408 0x43cc\_0410 0x43cc\_0418 0x43cc\_0428 0x43cc\_0440