Analysis and Modeling of a New Coupled-Inductor Buck–Boost DC–DC Converter for Renewable Energy Applications

Sara Hasanpour, Alfred Baghramian, and Hamed Mojallali

***Abstract*—A new coupled-inductor buck–boost converter (CIBuBoC) is proposed in this article. In the proposed CIBuBoC, an ultra-high step-up/step-down voltage conversion ratio and step-up/step-down boundary adjustment are achieved compared to the other related buck–boost converters using two power switches with simultaneous operation along with a coupled inductor. This circuit has a simple structure with two cascade semistage and some features including ultra-extended output voltage, continuous input current with low ripple, positive polarity of the output voltage, and common ground. These features make the CIBuBoC more suitable for many applications such as photovoltaic systems. Moreover, the voltage stress across each power switch is much lower than the other buck–boost converters, which led to power MOSFETs selection with lower drain-source ON-resistance (R_{ds}). Therefore, the proposed converter has also enough high efficiency. All steady-state and stress analysis, and also, comparisons with other related converters in continuous conduction mode are provided in detail. Also, using the state-space averaging technique, the low-frequency behavior of the proposed CIBuBoC is studied completely. Experimental results of a 100-W step-up 30–200 V and a 35-W step-down 30–22 V confirm the theoretical advantages of the proposed circuit.**

***Index Terms*—Coupled-inductor, quadratic buck-boost converter, small-signal modeling.**

I. Introduction

DC–DC buck–boost (step-up/step-down) converters that have adjustable output voltage with a wide range of variety are used as an important component for many power electronic applications such as renewable sources, portable devices, car electronic devices, mobile phones, LED products, and asymmetric digital subscriber line (ADSL) modems [1]–[6]. The desired features of these converters are noninverting wide high step-up/step-down voltage gain with proper efficiency, continuous input current with low ripple, low number of components, and low cost. However, because of the simple structure along with higher efficiency and cheaper implementation, the nonisolated structures of dc–dc converters are often used in low-power applications [7], [8].

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The conventional single-switch step-up/step-down converters consisting of CUK, ZETA, single-ended primary inductance, and the classic buck–boost converter are capable of converting the input voltage to both higher and lower voltage levels in the output. However, these conventional converters suffer from strong limitations on voltage gain ratio and component stresses, which limit their applications [9]–[11].

To improve the performance of the buck–boost converters, many modified nonisolated buck–boost converters have been introduced in recent years [10], [12]–[17]. In [10] and [12]–[14], new types of single-switch buck–boost converters with high voltage gain are introduced. Using a large number of components and discontinuous input current are common constraints for these topologies, which limits their applications. In [15] and [16], continuous input current single switch buck–boost converters are suggested. In these converters, a high-voltage conversion ratio using a large number of storage components has been provided. In addition, the negative polarity of the output voltage and lack of common ground between the input and output voltages are the main disadvantages of the converter in [15].

The double-switch buck–boost topologies reduce component stresses and increase the voltage gain simultaneously with a lower number of storage components. Two types of the double-switch buck–boost converter with low component stresses and a few numbers of storage components are suggested in [17] and [18]. However, the mentioned converters have demerits including limited voltage gain, input current with high ripple, lack of common ground, and nonsimultaneous switching process.

Recently, because of the importance of the step-up mode operation, further extension of voltage conversion range in buck–boost converters as a quadratic or semiquadratic coefficient has been paid more attention. A group of single-switch buck–boost structures with quadratic voltage gain ratios are introduced in [19]. However, these converters act more in step-down mode due to the use of clamp diode. To solve this problem, in [20], a new transformer-less buck–boost converter with quadratic high voltage gain along with common ground is suggested. Discontinuous input current with high ripple is the main disadvantage of this converter, which limits its application. Moreover, novel single- and double-switch buck–boost converters with semiquadratic voltage gain are introduced in [9], and [21]–[23]. The output voltage with negative polarity along with high voltage stress across the switch and input current with high ripple are the

main limitations of these mentioned converters. In [11], a new type of single-switch quadratic buck–boost topology with low input current ripple is proposed. This topology has been created from the cascade connection of boost, buck–boost, and buck converters. The negative polarity of output voltage and the use of a large number of semiconductor components are demerits of this converter. Furthermore, Fu *et al*. [24] and Mostaan *et al*. [25] proposed a new buck–boost converter with a semiquadratic voltage gain in low storage components. The lack of common ground is the main disadvantage of this converter. Also, a novel single switch semiquadratic buck–boost converter with continuous input current, common ground, and positive polarity has been recently suggested in [26].

Implementation of some efficient voltage boosting techniques such as multiplier cells, magnetic components, and switched-capacitors/inductors for buck–boost converters is limited since these methods often lead to loss of the step-down area. Therefore, the application of these methods for such converters with maintaining step-down specification has not been addressed adequately in the reported literature. In [27], an ultra-semi quadratic voltage gain with continous input current has been achieved using a switched-capacitor voltage boosting technique. However, the lack of common ground limits the application of this converter. Moreover, in [28] and [29], despite using a switched-capacitor cell in the middle stage of converter, high voltage gain has not been achieved.

Recently, coupled inductors (CL) have been more employed in dc–dc converters to achieve a wide range of voltage gain [2]. A great feature of using CL in buck–boost converters is a good adjustment of the step-down or step-up boundary by the help of the number of turns [30]–[34]. In [31], [32], and [34], high-gain buck–boost converters are achieved using CL. However, highinput current ripple and usage of a large number of switches with asynchronous gates are the main constraints for these converters. Also, a quasi-Y source-based buck–boost dc–dc converter is introduced in [33]. This converter has achieved a very high voltage gain using two inductors and one three winding CL. Nevertheless, the severe slope of the voltage gain ratio makes controlling of the converter very difficult.

The aim of this article is to provide a new configuration of a nonisolated double-switch buck–boost converter with CL as two-cascade semistage (CIBuBoC). In this converter, high semiquadratic voltage gain along with step-up/step-down boundary adjustment can be achieved with an appropriate turns ratio of the CL. Then, the duty cycle can be reduced, which leads to the decrease in the switching losses significantly. The other merits of the proposed CIBuBoC are continuous input current with low ripple, simple structure, output positive polarity, and common ground between the input and output voltages. In addition, because of lower component stresses, power losses are decreased, which leads to efficiency improvement.

The rest of this article organized as follows. Operational principles of the proposed CIBuBoC is in Section II. Steady-state analysis, efficiency analysis, and comparing with other related converters are presented in Sections III–V. Section VI describes modeling of the proposed converter. Key parameter design guidance is discussed in Section VII. To validate mathematical derivations, experimental results are given in Section VIII. Finally, the conclusion is drawn in Section IX.

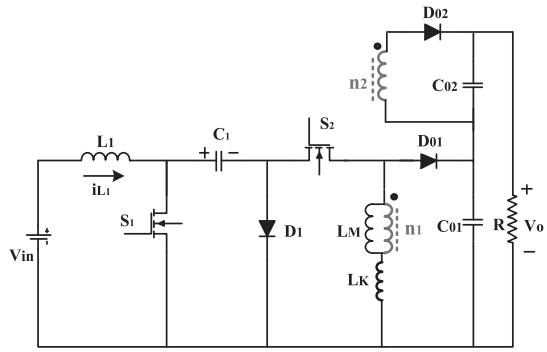

Fig. 1. Circuit diagram of the proposed CIBuBoC.

II. Operational Principles of the Proposed CIBuBoC

Fig. 1 shows the equivalent circuit of the proposed CIBuBoC. This converter consists of two power switches (S_1 and S_2), an input inductor (L_1), a CL, three diodes (D_1, $D_{01,}$ and D_{02}), and three capacitors (C_1, $C_{01,}$ and C_{02}). Two power switches of the converter are operated simultaneously. Based on the equivalent circuit, the conductivity of the diodes D_1, $D_{01,}$ and D_{02} is opposite of the switches S_1 and S_2. It is clear from this figure that the proposed CIBuBoC has continuous input current, simple structure, positive polarity in the output voltage, and common ground between the input and output voltages. To simplify the steady-state analysis, some assumptions are considered as follows.

1) All semiconductor components are ideal.
2) All capacitors are large enough such that their voltages are considered to be nearly constant values during a switching cycle.
3) The CL is modeled as an ideal transformer including magnetizing inductor (L_m) and merged leakage inductor in the primary side (L_k) with coupling coefficient $K = L_m/(L_m + L_k)$.
4) Input inductor and magnetizing inductor of CL are considered large enough, and therefore, the current ripples across them are neglected.

There are only two operating modes in each switching cycle of the proposed CIBuBoC. The current flow path of the proposed converter for operating modes is shown in Fig. 2. Also, key waveforms of components voltages and currents of the CIBuBoC in conduction mode (CCM) for one switching cycle are depicted in Fig. 3.

First mode [t_0–t_1]: At the beginning of this mode at $t = t_0$, the power switches S_1 and S_2 are turned ON simultaneously, whereas all diodes are reversely biased and turned OFF. As shown in Fig. 2(a), the voltages of input source and capacitor C_1 are applied to the input inductor (L_1) and the primary side of CL (L_m and L_k), respectively. Therefore, these inductors receive energy and their current (i_{L1}, i_{Lm}, and i_{Lk}) is increased linearly. In this time interval, the output capacitors C_{01} and C_{02} supply the load in series. The following equations are written in

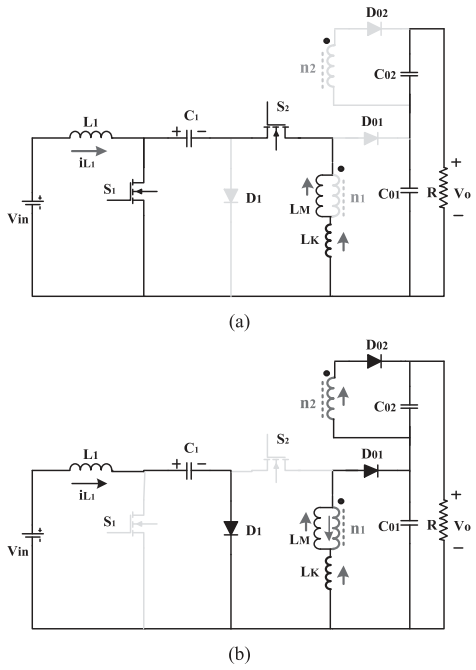

Fig. 2. Current-flow path of operating modes during one switching period at CCM operation. (a) Mode I. (b) Mode II.

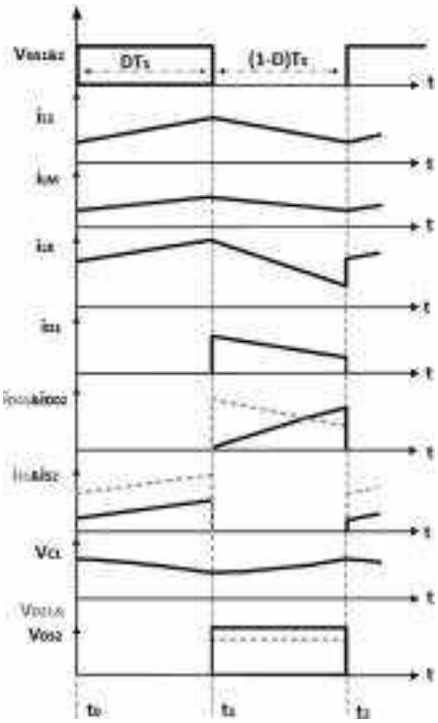

Fig. 3. Key waveforms of the proposed CIBuBoC components in CCM.

this mode

$$V_{L1} = V_{\text{in}} \tag{1}$$

$$V_{LM} + V_{LK} = V_{C1} \tag{2}$$

$$I_{S2} = I_{LM} = I_{LK} \tag{3}$$

$$I_{S1} = I_{L1} + I_{LM}. \tag{4}$$

Second mode [t_1–t_2]: In this mode, as shown in Fig. 2(b), the power switches S_1 and S_2 are turned OFF. Therefore, all diodes including D_1, D_{01}, and D_{02} are turned ON, simultaneously. During this time interval, the capacitor C_1 is charged by the input inductor current. The energy of magnetizing inductor L_m is transferred to the output through the output diodes D_{01} and D_{02}. Then, the currents of these inductors (i_{L1} and i_{LM}) are decreased. Since the magnetizing and leakage inductors' current are equal in the mode *I*, the output diode D_{02} current increases under the zero-current condition. The capacitor C_1 clamps the voltage across the power switch S_1. The following equations are expressed in this mode

$$V_{L1} = V_{\text{in}} - V_{C1} \tag{5}$$

$$V_{LM} + V_{LK} = V_{C01} \tag{6}$$

$$I_{D1} = I_{L1} \tag{7}$$

$$I_{D01} = I_{LK}. \tag{8}$$

III. Steady-State Analysis of the Proposed CIBuBoC

A. Voltage Gain

To simplify the determination of steady-state capacitor voltages and voltage gain of the proposed CIBuBoC, the leakage inductor is ignored. By applying the volt–second balance principle on the inductors L_1 and L_M and using (1)–(8), the following equations are given as

$$\begin{cases} DV_{\text{in}} + (1-D)(V_{\text{in}} - V_{C1}) = 0 \\ DV_{C1} - (1-D)V_{01} = 0 \\ V_{02} = nV_{01} \end{cases} \tag{9}$$

where D is the duty cycle of power switches, and $n = n_1/n_2$ is the turns ratio of the CL. By the help of (9), the voltage of middle capacitor C_1 is achieved as

$$V_{C1} = \frac{V_{\text{in}}}{1-D}. \tag{10}$$

The voltage stresses across the output capacitors V_{C01} and V_{C02} in CCM are expressed as

$$V_{C01} = \frac{D}{(1-D)^2} V_{\text{in}} \tag{11}$$

$$V_{C02} = nV_{C01} = \frac{n.D}{(1-D)^2} V_{\text{in}}. \tag{12}$$

The output voltage is obtained from the sum of the output capacitors voltages as follows:

$$V_O = V_{C01} + V_{C02}. \tag{13}$$

Consequently, the static voltage conversion ratio of the proposed CIBuBoC is achieved as

$$M_{\text{Ideal}}^{\text{CCM}} = \frac{V_o}{V_{\text{in}}} = \frac{(1+n)D}{(1-D)^2} V_{\text{in}}. \tag{14}$$

The ideal voltage conversion ratio of the proposed CIBuBoC is increased exponentially versus the duty cycle as semiquadratic form. Also, it is increased proportionally versus turns ratio of CL, which results in an ultra-voltage gain ratio. Fig. 4 shows

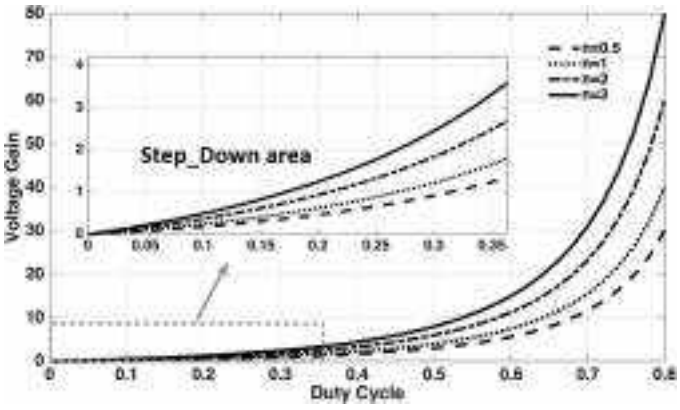

Fig. 4. Performance boundary between step-down and step-up of the CIBuBoC versus turns ratio of CL.

the voltage gain curve of the proposed converter under various turns ratio (*n)* of the CL and duty cycle. It is clearly obvious that the performance boundary between the step-down and step-up modes of converter depends directly on the turns ratio of CL. Increasing the number of turns ratio of CL leads to reduced step-down range and increased step-up range, which can be considered as benefits of the CIBuBoC.

B. Voltage Stresses of Semiconductors

One of the most important factors in proper selection of the circuit components is voltage stresses across the semiconductor components. Given the assumption of ignoring ripples of the circuit capacitors and using (1), (5), and (9), the maximal voltage stresses on semiconductor components consisting of the power switches S_1 and S_2 and diodes D_1, $D_{01,}$ and D_{02} on their OFF-state mode are obtained as follows:

$$V_{\mathrm{ds1}} = V_{D1} = \frac{V_{\mathrm{in}}}{1-D} = \frac{V_O(1-D)}{(1+n)D} \tag{15}$$

$$V_{\mathrm{ds2}} = V_{01} = \frac{DV_{\mathrm{in}}}{(1-D)^2} = \frac{V_O}{(1+n)} \tag{16}$$

$$V_{D01} = \frac{V_{\mathrm{in}}}{(1-D)^2} = \frac{V_O}{(1+n)D} \tag{17}$$

$$V_{D02} = \frac{nV_O}{(1+n)D}. \tag{18}$$

It is obvious from (15)–(18) that the maximal voltage stresses depends inversely on the turns ratio of CL. Therefore, by increasing the number of turns ratio, the voltage stresses are reduced significantly, and the efficiency is improved.

C. Current Stresses of Semiconductors

Assuming a lossless system and neglecting the current ripples of input and magnetizing inductors, the average value of the input inductor current is obtained as follows:

$$I_{\mathrm{in\,avg}} = I_{L1} = M_{\mathrm{Ideal}}^{\mathrm{CCM}} \cdot I_O. \tag{19}$$

Here, *M* is the static voltage conversion ratio expressed in (14), and I_o is the output load current. By applying the ampere–second balance on the output capacitors C_{01} and C_{02}, the maximal current passing through the diodes D_1, $D_{01,}$ and D_{02} is given as follows:

$$I_{D01(\mathrm{peak})} = I_{D02(\mathrm{peak})} = \frac{I_O}{1-D} \tag{20}$$

$$I_{D1(\mathrm{peak})} = I_{L1(\mathrm{Average})} = M_{\mathrm{Ideal}}^{\mathrm{CCM}} \cdot I_O. \tag{21}$$

Applying Kirchhoff's current law in the primary side of CL, the maximal current of the magnetizing inductor is calculated as

$$I_{LM(\mathrm{peak})} = \frac{(1+n)I_O}{1-D}. \tag{22}$$

Using (3), (4), (18), and (22), the maximal current and the root mean square (rms) values through the power switches are obtained as follows:

$$I_{S2(\mathrm{peak})} = I_{LM} = \frac{(1+n)I_O}{1-D} \tag{23}$$

$$I_{S2(\mathrm{rms})} = \frac{(1+n)V_O}{R(1-D)}\sqrt{D} \tag{24}$$

$$I_{S1(\mathrm{peak})} = I_{L1} + I_{LM} = \frac{(1+n)I_O}{(1-D)^2} \tag{25}$$

$$I_{S1(\mathrm{rms})} = \frac{(1+n)V_O}{R(1-D)^2}\sqrt{D}. \tag{26}$$

IV. Efficiency Analysis

Normally, the main power losses are caused by the parasitic elements of each one of the converter components. In fact, the power losses in dc–dc converters are divided into four groups including power switch devices (MOSFETs), magnetic components (inductors and CL), diodes, and capacitors. By assuming CCM operation along with ignoring the current ripple across the inductors (L_1 and L_M) and the voltage ripple of capacitors (C_1, $C_{01,}$ and C_{02}), the total power dissipation of the proposed CIBuBoC is obtained as follows:

$$\mathrm{Ploss} = P_{\mathrm{SW}}^{\mathrm{loss}} + P_{\mathrm{Diods}}^{\mathrm{loss}} + P_{\mathrm{Cap.}}^{\mathrm{loss}} + P_{\mathrm{Mag.}}^{\mathrm{loss}}. \tag{27}$$

A. Power Loss of MOSFETs

The power losses of MOSFETs are divided into two main parts: conduction losses and ON-OFF-state losses. The MOSFETs conduction losses are expressed as

$$P_{\mathrm{SW(Cond.)}}^{\mathrm{loss}} = R_{\mathrm{ds1(on)}} \cdot I_{\mathrm{ds1(rms)}}^2 + R_{\mathrm{ds2(on)}} \cdot I_{\mathrm{ds2(rms)}}^2 \tag{28}$$

where $R_{\mathrm{ds(on)}}$ is the field-effect transistors ON-resistor, and $I_{\mathrm{ds1(rms)}}$ and $I_{\mathrm{ds2(rms)}}$ are the rms values of the power MOSFETs S_1 and S_2 ON-state current, respectively. By substituting (23) and (25) into (28), the MOSFETs conduction losses are obtained as the following:

$$P_{\mathrm{SW(Cond.)}}^{\mathrm{loss}} = \frac{R_{\mathrm{ds1(on)}} \cdot (1+n)^2 P_o D}{R(1-D)^4} + \frac{R_{\mathrm{ds2(on)}} \cdot (1+n)^2 P_o D}{R(1-D)^2}. \tag{29}$$

Also, the turn-OFF/ON states losses of the power MOSFETs S_1 and S_2 associated with their drain-source voltage stresses are calculated as

$$P^{\text{loss}}_{\text{SW(on/off)}} = \frac{1}{2T_S}\left[I_{\text{ds1}}V_{\text{ds1}}(t_{d(\text{off1})} + t_{d(\text{on1})}) + I_{\text{ds2}}V_{\text{ds2}}(t_{d(\text{off2})} + t_{d(\text{on2})})\right] \quad (30)$$

where $t_{d(\text{off})}$ and $t_{d(\text{on})}$ are turn-ON and turn-OFF times of the MOSFETs. By substituting (15) and (16) in (30), the turn-OFF/ON states losses are obtained as

$$P^{\text{loss}}_{\text{SW(on/off)}} = \frac{1}{2T_S}\left[\frac{I_O}{(1-D)}\frac{V_O}{D}(t_{d(\text{off1})} + t_{d(\text{on1})}) + \frac{I_O}{(1-D)}V_O(t_{d(\text{off2})} + t_{d(\text{on2})})\right]. \quad (31)$$

B. Power Loss of Magnetics Components

The magnetic components L_1 and CL losses are calculated using the rms values of their currents as follows:

$$P^{\text{loss}}_{\text{Mag.}} = r_{L1}\cdot I^2_{L1(\text{rms})} + r_{LM}\cdot I^2_{LM(\text{rms})} \quad (32)$$

$$P^{\text{loss}}_{\text{Mag.}} = \frac{r_{L1}\cdot(1+n)^2D^2P_o}{R(1-D)^4} + \frac{r_{LM}\cdot(1+n)^2P_o}{R(1-D)^2} \quad (33)$$

where r_{L1} and r_{LM} are the parasitic resistors measured by using *RLC* meters.

C. Power Loss of Diodes

Diodes of the proposed converter in the ON-state present a forward resistance loss, and forward drop voltage losses are expressed as

$$P^{\text{loss}}_{\text{Diode}(r_D)} = r_{D1}\cdot I^2_{D1(\text{rms})} + r_{D01}\cdot I^2_{D01(\text{rms})} + r_{D02}\cdot I^2_{D02(\text{rms})} \quad (34)$$

$$P^{\text{loss}}_{\text{Diode}(V_F)} = V_{F1}I_{D1(\text{AVG})} + V_{F01}I_{D01(\text{AVG})} + V_{F02}I_{D02(\text{AVG})}. \quad (35)$$

By means of the rms and averaged values of diodes current, (34) and (35) are calculated as

$$P^{\text{loss}}_{\text{Diode}(r_D)} = \frac{r_{D1}\cdot(1+n)^2D^2P_o}{R(1-D)^3} + \frac{r_{D01}\cdot P_o}{R(1-D)} + \frac{r_{D02}\cdot P_o}{R(1-D)} \quad (36)$$

$$P^{\text{loss}}_{\text{Diode}(V_F)} = V_{F1}\cdot\frac{(1+n)DV_O}{R(1-D)} + V_{F01}\cdot\frac{V_O}{R} + V_{F02}\cdot\frac{V_O}{R}. \quad (37)$$

D. Power Loss of Capacitors

The power losses in the capacitors are caused by the equivalent series resistance (r_{esr}). The rms values of their currents can be simply expressed as follows:

$$P^{\text{loss}}_{\text{Cap.}} = r_{\text{esr}C1}\cdot I^2_{C1(\text{rms})} + r_{\text{esr}C01}\cdot I^2_{C01(\text{rms})} + r_{\text{esr}C02}\cdot I^2_{C02(\text{rms})} \quad (38)$$

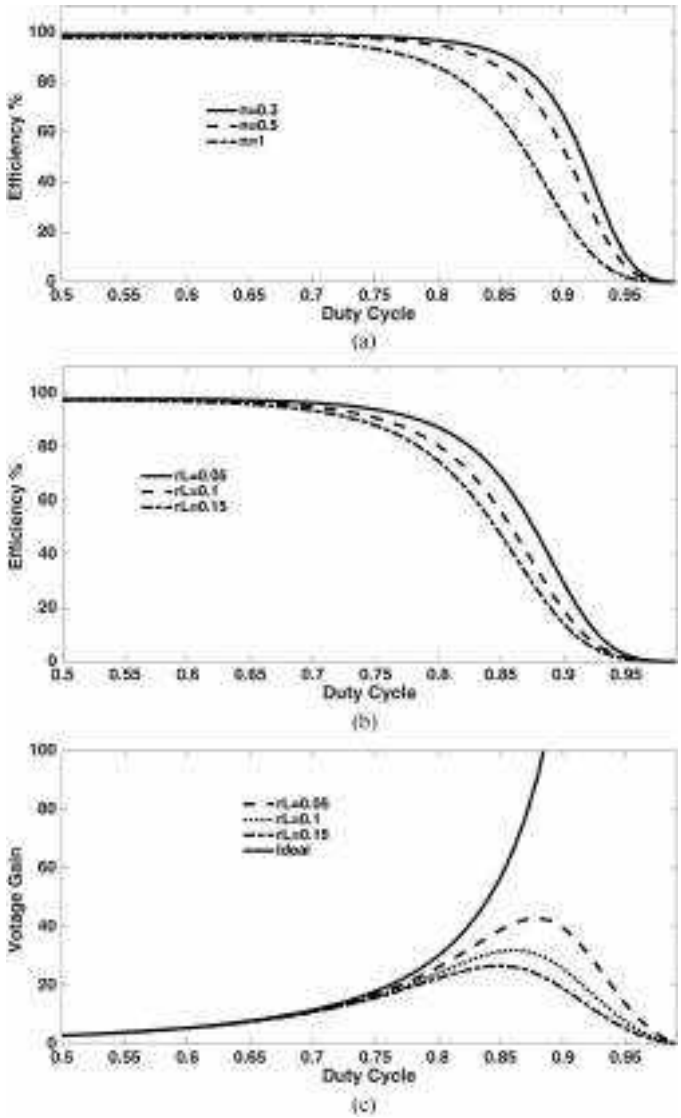

Fig. 5. CIBuBoC in nonideal conditions. (a) Efficiency versus the duty cycle and turns ratio of CL. (b) Efficiency versus the duty cycle and parasitic element. (c) Voltage gain versus the duty cycle and parasitic element.

$$P^{\text{loss}}_{\text{Cap.}} = \frac{r_{\text{esr}C1}(1+n)^2DP_O}{R(1-D)^3} + \frac{r_{\text{esr}C01}P_O}{R(1-D)} + \frac{r_{\text{esr}C02}P_O}{R(1-D)}. \quad (39)$$

Consequently, the efficiency of the proposed CIBuBoC is defined as

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}}. \quad (40)$$

Moreover, the voltage conversion ratio by considering (40) and the parasitic elements can be estimated as follow:

$$M = \eta\frac{(1+n)\,D}{(1-D)^2}. \quad (41)$$

The efficiency versus the duty cycle plot and the different turns ratio of CL of the CIBuBoC are demonstrated in Fig. 5(a). The values of parameters are selected as $V_{\text{in}} = 20$ V, $R_{\text{Load}} = 500\ \Omega$, $r_{L1} = \text{r}_{Lm} = 50\,\text{m}\Omega$, $f_s = 45$ kHz, $t_{d(\text{off})} = 35$ ns,

TABLE I
COMPARISON BETWEEN THE PROPOSED CIBUBOC AND OTHER RELATED CONVERTERS

Converter topology	No. of components					Voltage gain	L.I.C.R	C.G	Voltage stress on switches (S_1, S_2)	Current stress of the switches	Voltage stress on output diodes
	S	D	C	Core	=T						
[9]	1	3	2	2	8	$\frac{-(2D-D^2)}{(1-D)^2}$	NO	YES	$\frac{V_o}{2D-D^2}$	$\frac{(2-D)I_o}{(1-D)^2}$	$\frac{V_o}{2D-D^2}$
[10]	1	3	5	3	12	$\frac{-3D}{1-D}$	NO	YES	$\frac{Vo}{3D}$	$\frac{3I_o}{(1-D)}$	$\frac{V_o}{3D}$
[11]	1	5	3	3	12	$-(\frac{D}{1-D})2$	YES	YES	$\frac{Vo}{D^2}$	$\frac{(D^2-D+1)I_o}{(1-D)^2}$	$\frac{V_o}{D}$
[20]	2	2	2	2	8	$(\frac{D}{1-D})2$	NO	YES	$\frac{(1-D)Vo}{D^2}, \frac{Vo}{D}$	$\frac{D^3I_o}{(1-D)^4}, \frac{D^2I_o}{(1-D)^3}$	$\frac{V_o}{D}$
[21]	2	2	2	2	8	$\frac{-(2D-D^2)}{(1-D)^2}$	NO	YES	$\frac{(1-D)V_o}{2D-D^2}, \frac{V_o}{2D-D^2}$	$\frac{I_o}{(1-D)^2}, \frac{I_o}{(1-D)}$	$\frac{V_o}{2D-D^2}$
[22]	1	3	2	2	8	$\frac{-(2D-D^2)}{(1-D)^2}$	NO	YES	$\frac{Vo}{2D-D^2}$	$\frac{2I_o}{(1-D)}$	$\frac{(1-D)V_o}{2D-D^2}, \frac{V_o}{2D-D^2}$
[23]	2	2	2	2	8	$\frac{D}{(1-D)^2}$	NO	NO	$\frac{(1-D)V_o}{D}, \frac{(1-D^2)V_o}{D-D^2}$	$\frac{DI_o}{(1-D)^2}, \frac{I_o}{(1-D)}$	$\frac{V_o}{D}$
[24]	1	3	2	2	8	$\frac{D}{(1-D)^2}$	YES	NO	$\frac{(1-D)Vo}{D}$	$\frac{(2-D)I_o}{(1-D)^2}$	V_o
[25]	2	2	2	2	8	$(\frac{D}{1-D})2$	NO	NO	$\frac{(1-D)Vo}{D^2}, \frac{(1-2D)Vo}{D^2}$	$\frac{(D^2-D+1)I_o}{(1-D)^2}, \frac{DI_o}{(1-D)}$	$\frac{V_o}{D}$
[26]	2	2	2	2	8	$\frac{D}{(1-D)^2}$	YES	YES	$\frac{(1-D)Vo}{D}, V_o$	$\frac{I_o}{(1-D)^2}, \frac{I_o}{(1-D)}$	$\frac{V_o}{D}$
[27]	2	3	3	2	12	$\frac{2D}{(1-D)^2}$	YES	NO	$\frac{(1-D)Vo}{2D}, \frac{(1+D)Vo}{2D}$	$\frac{(1+D)I_o}{(1-D)^2}, \frac{I_o}{(1-D)}$	$\frac{V_o}{D}$
[29]	1	2	4	3	10	$\frac{2D}{1-D}$	NO	YES	$\frac{V_o}{2D}$	$\frac{4DI_o}{(1-D)^2}$	$\frac{V_o}{2D}$
Proposed CIBuBoC	2	3	3	2	10	$\frac{(1+n)D}{(1-D)^2}$	YES	YES	$\frac{(1-D)Vo}{(1+n)D}, \frac{V_o}{(1+n)}$	$\frac{(1+n)I_o}{(1-D)^2}, \frac{(1+n)I_o}{(1-D)}$	$\frac{V_o}{(1+n)D}, \frac{nV_o}{(1+n)D}$

S = Switch, D = Diode, C = Capacitor, T = Total device count, L.I.C.R = Low Input Current Ripple, C.G = Common ground between input and output voltage.

$t_{d(\mathrm{on})} = 30\,\mathrm{ns}$, $r_{\mathrm{ds1,2(ON)}} = 10\ \mathrm{m\Omega}$, $r_{D1} = r_{D01} = r_{D02} = 7\,\mathrm{m\Omega}$, $r_{\mathrm{esr}C1} = 25\,\mathrm{m\Omega}$, $r_{\mathrm{esr}C01} = r_{\mathrm{esr}C02} = 250\,\mathrm{m\Omega}$, $V_{F1} = V_{F01} = V_{F02} = 0.7\,\mathrm{V}$, and $n = 0.5$. In addition, the calculated efficiency and voltage gain curves versus the duty cycle of the proposed CIBuBoC under some copper resistances of the input inductor are shown in Fig. 5(b) and (c), respectively. It is worth noting that the losses of the parasitic resistance of the input inductor due to the high current level have a significant share of the total losses. As shown in these figures, the converter efficiency is decreased by increasing duty cycles, turns ratio of CL, and parasitic resistance. Moreover, the significant increase of the power losses in high duty cycles leads to a sudden drop in converter efficiency.

V. COMPARING WITH OTHER RELATED BUCK–BOOST CONVERTERS

Table I shows the number of components, voltage conversion ratio, input current ripple, common ground between input and output voltages, and voltage stress on devices of the proposed CIBuBoC in comparison with the recently reported converters in [9]–[10], [11], [20]–[27], and [29].

According to Table I, only converters in [11], [24], [26], [27], and the proposed CIBuBoC have low input current ripple. Also, Fig. 6 shows the voltage gain versus the duty cycle of the converters introduced in the Table I. As shown in the figure, the voltage gain ratio of the CIBuBoC for $n > 1$ is higher than the others significantly. This is due to the dependence of the voltage gain ratio of the proposed converter to the turns ratio of the CL (n) along with the duty cycle. Therefore, by increasing the number of turns ratio, a higher voltage gain can occur in small duty cycles. Although, the converter in [27] also has high voltage gain, more storage components and the lack of common ground between input and output voltage restrict applications of this converter. Also, in [9], [21], and [22], despite the lower number of elements, the converter cannot offer better performance because of its negative polarity of the output voltage, high input current ripple, and lower voltage gain.

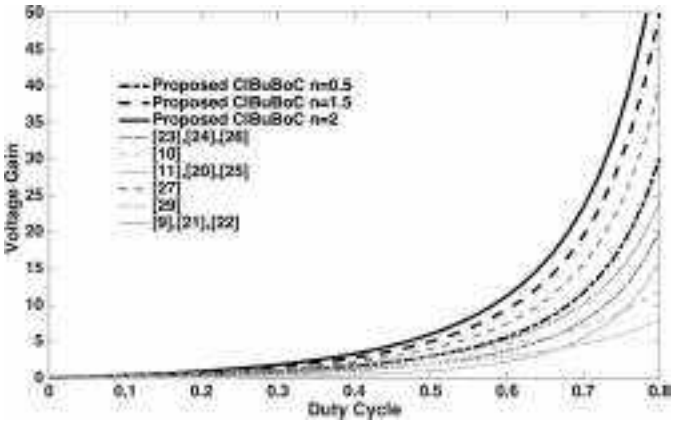

Fig. 6. Voltage gain comparison between the proposed CIBuBoC and other related converters in Table I.

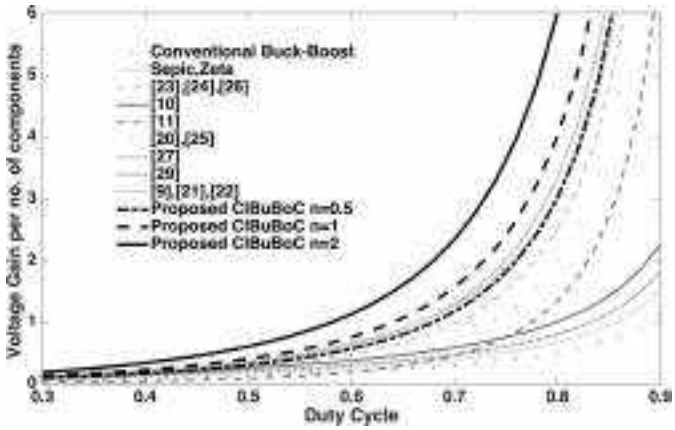

Fig. 8. Voltage gain per the number of components comparison between the proposed CIBuBoC and other related converters in Table I.

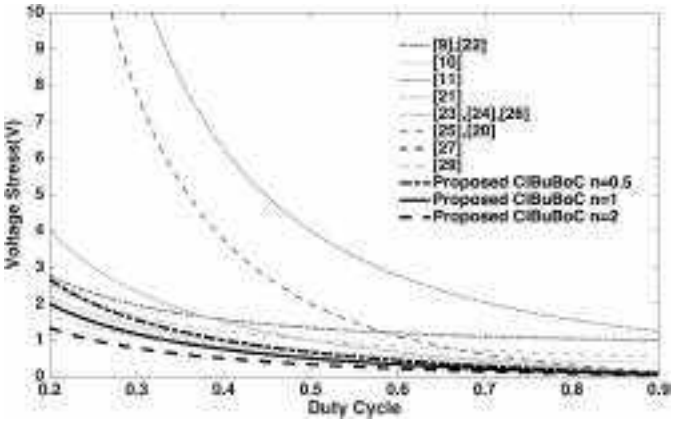

Fig. 7. Switch voltage stress comparison between the proposed CIBuBoC and other related converters in Table I.

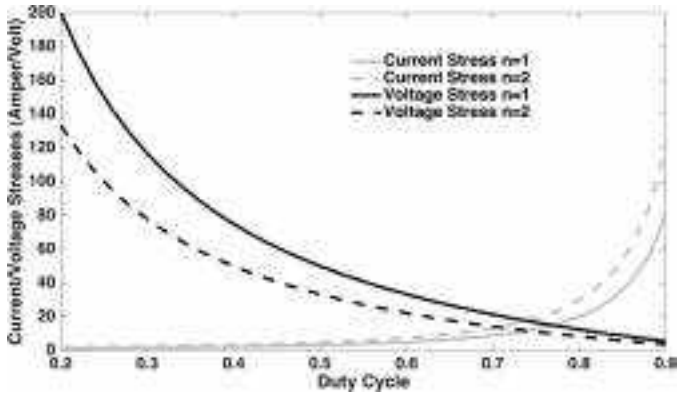

Fig. 9. Power switch voltage and current stress comparison for S_1 of the proposed CIBuBoC under $V_{\rm out} = 100$ Volt and $R_{\rm load} = 250\ \Omega$.

Moreover, Fig. 7 demonstrates the voltage stress across the main power switch versus the duty cycle of the converters introduced in Table I in the same output voltage. It can be seen that the voltage stress in the proposed CIBuBoC is at the lowest level compared to the other converters. On the other hand, by increasing the turns ratio of CL, the voltage stress of the proposed converter components can be reduced more. In addition, the voltage stress across the second power switch S_2 in the CIBuBoC is much lower than the similar double-switch converters in [27] and [26].

One of the main criteria for evaluating power density is the ratio of voltage gain to the number of components of the converter. For this purpose, a comparison curve between voltage gain and the whole number of components as a function of the duty cycle for converters listed in Table I is provided in Fig. 8. As it is shown, by increasing the turns ratio of CL in low value, the CIBuBoC exhibits a higher value of "Voltage gain / No. of component (N)" than the others, which indicates a higher power density. On the other hand, by means of a lower number of components, the proposed converter provides higher voltage gains compared to the high-gain converter [27]. Also, Fig. 9 illustrates the maximum current and voltage rate across the power switch S_1 of the CIBuBoC that has a dominant power loss. According to this figure, the minimum stresses are accrued at the duty cycle range $0.5 < D < 0.8$. Therefore, this reasonable range of duty cycles should be considered in the converter parameter design.

For further illustration of the current and voltage stresses of the semiconductor components of the proposed converter against the other converters, numerical analysis is performed and shown in Table II. The value of parameters are selected as $V_{\rm in} = 20$ V, $V_{\rm out} = 100$ V, $P_{\rm out} = 100$ W, and $n = 0.5$. According to this table, compared to converters [26] and [11] with similarities of the performance indicators, the CIBuBoC has less voltage stress across its power switches. In addition, according to this table, the proposed converter demonstrates enough high efficiency against other buck–boost converters because of its lower number of components and lower voltage stress. These efficiencies are obtained under the same conditions (input 20 V and output 100 V/100 W). Parasitic resistors are selected based on related catalogs from Aluminum Electrolytic for Capacitors (Vishay), Schottky barrier rectifier (RECTORN) for diodes, IRFP4227 (international IOR rectifier) for MOSFETs, and also EE Ferrite core and iron powder toroidal core for CL and inductors, respectively.

TABLE II
COMPARISON BETWEEN THE CURRENT AND VOLTAGE TENSIONS OF THE SWITCHES BETWEEN THE PROPOSED CIBUBOC AND OTHER RELATED CONVERTERS

Ref./ Duty Cycle	[9] D=0. 59	[10] D=0.63	[11] D=0.69	[20] D=0.69	[21] D=0.59	[22] D=0.59	[23] D=0.64	[24] D=0.64	[25] D=0.69	[26] D=0.64	[27] D=0.54	[29] D=0.72	**Proposed CIBuBoC D=0.58**
Current stress	*	*	*	*	*	*	*	*	*	*	*	*	*
S_1	8.4A	8.0A	8.2A	8.6A	5.9A	4.8A	5A	10.6A	8.2A	7.8A	7.27A	7.6A	8.4A
S_2	-	-	-	4.1A	2.4A	-	2.8A	-	2.2A	2.8A	2.17A	-	3.57A
RMS Current	*	*	*	*	*	*	*	*	*	*	*	*	*
S_1	6.4A	6.3A	6.8A	6.55A	4.5A	3.7A	4A	8.5A	6.8A	6.24A	5.37A	6A	6.3A
S_2	-	-	-	2.83A	1.8A	-	2.2A	-	1.8A	2.24A	1.6A	-	2.7A
Voltage Stress	*	*	*	*	*	*	*	*	*	*	*	*	*
S_1	120	53	210	65	49	120	56	56	65	56	42	70	48
S_2	-	-	-	145	120	-	256	-	79.8	100	142	-	66
Efficiency	92.3 %	93.5%	94.1%	94.5%	93.2%	95.1%	94.2%	91.8%	92%	95.2%	94.7%	94.6%	95%

A higher voltage conversion ratio in the proposed converter leads to a reduced turns ratio of the magnetic devices and the duty cycle. This improves the performance indicators of the CIBuBoC, such as power dissipation, voltage stresses, power density, costs and volume, and compact design in magnetic devices against other related step-up/step-down converters in the same conditions. Therefore, this proposed converter can be a proper choice for high step-up/step-down voltage applications such as renewables sources.

VI. SMALL-SIGNAL MODELING OF THE PROPOSED CIBUBOC

Small signal derivation and analysis of low-frequency behavior of the CIBuBoC are provided in this section. For this purpose, the state-space averaging technique is used to model the converter [35], [36]. For achieving the maximum practical situation, the magnetizing and leakage inductances (L_m and L_k) of CL are considered as separate state variables. Also, for the nonconservation of the model, the parasitic resistance r_L is also considered for the input inductor because of the high input current level of high step-up converters. With the above considerations, the state vector of the proposed CIBuBoC is defined as

$$x(t) = \left[i_{L1}\ i_{LM}\ i_{LK}\ v_{C1}\ v_{C01}\ v_{C02} \right]. \tag{42}$$

The state equations are obtained from the proposed converter equivalent circuits for switch-ON and switch-OFF states as given in Fig. 2 as the following.

Switch-ON state ($0 < t < dT_s$):

$$\begin{cases} \dfrac{di_{L1}}{dt} = \dfrac{v_{in}}{L_1} - \dfrac{r_{L1}}{L_1} i_{L1} \\ \dfrac{di_{LM}}{dt} = k \cdot \dfrac{v_{C1}}{L_M} \\ \dfrac{di_{LK}}{dt} = (1-k) \cdot \dfrac{v_{C1}}{L_K} \\ \dfrac{dv_{C1}}{dt} = -\dfrac{i_{LM}}{C_1} \\ \dfrac{dv_{C01}}{dt} = \dfrac{dv_{C02}}{dt} = \dfrac{-(v_{C01}+v_{C02})}{RC_{01}} \end{cases}. \tag{43}$$

Switch-OFF state ($dT_s < t < T_s$):

$$\begin{cases} \dfrac{di_{L1}}{dt} = \dfrac{v_{\text{in}} - v_{C1}}{L_1} - \dfrac{r_{L1}}{L_1} i_{L1} \\ \dfrac{di_{LM}}{dt} = -\dfrac{v_{C02}}{n \cdot L_M} \\ \dfrac{di_{LK}}{dt} = -\dfrac{v_{C01}}{L_K} + \dfrac{v_{C02}}{n \cdot L_K} \\ \dfrac{dv_{C1}}{dt} = \dfrac{i_{L1}}{C_1} \\ \dfrac{dv_{C01}}{dt} = \dfrac{i_{LK}}{C_{01}} \dfrac{-(v_{C01}+v_{C02})}{RC_{01}} \\ \dfrac{dv_{C02}}{dt} = \dfrac{i_{LM} - i_{LK}}{nC_{02}} \dfrac{-(v_{C01}+v_{C02})}{RC_{02}} \end{cases} \tag{44}$$

where *k* is the coupling coefficient of the CL. The state-space form using the weighting factors (*d* and (1-*d*)) of switch-ON/OFF states is expressed as

$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx + Du \end{cases} \tag{45}$$

where *x* is the variable states, *y* is the converter output voltage, and *u* is the input voltage source. Also, *A*, *B*, *C*, and *D* are the state-space matrices obtained from (43) and (44) in the duty-dependent form as

$$A = \begin{bmatrix} \frac{-r_{L1}}{L1} & 0 & 0 & \frac{-(1-d)}{L1} & 0 & 0 \\ 0 & 0 & 0 & \frac{dK}{L_M} & 0 & \frac{-(1-d)K}{L_M} \\ 0 & 0 & 0 & \frac{d(1-K)}{L_K} & \frac{-(1-d)}{L_K} & \frac{(1-d)}{L_K} \\ \frac{(1-d)}{C_1} & \frac{-(1-d)}{C_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{(1-d)}{C_{01}} & 0 & \frac{-1}{RC_{01}} & \frac{-1}{RC_{01}} \\ 0 & \frac{(1-d)}{C_{02}} & \frac{-(1-d)}{C_{02}} & 0 & \frac{-1}{RC_{02}} & \frac{-1}{RC_{02}} \end{bmatrix} \tag{46}$$

$$B^T = \begin{bmatrix} \frac{1}{L1} & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$
$$C = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$
$$D = [0]. \tag{47}$$

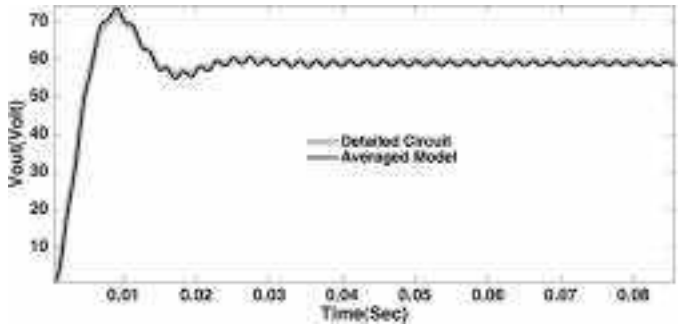

Fig. 10. Averaged large signal response comparison between model and circuit.

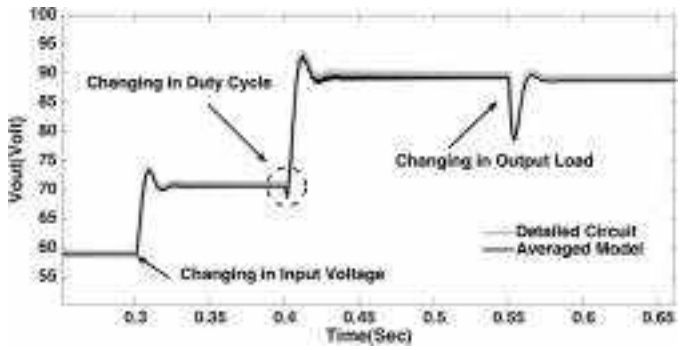

Fig. 11. Small signal response comparison between model and circuit to a step change 20% in input voltage, 8% in the duty cycle, and 20% in the output load.

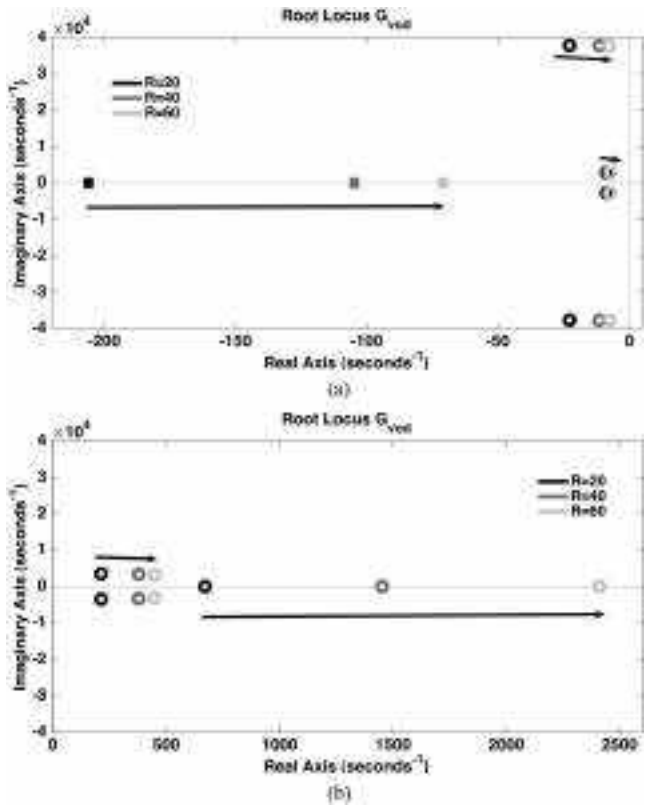

Fig. 12. Root locus graph. (a) Position of left hand of graph under variable output load. (b) Position of right hand of graph under variable output load.

In order to linearize (45) and derive small-signal modeling, small perturbations are superimposed to the duty cycle, input voltage, and the converter variable states as

$$\begin{cases} d = D + \hat{d} \\ v_{\rm in} = V_{\rm in} + \hat{v}_{\rm in} \\ x = X + \hat{x} \end{cases} \tag{48}$$

where lowercase variables ($\hat{}$) represent a small value of parameters and capital variables represent steady-state values that are much bigger than the case variables. Substituting (48) into (45), neglecting steady-state terms, and applying Laplace transformation, the output-to-input voltage ($G_{\rm vov}$) and the output voltage-to-duty ratio ($G_{\rm vod}$) transfer functions are calculated as follows:

$$\begin{cases} G_{{\rm vov}(s)} = \frac{v_o}{v_{\rm in}} = C(SI - A)^{-1}B + D \\ G_{{\rm vod}(s)} = \frac{v_o}{d} = C(SI - A)^{-1}((A_1 - A_2)X \ . \\ \qquad\qquad -(B_1 - B_2)U) \end{cases} \tag{49}$$

The averaged large signal response between the averaged model and the detailed circuit of the proposed CIBuBoC is presented in Fig. 10. Moreover, the ac small-signal response for 20% increment in the input voltage from 10 to 12 V in 0.3 s, 8% increment in the duty cycle from 0.5 to 0.54 in 0.4 s, and 20% decrement in the output load from 25 to 20 Ω are shown in Fig. 11. The values of simulation parameters are selected as $V_{\rm in} = 10$ V, $D = 0.5$, $R = 25\ \Omega$, $n = 2$, $L_1 = 0.5$ mH, $L_K = 1{\rm e}-6$, $L_m = 1{\rm e}-3$, $C_1 = 100\ \mu$F, $C_{01} = C_{02} = 220\ \mu$F, and $r_{L1} = 0.01\,\Omega$. These figures show that good agreement is achieved between the averaged model and the detailed simulation of the converter.

The effect of output load resistance and input voltage on the displacement of zeros and poles of the converter is investigated and shown in Figs. 12 and 13. As it is shown, the CIBuBoC represents a nonminimum phase (NMP) behavior because of the right half-plane (RHP) zeros in their $G_{\rm vod}$ transfer function (also as shown in Fig. 11). This behavior is one of the prominent features of most current-fed high step-up converters that led to an inverse response, narrow bandwidth, low transient response, and destabilization in higher voltage gain. Fig. 12 shows the root locus of the $G_{\rm vod}$ for different output load resistance from 20 to 60 Ω under constant input voltage ($V_{\rm in} = 10$ V). Based on this figure, increasing the output load resistance leads to an extreme displacement in the system RHP zeros and dominant conjugate poles. Therefore, the RHP moves away from the origin, whereas the conjugate poles move toward the real axis. Then, a higher output load leads to a reduced system damping ratio, an improved NMP effect, and a higher overshoot of the output voltage. Moreover, Fig. 13 represents the root locus for several input voltages from 10 to 30 V under constant output load $R = 30\ \Omega$ and output voltage $V_{\rm out} = 80$ V. With the increase in the input voltage, the dominant conjugate poles move toward the real axis slightly.

Also, the RHP zero moves away from the origin significantly. This leads to decrease the system damping ratio, settling time, and decrease the NMP effect. The frequency response of

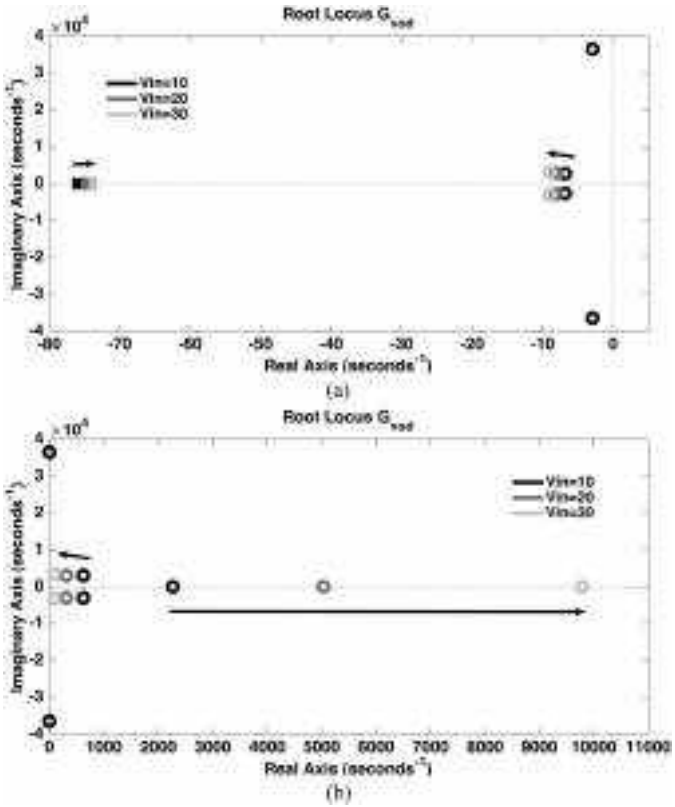

Fig. 13. Root locus graph. (a) Position of left hand of graph under variable input voltage. (b) Position of right hand of graph under variable input voltage.

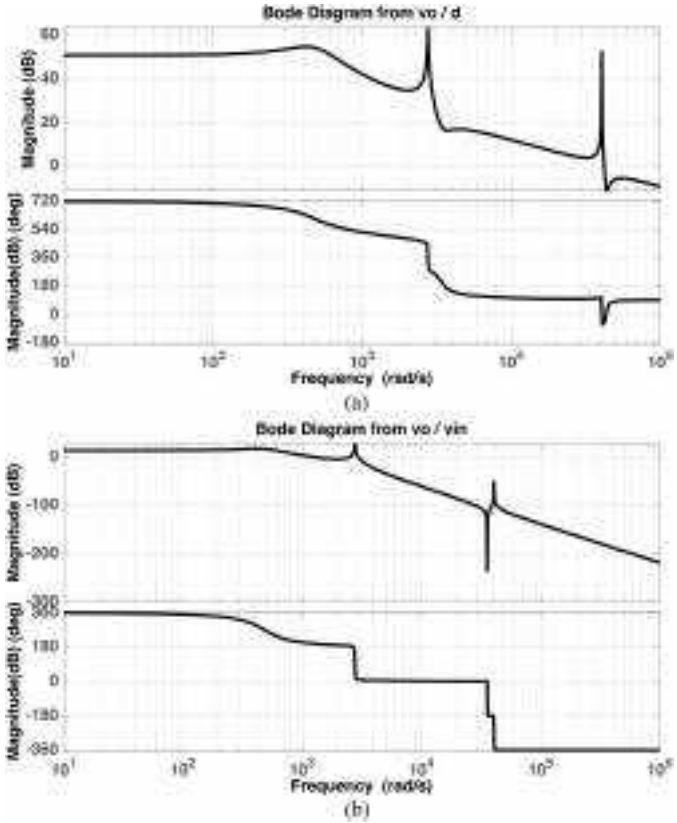

Fig. 14. Bode diagrams of the CIBuBoC. (a) Control-to-output transfer function G_{vod}. (b) Input-to-output transfer function G_{vovi}.

input-to-output G_{vov} and control-to-output G_{vod} transfer functions of the proposed converter are illustrated in Fig. 14.

VII. Key Parameter Design Guidance of the CIBuBoC

The turns ratio of the CL that acts as an inductor is determined by the static gain ratio (5) as

$$n = \frac{M(1-D)^2}{D} + 1. \tag{50}$$

Note that the value of the duty cycles and the number of turns ratio of the CL are very effective in reducing the stress of circuit components. According to Fig. 9, the best selection for the duty cycle to have minimum stress on the MOSFETs is larger than 0.5.

Circuit design in CCM with low input current ripple is desired to apply the proposed CIBuBoC for renewable dc low-voltage sources with proper performance. Normally, the input current ripple is considered 20% of the average input current (allowable current ripple). Then, the minimum value of the input inductor L_1 is designed as follows:

$$L_1 = \frac{V_{\mathrm{in}} \cdot D}{\Delta i_{L1} \cdot f_s} > \frac{V_{\mathrm{in}} \cdot D}{20\% I_{L1} \cdot f_s} \tag{51}$$

where f_s is the switching frequency of the power switches S_1 and S_2.

In order to reduce the volume of the CL located in the middle stage of the converter, the maximum allowable current ripple can be selected larger than 20%. Using (10), (14), and (22), the minimum value of magnetizing inductor L_M is given as

$$L_M = \frac{V_{C1} D}{\Delta I_{LM} f_s} = \frac{V_{C1} D}{50\% i_{LM} f_s} = \frac{RD\,(1-D)}{50\% M\,(1+n)\,f_s}. \tag{52}$$

In the proposed converter, by considering the maximum tolerant voltage ripple as 1% of the steady-state output voltage, appropriate value of the output capacitors C_{01} and C_{02} are written as

$$\begin{aligned} C_{01} &= \frac{P_{\mathrm{out}}}{V_{\mathrm{out}} \cdot \Delta V_{C01}.f_s} > \frac{P_{\mathrm{out}}}{V_{\mathrm{out}} \cdot 1\% V_{C01} \cdot f_s} \\ &> \frac{(1+n)P_{\mathrm{out}}}{V_{\mathrm{out}} \cdot 1\% V_O \cdot f_s} \end{aligned} \tag{53}$$

$$\begin{aligned} C_{02} &= \frac{P_{\mathrm{out}}}{V_{\mathrm{out}} \cdot \Delta V_{C02} \cdot f_s} > \frac{P_{\mathrm{out}}}{V_{\mathrm{out}} \cdot 1\% V_{C01} \cdot f_s} \\ &> \frac{(1+n)P_{\mathrm{out}}}{V_{\mathrm{out}} \cdot 1\% n V_O \cdot f_s}. \end{aligned} \tag{54}$$

By means (10), (14), and (19) and also considering 1% allowable tolerant voltage ripple, the relation for the selection of middle capacitor C_1 is given as follows:

$$C_1 = \frac{I_{L1}(1-D)}{\Delta V_{C1} \cdot f_s} > \frac{M^2(1-D)^2}{1\% R \cdot f_s}. \tag{55}$$

Fig. 15. Experimental setup of the proposed CIBuBoC.

TABLE III
SPECIFICATIONS OF THE IMPLEMENTED PROTOTYPE

Parameter	Values	
	Step-Up	Step-Down
Output Power(P_{out})	100W	35W
Input Voltage(V_{in})	30V	30V
Output Voltage(V_{out})	200V	22V
Load(R_{Load})	400Ω	14Ω
Switching Frequency(f_s)	45 KHZ	
Capacitors C_1, C_{01} , C_{02}	100uF/250V With ESR=0.2Ω	
Power Switches S_1,S_2	IRFB4227PbF With $R_{DS(ON)}$=19.7mΩ, $t_{d(on)}$=33ns, $t_{d(off)}$=21ns	
Input Inductor L_1	0.5mH with r_{L1}=0.1Ω	
CL	EE42/21/20 n_1/n_2=58/29	
Magnetizing Inductor L_M	2mH	
Diode D_1, D_{01} and D_{02}	BYV 28-200 With Maximum V_F=0.89 in 5A	

VIII. EXPERIMENTAL RESULTS OF THE CIBUBOC

To further verify the theoretical and simulation results, a prototype is provided with output power $P_O = 100$ W for step-up and output power $P_O = 35$ W for step-down modes as shown in Fig. 15. The detailed parameters of the implemented prototype are summarized in Table III.

The duty cycle is selected $D = 0.63$ for step-up mode and $D = 0.26$ for step-down modes. The converter diodes D_1, $D_{01,}$ and D_{02} are selected as ultra-fast avalanche sinterglass diode with low forward voltage drop and ultra-fast recovery time. IRFB4227PbF MOSFET with insignificant ON state-resistance $R_{\rm on} = 19.7$ mΩ is selected for power switches S_1 and S_2. In addition, two isolated gate driving signals for low-side and high-side MOSFETs are produced by means of a TL949CN along with TLP250. An iron powder toroidal core T157-52 and a ferrite core EE42/21/20 with 0.2-mm air gap are selected for input inductor and CL. In order to obtain the current waveforms with high accuracy, a high-frequency current probe Pintek PA-667 1 MHZ is used. Experimental results are recorded by an oscilloscope GW INSTEK GDS-1104-B.

The experimental results for components voltage and current of CIBuBoC prototype in CCM of step-up and step-down modes are depicted in Figs. 16–23. Fig. 16 shows the driving

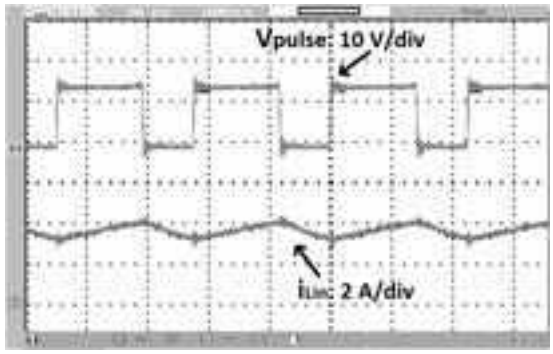

Fig. 16. Measured MOSFETs gate voltage and input inductor current i_{L1} in step-up mode.

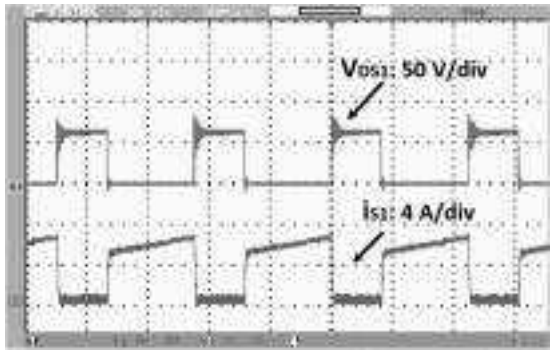

Fig. 17. Experimental waveforms for switch S_1 in step-up mode.

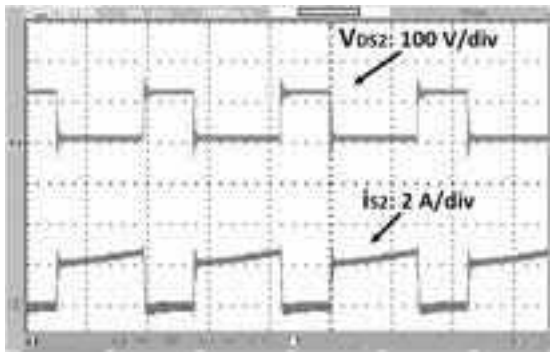

Fig. 18. Experimental waveforms for switch S_2 in step-up mode.

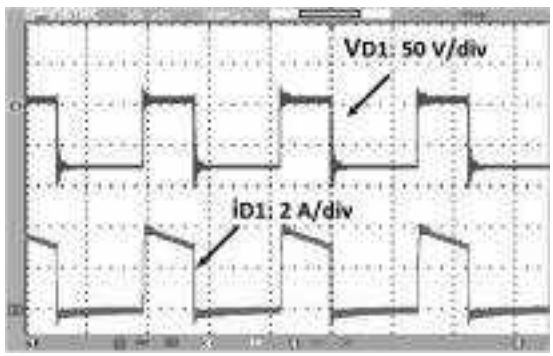

Fig. 19. Experimental waveforms for switch D_1 in step-up mode.

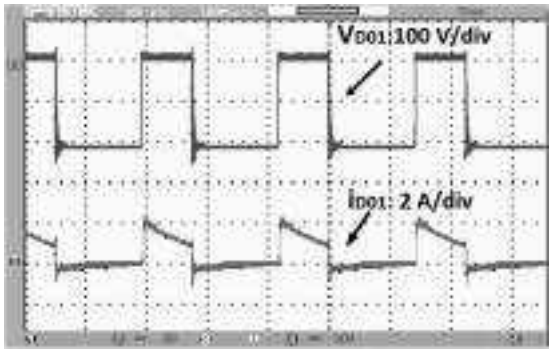

Fig. 20. Experimental waveforms for output diode D_{01} in step-up mode.

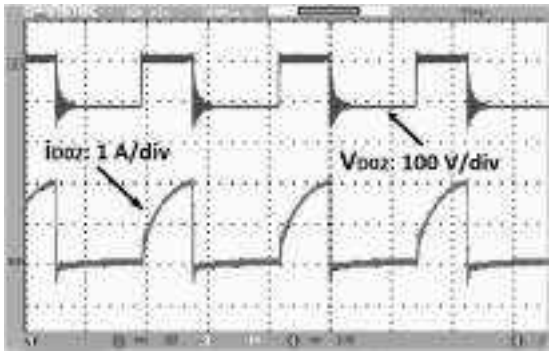

Fig. 21. Experimental waveforms for output diode D_{02} in step-up mode.

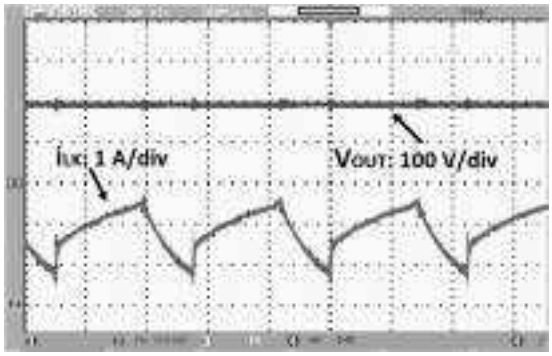

Fig. 22. Experimental voltage for output Voltage and CL primary current (leakage inductor L_k) in step-up mode.

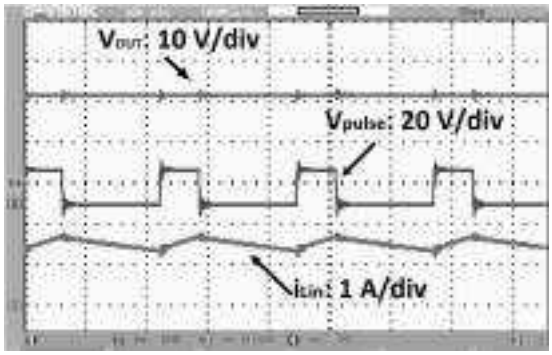

Fig. 23. Experimental results in the step-down mode ($V_{\rm out}$, $V_{\rm pulse,}$ and i_{Lin}).

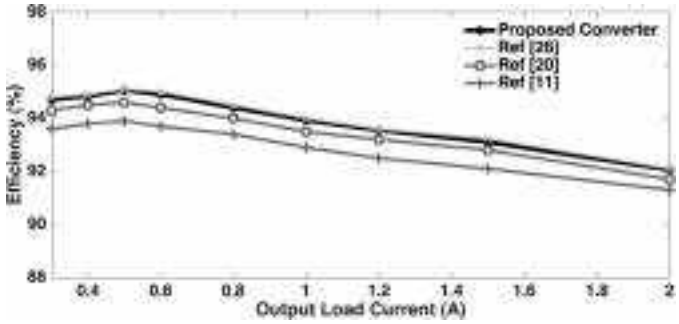

Fig. 24. Experimental comparison of the efficiency of the CIBuBoC against converters in [11], [20], and [26].

signal applied to power switches, along with the input inductor current waveform of the step-up mode in the time domain. By considering circuit design conditions in CCM, the input current is achieved in continuous form with $\Delta i_{Lin} = 0.8$ A ripple, which closely agrees with the theoretical analysis. The measured voltage and current stresses in step-up mode across the power switches S_1 and S_2 are illustrated in Figs. 17 and 18. As it is shown, the maximum voltage stress across S_1 and S_2 is under 77 and 134 V, respectively, which is much lower than the output voltage. The maximum voltage and current stress values of the converter diodes D_1, $D_{01,}$ and D_{02} are depicted in Figs. 19–21. Because of considering the minimum value of the leakage inductance (L_k) of CL, which is caused by a small air gap of 0.2 mm, the current shape of the output diodes and the leakage inductor in the switch-OFF state offer a nonlinear form. However, this current shape can be linearized in a larger air gap (g >1 mm), which, in turn, leads to an increase in the leakage flux and current ripple on magnetizing inductor that is not desirable. The measured output voltage and the leakage inductance current waveforms in the step-up mode in the time domain are displayed in Fig. 22. Moreover, experimental waveforms including the input current and output voltage in step-down mode of the prototype in $V_{\rm out} = 22$ V, $V_{\rm in} = 30$ V, $P_{\rm out} = 35$ W are illustrated in Fig. 23.

Fig. 24 shows comparison of the experimental efficiency results versus several output load currents of the CIBuBoC against the converters [11], [20], and [26] at the same conditions ($V_{\rm in} = 30$, $V_{\rm out} = 120$, $R_{\rm Load} = 60$–$400\ \Omega$, and $f_s = 45$ kHz). From this figure, the CIBuBoC operates with an acceptable efficiency characteristic under different load currents compared to the other converters. It can be seen that the efficiency of the proposed converter is very close to the converter [26] that has eight components. However, the adjustment capability of the step-down or step-up area, higher step-up and step-down voltage conversion ratio, lower voltage stress, and a higher value of "Voltage gain / No. of component (*N*)" are the advantages of the CIBuBoC over the converter [26]. In addition, the experimental efficiency curves of the prototype CIBuBoC at various output voltage from 12 to 250 V in currents 0.5 and 1 A are presented in Fig. 25. The maximum efficiency of the CIBuBoC in $V_o = 180$ V and $V_{\rm in} = 20$ V in 0.5 A can be reached around 95.4%. According

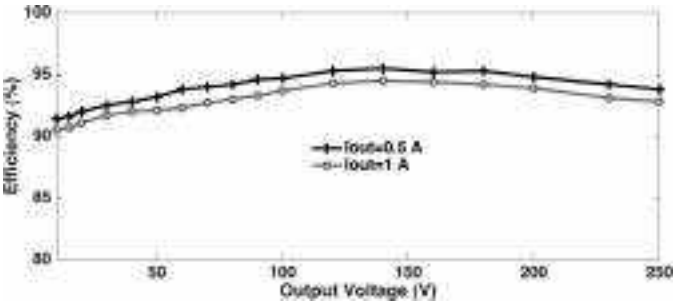

Fig. 25. Efficiencies plot in step-up mode for several output voltages and output current.

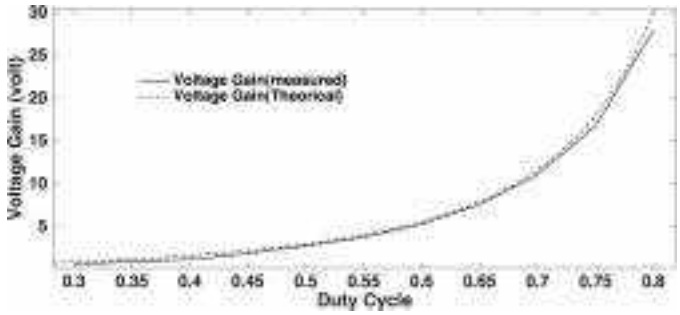

Fig. 27. Verification plot of the measured voltage gain ratio and theoretical relationship.

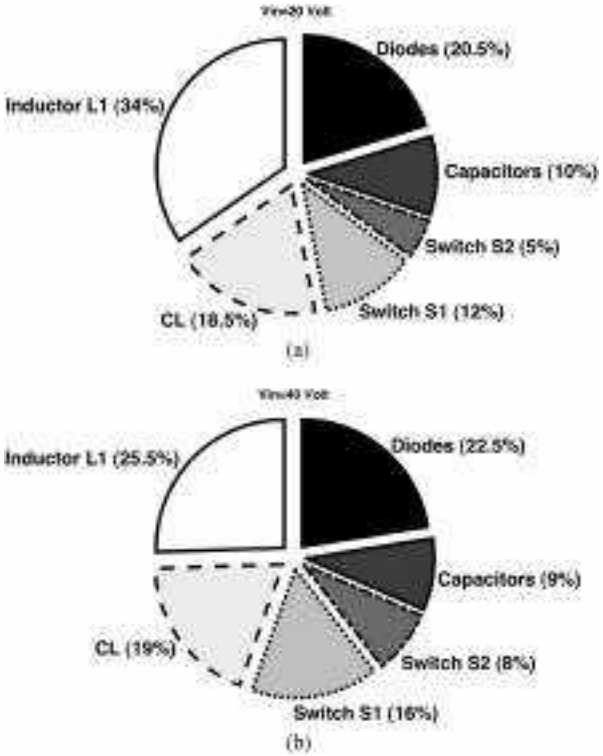

Fig. 26. Break-down of power losses at $V_{\rm O} = 200$ V, $P_{\rm out} = 100$ W. a) Under $V_{\rm in} = 20$ V. b) Under $V_{\rm in} = 40$ V.

to this figure, by increasing the output voltage, the efficiency is slightly decreased.

The breakdown of power losses of the CIBuBoC components with the output voltage 200 V and the input voltages of 20 and 40 V based on the mentioned method in Section IV are calculated and illustrated in Fig. 26(a) and (b). As is evident from these figures, due to the high current rate in the input section of the converter, the input inductor parasitic resistor r_{L1} has dominant dissipation loss than other components. Also, by increasing the input voltage from 20 to 40 V, which leads to decreased voltage gain, the input inductor loss is reduced in comparison to the total losses. It is worth noting that this power loss can be reduced by means of better-graded wires and core material and also decreased the conversion current rate of the converter in higher input voltages. Moreover, to verify the performance of the CIBuBoC in a wide range of the output voltage, the verification plot of the measured and theoretical voltage gain ratio is provided in Fig. 27. The values of converter parameters are selected as $V_{\rm in} = 30$ V, $I_{\rm out} = 1$ A, and $n = 0.5$. According to this figure, the experimental results are closely followed by theoretical results.

IX. Conclusion

This article introduced a new CIBuBoC. The proposed converter can provide a semiquadratic high step-up and step-down voltage gain, low input current ripple, output voltage with positive polarity while low voltage stresses are applied across components. After introducing the converter structure and its steady-state analysis, advantages of the proposed CIBuBoC as the performance indicators have been shown and compared with the other related converters. Moreover, by the help of the state-space averaging technique, small-signal modeling of the proposed converter has been derived and verified, and then, its low-frequency behavior is analyzed. Finally, the feasibility of the proposed converter is verified by experimental results in step-up and step-down modes at 100 and 35 W, respectively.

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