Burak Aslantaş

Question 1- (25 pts) Decrement the bit patterns @ memory address 0x72 (in hex)
Answer:

- "1272" – LOAD the register "2" with the bit pattern found in the memory cell whose address is "72".
- "23FF" – LOAD the register "3" with the bit pattern found in the memory cell whose address is "FF" which represents the number "-1".
- "5423" – ADD the bit patterns in registers "2" and "3" as though they were two's complement representations and leave the result in register "4".
- "3472" – STORE the bit pattern found in register "4" in the memory cell whose address is "72".

Question 2- (25 pts) Add the value @ memory address 0x33 and the value @ memory address 0x22, and store the result @ memory address 0x44
Answer:

- "1233" – LOAD the register "2" with the bit pattern found in the memory cell whose address is "33".
- "1322" – LOAD the register "3" with the bit pattern found in the memory cell whose address is "22".
- "5423" – ADD the bit patterns in registers "2" and "3" as though they were two's complement representations and leave the result in register "4".
- 3444" – STORE the bit pattern found in register "4" in the memory cell whose address is "44".

Question 3- (25pts) Store the inverse of the bit patterns @ memory address 0x36 in Register 5.
Answer:

- "1236" – LOAD the register "2" with the bit pattern found in the memory cell whose address is "36".
- "23FF" – LOAD the register "3" with the bit pattern found in the memory cell whose address is "FF" which represents the number "-1".
- "9523" – EXCLUSIVE OR the bit patterns in registers "2" and "3" and place the result in register "5".

Question 4- (25 pts) Multiply the contents of Register 11 by 2.
Answer:

- "52BB" – ADD the bit patterns in registers "B" and "B" as though they were two's complement representations and leave the result in register "2".
- "402B" – MOVE the bit pattern found in register "2" to register "B".