Student Id: Name: Signature:

CSE 221 - Principles of Logic Design - 2021 Fall
Homework3

You will use a "**key**" to solve the questions in this homework. The key is the number formed by the last two digits of your student id. **If your key is less than 20, add 20 to it!** (*So for example, if your student id was 201007020**47** your key would be "**47**"; if your student id was 201007020**08** your key would be "**28**".*) *We will assume that the key is 47* while explaining the questions (you should replace it with your own key).

So, first write down your id and key: **Student Id: . . . . Key: . . . . . .**

1) Some terms are listed in the table below.

Term #	Term	Term #	Term	Term #	Term	Term #	Term
0 (t_0)	xyz	4	xy	8	x'+y'+z	12	x+y
1	x'yz	5	xz	9	x+y+z'	13	x+z
2	xyz'	6	yz	10	x+y'+z'	14	y+z
3	x'yz'	7	x'y	11	x+y+z	15	x+y'

m = key mod 3 (*m=47 mod 3=2*). Find your m. **m = ... mod 3 = ...**

n = key mod 5 (*n=47 mod 5=2*). Find your n. **n = ... mod 5 = ...**

p = key mod 8 (*p=47 mod 8=7*). Find your p. **p = ... mod 8 = ...**

$F_1 = t_m + t_n + t_p$ (*$F_1 = t_2 + t_2 + t_7 = xyz' + x'y$*)

Find your F_1. $F_1 = t_{...} + t_{...} + t_{...} =$

Using algebraic methods, find the minterms of this function; then list the minterms in minterm shorthand form (∑(…)) and using any method write the function in product of maxterms form (F = (x+y'+z) ∧ (x+y'+z') ∧…).

2) Use m, n and p from question 1.

m = key mod 3 (*m=2*). Write down your m. **m = ...** **x = m+7 = ...** (*x=9*)

n = key mod 5 (*n=2*). Write down your n. **n = ...** **y = n+4 = ...** (*y=6*)

p = key mod 8 (*p=7*). Write down your p. **p = ...** **z = p+5 = ...** (*z=12*)

$F_2(A, B, C, D) = \Sigma(m, n, p, x, y, z)$ (*F= Σ(2, 2, 7,9, 6, 12) = Σ(2, 6, 7, 9, 12)*).

Write down your F. F = Σ(, , , , ,) = Σ( )

Using the map method, simplify F to SOP form	Write F in NAND-NAND form Draw its circuit with NAND gates
Using the map method, simplify F to POS form	**Write F in NOR-NOR form Draw its circuit with NOR gates**

3) Use m from question 1; m = key mod 3 (*m=2*). Write down your m. **m = ...**

Select one of the three functions below (F_m is your function). (*F_2 is my function*)

$F_0 = AB'CD' + A'BCD' + AB'C'D + A'BC'D$

$F_1 = ABC'D + ABCD'$

$F_2 = A'D + B'C'D + BCD + AB'CD' + ABC'D'$

Implement F_m with XOR and AND gates.

4) Write down your function in question 1. (*$F_1 = xyz'+x'y$*)

$F_1 =$

Implement F_1 using a high-active 3x8 Decoder.

Implement F_1 using a low-active 3x8 Decoder.

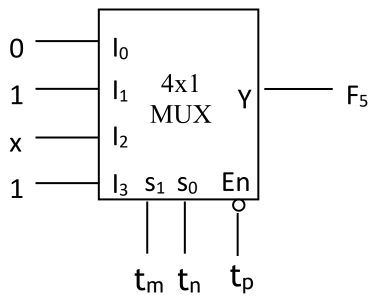
Implement F_1 using an 8x1 Multiplexer.

Implement F_1 using a 4x1 Multiplexer.

5) Write down your terms from question 1: t_m: .... t_n : .... t_p : ....

F_5 is implemented with a 4x1 MUX (with a low-active enable input) as seen on the right.

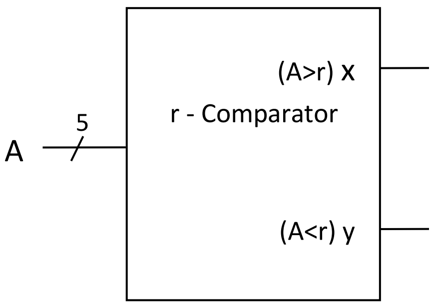
Find F_5.



6) r = 10 + key mod 20 (*r=10+47 mod 20=10+7=17*).
Find your r.   **r = 10 + ... mod 20 = 10 + ... = ...**

Design the circuit on the right. It has a 5-bit input A ($A_4A_3A_2A_1A_0$) and two outputs x and y. If A is larger than your number r, x should ve equal to 1; if it is smaller, y should be 1 and otherwise both outputs should be 0.

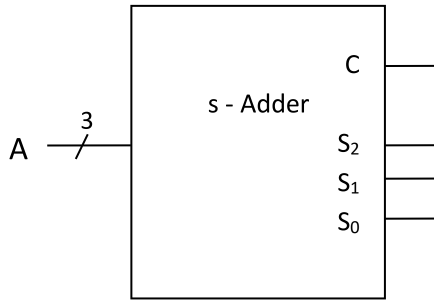
Don’t draw the circuit; writing the equations of x and y is enough.



7) s = 2 + key mod 4 (*s=2+47 mod 4=2+3=5*).
Find your s. **s = 2 + ... mod 4 = 2 + ... = ...**

Design the circuit on the right. It has a 3-bit input A ($A_2A_1A_0$) and four outputs. The circuit should add your number “s” to A.

Use minimum number of half-adders and full-adders (you should find the optimal design; so for example if a half-adder is enough for some part of the circuit you should not put a full-adder instead).



8) t = 3 + 2 * (key mod 3) (*t=3+2*(47 mod 3)=3+2*2=7*).
Find your t. **t = 3 + 2 * (. . . . . mod 3) = 3 + 2* . . . . . = ...**

Design the circuit on the right. It has a 3-bit input A ($A_2A_1A_0$) and *n* outputs(b_0 b_1… b_{n-1}). The circuit should multiply A with your number “t”.

Use **at most two** binary adders (of any size).