Student Id: Name: Signature:

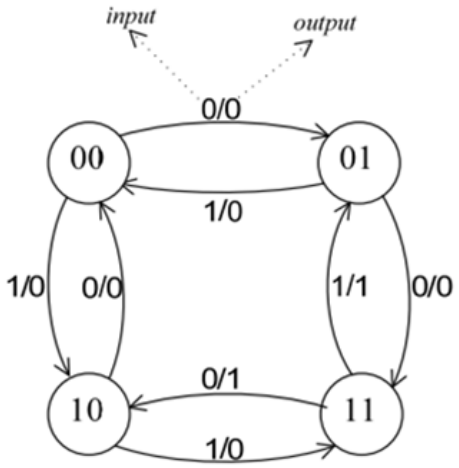
CSE 221 - Principles of Logic Design - 2021 Fall
Homework4

1) **Draw the state diagram** of a sequential circuit which produces 1 at its output when its last three inputs are equal. For example:

	t0	t1	t2	t3	t4	t5	t6	t7	t8	t9
input x:	0	0	0	0	1	1	1	1	0	1
output y:	0	0	1	1	0	0	1	1	0	0

2)

Given the state diagram below, generate the state table and design a sequential circuit using JK flip fops. Draw the circuit.



3) Design a counter which counts down, with the repeated sequence: 2, 1, 0, when the input to the counter circuit is 1. The counter doesn't count (stays at the same state) when the input is 0. Use T flip-flops. Draw the circuit.

4) We want to design a non-resetting sequence detector using a finite state machine with one input x and one output y. The FSM (Finite State Machine – State Diagram) asserts its output y when it recognizes the following input bit sequence: "1011". The machine will keep checking for the proper bit sequence and does not reset to the initial state after it has recognized the string. [Note: As an example the input string X= "..1011011.." will cause the output to go high twice: Y = "..0001001.."]

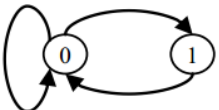
a) Draw the Mealy FSM (state diagram)

b) Draw the Moore FSM (state diagram) (Only draw the state diagrams)

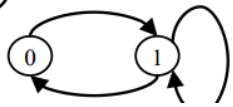
5)

The correct state diagram for the shown circuit is:

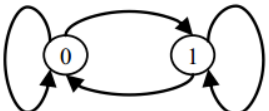
a)



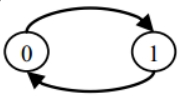
b)

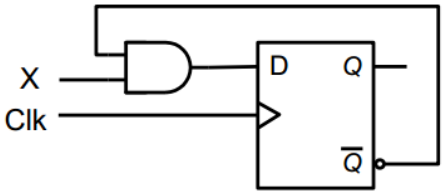


c)



d)

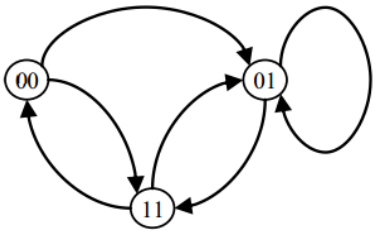




Explain…

6)

Two 'T' Flip-Flops, A and B, are used to implement the shown state diagram. To go from state "AB = 01" to "AB = 11" we need:

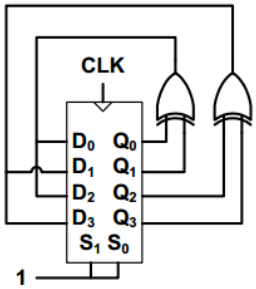


a) $T_A = 0, T_B = 0$
b) $T_A = 0, T_B = 1$
c) $T_A = 1, T_B = 0$
d) $T_A = 1, T_B = 1$
e) $T_A = 1, T_B = x$ (x is don't care)

Explain...

7)

A Universal Shift Register, USR, is connected as shown. S_1=1, S_0 =1 select the load operation. Initially $Q_3Q_2Q_1Q_0 = 1010$. <u>After</u> 2 clocks:



a) $Q_3Q_2Q_1Q_0 = 0000$
b) $Q_3Q_2Q_1Q_0 = 1010$
c) $Q_3Q_2Q_1Q_0 = 0101$
d) $Q_3Q_2Q_1Q_0 = 1001$
e) $Q_3Q_2Q_1Q_0 = 1111$

Explain...

8)

A serial adder is a circuit that has two inputs (X and Y) and one output (S). The inputs represent two binary numbers that have bit values that appear serially beginning with the lowest significant bit first. The output is the serial sum of the two numbers. The diagram below shows the behavior of this circuit for two numbers, X = …01101 and Y = …11100 and the sum is S = …01001. Draw a state diagram for the serial adder.