## **DEUARC Control Functions and Microoperations Table**

Fetch	ТО	IR←IM[PC]
	T1	PC←PC+1
Decode	T2	D0D15← IR[96],
		Q←IR[10]=1, S2←IR[10],
		S1←IR[32], D←IR[54]
<b>D:</b> Destination register selection of decoder <b>S1:</b> Source register selection of Mux A <b>S2:</b> Source register		
selection of Mux B  Arithmetic and Logic Operations		
Anthimetic and Logic Operati	DOT3	D←S1+S2,
ADD	D013	SC←0
INC	D1T3	D←S1+1,
INC	D113	SC←0
DBL	D2T3	D←S1+S1,
552	DZ13	SC←0
DBT	D3T3	D←S1>>,
		SC←0
NOT	D4T3	D←S1'1s (ONES
		COMPLEMENT)
AND	D5T3	DR←S1^S2,
		SC←0
<b>D:</b> Destination register selection of decoder		
If Q=0 S1S2 is 4 bit data memory address, if Q=1 S1S2 is 4 bit data		
Data Transfer		
LD	D6QT3	D←S1S2, SC←0
	D6Q'T3	AR←S1S2
	D6Q'T4	D←DM[AR], SC←0
ST	D7QT3	S2←D, SC←0
	D7Q'T3	AR←S1S2
TCF	D7Q'T4	DM[AR]←D, SC←0
TSF	D9T3	D←S1, SC←0
Program Control	D10T2	CM(CD), DC
CAL	D10T3 D10T4	SM[SP]←PC   PC←IR[40],
	D1014	SP←SP+1,SC←0
RET	D11T3	SP←SP-1
NE.	D11T4	PC←SM[SP],SC←0
JMP	D12Q'T3	PC←IR[40],SC←0
	D12QT3	IF V=1 THEN PC←IR[40],
		SC←0
JMR	D13T3	PC←PC+IR[30]
PSH	D14T3	AR←IR[30]
	D14T4	SM[SP]←DM[AR]
	D14T5	SP←SP+1
POP	D15T3	AR←IR[30]
	D15T4	SP←SP-1
	D15T5	DM[AR]←SM[SP]