EHB 335E - Analog Electronic Circuits Term Project: Designing a Two-Stage Operational Amplifier

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Abstract

This project aims to design a two-stage CMOS operational amplifier that meets certain specifications in terms of voltage gain, bandwidth, phase margin, and load capacitance. The design also competes for the highest figure of merit (FOM), which is a function of gain, bandwidth, settling time, and power consumption. The project involves using SPICE simulations to verify the performance metrics and optimize the FOM under various constraints.

I. Introduction

Operational amplifiers (op-amps) are widely used in analog and mixed-signal circuits for various applications, such as amplification, filtering, buffering, and feedback [1]. A common op-amp topology is the two-stage CMOS op-amp, which consists of a differential input stage and a common-source output stage as it can be observed in the Fig. 1. The two-stage CMOS op-amp offers several advantages, such as high gain, low power, and simple design. However, it also faces some challenges, such as limited bandwidth, stability, and slew rate [2]. Therefore, designing a two-stage CMOS op-amp requires careful trade-offs among different performance metrics and constraints. In this project, we will design a two-stage CMOS op-amp that meets the following specifications dedicated in the Table I.

TABLE I
Design Requirements of the Two-stage CMOS op-amp

Parameter	Value
Voltage Gain	$> 57\,\text{dB}$
Bandwidth (Unity Gain)	$> 220\,\text{MHz}$
Phase Margin	$> 55^\circ$
Load Capacitance	$1.8\,\text{pF}$

In this project it is also competed for the highest figure of merit (FOM), which is defined in the Eq. 1.

$$\text{FOM} = \frac{\text{Gain [dB]} \times \text{Bandwidth [Hz]}}{\text{Settling Time [ns]} \times \text{Power [mW]}} \tag{1}$$

To achieve these goals, we will use SPICE simulations to model the op-amp behavior and optimize the FOM. We will use the 65 nm CMOS technology with a supply voltage of 1.2V and follow the design rules and constraints given in the project description. The project report will present the design methodology, simulation results, and analysis of the op-amp performance and FOM.

II. Circuit Analysis

A. DC Voltage Gain

The circuit depicted in Fig. 1 has two gain stages. The initial stage involves the MOSFET differential pair Q_1 - Q_2 with its current-mirror load. This specific differential pair configuration yields a voltage gain spanning from 10 V/V to 60 V/V. The current mirror is supplied with a reference current denoted as I_{REF}. The gain expression for initial stage is given in the Eq. 2.

$$A_1 = -G_{m1}R_1 = -g_{m1}(r_{o2} \parallel r_{o4}) \tag{2}$$

The second amplification phase comprises the common-source transistor Q_6 along with its current-source load Q_7. This stage generally delivers a gain ranging from 8 V/V to 80 V/V. Moreover, it plays a role in frequency compensation for the operational amplifier. The circuit incorporates a compensation capacitance C_c connected within the negative-feedback route of the second-stage amplifying transistor Q_6, ensuring the necessary dominant pole for optimal performance. The gain of the second amplification stage is given in the Eq. 3.

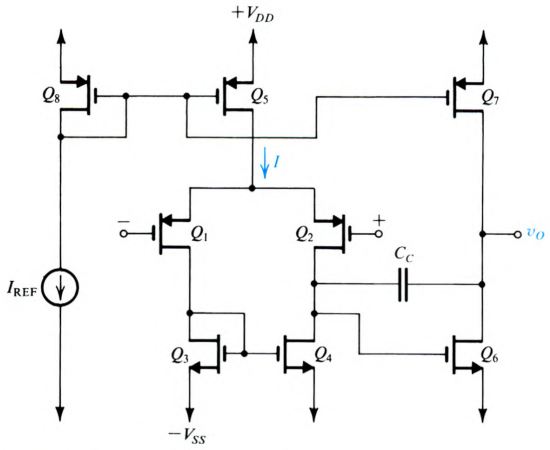


Fig. 1. The two-stage CMOS operational amplifier used in the project.

$$A_2 = -G_{m2}R_2 = -g_{m6}(r_{o6} \parallel r_{o7}) \tag{3}$$

Inevitably, total gain expression of the circuit is shown in the Eq. 4. Gain value of the circuit ranges from 100 V/V to 5000 V/V.

$$A_v = A_1A_2 = G_{m1}R_1G_{m2}R_2 = g_{m1}(r_{o2}||r_{o4})g_{m6}(r_{o6}||r_{o7}) \tag{4}$$

B. Overdrive and Common-Mode Voltage

Overdrive voltage is the difference between the input voltage and the voltage at which the amplifier is biased for optimal performance. It is initiated the design process by choosing overdrive voltages for the transistors. Given that the drain currents of Q_1, Q_2, Q_3 and Q_4 are all equal and half of the drain current of Q_5, it is aimed for lower overdrive voltage values to maximize flexibility in adjusting transistor aspect ratios thus overdrive voltage is chosen as 0.1V. Furthermore, overdrive voltage inversely correlated to the gain of the amplifier thus lower overdrive voltage, results with better gain. It is needed to establish the value of the source of Q_5 to generate inputs resulting in these overdrive voltages. Given V_{DD} = 1.2V, it is determined the source value of Q_5 to be approximately 0.8V, allocating each MOSFET a V_{DS} value of 0.4V. Expression for the overdrive voltage is shown in the Eq. 5.

$$V_{OV} = V_{SG} - |V_{TH}| = V_S - V_G - |V_{TH}| \tag{5}$$

Therefore, expression for the common-mode voltage shown in Eq. 6 can be deduced from the Eq. 5.

$$V_{CM} = V_G = V_S - |V_{TH}| - V_{OV} \tag{6}$$

Since absolute value of the threshold voltage of the MOSFET's is given in the transistor file *"65nm_bulk.txt"* as 0.22V, common mode voltage is calculated as 0.48V from the Eq. 6.

C. Transistor Parameters

After algebraic manipulations, Eq. 2 and Eq. 3 are deduced to Eq. 7 and Eq. 8, respectively. It can thus be concluded that the amplifier gain is not only influenced by the overdrive voltages but is also affected by the early voltages of the transistors.

$$A_1 = -G_{m1}R_1 = -g_{m1}(r_{o2}||r_{o4}) = -\frac{2}{|V_{OV1}|}/\sqrt{\frac{1}{|V_{A2}|} + \frac{1}{V_{A4}}} \tag{7}$$

$$A_2 = -G_{m2}R_2 = -g_{m6}(r_{o6}||r_{o7}) = -\frac{2}{V_{OV6}}/\sqrt{\frac{1}{|V_{A7}|} + \frac{1}{V_{A6}}} \tag{8}$$

Larger channel length values lead to increased early voltages. To enhance the amplifier gain, the utilization of larger channel lengths for transistors can be considered. Given the project description, the utilization of 65nm, 130nm, and 195nm as channel lengths for the MOS devices is stricted. Thus, larger channel length values have been chosen for transistors which is 195nm, which have an impact on gain. The transistor parameters for all transistors can be observed in Table II.

TABLE II
TRANSISTOR PARAMETERS: CHANNEL LENGTH AND WIDTH

$MOSFET$	$L(nm)$	$W(\mu m)$
Q1	130	5
Q2	130	5
Q3	195	1
Q4	195	1
Q5	195	4
Q6	195	1.5
Q7	195	3
Q8	195	0.1

Furthermore, in a properly designed CMOS op-amp circuit, in order to eliminate systematic output dc offset voltage, constraint given in the Eq. 9 should be satisfied. As it can be observed, transistor values chosen, satisfy this condition.

$$\frac{(W/L)_6}{(W/L)_4} = 2\frac{(W/L)_7}{(W/L)_5} \tag{9}$$

In current mirror transistors, the lengths of transistors are maintained equivalently to ensure matching operational conditions and consistent current replication. This practice minimizes the impact of process variations and enhances the accuracy and reliability of current mirroring, aligning with the circuit's intended performance.

D. Compensation Capacitor and Miller Effect

The Miller effect introduces two poles, one at the output of the common-source stage and another at the output of the differential pair, through the compensation capacitance (C_C). Miller effect can be observed in the Eq. 10. The output pole significantly impacts the phase margin, thus to ensure a phase margin of 55 degrees or more, gain of the second stage should be optimized. Therefore, a balance is sought between maintaining an adequate phase margin and achieving the desired bandwidth.

$$C_{\text{out}} = C_{\text{C}} \left(1 - \frac{1}{A_2}\right) \tag{10}$$

According to the resource [3], it has been determined that, to achieve a minimum phase margin of 60 degrees, the compensation capacitance (C_C) should be at least 0.22 times that of the load capacitance (C_L). Since C_L is equal to 1.8 pF, C_C should be at least 0.396 pF. Therefore, it has been chosen as $C_C = 0.5pF$.

E. Additional Resistor to Improve Phase Margin

In the examination of feedback amplifier stability, it has been determined that the closed-loop gain is significantly influenced by the phase margin. The issue of the additional phase lag introduced by the right-half-plane zero can be solved by inclusion of a resistance series with compensation capacitor. Through this modification, the transmission zero can be relocated to more favorable positions. In the project, a resistor added in series with compensation capacitor to improve phase margin and it's value is determined as $R = 20k\,\Omega$.

III. RESULTS

To simulate the circuit depicted in Fig. 1, LTspice is employed [4]. *"65nm Bulk"* model is used for NMOS and PMOS by SPICE Directive command *".inc 65nm_bulk.txt"*. By incorporating an additional resistor and specifying determined parameters, the simulated circuit in LTspice is presented in Fig. 2. DC operational voltage points reveals that all transistors are operating in the saturation mode.

A. AC Simulation

In order to determine voltage gain, unity gain bandwidth and phase margin of the circuit in Fig. 2, AC simulation is conducted. Voltage gain and unity gain bandwidth can be directly observed from the Fig. 3. However in order to calculate phase margin, Eq. 11, should be used.

$$\phi_{PM} = 180^\circ - \phi_{GX} \tag{11}$$

where:

ϕ_{PM} : Phase Margin

ϕ_{GX} : Phase at Gain Crossover Frequency

After calculation, phase margin is calculated as 68 degrees. Thus all constraints for the project is satisfied. Simulation results in comparison with project constraints can be observed in Table III.

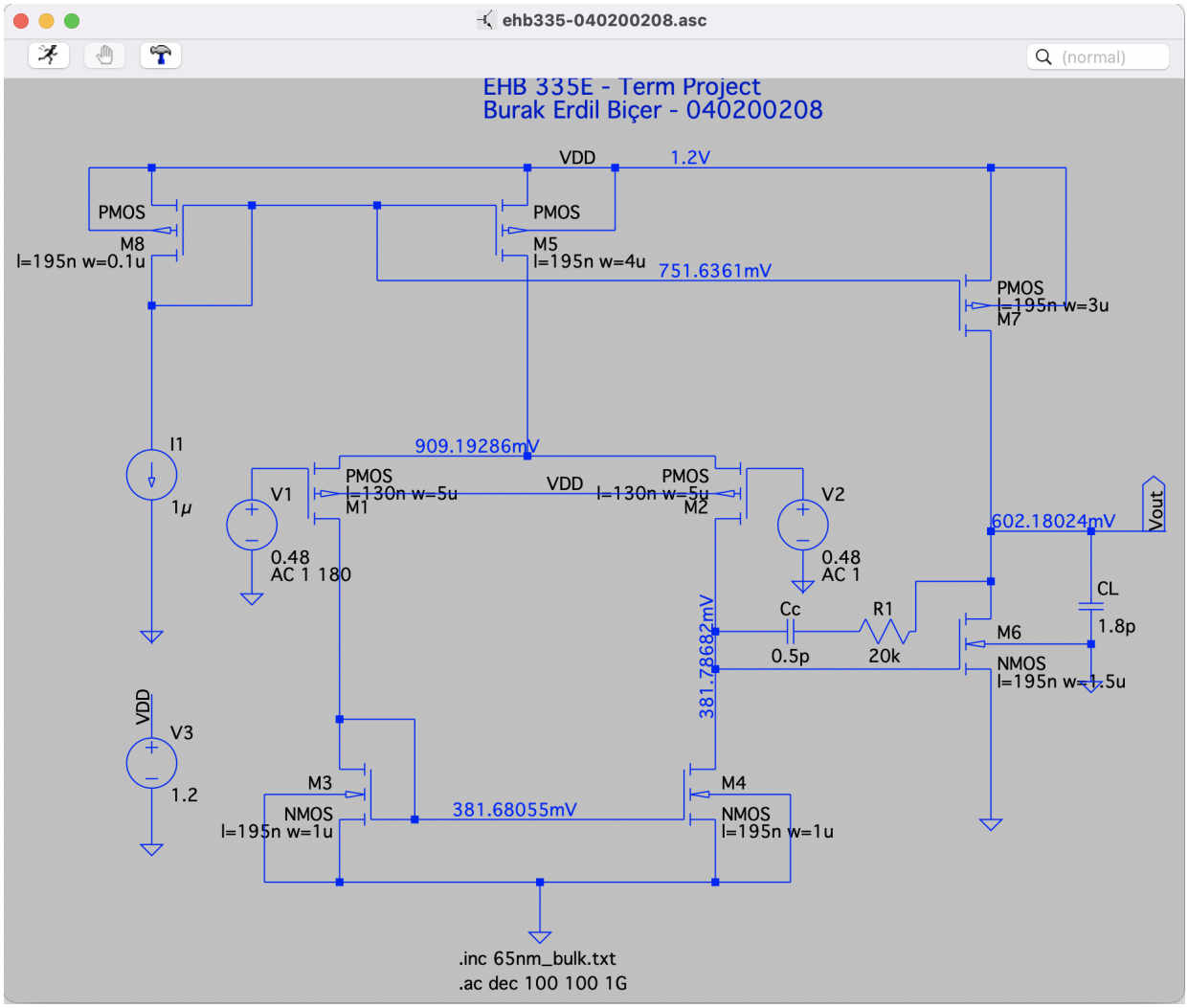


Fig. 2. The two-stage CMOS operational amplifier with an additional resistor and determined parameters in LTSpice.

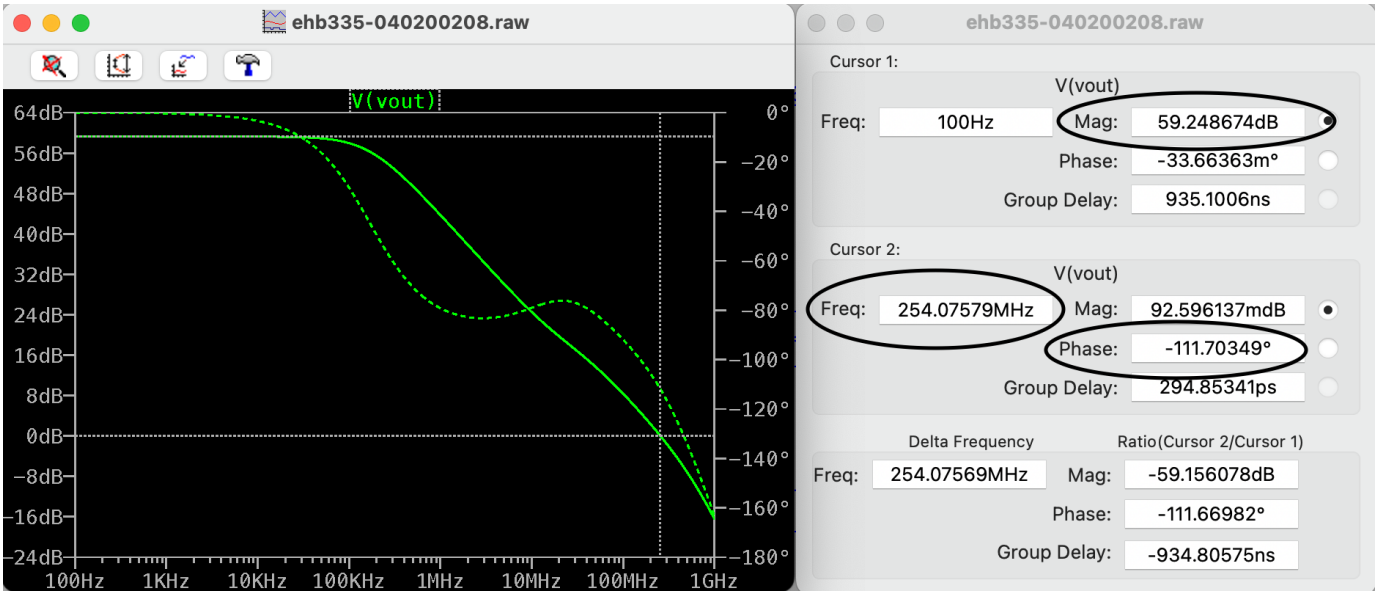


Fig. 3. AC simulation results that shows voltage gain, phase at gain crossover frequency and unity gain bandwidth of the two-stage CMOS op-amp.

TABLE III
AC SIMULATION RESULTS AND COMPARISON WITH PROJECT CONSTRAINTS

Parameter	Constraint	Result
Voltage Gain	$> 57\,\text{dB}$	$59.25\,\text{dB}$
Bandwidth (Unity Gain)	$> 220\,\text{MHz}$	$254\,\text{MHz}$
Phase Margin	$> 55°$	$68°$

B. Transient Simulation

The time it takes for a circuit's output to reach and stay within a specified range around its final value after applying an input signal is referred to as the settling time. The settling time proves to be a critical parameter for a two-stage CMOS op-amp, exhibiting an inverse correlation with the system's performance. To determine the settling time of the circuit, a square wave is applied at the positive input, ranging from 0 to 0.6 V with a period of 40ns and a duty cycle of 50%. The observed rise time is approximately 7ns as it can be observed from Fig. 4 which is the output of the transient simulation.

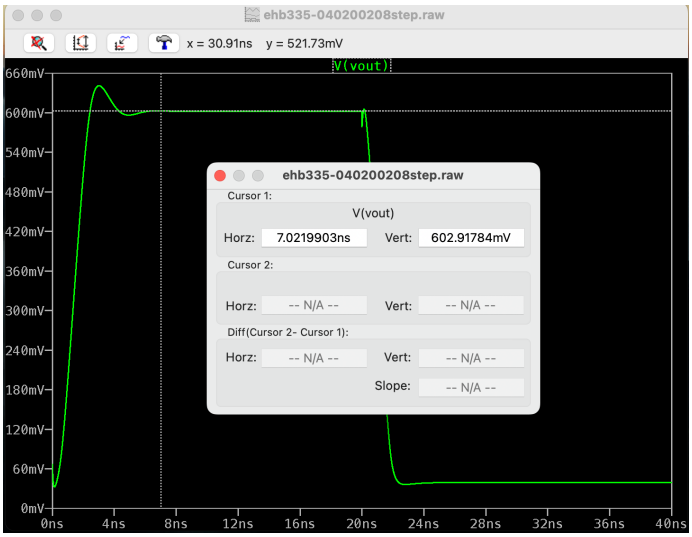


Fig. 4. Output of the transient simulation. Settling time can be observed as approximately 7ns.

C. DC Operating Point Simulation

In order to check whether transistors in saturation or not and check power consumption of the system, DC operating point simulation is crucial. Results for the DC operating point simulation is given in Fig. 5. As it is discussed in Fig. 1, according to the DC operating point simulation all transistors are in saturation mode.

In order to calculate power of the circuit, Eq. 12 can be considered.

$$P = (I_{\text{REF}} + I_{\text{D\_M5}} + I_{\text{D\_M7}}) \times V_{\text{DD}} \tag{12}$$

If values that has obtained from the Fig. 5 is used to calculate power,

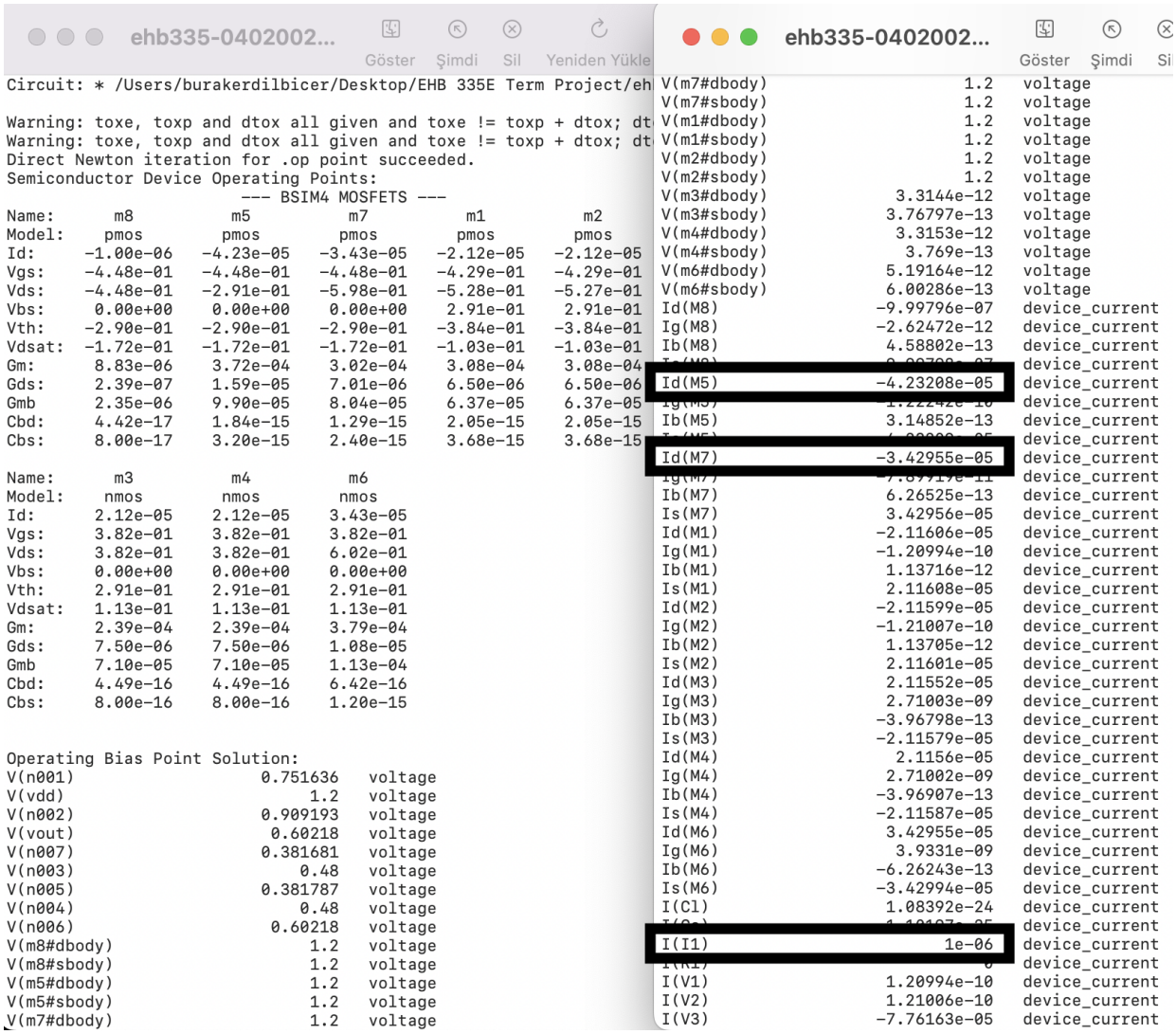
$$P = (1\,\mu\text{A} + 42.32\,\mu\text{A} + 34.29\,\mu\text{A}) \times 1.2\,\text{V} = 93.13\,\mu\text{W} \tag{13}$$

Thus power consumption of the system is calculated as $93.13\mu W$.

D. Figure of Merit (FOM) Calculation

The efficiency or overall performance of a particular system is frequently assessed using the Figure of Merit. In this project, the Figure of Merit is calculated according to the formula presented in Eq. 1. The system's voltage gain and unity gain bandwidth have been determined through AC simulation, as detailed in Table III. The settling time of the system has been obtained through transient simulation, as illustrated in Fig 4, and the power consumption of the system has been calculated through DC operating point simulation, as expressed in Eq. 13. Consequently, if the obtained results are incorporated into Eq. 1,

$$FOM = \frac{(59.25\ dB) \times (254\ \ MHz)}{(7\,ns) \times (93.13\,\mu W)} = 23805 \tag{14}$$



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Circuit: * /Users/burakerdilbicer/Desktop/EHB 335E Term Project/eh

Warning: toxe, toxp and dtox all given and toxe != toxp + dtox; dt
Warning: toxe, toxp and dtox all given and toxe != toxp + dtox; dt
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                        --- BSIM4 MOSFETS ---
Name:       m8          m5          m7          m1          m2
Model:    pmos        pmos        pmos        pmos        pmos
Id:     -1.00e-06   -4.23e-05   -3.43e-05   -2.12e-05   -2.12e-05
Vgs:    -4.48e-01   -4.48e-01   -4.48e-01   -4.29e-01   -4.29e-01
Vds:    -4.48e-01   -2.91e-01   -5.98e-01   -5.28e-01   -5.27e-01
Vbs:     0.00e+00    0.00e+00    0.00e+00    2.91e-01    2.91e-01
Vth:    -2.90e-01   -2.90e-01   -2.90e-01   -3.84e-01   -3.84e-01
Vdsat:  -1.72e-01   -1.72e-01   -1.72e-01   -1.03e-01   -1.03e-01
Gm:      8.83e-06    3.72e-04    3.02e-04    3.08e-04    3.08e-04
Gds:     2.39e-07    1.59e-05    7.01e-06    6.50e-06    6.50e-06
Gmb      2.35e-06    9.90e-05    8.04e-05    6.37e-05    6.37e-05
Cbd:     4.42e-17    1.84e-15    1.29e-15    2.05e-15    2.05e-15
Cbs:     8.00e-17    3.20e-15    2.40e-15    3.68e-15    3.68e-15

Name:       m3          m4          m6
Model:    nmos        nmos        nmos
Id:      2.12e-05    2.12e-05    3.43e-05
Vgs:     3.82e-01    3.82e-01    3.82e-01
Vds:     3.82e-01    3.82e-01    6.02e-01
Vbs:     0.00e+00    0.00e+00    0.00e+00
Vth:     2.91e-01    2.91e-01    2.91e-01
Vdsat:   1.13e-01    1.13e-01    1.13e-01
Gm:      2.39e-04    2.39e-04    3.79e-04
Gds:     7.50e-06    7.50e-06    1.08e-05
Gmb      7.10e-05    7.10e-05    1.13e-04
Cbd:     4.49e-16    4.49e-16    6.42e-16
Cbs:     8.00e-16    8.00e-16    1.20e-15


Operating Bias Point Solution:
V(n001)                   0.751636   voltage
V(vdd)                         1.2   voltage
V(n002)                   0.909193   voltage
V(vout)                    0.60218   voltage
V(n007)                   0.381681   voltage
V(n003)                        0.48   voltage
V(n005)                   0.381787   voltage
V(n004)                        0.48   voltage
V(n006)                    0.60218   voltage
V(m8#dbody)                    1.2   voltage
V(m8#sbody)                    1.2   voltage
V(m5#dbody)                    1.2   voltage
V(m5#sbody)                    1.2   voltage
V(m7#dbody)                    1.2   voltage
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V(m7#dbody)                    1.2   voltage
V(m7#sbody)                    1.2   voltage
V(m1#dbody)                    1.2   voltage
V(m1#sbody)                    1.2   voltage
V(m2#dbody)                    1.2   voltage
V(m2#sbody)                    1.2   voltage
V(m3#dbody)              3.3144e-12  voltage
V(m3#sbody)              3.76797e-13 voltage
V(m4#dbody)              3.3153e-12  voltage
V(m4#sbody)               3.769e-13  voltage
V(m6#dbody)              5.19164e-12 voltage
V(m6#sbody)              6.00286e-13 voltage
Id(M8)                  -9.99796e-07 device_current
Ig(M8)                  -2.62472e-12 device_current
Ib(M8)                   4.58802e-13 device_current
I(M8)                    9.99708e-07 device_current
Id(M5)                  -4.23208e-05 device_current
Ig(M5)                   1.22442e-10 device_current
Ib(M5)                   3.14852e-13 device_current
I(M5)                    4.23208e-05 device_current
Id(M7)                  -3.42955e-05 device_current
Ig(M7)                   7.89919e-11 device_current
Ib(M7)                   6.26525e-13 device_current
Is(M7)                   3.42956e-05 device_current
Id(M1)                  -2.11606e-05 device_current
Ig(M1)                  -1.20994e-10 device_current
Ib(M1)                   1.13716e-12 device_current
Is(M1)                   2.11608e-05 device_current
Id(M2)                  -2.11599e-05 device_current
Ig(M2)                  -1.21007e-10 device_current
Ib(M2)                   1.13705e-12 device_current
Is(M2)                   2.11601e-05 device_current
Id(M3)                   2.11552e-05 device_current
Ig(M3)                   2.71003e-09 device_current
Ib(M3)                  -3.96798e-13 device_current
Is(M3)                  -2.11579e-05 device_current
Id(M4)                    2.1156e-05 device_current
Ig(M4)                   2.71002e-09 device_current
Ib(M4)                  -3.96907e-13 device_current
Is(M4)                  -2.11587e-05 device_current
Id(M6)                   3.42955e-05 device_current
Ig(M6)                    3.9331e-09 device_current
Ib(M6)                  -6.26243e-13 device_current
Is(M6)                  -3.42994e-05 device_current
I(Cl)                    1.08392e-24 device_current
I(C2)                    1.12107e-05 device_current
I(I1)                          1e-06 device_current
I(R1)                              0 device_current
I(V1)                    1.20994e-10 device_current
I(V2)                    1.21006e-10 device_current
I(V3)                   -7.76163e-05 device_current
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Fig. 5. Results of the DC operating point simulation. Important parameters to calculate power is highlighted.

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