Middle East Technical University - Department of Computer Engineering

CENG 232

Logic Design

Spring 2021-2022

Lab Assignment 2

Due date: Friday, April 15, 2022, 23:59

1 Introduction

This laboratory aims to familiarize you with some of the most important IC components like multiplexers and decoders. You will draw the circuit using the Logisim tool with the given gates.

The Logisim submission will be different from the demo circuit you will build in the lab. It will contain an additional output and related IC components to generate that output.

2 IC Pool

- 74LS08 (AND)
- 74LS32 (OR)
- 74LS04 (Inverter)
- 74LS02 (NOR)
- 74LS00 (NAND)
- 74LS153 (Multiplexer)
- 74LS86 (XOR)
- 74LS138 (Decoder)

3 Lab Work

Suppose we would like to implement a hypothetical 7-bit computer's ALU (Arithmetic and Logic Unit) part. The ALU part receives 7-bit long instructions, yields the corresponding operation results. Every 7-bit instruction consists of 3-bit opcode (operation code), 2-bit first operand, 2-bit second operand as shown below.

$$\text{Instruction: } 0010011 \rightarrow 001 - 00 - 11$$

$$\text{opcode: } 001, \text{first operand: } 00, \text{second operand: } 11$$

Since the opcode is 3-bit long, the ALU can only process 8 (7 of them are subject of this assignment) different instructions which are Addition, Subtraction, Left Shift, Greater/Equal Check, XOR, AND, and NOR. The ALU applies the operation determined by opcode onto the first operand and the second operand then reflects the result to its outputs. Note that all logical operations are applied bitwise. The table below depicts the ALU operations for given opcodes.

Instruction Set							
Opcode			First Operand		Second Operand		Output
3^{rd} bit	2^{nd} bit	1^{st} bit	2^{nd} bit	1^{st} bit	2^{nd} bit	1^{st} bit	
O2	O1	O0	A1	A0	B1	B0	
0	0	0	a1	a0	b1	b0	$B + A$
0	0	1	a1	a0	b1	b0	$B - A$
0	1	0	a1	a0	b1	b0	$B << A$
0	1	1	a1	a0	b1	b0	$B >= A$
1	0	0	a1	a0	b1	b0	$B \oplus A$
1	0	1	a1	a0	b1	b0	$B \wedge A$
1	1	0	a1	a0	b1	b0	$\neg(B \vee A)$

$\oplus$: XOR, $\vee$: OR, $\wedge$: AND, $\neg$: NOT, $<<$: Left Shift + : Addition, - : Subtraction, $\geq$: Greater/Equal Check

a1,a0,b1,b0 $\in \{0, 1\}$

Opcode = O2O1O0, First Operand = A = A1A0, Second Operand = B = B1B0

3.1 Inputs and Outputs

The output of the ALU consists of 1 pin indicating the sign of the result and 7 pins each of which represents a numerical value between 0 and 6. Operands of it (A and B) are unsigned 2-bit integers. All operations except Subtraction yield non-negative numerical values. Subtraction operation generates negative results whenever A > B. When the unit issues an operation and yields a result, the output pin that corresponds to a numerical value of the result is active. Furthermore, if the result is a negative number the sign output pin is active (1), otherwise inactive (0). Output pin names and their numerical values are as follows: L6: 6, L5: 5, L4: 4, L3: 3, L2: 2, L1: 1, L0: 0.
Here is an example of states of output pins for Subtraction operation (Opcode = 001).

First Operand		Second Operand		Output							
A1	A0	B1	B0	S	L6	L5	L4	L3	L2	L1	L0
0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	1	0	0	0
0	1	0	0	1	0	0	0	0	0	1	0
0	1	0	1	0	0	0	0	0	0	0	1
0	1	1	0	0	0	0	0	0	0	1	0
0	1	1	1	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	0	1	0	0
1	0	0	1	1	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	0	0	1
1	0	1	1	0	0	0	0	0	0	1	0
1	1	0	0	1	0	0	0	1	0	0	0
1	1	0	1	1	0	0	0	0	1	0	0
1	1	1	0	1	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1

Here is further examples, including the other opcodes.

Opcode			First Operand		Second Operand		Output							
O2	O1	O0	A1	A0	B1	B0	S	L6	L5	L4	L3	L2	L1	L0
0	0	0	1	1	1	0	0	0	1	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	1	0	0	1	0	0	0	0	0	1	0
0	1	0	0	1	0	1	0	0	0	0	0	1	0	0
0	1	0	0	1	1	0	0	0	0	1	0	0	0	0
0	1	0	0	0	1	1	0	0	0	0	1	0	0	0
0	1	1	1	1	0	0	0	0	0	0	0	0	0	1
0	1	1	1	1	1	1	0	0	0	0	0	0	1	0
1	0	0	1	0	1	1	0	0	0	0	0	0	1	0
1	0	0	1	0	0	1	0	0	0	0	1	0	0	0
1	0	1	1	1	1	0	0	0	0	0	0	1	0	0
1	0	1	0	1	1	1	0	0	0	0	0	0	1	0
1	1	0	0	0	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	0	0	1	0	0	0

You are supposed to implement this ALU as your second assignment. You need to use "input pins" for instruction (3-bit opcode, 2-bit first operand, 2-bit second operand) and "output pins" for the output of the unit from Toolbar at the top of Logisim. Set their labels correctly using the following names. **Please, only set the "label" property of the "pin" objects, do not add a "text" object onto the Logisim canvas.**

Note: For the Greater/Equal operation, if the condition is satisfied only the L1 pin is active otherwise only L0 is active.
Note: Instructions whose results could not be represented with the outputs (e.g 1 << 3, B=1, A=3) are not going to be checked/tested.
Note: You are expected to implement your circuitry by using only the ICs specified in the IC pool section.

4 Logisim-Only Part

In your Logisim submission, you are expected to implement all the functionality of the ALU of this hypothetical computer. All 8 outputs must be implemented. **Due to hardware restrictions** Subtraction operation and S output are removed from your lab work (For the Logisim assignment, they should be implemented as described, but in the demo session you are exempt from this operation and the S output).

5 Input-Output Sharing Rule for Free and Demo Sessions

This assignment requires 7 inputs and 8 outputs for the Logisim part. Since there are not sufficiently many inputs and outputs on CADET for each individual person, for free and demo sessions we have had to reduce the number of output pins. Only L3, L2, L1, and L0 outputs will be used and grading will be done accordingly. All input usage is mandatory to test 7 operations so we ask you to share the opcode pins (3 pins, O2, O1, O0) with your partners.

6 Free Session

There will be a *free session week* after your homework is announced (one week later). You will have 2 hours in your free session slot. At the very beginning, a couple of the new ICs (for this assignment) will be introduced and in the remaining time of the free session, you may build your solution circuit on a breadboard by using IC components, and practice how to handle possible problems related to a physical circuit on a breadboard.

7 Demo Session

There will be a 2-hour-long *demo session week* following the free session week. In the demo session:

- You will take a short quiz about the logic concepts that involve the coverage of this lab.
- You will reconstruct your circuit on your breadboard (without the Subtraction operation and S output, only L3, L2, L1, L0 outputs should be implemented).
- You will show that the circuit drawn in Logisim works as specified (without the Subtraction operation and S output, only L3, L2, L1, L0 outputs should be implemented).
- A sample solution will be published before the first demo session.

8 Labelling Specifications

- You have to use **pins** for your inputs and outputs. Only set **label property** of the **pin** objects, do not add a **text object**.
- Your input pins should be labeled as O2, O1, O0, A1, A0, B1, B0.
- Your output pins should be labeled as S, L6, L5, L4, L3, L2, L1, L0.
- Label properties are case-sensitive. Note that all labels consist of an uppercase letter followed by a number. **Please be very careful with the naming of labels.**
- If you need to feed any input with a constant value, you can use a constant gate. This gate is under the CENG232 Gates section. We will only set values for O2, O1, O0, A1, A0, B1, and B0.
- You will receive a grade **penalty** unless labeling is done properly.

9 Deliverables

- Submit the circuit named e1234567.circ prepared in Logisim, which is your preliminary work, until the specified deadline. Do not forget to replace e1234567 with your 7-digit student ID.
- The evaluation of the submission will be a **black-box test**.
- In the demo session, you will reconstruct and show that the circuit drawn in Logisim works. This part will be graded in the lab.
- You should use the CENG version of Logisim which is available on ODTUClass course page. Circuits designed with other Logisim versions, other tools, or that are not named properly **will not be graded**!

10 What to Bring in the Lab

- Print-out of the submitted file of the circuit.
- Data-sheets (www.alldatasheet.com) of chips (you can have them printed or downloaded on your phone/tablet, etc.).
- Pencil, as you will have a quiz at the very beginning of the DEMO lab.

11 Cheating Policy

All the lab work should be individual and there is a zero-tolerance policy for cheating. See the course website for further information about the cheating policy.

12 References

- CENG Logisim Version
- Discussions Page