# CS224 Computer Organization
# Preliminary Report

# Lab 06
# Section 2

# Burak Ozturk
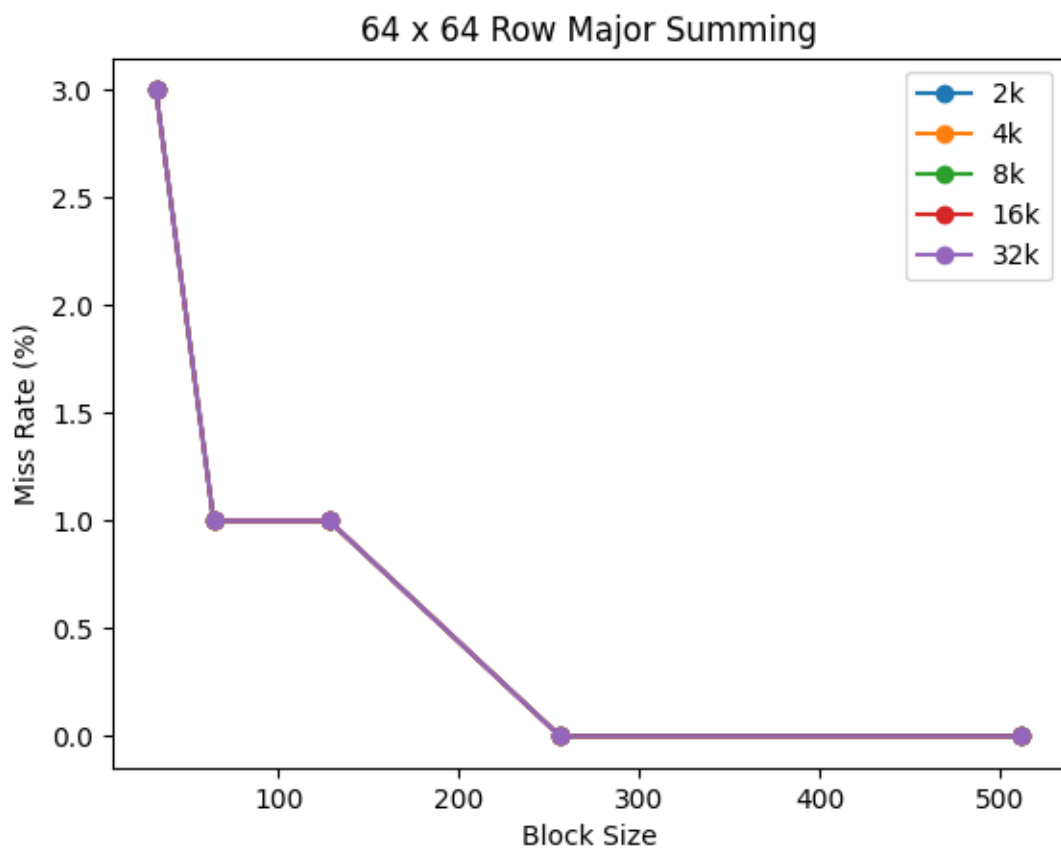# 21901841

# a. Direct Mapped Caches

## Row Major Summing

Matrix Size: 64 x 64

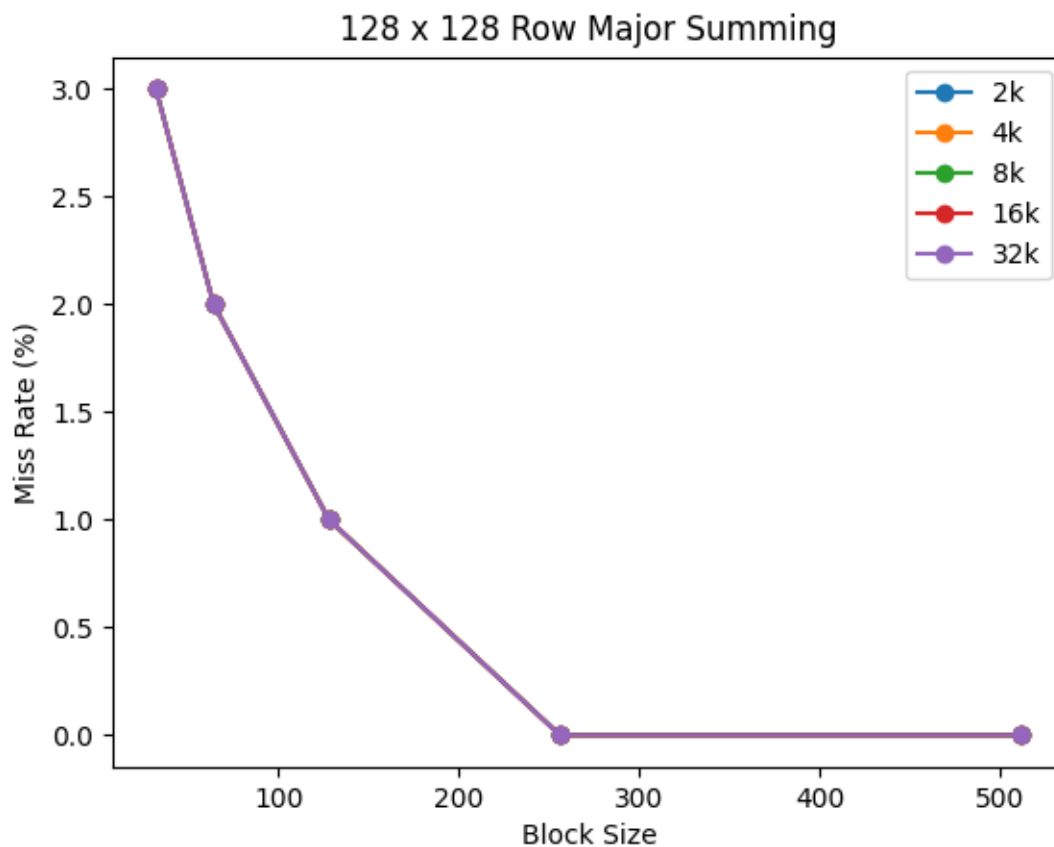| Cache Size (bytes) | Block Size (number of words) | | | | |
| --- | --- | --- | --- | --- | --- |
| | 32 | 64 | 128 | 256 | 512 |
| 2048 | Miss Rate: 3%<br>Miss #: 132 | Miss Rate: 1%<br>Miss #: 66 | Miss Rate: 1%<br>Miss #: 33 | Miss Rate: 0%<br>Miss #: 17 | Miss Rate: 0%<br>Miss #: 9 |
| 4096 | Miss Rate: 3%<br>Miss #: 132 | Miss Rate: 1%<br>Miss #: 66 | Miss Rate: 1%<br>Miss #: 33 | Miss Rate: 0%<br>Miss #: 17 | Miss Rate: 0%<br>Miss #: 9 |
| 8192 | Miss Rate: 3%<br>Miss #: 132 | Miss Rate: 1%<br>Miss #: 66 | Miss Rate: 1%<br>Miss #: 33 | Miss Rate: 0%<br>Miss #: 17 | Miss Rate: 0%<br>Miss #: 9 |
| 16384 | Miss Rate: 3%<br>Miss #: 132 | Miss Rate: 1%<br>Miss #: 66 | Miss Rate: 1%<br>Miss #: 33 | Miss Rate: 0%<br>Miss #: 17 | Miss Rate: 0%<br>Miss #: 9 |
| 32768 | Miss Rate: 3%<br>Miss #: 132 | Miss Rate: 1%<br>Miss #: 66 | Miss Rate: 1%<br>Miss #: 33 | Miss Rate: 0%<br>Miss #: 17 | Miss Rate: 0%<br>Miss #: 9 |

Graph:

Matrix Size: 128 x 128

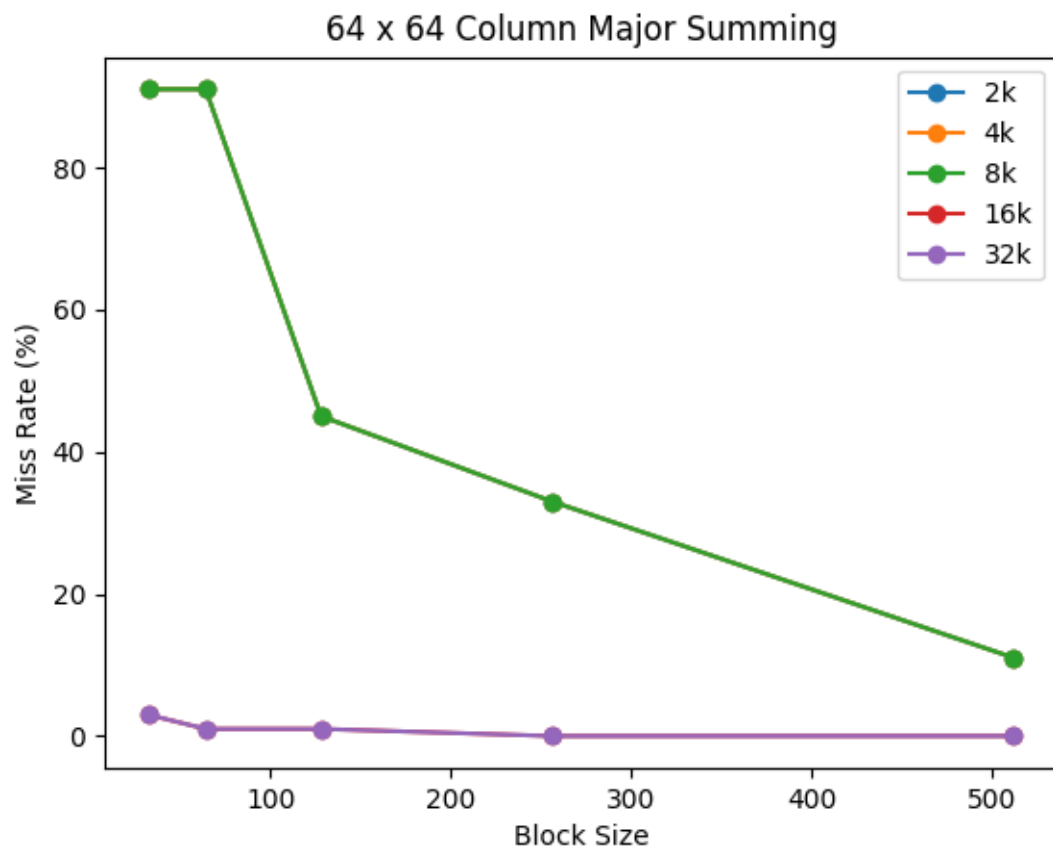| Cache Size (bytes) | Block Size (number of words) | | | | |
|---|---|---|---|---|---|
| | 32 | 64 | 128 | 256 | 512 |
| 2048 | Miss Rate: 3%<br>Miss #: 516 | Miss Rate: 2%<br>Miss #: 258 | Miss Rate: 1%<br>Miss #: 129 | Miss Rate: 0%<br>Miss #: 65 | Miss Rate: 0%<br>Miss #: 33 |
| 4096 | Miss Rate: 3%<br>Miss #: 516 | Miss Rate: 2%<br>Miss #: 258 | Miss Rate: 1%<br>Miss #: 129 | Miss Rate: 0%<br>Miss #: 65 | Miss Rate: 0%<br>Miss #: 33 |
| 8192 | Miss Rate: 3%<br>Miss #: 516 | Miss Rate: 2%<br>Miss #: 258 | Miss Rate: 1%<br>Miss #: 129 | Miss Rate: 0%<br>Miss #: 65 | Miss Rate: 0%<br>Miss #: 33 |
| 16384 | Miss Rate: 3%<br>Miss #: 516 | Miss Rate: 2%<br>Miss #: 258 | Miss Rate: 1%<br>Miss #: 129 | Miss Rate: 0%<br>Miss #: 65 | Miss Rate: 0%<br>Miss #: 33 |
| 32768 | Miss Rate: 3%<br>Miss #: 516 | Miss Rate: 2%<br>Miss #: 258 | Miss Rate: 1%<br>Miss #: 129 | Miss Rate: 0%<br>Miss #: 65 | Miss Rate: 0%<br>Miss #: 33 |

Graph:

# Column Major Summing

Matrix Size: 64 x 64

| Cache Size (bytes) | Block Size (number of words) | | | | |
|---|---|---|---|---|---|
| | 32 | 64 | 128 | 256 | 512 |
| 2048 | **Miss Rate: 91%**<br>**Miss #: 4100** | Miss Rate: 91%<br>Miss #: 4098 | **Miss Rate: 45%**<br>**Miss #: 2049** | Miss Rate: 33%<br>Miss #: 1025 | Miss Rate: 11%<br>Miss #: 513 |
| 4096 | Miss Rate: 91%<br>Miss #: 4100 | Miss Rate: 91%<br>Miss #: 4098 | Miss Rate: 45%<br>Miss #: 2049 | Miss Rate: 33%<br>Miss #: 1025 | Miss Rate: 11%<br>Miss #: 513 |
| 8192 | Miss Rate: 91%<br>Miss #: 4100 | Miss Rate: 91%<br>Miss #: 4098 | Miss Rate: 45%<br>Miss #: 2049 | Miss Rate: 33%<br>Miss #: 1025 | Miss Rate: 11%<br>Miss #: 513 |
| 16384 | Miss Rate: 3%<br>Miss #: 132 | Miss Rate: 1%<br>Miss #: 66 | Miss Rate: 1%<br>Miss #: 33 | Miss Rate: 0%<br>Miss #: 17 | **Miss Rate: 0%**<br>**Miss #: 9** |
| 32768 | Miss Rate: 3%<br>Miss #: 132 | Miss Rate: 1%<br>Miss #: 66 | Miss Rate: 1%<br>Miss #: 33 | Miss Rate: 0%<br>Miss #: 17 | Miss Rate: 0%<br>Miss #: 9 |

Graph:

Matrix Size: 128 x 128

| Cache Size (bytes) | Block Size (number of words) | | | | |
|---|---|---|---|---|---|
| | 32 | 64 | 128 | 256 | 512 |
| 2048 | Miss Rate: 98% Miss #: 16388 | **Miss Rate: 98% Miss #: 16386** | Miss Rate: 98% Miss #: 16385 | **Miss Rate: 49% Miss #: 8193** | **Miss Rate: 24% Miss #: 4097** |
| 4096 | Miss Rate: 98% Miss #: 16388 | Miss Rate: 98% Miss #: 16386 | Miss Rate: 98% Miss #: 16385 | Miss Rate: 49% Miss #: 8193 | Miss Rate: 24% Miss #: 4097 |
| 8192 | Miss Rate: 98% Miss #: 16388 | Miss Rate: 98% Miss #: 16386 | Miss Rate: 98% Miss #: 16385 | Miss Rate: 49% Miss #: 8193 | Miss Rate: 24% Miss #: 4097 |
| 16384 | Miss Rate: 98% Miss #: 16388 | Miss Rate: 98% Miss #: 16386 | Miss Rate: 98% Miss #: 16385 | Miss Rate: 49% Miss #: 8193 | Miss Rate: 24% Miss #: 4097 |
| 32768 | Miss Rate: 98% Miss #: 16388 | Miss Rate: 98% Miss #: 16386 | Miss Rate: 98% Miss #: 16385 | Miss Rate: 49% Miss #: 8193 | Miss Rate: 24% Miss #: 4097 |

Graph:
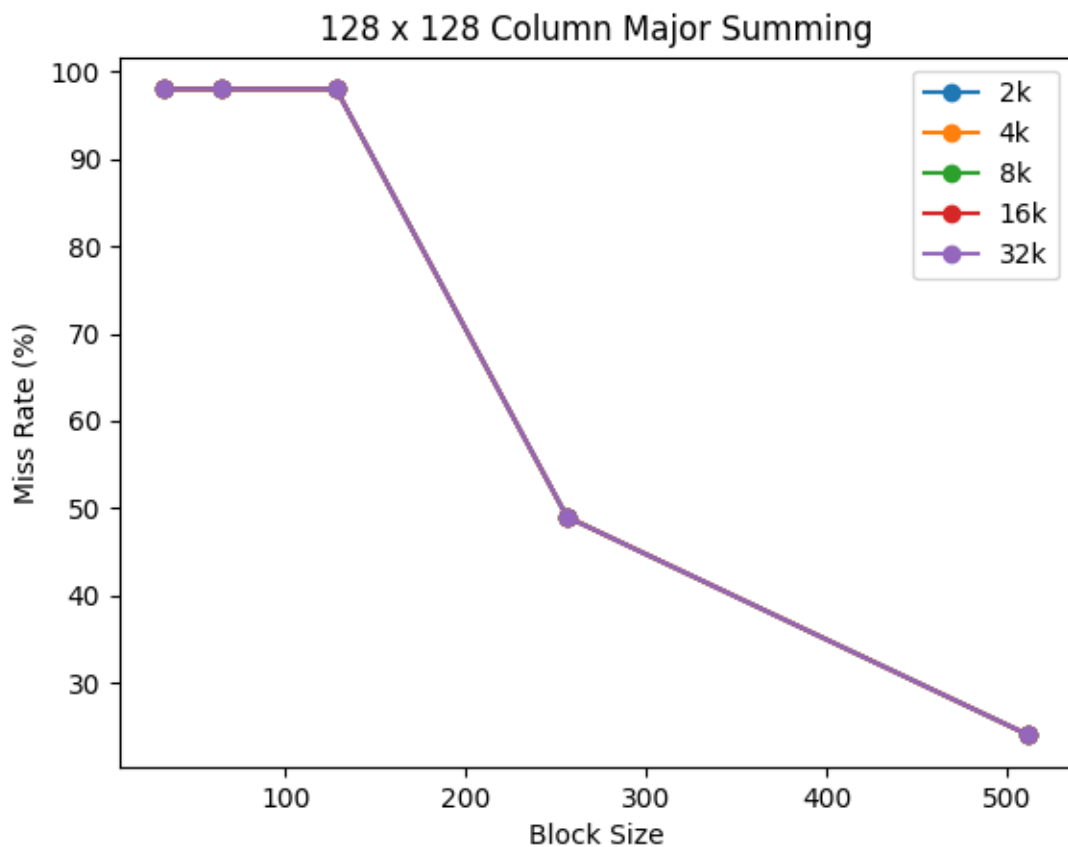
## b. Fully Associative Caches
Column Major Summing

Matrix Size: 64 x 64

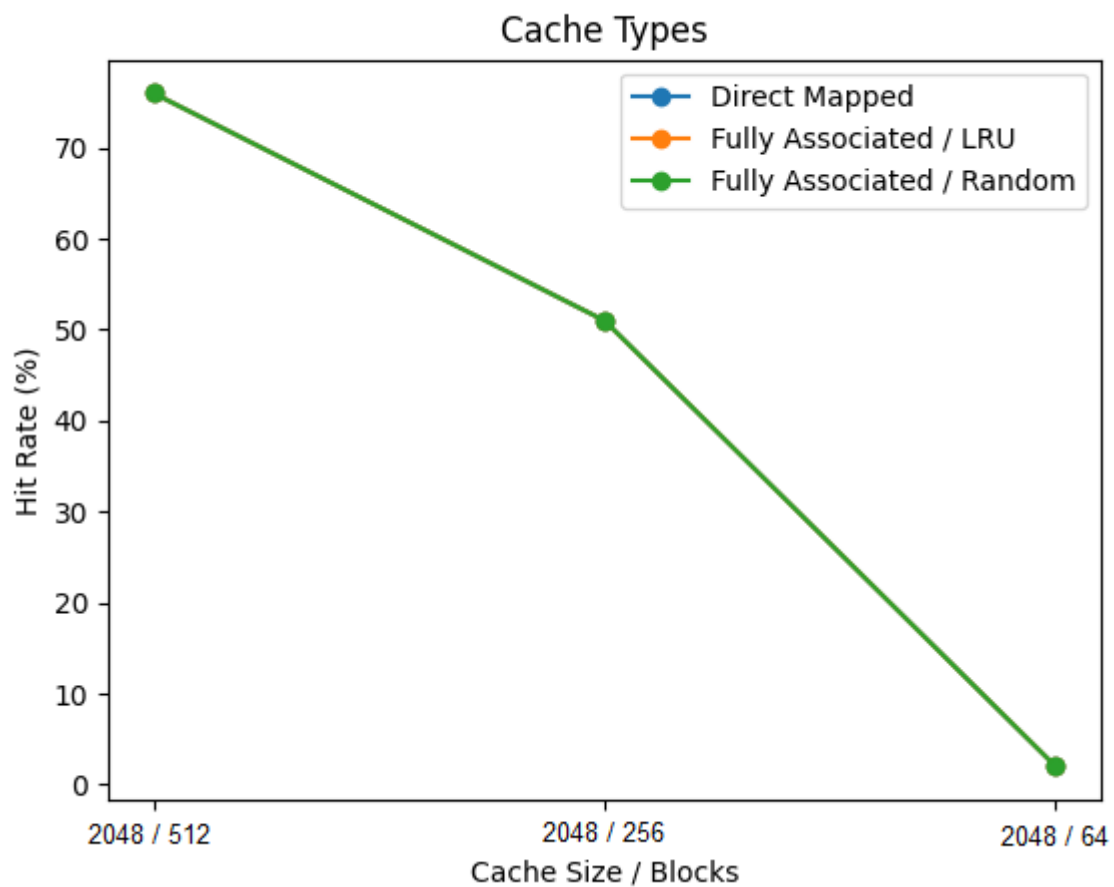| Cache Size/Block Size | Cache Type | | |
|---|---|---|---|
| | Direct Mapped | Fully Associative / LRU | Fully Associative / Random |
| 16384 / 512 (Good) | ~100% | ~100% | ~100% |
| 2048 / 128 (Medium) | 55% | 55% | 55% |
| 2048 / 32 (Poor) | 9% | 9% | 11% |

Graph:
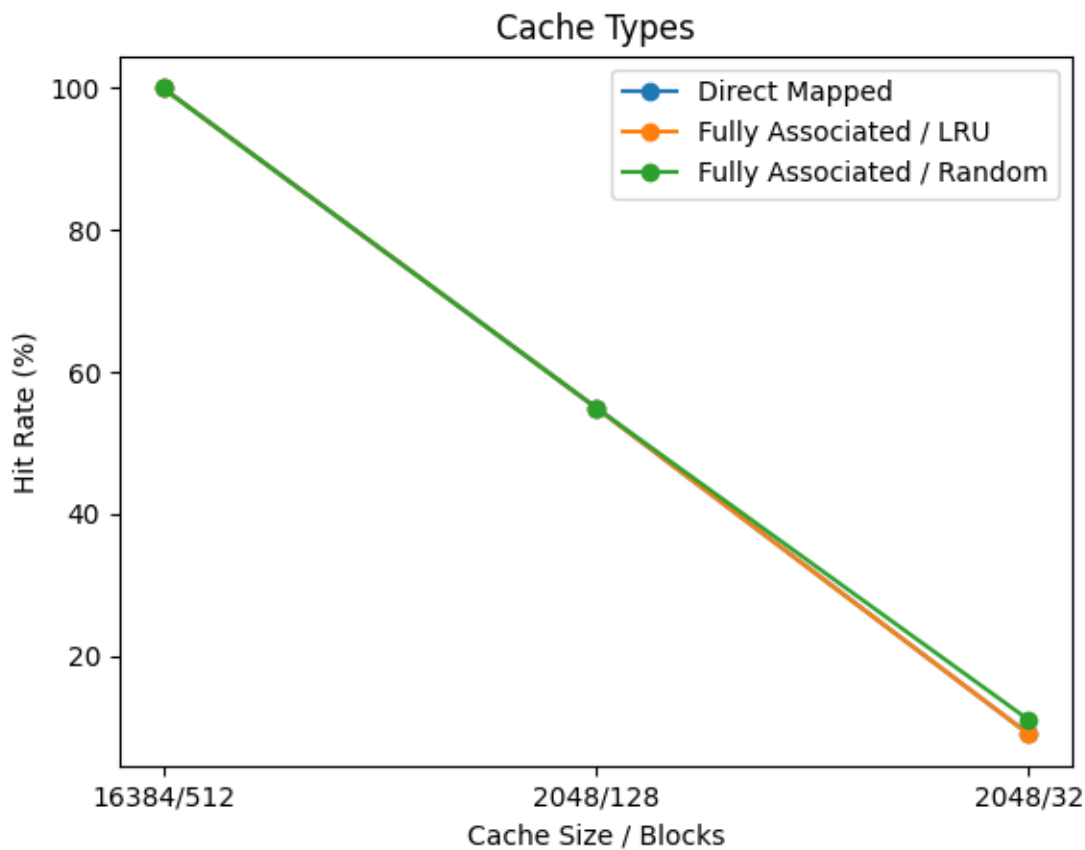


As seen in the graph, results are exactly same for all three caches (Fully associative / Random is a little better due to randomness.). Change from direct mapped to fully associative cache does not make a difference because while doing column by column reading neighboring integers are placed in cache too and cache is large enough to get same miss rate for every cache. That means for "good" cache, there is enough cache size in direct mapped therefore fully associative is not needed and for "medium" and "poor" caches, most of the misses are not conflict misses but capacity miss therefore fully associativity does not help.

Matrix Size: 128 x 128

| Cache Size/Block Size | Cache Type | | |
| --- | --- | --- | --- |
| | Direct Mapped | Fully Associative / LRU | Fully Associative / Random |
| 2048 / 512 (Good) | 76% | 76% | 76% |
| 2048 / 256 (Medium) | 51% | 51% | 51% |
| 2048 / 64 (Poor) | 2% | 2% | 2% |

Graph:



Same with 64 x 64 Fully Associative but randomness doesn't help that much this time.

## c. N-way Set Associative Caches

Column Major Summing

Matrix Size: 64 x 64

| Cache Size/Block Size: 2048 / 128 (Medium) | | | |
|---|---|---|---|
| N-way Cache | 1 | 2 | 4 |
| Hit Rate | 2 | 2 | 2 |
| Miss Rate | 98 | 98 | 98 |
| Miss Count | 16385 | 16385 | 16385 |

| Cache Size/Block Size: 16384 / 512 (Good) | | | |
|---|---|---|---|
| N-way Cache | 1 | 2 | 4 | 8 |
| Hit Rate | ~100% | ~100% | ~100% | ~100% |
| Miss Rate | ~0% | ~0% | ~0% | ~0% |
| Miss Count | 9 | 9 | 9 | 9 |

| Cache Size/Block Size: 2048 / 32 (Poor) | | | |
|---|---|---|---|
| N-way Cache | 1 | 2 | 4 | 8 |
| Hit Rate | 9 | 9 | 9 | 9 |
| Miss Rate | 91 | 91 | 91 | 91 |
| Miss Count | 4100 | 4100 | 4100 | 4100 |

For all three cases, miss rate does not change as the N increases or decreases because as in Part B, misses are not conflict misses but capacity misses. Therefore making cache more divided by increasing N, does not do any good other than wasting resources.

Column Major Summing

Matrix Size: 128 x 128

| Cache Size/Block Size: 2048 / 256 (Medium) | | |
|---|---|---|
| N-way Cache | 1 | 2 |
| Hit Rate | 51 | 51 |
| Miss Rate | 49 | 49 |
| Miss Count | 8193 | 8193 |

| Cache Size/Block Size: 2048 / 512 (Good) |
|---|
| N-way Cache | 1 |
| Hit Rate | 76% |
| Miss Rate | 24% |
| Miss Count | 4097 |

| Cache Size/Block Size: 2048 / 64 (Poor) | | | |
|---|---|---|---|
| N-way Cache | 1 | 2 | 4 | 8 |
| Hit Rate | 2 | 2 | 2 | 2 |
| Miss Rate | 98 | 98 | 98 | 98 |
| Miss Count | 16386 | 16386 | 16386 | 16386 |