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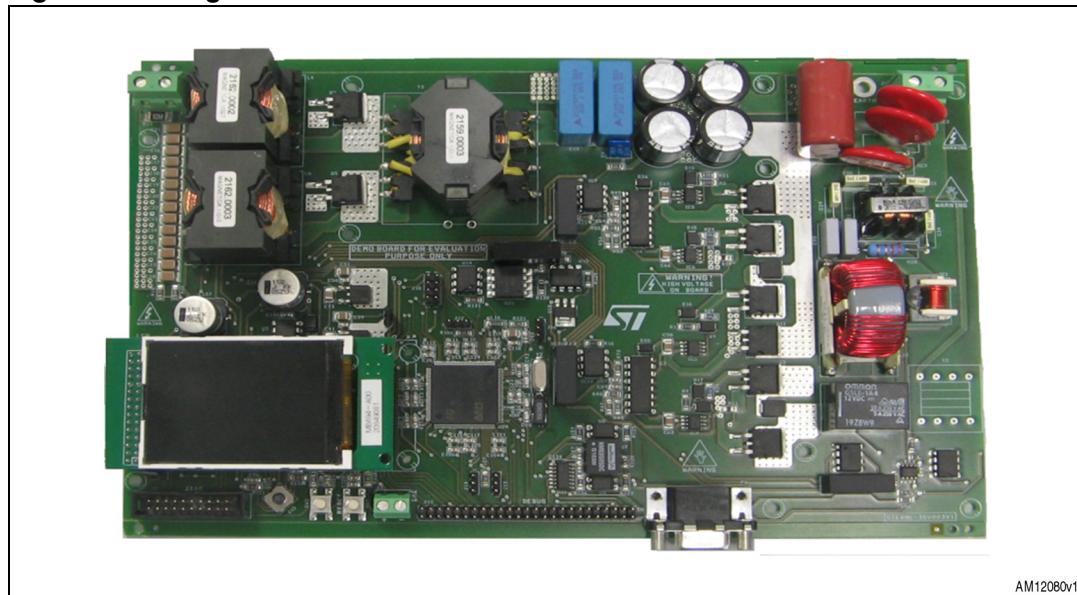
## Introduction

This application note describes the implementation of a 250 W grid connected DC-AC system suitable for operation with standard photovoltaic (PV) modules. The design is associated to the STEVAL-ISV003V1 demonstration board which demonstrates the possibility of implementing a full microinverter solution (MIC) using STMicroelectronics products.

In fact, both the components used to implement the power, control and communication section belong to the product portfolio offered by STMicroelectronics.

The design is based on two power stages, namely, an interleaved isolated boost DC-DC converter and a mixed frequency DC-AC converter. The control section is based on an STM32F103xx microcontroller which ensures proper maximum power point tracking (MPPT) on the input side of the system and decoupled control of the active and reactive power on the output. The control algorithm has been developed to allow system operation both with 230 V AC, 50 Hz grids and with 240 V AC, 60 Hz without any hardware modifications. The connection to a 120 V AC, 50/60 Hz grid requires few hardware modifications to ensure the best system performance. An image of the STEVAL-ISV003V1 demonstration board is shown in *Figure 1*.

**Figure 1.** Image of the 250 W MIC



## Contents

1	<b>System description</b> .....	5
2	<b>DC-DC converter design</b> .....	7
3	<b>Schematic description</b> .....	20
4	<b>STM32F103xx based current control for inverter grid connection</b> ...	29
5	<b>Experimental test results</b> .....	35
	<b>Appendix A Magnetic components datasheets</b> .....	42
	<b>Appendix B Alternative DC-DC converter magnetic components with low profile</b> .....	49
6	<b>Conclusions</b> .....	51
	<b>Revision history</b> .....	52

## List of tables

Table 1.	Summary of main electrical specifications . . . . .	6
Table 2.	DC-DC converter main specifications . . . . .	10
Table 3.	DC-DC converter MOSFET main characteristics . . . . .	13
Table 4.	DC-DC converter rectifier diodes main characteristics. . . . .	13
Table 5.	HF transformer specifications . . . . .	14
Table 6.	RM14 core with N87 Ferrite main characteristics . . . . .	15
Table 7.	STB11N65M5 MOSFET main electrical characteristics . . . . .	19
Table 8.	Document revision history . . . . .	52

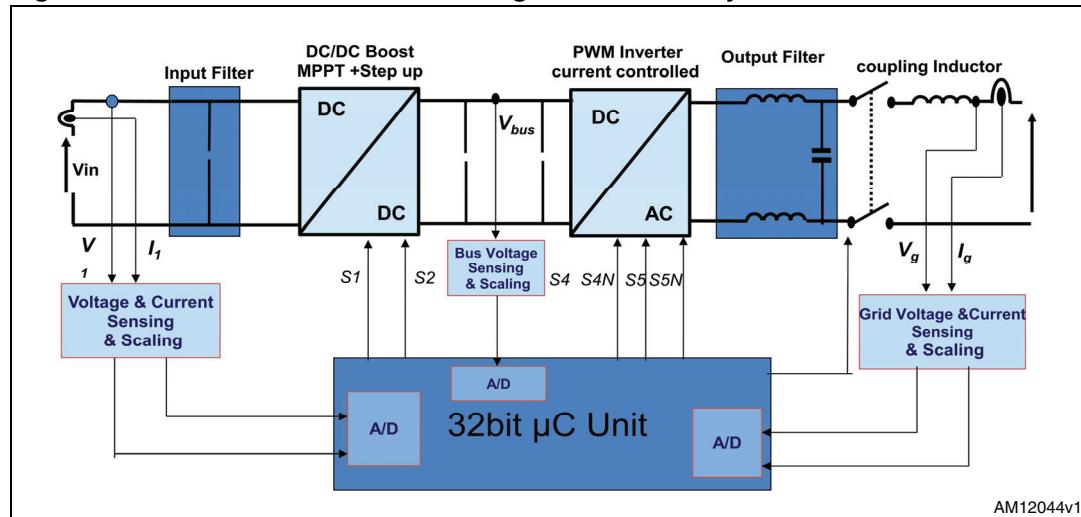
## List of figures

Figure 1.	Image of the 250 W MIC . . . . .	1
Figure 2.	Block scheme of the 250 W grid connected system . . . . .	5
Figure 3.	DC-DC converter topology . . . . .	7
Figure 4.	Gate driving signals of the DC-DC converter . . . . .	8
Figure 5.	Currents through the input inductors . . . . .	8
Figure 6.	MOSFET MOS1 and MOS2 currents . . . . .	9
Figure 7.	Rectifier diode currents . . . . .	9
Figure 8.	HF transformer current . . . . .	10
Figure 9.	Basic scheme of the DC-AC converter . . . . .	17
Figure 10.	Schematic of the two main power stages . . . . .	22
Figure 11.	Schematic of the filtering and relay circuit . . . . .	23
Figure 12.	DC-DC converter driver . . . . .	24
Figure 13.	DC-AC converter driver . . . . .	25
Figure 14.	Auxiliary power supply of the demonstration board . . . . .	26
Figure 15.	AC line current sensing . . . . .	26
Figure 16.	AC line voltage sensing . . . . .	27
Figure 17.	PV current sensing . . . . .	28
Figure 18.	PV voltage sensing . . . . .	28
Figure 19.	Block diagram of the implemented control . . . . .	29
Figure 20.	Implemented PLL structure . . . . .	30
Figure 21.	Block diagram of the control algorithm implemented on the 250 W MIC STM32F103xx . . . . .	32
Figure 22.	DC-DC converter MOSFET current (green) and drain to source voltage (purple) @250 W35 . . . . .	35
Figure 23.	DC-DC converter input current ripple cancellation and inductor currents . . . . .	36
Figure 24.	DC-DC converter HF transformer waveforms . . . . .	36
Figure 25.	DC-DC converter rectifier diode waveforms . . . . .	37
Figure 26.	Inverter modulating signals . . . . .	37
Figure 27.	DC-AC converter output voltage and current waveforms . . . . .	38
Figure 28.	DC-DC converter efficiency . . . . .	39
Figure 29.	Microinverter efficiency . . . . .	39
Figure 30.	MIC output current and voltage waveforms during grid connection . . . . .	40
Figure 31.	Output current THD% . . . . .	40
Figure 32.	Power factor . . . . .	41
Figure 33.	DC-DC boost converter inductors (part1) . . . . .	42
Figure 34.	DC-DC boost converter inductors (part2) . . . . .	43
Figure 35.	AC voltage TV . . . . .	44
Figure 36.	DC-DC converter HF transformer (part 1) . . . . .	45
Figure 37.	DC-DC converter HF transformer (part 2) . . . . .	46
Figure 38.	Inverter filter inductor (part 1) . . . . .	47
Figure 39.	Inverter filter inductor (part 2) . . . . .	48
Figure 40.	DC/DC inductor for 250 W microinverter . . . . .	49
Figure 41.	DC-DC transformer for 250 W microinverter . . . . .	50

# 1 System description

The block diagram reported in [Figure 2](#) shows the main concepts behind the proposed microinverter solution.

**Figure 2.** Block scheme of the 250 W grid connected system



AM12044v1

Although the characteristics of an MIC may change according to the modules' electrical specifications, its structure can be composed by up to three stages to perform the MPPT function and deliver power to the grid. The very first MICs used three stages to perform such a conversion but, nowadays, the trend is to reduce the stages to two or even one. The reduction of the number of stages dramatically increases efficiency, up to 96%. On the other hand, the single-stage conversion scheme is not capable of controlling reactive power, performing power factor correction according to specific needs that may be dictated by the utility. These considerations, together with the possibility of reducing the size of electrolytic capacitors, thanks to the use of a high voltage DC link, have mainly driven the design of the 250 W MIC, which then belongs to the two-stage category. The DC-DC stage is used to boost the output voltage of the PV module up to about 400 V DC and is also responsible for implementing the maximum power point tracking (MPPT). High efficiency and high input to output voltage step ratio are the most important requirements for this stage. High voltage gain can be obtained through capacitor multiplier systems or high-frequency transformers but, since galvanic isolation is required for MIC applications, the HF transformer is always necessary. The transformer turns ratio depends on the input and output voltage, but also on the topology choice which can be either a voltage source one or a current source one. However, special care must be taken when designing and manufacturing the HF transformer to keep the leakage flux as low as possible. The leakage flux mainly depends on the winding construction which, in turn, is affected by the transformer turns ratio. The lower the turns ratio is, the simpler it is to realize a transformer with low leakage flux. This consideration has led to the use of a capacitor voltage doubler on the output stage of the DC-DC converter.

The DC-AC converter is a full bridge characterized by a high frequency leg switching with sinusoidal PWM and low frequency leg switching at grid frequency. The adoption of this modulating strategy allows optimization of the efficiency of the MIC in the low load part of the operating profile since a sensible reduction in switching losses is achieved. The selection of the power devices is also crucial for the correct operation of the topology in terms of efficiency.

The system is powered up by an auxiliary power supply which generates a +15 V and a +5 V bus from the input voltage using an L4951 integrated circuit and few external components. The startup voltage of the auxiliary power supply is 18 V while the maximum voltage is 55 V. The STM32F103xx supply voltage is scaled down from the +5 V bus using a low drop linear regulator. Five feedback signals are used by the microcontroller in order to fully control the system. In particular, a voltage transformer and a Hall effect sensor are used to sense grid voltage and current, respectively. Two resistive voltage dividers are used to sense the DC-DC converter input and output voltage. Since the microcontroller is supplied from the input side of the system, the high voltage bus feedback signal is opto-isolated to ensure galvanic isolation between the input and the output of the system. Finally, the input current generated by the PV module is sensed using a simple current shunt resistor. These five feedback signals are sampled at 17.4 kHz using the STM32F103xx 12-bit A-D converters.

The control strategy is based on a standard perturb and observe (P&O) MPPT algorithm to adapt the input system impedance to the PV module electrical characteristics, while it uses DQ axes control to ensure that MIC generated current and voltage are able to cope with grid characteristics. The main system specifications are summarized in [Table 1](#).

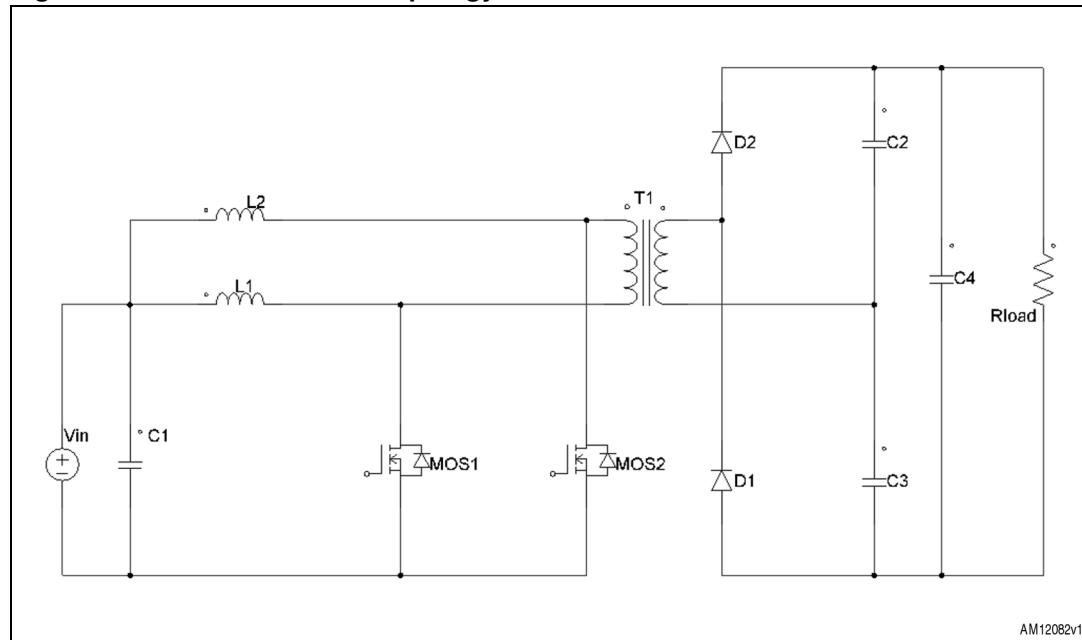
**Table 1. Summary of main electrical specifications**

Parameter	Value
Vin (nominal input voltage)	35.8 V
Vin_max (maximum input voltage)	55 V
Vin_min (minimum input voltage)	18 V
MPPT range	20 V to 40 V
Iin (nominal input current)	7.6 A
Imax (max. input current)	11 A
DC-DC output voltage nominal	380 V
DC-DC max. output voltage	450 V
Vout AC	230 V, 50 Hz - 240 V, 60 Hz
Iout (nominal)	1.1 A (230 V AC) / 1.06A (240 V AC)
Power factor	0.98 @ full load
Nominal output power	250 W
DC-DC switching frequency	35 kHz
DC-AC switching frequency	17.4 kHz

## 2 DC-DC converter design

The topology chosen for the DC-DC section of the MIC is an isolated, interleaved boost converter. The basic electrical scheme of such a converter is shown in [Figure 3](#).

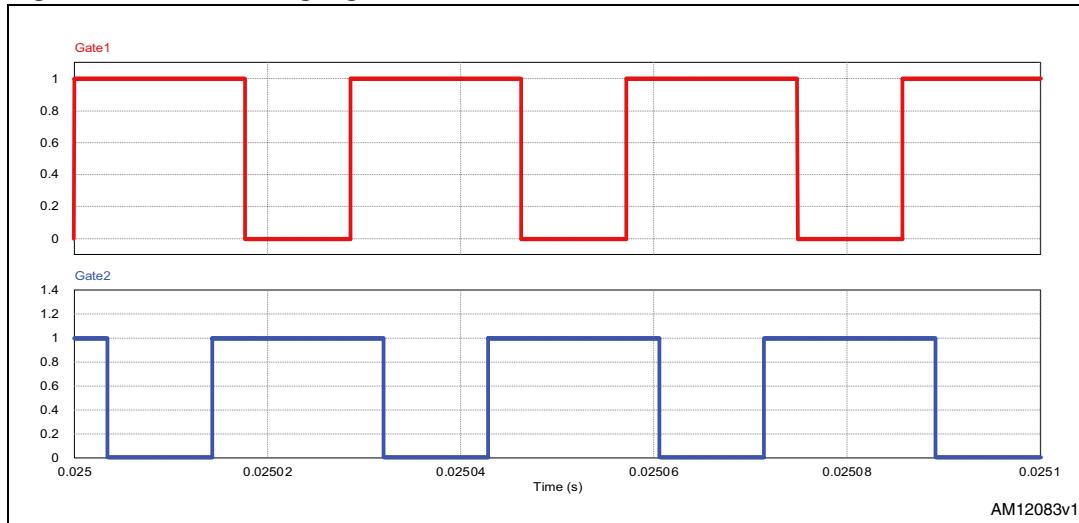
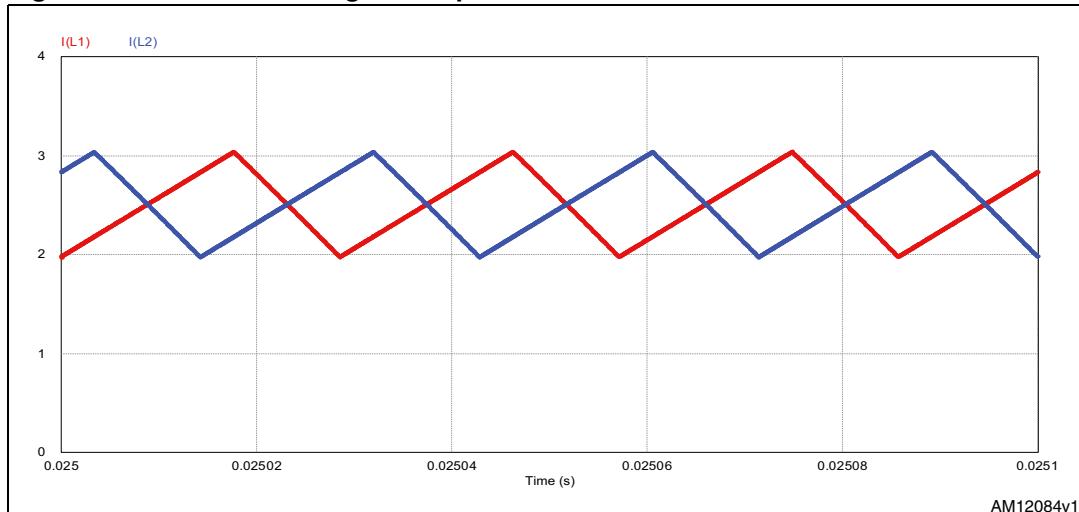
**Figure 3.** DC-DC converter topology



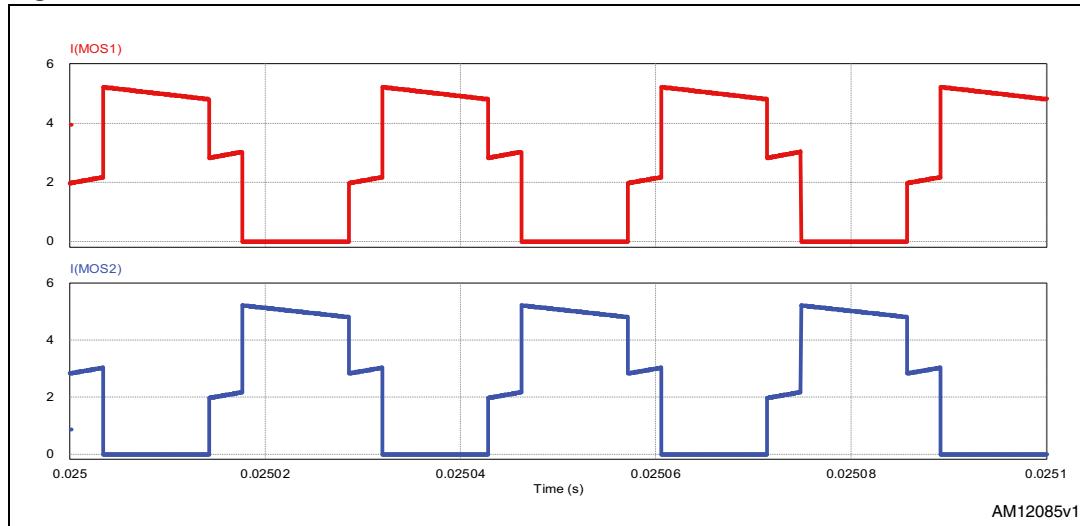
It consists of an input capacitor C1, two inductors, L1 and L2, two ground referenced MOSFETs, MOS1 and MOS2, a high frequency transformer, T1, two rectifier diodes, D1 and D2, and three output capacitors, C2, C3 and C4. The two rectifier diodes, together with C2 and C3, form a voltage doubler circuit which is used to further boost the HF transformer output voltage. The advantage of such a solution, compared to a standard one using four rectifier diodes, is to halve the transformer turns ratio, with consequent realization of a shorter secondary winding which, in turn, means better primary to secondary flux coupling and lower secondary winding conduction losses. The two driving signals used to command the two MOSFET gates are 180 degree phase shifted with respect to each other and always have a duty cycle >0.5.

This introduces the problem of controlling the DC-DC operation at very low output power. Two solutions can be used to overcome this problem. With the first solution the DC-DC converter is controlled by keeping the duty cycle at the minimum allowable value and the switching frequency is used as a control variable. The second solution uses a constant switching frequency and enables burst mode operation. This second case is the preferred method of control at low power. The implementation of burst mode is based on the definition of a suitable hysteresis bandwidth for the output voltage which is used to turn on and off the modulation of the DC-DC converter.

[Figure 3](#) shows the theoretical gate driving signals used to control MOS1 and MOS2. The 180 degree phase shift produces two phase shifted inductor currents ([Figure 4](#)) which in turn produce the beneficial effect of input and output current ripple cancellation. This allows the use of small capacitor values to filter the high frequency content of input and output currents.

**Figure 4.** Gate driving signals of the DC-DC converter**Figure 5.** Currents through the input inductors

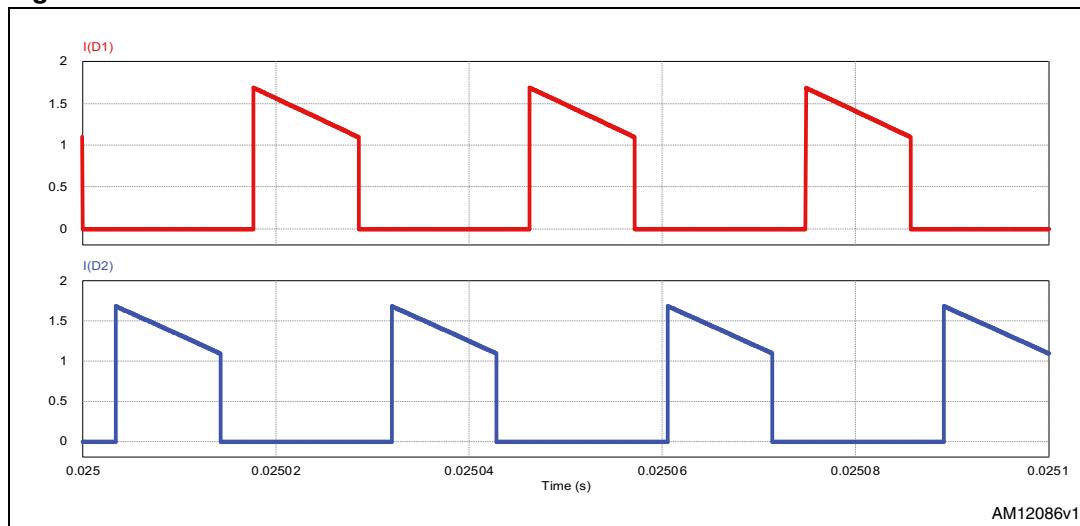
As the control strategy requires the two gate drive signals to be overlapped during part of the switching period, there is an operating interval during which both the MOSFET devices are ON and therefore both the input inductor chokes, L1 and L2, store energy. During this interval the input current is equally divided in the two MOSFETs, as shown in [Figure 6](#), and no current flows across the secondary winding and the diodes. The load is supplied by the output capacitors.

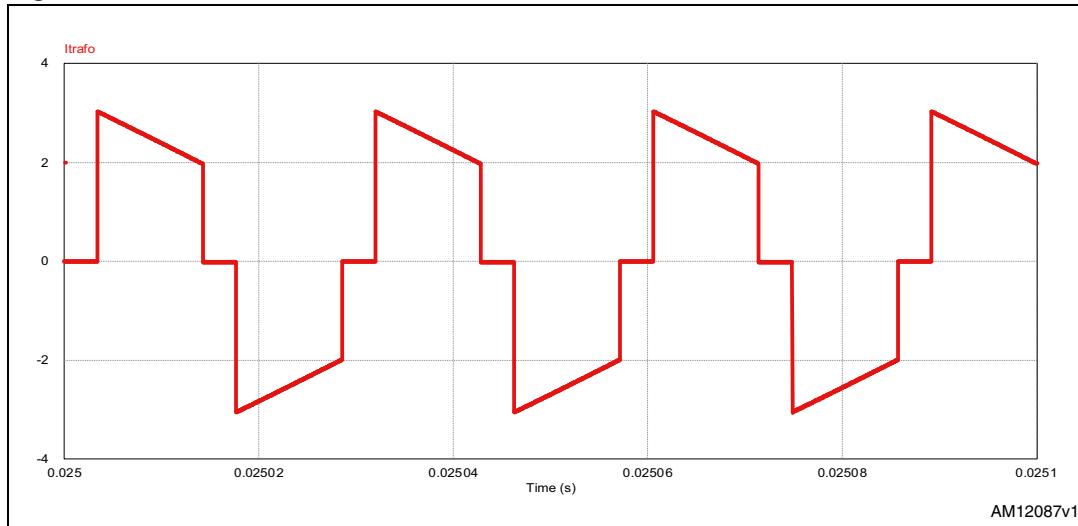
**Figure 6.** MOSFET MOS1 and MOS2 currents

During the second switching interval MOS1 is still on while MOS2 is turned off. The energy, previously stored in L2 is now transferred to the secondary while inductor L1 is charged by the input voltage and its current continues to build up. The primary current is delivered to the transformer secondary winding and output capacitor C2 is charged since diode D2 is in conduction ([Figure 7](#)). During the third time interval both MOSFETs conduct again.

Therefore, energy is stored both in L1 and L2 while the load is supplied by the output capacitors. During the fourth time interval MOS1 is off and MOS2 is kept on, which means that the energy previously stored in L1 is discharged on C3 with the transformer secondary current flowing through D1.

In reality, some additional operating intervals must be taken into account. This is mainly due to the presence of system parasitic elements such as transformer leakage inductance and semiconductor output capacitances.

**Figure 7.** Rectifier diode currents

**Figure 8.** HF transformer current

The main specifications used for the design of the DC-DC stage are reported in [Table 2](#).

**Table 2.** DC-DC converter main specifications

Specification	Value
Nominal input voltage	35.8 V
Maximum input voltage	40 V
Minimum input voltage	20 V
Nominal output power	250 W
Nominal output voltage	380 V
Maximum output voltage	430 V
Minimum output voltage	370 V
Target efficiency	>97%
Switching frequency	35 kHz

The design equations used to carry out the implementation of the DC-DC converter are described and commented on in the following part of this document.

1. Calculation of the switching period:

#### Equation 1

$$T = \frac{1}{f} = \frac{1}{35000} = 28.57\mu s$$

2. Calculation of the maximum duty cycle:

In this topology the switch duty cycle is always >0.5. Let's call D the time beyond  $T_s/2$  for which the MOSFET is still closed:

**Equation 2**

$$D_{\max} = \frac{t_{on\max}}{T_s} - 0.5 = 0.2 \quad V_0 = \frac{2 \cdot V_{in}}{1-D} \cdot \frac{N_2}{N_1}$$

$$t_{on\max} = 0.7 \cdot T_s$$

3. Calculation of maximum input power:

**Equation 3**

$$P_{in} = \frac{P_{out}}{\eta} = \frac{250}{0.97} = 257.7W$$

4. Calculation of maximum average input current:

**Equation 4**

$$I_{in\max} = \frac{P_{in}}{V_{in\min}} = \frac{257.7}{20} = 12.8A$$

5. Calculation of the maximum switch RMS current:

**Equation 5**

$$I_{rms\max} = \frac{\sqrt{2-D}}{2} \cdot I_{in\max} = \frac{\sqrt{2-0.2}}{2} \cdot 12.8 = 8.6A$$

6. Calculation of maximum average output current:

**Equation 6**

$$I_{out\max} = \frac{P_{out}}{V_{out\min}} = \frac{250}{370} = 0.67A$$

7. Calculation of transformer turns ratio:

**Equation 7**

$$\frac{N_2}{N_1} = \frac{\frac{V_{out}}{2} \cdot (1-D)}{2 \cdot V_{in}} = \frac{\frac{380}{2} \cdot (1-0.2)}{2 \cdot 30} = 2.53$$

where  $V_{in}$  is chosen as the average between the maximum and minimum input voltage value. The final transformer turns ratio has been chosen equal to 2.6.

8. Calculation of minimum current value for CCM operation:

**Equation 8**

$$P_{lim} = 10\% P_{out}$$

$$P_{lim} = 0.1 \cdot 250 = 25W$$

$$I_{lim} = \frac{1}{2} \cdot \frac{P_{lim}}{V_{in}} = \frac{12.5}{30} = 0.625A$$

to ensure CCM for  $I > I_{lim}$ .

9. Calculation of input current ripple:

**Equation 9**

$$\begin{aligned}\Delta I_{ind} &= I_{lim} = 0.625A \\ \Delta I_{in} &= \frac{\Delta I_{ind}}{2} = 0.31A \\ I_{ripple} &= \frac{\Delta I_{in}}{2} = \frac{0.31}{2} = 0.15A\end{aligned}$$

10. Calculation of input inductors value:

**Equation 10**

$$\begin{aligned}\Delta I_{ind} &= 2 \cdot \Delta I_{in} = 0.625A \\ L &= \frac{V_{in\_min} \cdot D_{switch\_max}}{\Delta I_{ind} \cdot f_s} = 640\mu H\end{aligned}$$

11. Calculation of diodes RMS current:

**Equation 11**

$$I_{D_{rms\max}} = \sqrt{2 - D} \cdot \frac{I_{in\max}}{2 \cdot n} = \sqrt{2 - 0.2} \cdot \frac{12.8}{2 \cdot 2.6} = 3.3A$$

12. Calculation of output capacitor value:

**Equation 12**

$$C \geq \frac{I_o \cdot D \cdot T_s}{\Delta V_{max}} = \frac{0.675 \cdot 0.2 \cdot 28.57 \cdot 10^{-6}}{0.2} = 1.92\mu F$$

13. Calculation of capacitor ripple current:

**Equation 13**

$$\Delta I_{cap} = \frac{I_{in}}{2 \cdot n} = 2.4A$$

14. Calculation of maximum capacitor ESR:

**Equation 14**

$$ESR_{cap_{max}} = \frac{\Delta V_{max}}{\Delta I_{cap}} = \frac{0.2}{2.4} = 83.3m\Omega$$

15. Calculation of main power devices breakdown voltage:

**Equation 15**

$$V_{brdw} \geq 1.2 \cdot \frac{V_{out\max}}{2 \cdot n} = \frac{430}{2 \cdot 2.6} = 99.2V$$

16. Calculation of diodes breakdown voltage:

**Equation 16**

$$V_{brdwdiode} = 1.2 \cdot V_{out\max} = 1.2 \cdot 430 = 516V$$

17. Calculation of input capacitor RMS current:

**Equation 17**

$$C_{in} = \frac{\Delta i_c}{35000 \cdot \Delta V_c} = \frac{0.675}{35000 \cdot 2} = 9.6\mu F$$

$$\Delta V_c = 10\% V_{in\min}$$

$$ESR_{max\ C_{in}} = \frac{\Delta V_c}{\Delta i_c} = \frac{2}{0.675} = 2.96\Omega$$

18. MOSFET selection and losses calculations:

**Table 3. DC-DC converter MOSFET main characteristics**

Device	Type	R <sub>DS(on)</sub>	T <sub>swoff</sub>	V <sub>br</sub>	I <sub>d</sub> @ 100 °C	Q <sub>g</sub>
STH180N100F3	MOSFET	4.5 mΩ	106.8 ns	100 V	120 A	114.6 nC

**Equation 18**

$$P_{sw\max} \geq \frac{V_{ds\max} \cdot I_{drain\max} \cdot t_{sw\off}}{2 \cdot T_s} = \frac{99.2 \cdot \frac{12.86}{2} \cdot (106.8 \cdot 10^{-9})}{2 \cdot 28.57 \cdot 10^{-6}} = 1.19W$$

$$P_{cond\max} = 1.6 \cdot R_{dson} \cdot I^2_{rms} = 1.6 \cdot 0.0045 \cdot (8.6)^2 = 0.53W$$

$$P_{drv} = V_{gs} \cdot Q_g \cdot f_s = 15 \cdot 114.6 \cdot 10^{-9} \cdot 35000 = 0.06W$$

$$P_{mostot} = 2 \cdot P_{sw\max} + 2 \cdot P_{cond\max} + 2 \cdot P_{drv} = 3.56W$$

19. Diode selection and losses calculations:

**Table 4. DC-DC converter rectifier diodes main characteristics.**

Device	Type	Vf@ 12 A	Trr	V <sub>br</sub>	I <sub>d</sub> @ 100 °C	IRM (typ.)
STTH12R06	Ultrafast soft recovery	1.4 V	25 ns	600 V	12 A	7 A

**Equation 19**

$$P_{sw\max} = \frac{1}{2} \cdot \frac{V_{brdw\max} \cdot I_{RM} \cdot t_{rr}}{T_s} = \frac{1}{2} \cdot \frac{516 \cdot 7 \cdot 25 \cdot 10^{-9}}{28.56 \cdot 10^{-6}} = 1.58W$$

$$P_{cond\max} = 1.16 \cdot I_{Davg} + 0.053 \cdot I^2_{DRMS} = 1.16 \cdot 0.675 + 0.053 \cdot (3.2)^2 = 1.3W$$

$$P_{diodeltot} = 2 \cdot P_{sw\max} + 2 \cdot P_{cond\max} = 5.76W$$

### HF transformer design

The design is based on the specifications reported in [Table 5](#) and has been used to provide the main parameters required by HF transformer manufacturers for the realization of the prototypes.

**Table 5. HF transformer specifications**

Specification	Value
Turns ratio	2.6
RMS input current	4.7 A
Nominal output voltage	380 V
Minimum output voltage	370 V
Output current	1.77 A
Switching frequency	35 kHz
Efficiency	98%
Max. operating flux density	0.05T
Window utilization	0.3
Duty cycle	0.45
Temperature rise	30 °C

The design procedure and equations are shown in the section below.

1. Calculation of total transformer power:

#### Equation 20

$$P_{app\_T} = \frac{P_{outT}}{\eta_T} = \frac{250}{0.98} = 255.1W$$

2. Core selection:

Based on the maximum power that the HF transformer has to manage, the RM14 core with N87 Ferrite from Epcos-TDK has been selected. The main characteristics of this core are reported in [Table 6](#).

**Table 6.** RM14 core with N87 Ferrite main characteristics

Specification	Value
Equivalent core section area $A_c$	170 mm <sup>2</sup>
Core volume $V_e$	14000 mm <sup>3</sup>
Mean turn length MLT	71,5 mm
Saturation flux density $\Delta B$	390 mT
Optimum frequency range	25-500 kHz
$A_l$	7898.9 nH
Pmax@35 Hz	530 W
R <sub>th</sub>	18 °C/W

3. Calculation of the number of primary turns:

Assuming a maximum flux density swing of 200 mT, the minimum number of primary turns to avoid core saturation is given by:

**Equation 21**

$$N_1 = \frac{V_{inT_{min}} \cdot D_{max} \cdot T_s}{\Delta B \cdot A_c} = \frac{\frac{370}{2 \cdot 2.6} \cdot 0.2 \cdot 28.56}{0.2 \cdot 170} \cong 12$$

4. Calculation of the number of primary turns:

Assuming a maximum flux density swing of 200 mT the minimum number of primary turns to avoid core saturation is given by:

**Equation 22**

$$N_2 = N_1 \cdot n = 12 \cdot 2.6 \cong 32$$

5. Calculation of the magnetizing inductance:

**Equation 23**

$$L_l = N_1^2 \cdot A_l = 144 \cdot 7898.9 \cdot 10^{-9} \cong 1.13mH$$

6. Wire size calculation:

At 35 kHz the current penetration depth is given by:

**Equation 24**

$$\delta = \frac{6.62}{\sqrt{f}} = 0.353mm$$

The maximum wire diameter to avoid skin effect is given by:

**Equation 25**

$$d = 2\delta = 0.7\text{mm}$$

Assuming a current density J of 5 A/mm<sup>2</sup>:

**Equation 26**

$$J = 5 \frac{A}{mm^2}$$

The primary and secondary wire selection can be done according to the following equation:

**Equation 27**

$$A_{wp} = \frac{I_{inT}}{J} = \frac{4.3}{5} = 0.86\text{mm}^2$$

where  $A_{wp}$  and  $A_{ws}$  are the primary and secondary wire cross sectional areas.

Considering the mean turn length value reported in [Table 6](#), the primary and secondary winding length can be calculated using the following equations:

**Equation 28**

$$\begin{aligned} MLP &= N_1 \cdot MLT = 12 \cdot 71.5 \cdot 10^{-3} = 0.858\text{m} \\ MLS &= N_2 \cdot MLT = 32 \cdot 71.5 \cdot 10^{-3} = 2.288\text{m} \end{aligned}$$

Knowing that copper resistivity  $\rho$  is equal to:

**Equation 29**

$$\rho = 0.0175 \frac{\Omega}{mm^2}$$

The primary and secondary winding resistance values are given by:

**Equation 30**

$$\begin{aligned} R_p &= \rho \cdot \frac{MLP}{A_{wp}} = 0.0175 \cdot \frac{0.858}{0.86} \cong 25\text{m}\Omega \\ R_s &= \rho \cdot \frac{MLS}{A_{ws}} = 0.0175 \cdot \frac{2.28}{0.35} \cong 114\text{m}\Omega \end{aligned}$$

7. Transformer losses calculation:

Having calculated the values of primary and secondary winding resistance the calculation of copper losses is straightforward with the following equation:

**Equation 31**

$$P_{Fe} = P_{lm} \cdot V_e = 141 \cdot 10^3 \cdot 14000 \cdot 10^{-9} = 0.19W$$

The second major contribution to transformer losses is given by core losses. The value of specific core loss,  $P_{lm}$ , for an RM14 core operating at 35 kHz, 100 °C and with a maximum flux density of 200 mT, is equal to 141 kW/m<sup>3</sup>.

The total core loss is therefore given by the following equation:

### Equation 32

$$P_{Fe} = P_{lm} \cdot V_e = 141 \cdot 10^3 \cdot 14000 \cdot 10^{-9} = 1.9W$$

### 8. Transformer temperature rise:

Using the value of thermal resistance reported in [Table 6](#), the maximum temperature rise for the HF transformer is given by:

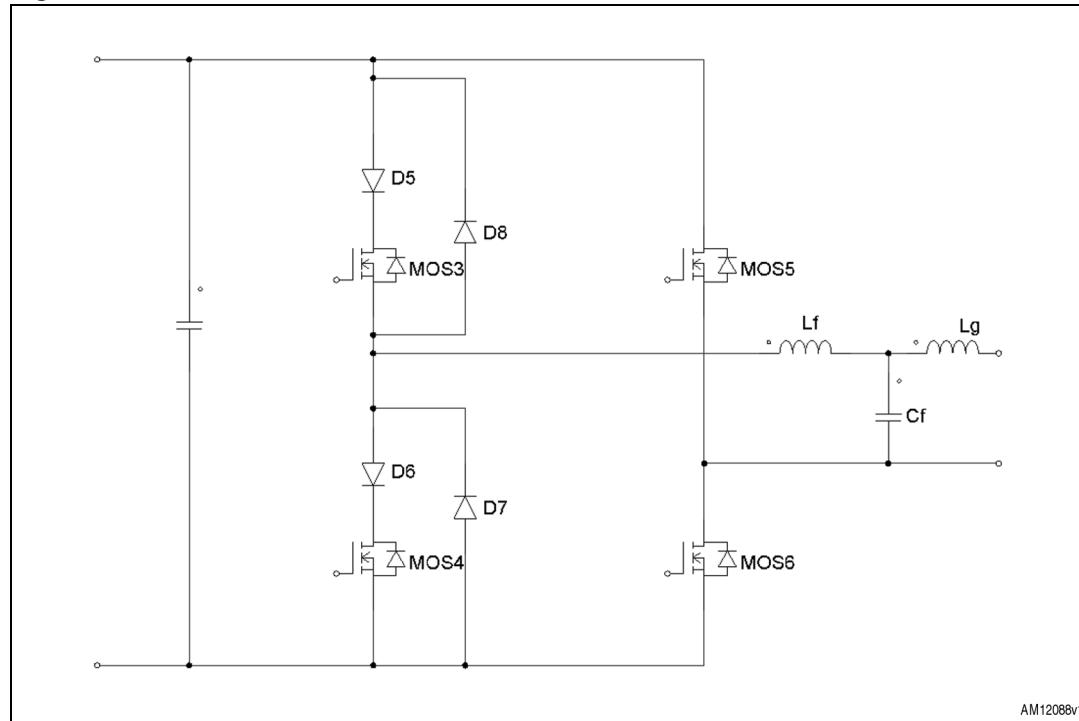
### Equation 33

$$\Delta T = R_{th} \cdot (P_{Fe} + P_{cu}) = 18 \cdot 2.09 = 37.62^\circ C$$

## DC-AC converter design

The basic scheme of the DC-AC converter topology is depicted in [Figure 9](#). MOS5 and MOS6 are connected in one leg and switch at a frequency of 17.4 kHz. Two Schottky diodes are connected to the drain of these two MOSFETs in order to inhibit the internal body diode. Two external silicon carbide (SiC) diodes are therefore connected in anti-parallel for current freewheeling while avoiding problems connected to reverse recovery at MOSFET turn-on. MOS7 and MOS 8 are connected in the second leg and switch at grid frequency, either 50 Hz or 60 Hz. An LCL filter is connected to the mid-point of each inverter leg and is used to interface the system to the grid. On the DC side a bank of four electrolytic capacitors is used to store and deliver energy whenever this is required during normal operation.

**Figure 9. Basic scheme of the DC-AC converter**



The minimum value of capacitance required on the DC bus is calculated according to the following equation:

**Equation 34**

$$C_{bus} = \frac{4 \cdot P_{out}}{V_{bus_{min}}^2} \cdot t_1 = \frac{4 \cdot 250 \cdot 5 \cdot 10^{-3}}{370^2} = 36.52 \mu F$$

where  $t_1$  is given by:

**Equation 35**

$$t_1 = 5ms = \frac{1}{4 \cdot F_{grid}}$$

A total capacitance of about twice the calculated value, rated at 450 V and having an operating temperature of 105 °C, is selected for the inverter implementation. The capacitor bank is realized with the parallel connection of four 22 µF, 450 V capacitors.

The value of  $L_f$  is designed in order to limit the current ripple to about 20% of the nominal current value. The following equations have been used to calculate the filtering inductance value:

**Equation 36**

$$L_f = \frac{1}{n} \cdot \frac{(V_{bus} - V_{grid\ pk}) \cdot D}{\Delta i \cdot f_{sw}} = \frac{1}{3} \cdot \frac{(380 - 325) \cdot 0.75}{0.22 \cdot 17.400} = 3.54 mH$$

where  $n$  is the number of inverter levels ( $+V_{bus}$ , 0 and  $-V_{bus}$ ) and  $D$  is the inverter duty cycle.

The filter capacitor value is selected to limit the exchange of reactive power below 5% of nominal active power:

**Equation 37**

$$P_{reactive} < 0.05 \cdot P_{active}$$

$$X_{C_f} \geq \frac{V_{grid}^2}{0.05 \cdot P_{active}} = \frac{230^2}{12.5} = 4232 \Omega$$

$$C_f \leq \frac{1}{\omega \cdot X_{C_f}} = 750 nF$$

To avoid resonance problems for the filter, due to low and high order harmonics, the resonant frequency should be chosen in a range between ten times the line frequency and one half of the switching frequency. The resonant frequency of an LCL filter is given by:

**Equation 38**

$$f_{res} = \frac{1}{2 \cdot \pi} \cdot \sqrt{\frac{L_f + L_g}{L_f \cdot L_g \cdot C_f}}$$

Choosing a filter capacitor value of 470 nF and a grid coupling inductor value equal to the filtering inductor value, the resulting filter resonant frequency is equal to 5.4 kHz which falls in the frequency range mentioned above.

The four MOSFETs selected for the inverter stage are 9 A, 650 V MDMeshV devices. The part number is STB11N65M5 and the main electrical characteristics are reported in [Table 7](#).

**Table 7. STB11N65M5 MOSFET main electrical characteristics**

Device	Type	R <sub>DSmax</sub>	V <sub>br@Tjmax</sub>	I <sub>dcont. @ 100 °C</sub>	Q <sub>g</sub>
STB11N65M5	MOSFET	0.48 Ω	710 V	5.6 A	17 nC

The blocking diodes are two STPS1545, 15 A, 45 V Schottky diodes while the freewheeling diodes are two STPSC606, 6 A, 600 V silicon carbides.

### 3 Schematic description

This section of the application note is intended to provide information on the main circuits adopted in the MIC design.

The two main power processing stages of the microinverter are shown in [Figure 10](#). The input filter capacitance is realized with the parallel connection of fourteen, 100 V, 1  $\mu$ F ceramic capacitors. The two DC-DC converter MOSFETs have the source pins connected to ground and the drain connected both to the high frequency transformer and one of the input chokes. A 100 V Zener diode is connected between the drain and the source of each MOSFET in order to limit the voltage across the device whenever this exceeds the clamping voltage of the Zener itself. This may happen when the inductor current is suddenly interrupted. Separate gate resistances for turn-on and turn-off allow to independently control the two switching transitions.

The high frequency transformer is connected between the input stage and the rectifier stage of the DC-DC converter. The transformer is realized with a very low value of leakage inductance which is beneficial both to efficiency and reliability of the converter since the maximum drain to source voltage, appearing at turn-off due to the energy stored in this parasitic element, is limited and never exceeds the breakdown voltage of the input MOSFETs.

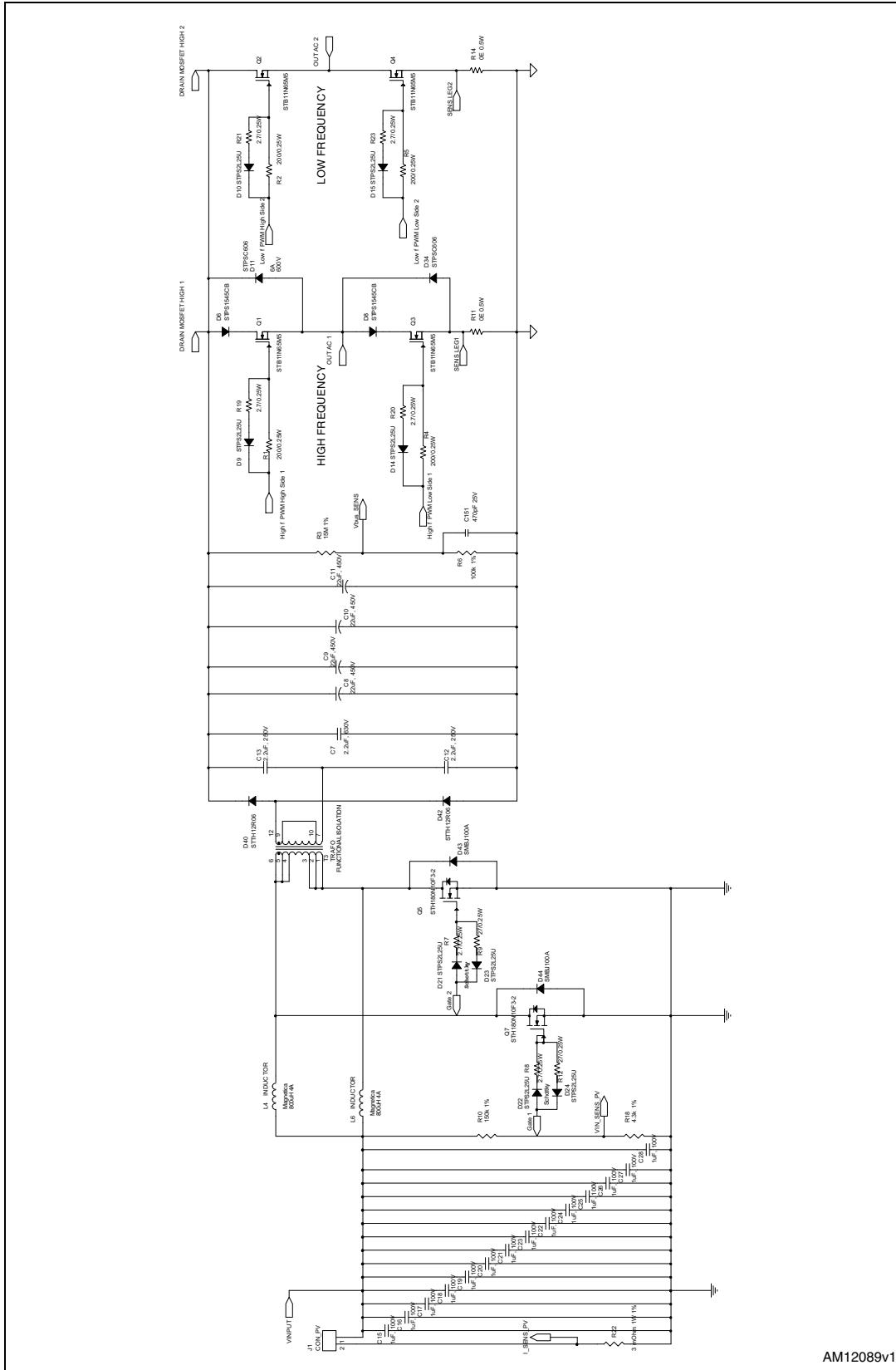
The high voltage DC bus is realized with four 22  $\mu$ F, 450 V electrolytic capacitors and a 2.2  $\mu$ F, 600 V plastic film capacitor. The DC-AC converter is supplied from this bus and used to inject current into the grid at 50 Hz or 60 Hz. In the low frequency leg, the low-side device is kept in conduction when the grid voltage is positive while the high-side device is kept in conduction for the period during which the grid voltage is negative. Two complementary sinusoidal PWM signals are provided to the gate driving network of the high frequency leg devices to ensure sinusoidal output current and voltage waveforms. The inverter is interfaced to the grid via an LCL filter. A relay is used to connect and disconnect the inverter from the grid whenever required by the application. The schematic in [Figure 11](#) shows the filtering and relay schematic section. The grid current feedback signal is obtained using a Hall effect sensor while the grid voltage sensing is performed using a voltage transformer. The two signals are then reported to the 0/3.3V voltage range required by the A-D converters of the STM32F103xx microcontrollers, by means of standard circuitry based on operational amplifiers.

Both the DC-DC converter and inverter MOSFETs are driven by 0/+15 V gate signals. The DC-DC MOSFETs are driven by a PM8834 driver, which features two independent outputs capable of sourcing up to 2 A of current. The DC-DC converter driver circuit is shown in [Figure 12](#). The two driver outputs can also be connected in parallel to provide up to 4 A. This configuration is used for the DC-AC converter drivers, as shown in the schematic in [Figure 13](#). Two control signals are generated by the STM32F103xx: one is dedicated to the high frequency leg and the other to the low frequency one. These two signals are sent to the input of an ACPL 4506 opto-isolator whose output is used as an input for an L6390. This charge pump driver generates two complimentary outputs provided with deadtime and is characterized by an internal comparator and an internal operational amplifier which can be used to implement short-circuit current protection for each leg of the inverter. The demonstration board allows the implementation of this option since it is already provided with all the necessary hardware. However, since the two shunt resistors, R11 and R14 shown in [Figure 10](#), are zero Ohm resistors the short-circuit hardware protection is, in fact, disabled and replaced by firmware overcurrent detection. The source current capability of the L6390 is then amplified by means of four PM8834s whose outputs are directly

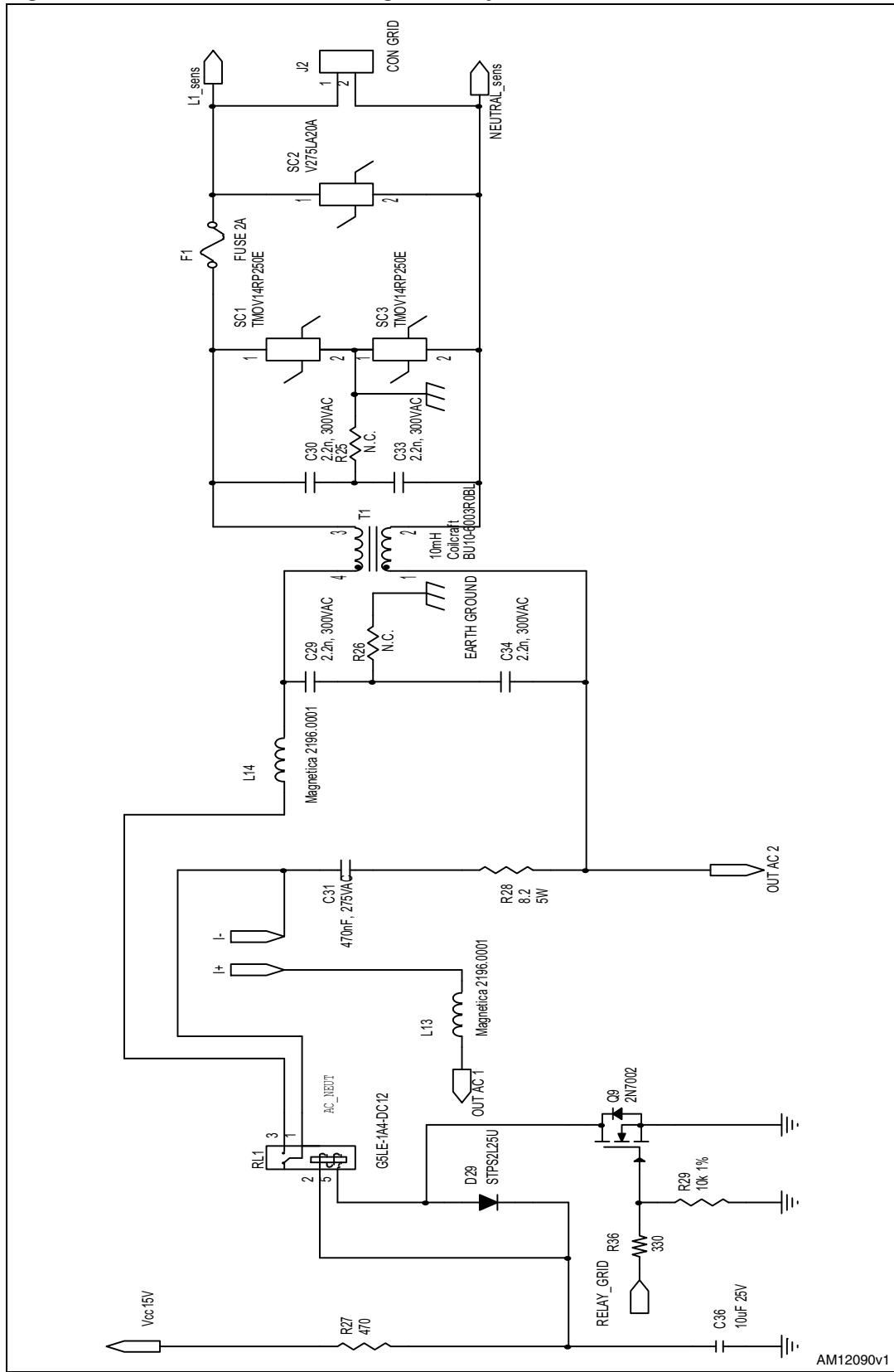
connected between the gate and source of each inverter MOSFET. The supply voltage of the inverter gate drive circuit is provided by two isolated, integrated DC-DC converters whose input is the 5 V generated by the auxiliary power supply connected to the PV input. The schematic of the auxiliary power supply is shown in [Figure 14](#). The two L4971s are connected to few external components in order to implement two buck converters used to step down the input voltage to +15 V and to +5 V.

The 3.3 V supplying the STM32F103xx microcontroller is then generated from the 5 V using a standard linear regulator. The 3.3 V is also used to supply a digital-to-analog converter mounted on the demonstration board for debugging purposes.

**Figure 10. Schematic of the two main power stages**



**Figure 11. Schematic of the filtering and relay circuit**



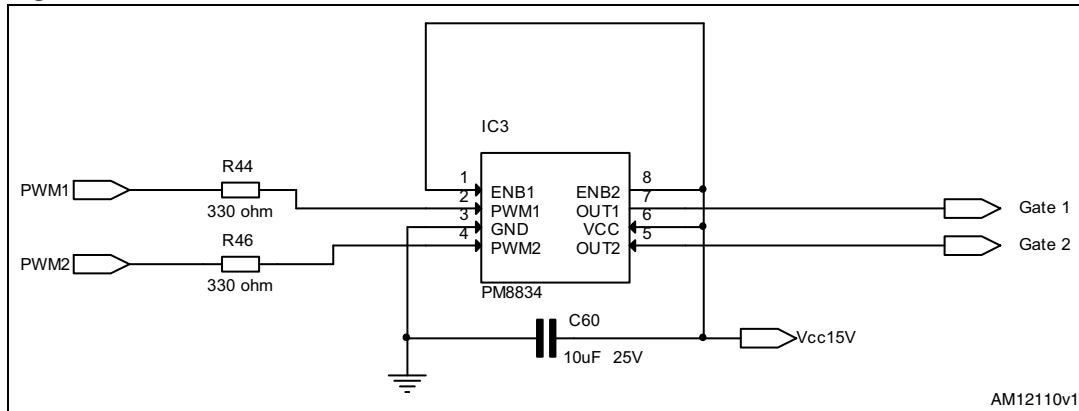
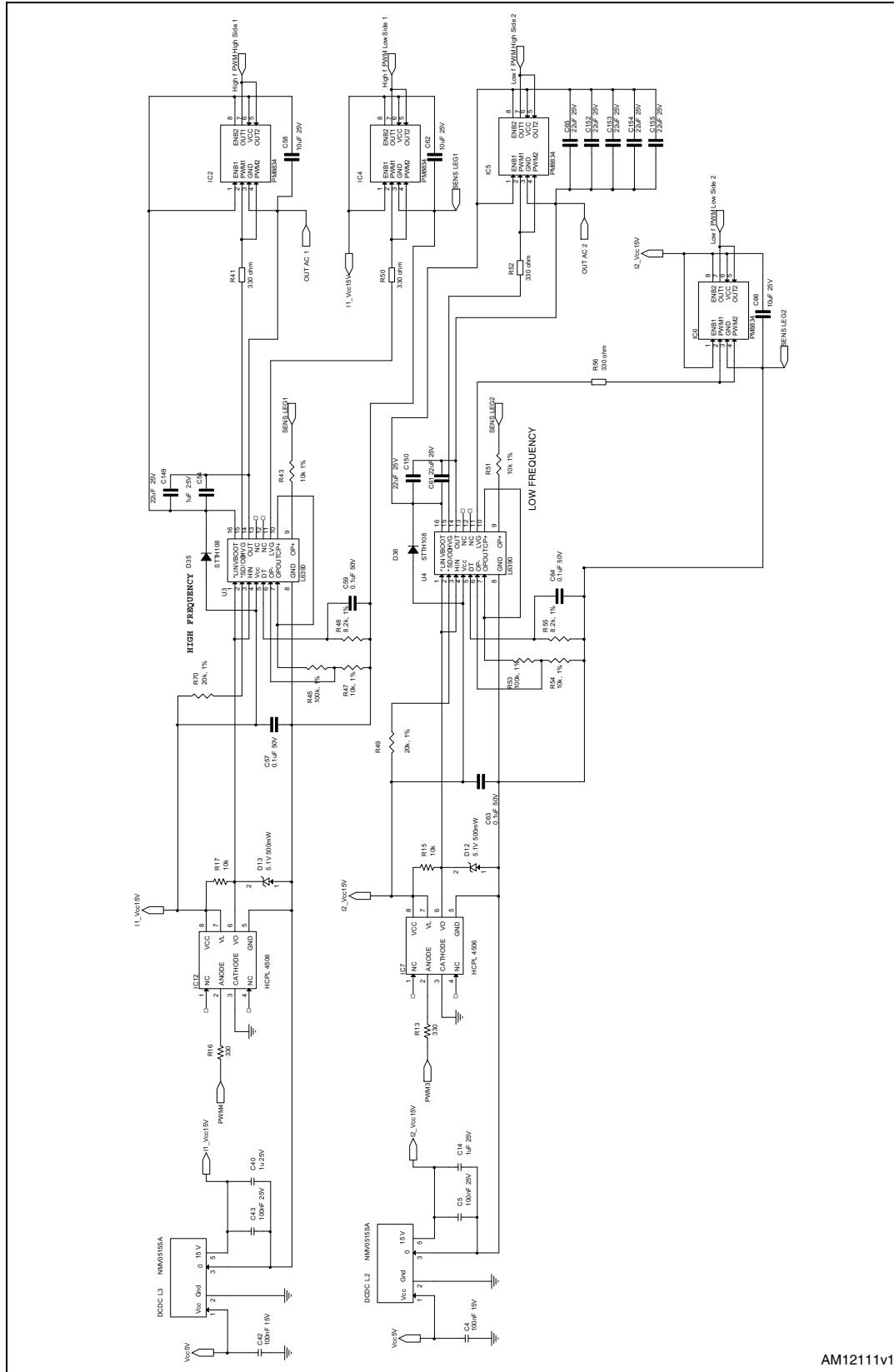
**Figure 12. DC-DC converter driver**

Figure 13. DC-AC converter driver



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Figure 14. Auxiliary power supply of the demonstration board

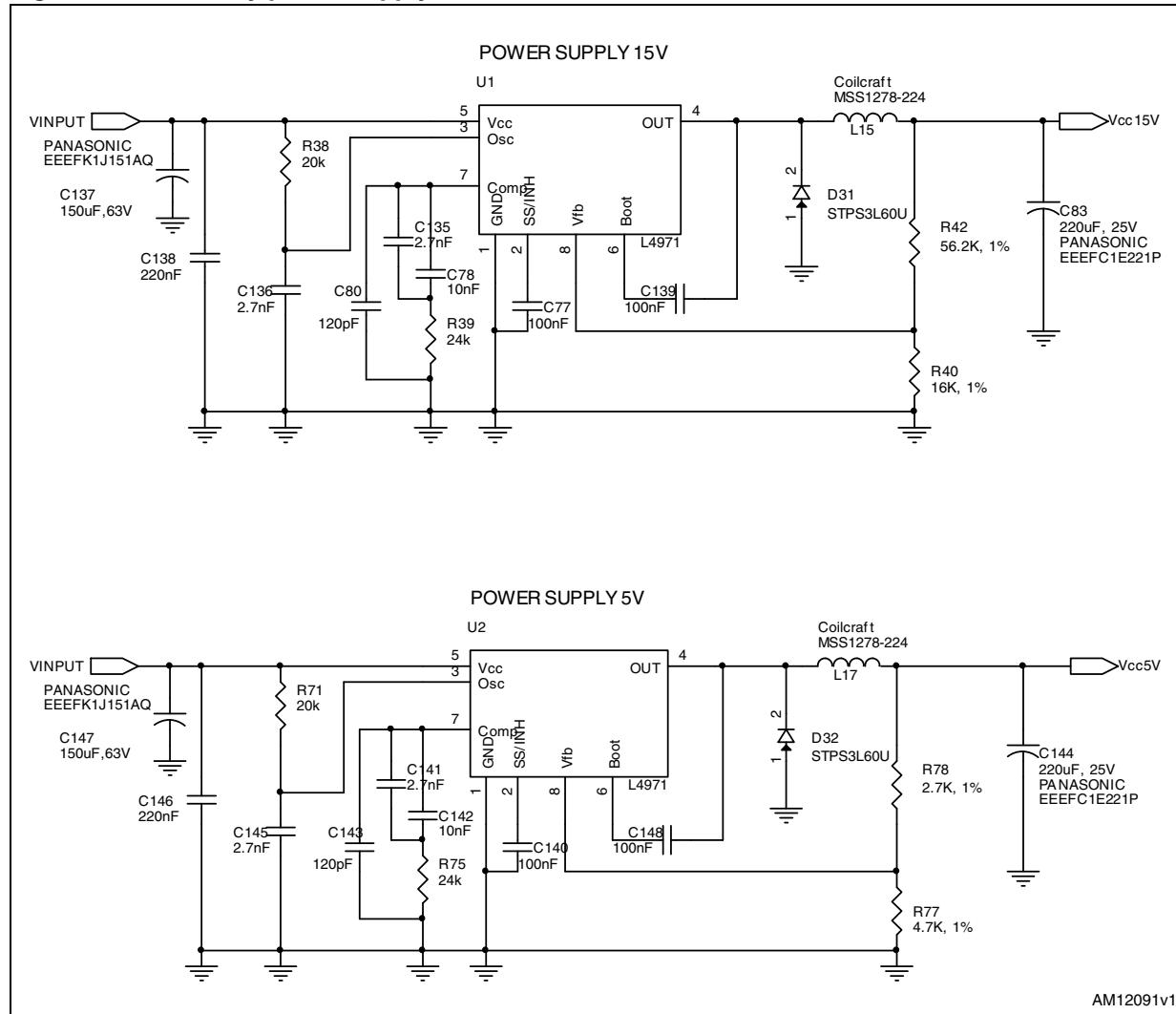


Figure 15. AC line current sensing

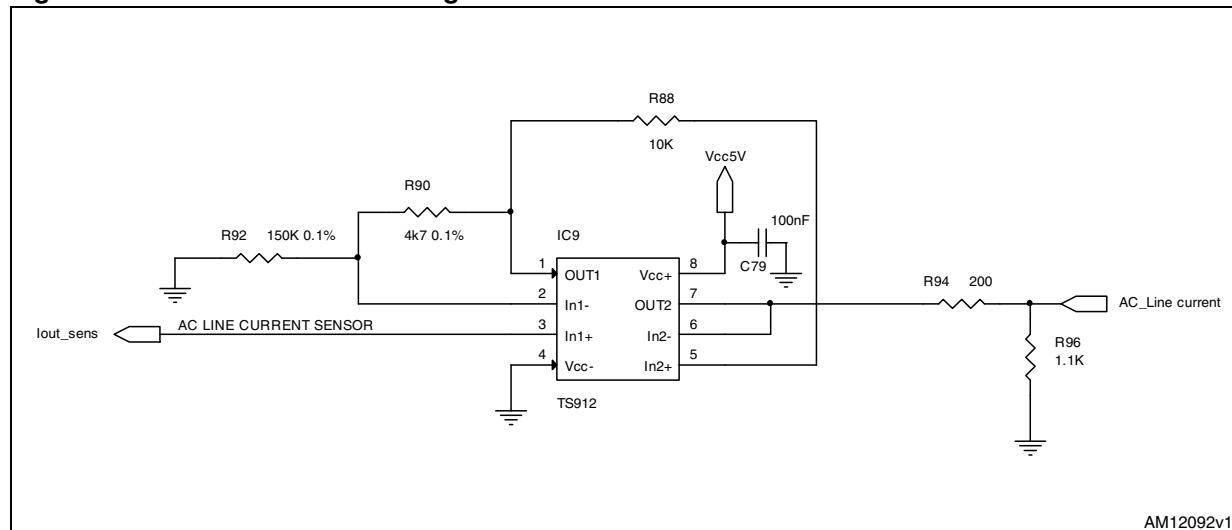
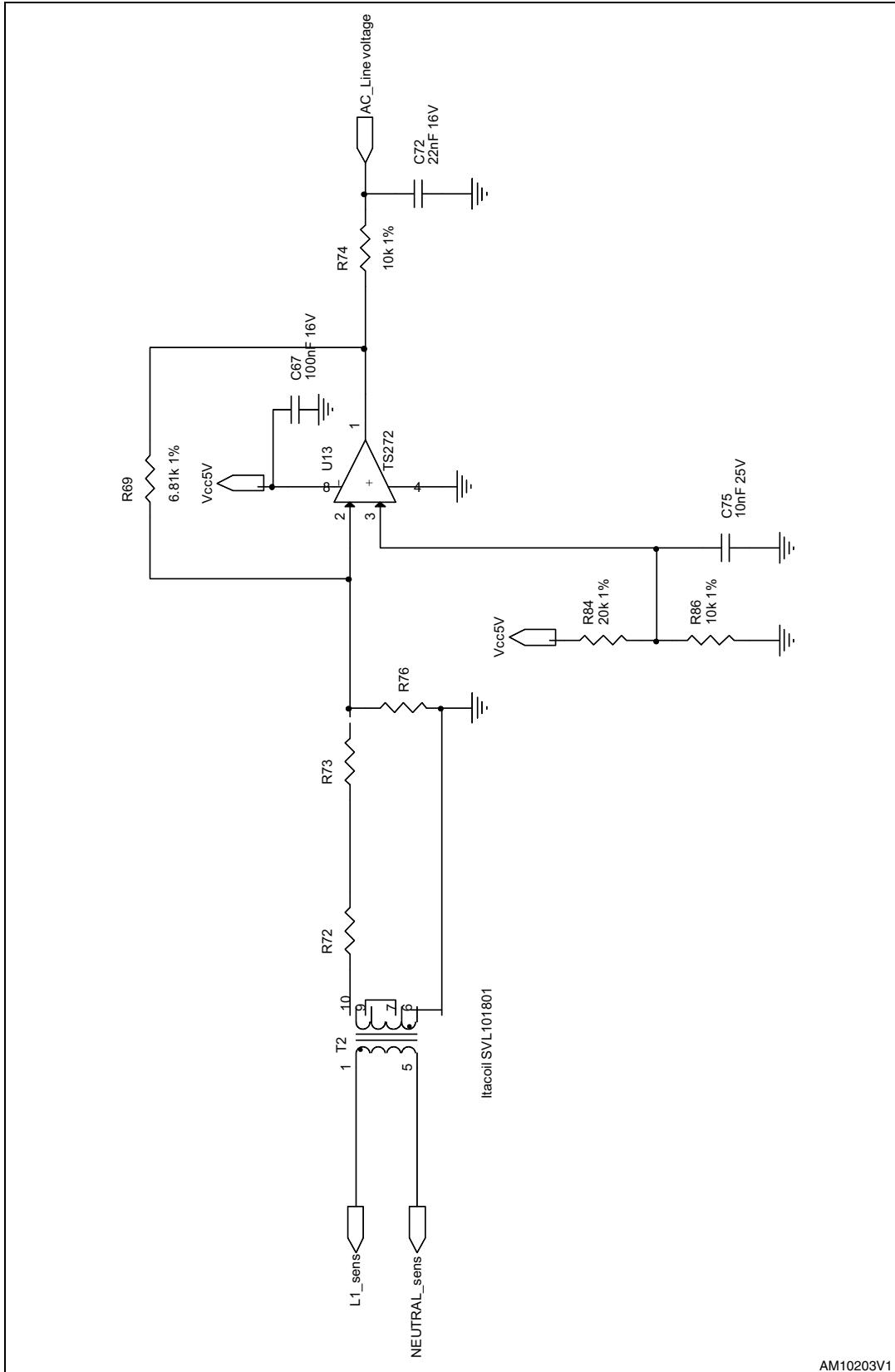
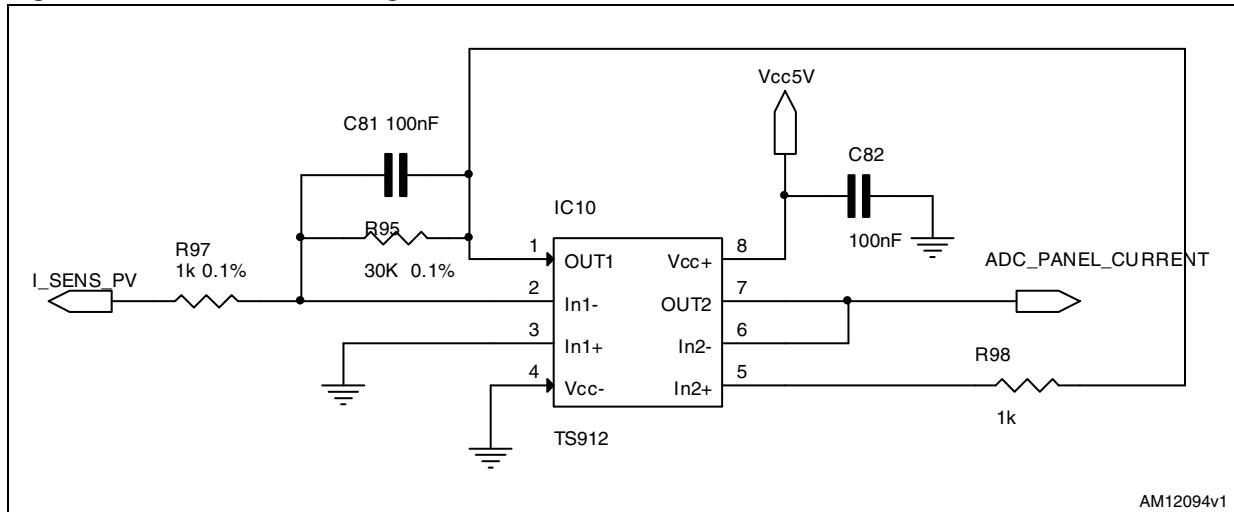


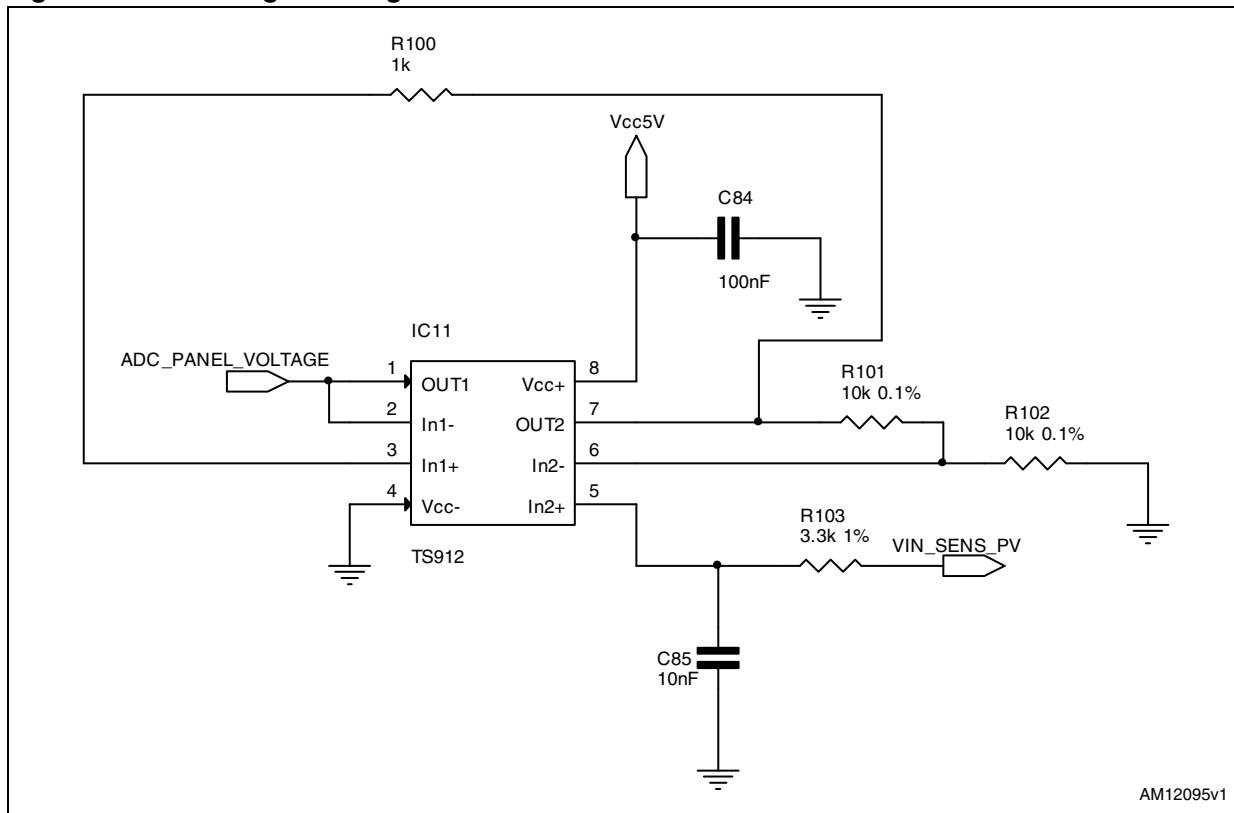
Figure 16. AC line voltage sensing



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**Figure 17. PV current sensing**

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**Figure 18. PV voltage sensing**

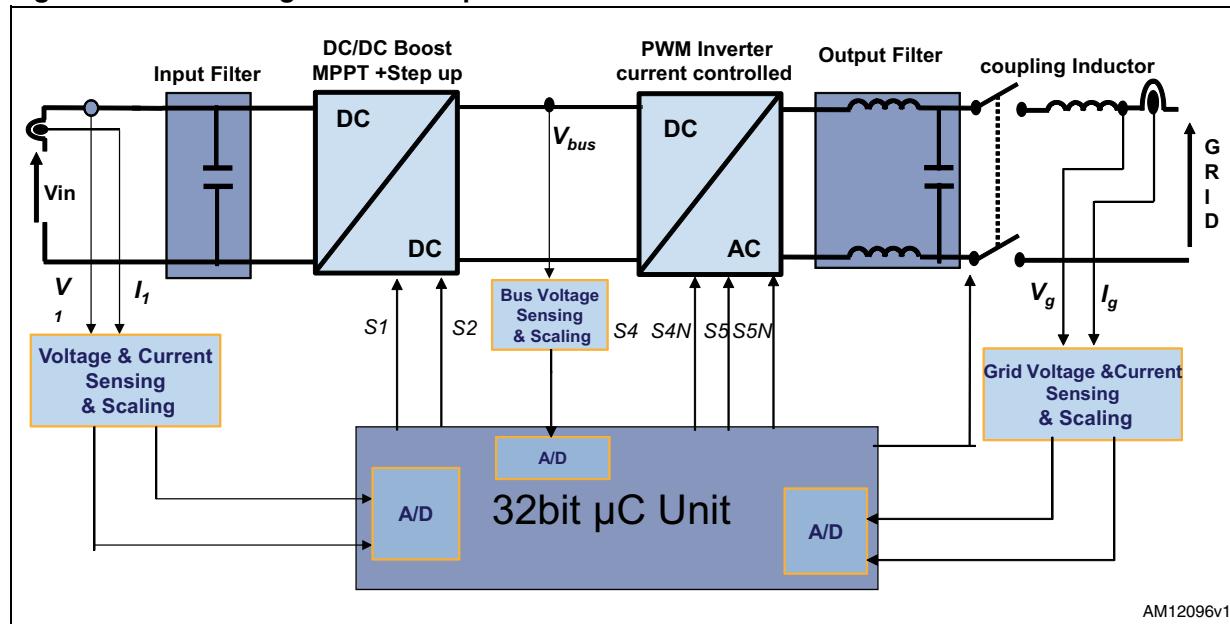
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## 4 STM32F103xx based current control for inverter grid connection

The current control method is based on a d-q synchronous reference frame which provides both the advantage of zero steady-state error, thanks to the use of PI controllers, and simple implementation. This method has been implemented on a 32-bit, ARM based microcontroller (STM32F103xx) and its performance was verified through simulations and experimental results.

A block diagram showing the five feedback signals processed by the microcontroller for the correct operation of the control algorithm is shown in [Figure 18](#).

**Figure 19. Block diagram of the implemented control**



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Every algorithm for grid-connected inverter operation is based on the estimation or direct measurement of grid voltage frequency and phase angle. The detection method used in this implementation for a single-phase inverter is based on a synchronous reference frame PLL. Single-phase inverters require a virtual bi-phase system. In fact, to create a rotating d-q reference, starting from a stationary frame, at least two independent phases are required. This problem is overcome with the creation of a virtual voltage,  $V_\beta$ , phase shifted with respect to the real grid voltage,  $V_\alpha$ , of 90 degrees. This is done via firmware. Knowing the two voltage components  $V_\beta$  and  $V_\alpha$ , the transformation from the stationary reference frame to the d-q rotating frame is given by the following equations:

**Equation 39**

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \cdot \begin{bmatrix} V_\beta \\ V_\alpha \end{bmatrix}$$

where  $\theta$  is the angle between the d-q reference frame and the stationary reference frame ([Figure 27](#)). The reverse transformation is given by:

**Equation 40**

$$\begin{bmatrix} V_\beta \\ V_\alpha \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} V_d \\ V_q \end{bmatrix}$$

where:

**Equation 41**

$$\begin{bmatrix} V_\beta \\ V_\alpha \end{bmatrix} = \begin{bmatrix} V_m \cos\theta_e \\ V_m \sin\theta_e \end{bmatrix}$$

Then the two components on the d-q reference frame are:

**Equation 42**

$$\begin{aligned} V_d &= V_m \cos\theta_e \cos\theta + V_m \sin\theta_e \sin\theta = V_m \cos(\theta - \theta_e) \\ V_q &= -V_m \cos\theta_e \sin\theta + V_m \sin\theta_e \cos\theta = V_m \sin(\theta - \theta_e) \end{aligned}$$

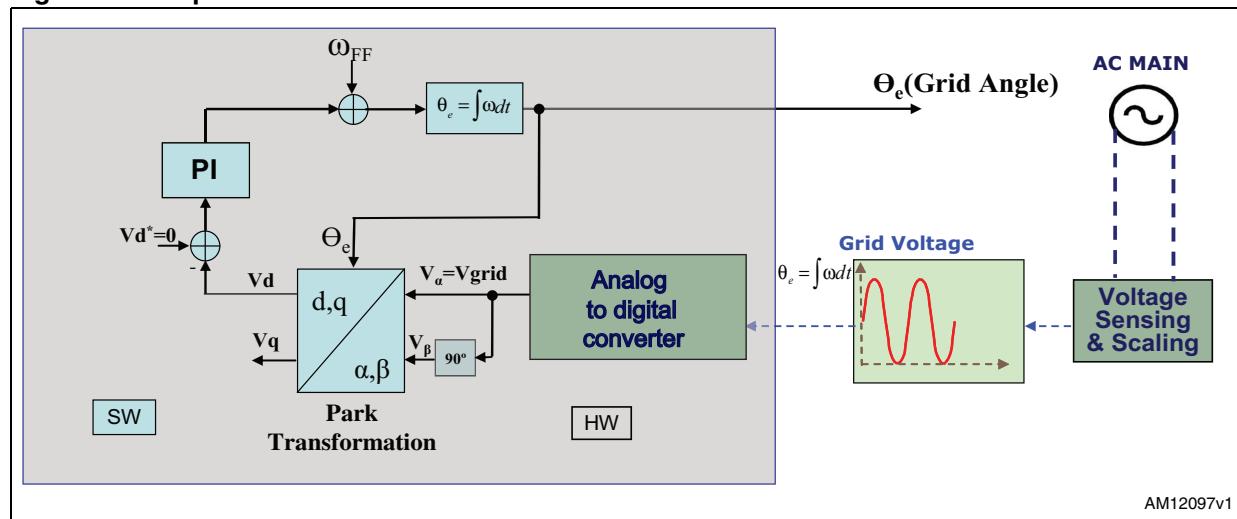
Therefore, if  $\theta = \theta_e$ , the two components are reduced:

**Equation 43**

$$\begin{aligned} V_d &= V_m \\ V_q &= 0 \end{aligned}$$

The grid voltage angle is detected using the PLL structure shown in [Figure 20](#).

**Figure 20. Implemented PLL structure**



The grid voltage and the 90 degree phase shifted voltage are used to perform the reference frame change, or “Park transformation”, and create two voltage components on the d-q reference frame called  $V_d$  and  $V_q$ . One of the two components is controlled to zero with a PI regulator. The output of the PI regulator is the grid frequency which can be integrated to obtain the grid angle.

It is worth noting that if the  $V_q$  component is controlled to zero then the  $V_d$  component follows the grid voltage rotation. In this case, the active power injected into the grid can be

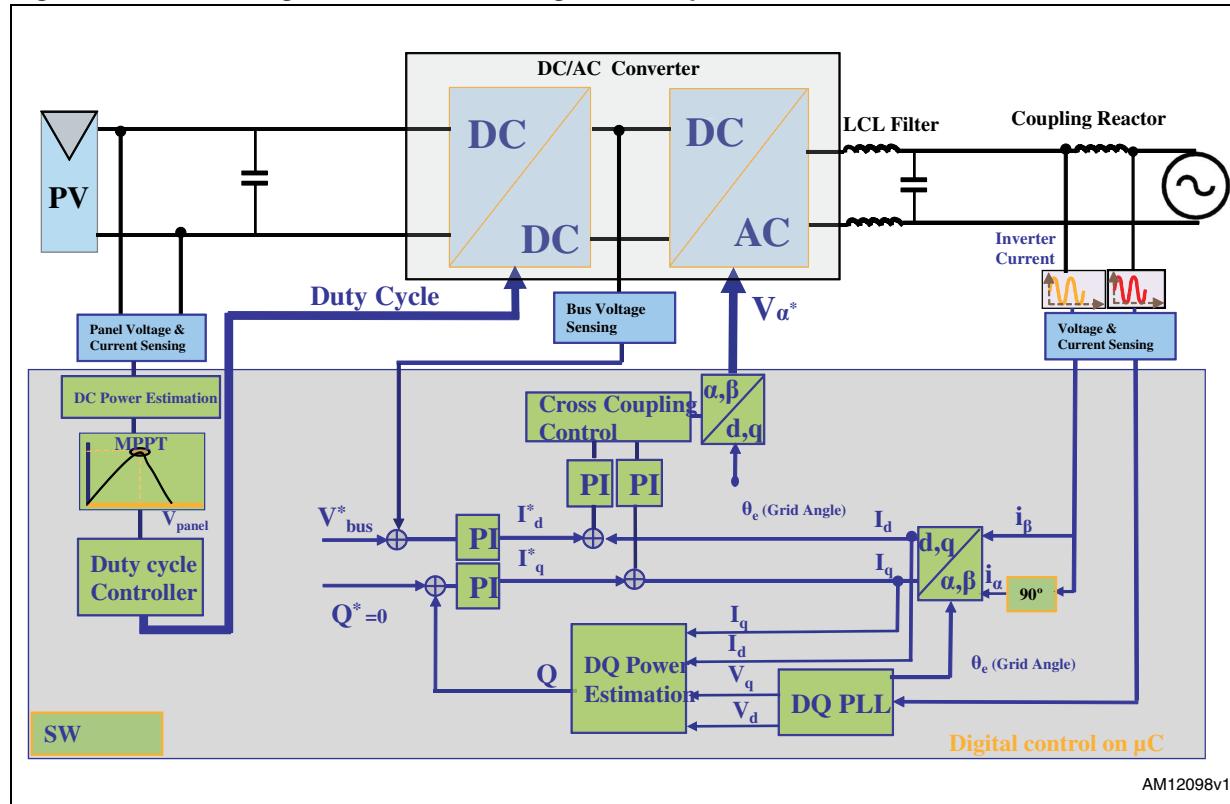
controlled transforming the current in the same reference frame and by acting on the amplitude of the  $I_d$  component. The  $I_q$  component must, also, be controlled in order to ensure zero reactive power injection. On the contrary, if the  $V_q$  component is controlled to zero in the PLL, the active power is controlled with the  $I_d$  current component and the  $I_q$  current component is used to control the reactive power to zero or to the desired value.

The reference values for the active and reactive component of the current are set by two additional PI regulators in the outer control loop. The active reference current component is generated by confronting the DC bus voltage with the reference voltage value. The error between the actual value and the reference DC bus voltage is sent to a PI regulator whose output is the active current component value.

Similarly, the reactive current reference value is set by another PI regulator whose input is the error generated between the reactive power command and the actual estimated value.

The difference between the reference components of the current and the actual d-q components are the inputs of the PI regulators in the inner control loop. The outputs of the PI regulators in the inner loop are two voltage components,  $V_d$  and  $V_q$ . By performing a reverse Park transformation two AC voltages are generated back on the stationary reference frame, and so the generation of the modulating signals of the DC-AC converter can be executed by the microcontroller. The block diagram of the control strategy described above is shown in [Figure 21](#). The amount of power injected into the grid depends on the power available from the PV panel. This power is then processed by the DC-DC converter which is controlled in order to maximize the energy yield from the array, independently from temperature variations and irradiation conditions, by controlling its input impedance. The control of the input impedance requires both PV array current and voltage sensing and some simple calculations executed by the well known maximum power point algorithm. The perturb & observe (P&O) method is a very common and easy way to implement an MPPT technique. The DC-DC converter duty cycle is incremented or decremented according to both array power and voltage change.

Figure 21. Block diagram of the control algorithm implemented on the 250 W MIC STM32F103xx



Apart from grid connection and MPPT, some other functions are implemented for the correct operation of the conversion system. Here below a brief description of these functions:

- Input voltage monitoring  
Input voltage value is constantly monitored to ensure that the array voltage is always in the correct operating range, between 18 V and 40 V.
- Input current monitoring  
The input current is also sampled to detect any condition of overcurrent in the system. This protection is enabled when the average input current is above 12 A.
- Bus DC voltage control  
The output of the bus DC is controlled in order to stabilize the inverter input voltage to the bus DC reference voltage. The minimum DC bus voltage is a function of the peak-to-peak AC line voltage in order to minimize the total harmonic distortion (THD) of the injected current. This limit depends on grid voltage fluctuations and can be calculated according to the following equation:

#### Equation 44

$$V_{bus\_ref\_min} = \sqrt{2} \left( V_{grid\_max} + \frac{P_{dc} * Z_c}{V_{grid\_max}} \right)$$

where  $P_{dc}$  is the average power on the DC bus,  $V_{grid\_max}$  is the maximum RMS value of the grid voltage and  $Z_c$  is the output LCL filter impedance. In other words, the DC bus must never decrease below the peak grid voltage value plus the drop across the MOSFETs and the LCL filter. To ensure safe operation, this voltage must never surpass the protection

threshold of 440 V. In the case of bus DC under/overvoltage the system is disconnected from the grid according to the strategy already described. During normal operation the DC bus is regulated at 380 V.

- **Burst mode operation at startup**

Burst mode operation is active during system startup and can also be activated for low load operation.

During burst mode operation the DC bus voltage is regulated with hysteresis control. The boundary values of the hysteresis window  $V_{b_1}$ ,  $V_{b_2}$  are chosen to limit the DC bus voltage ripple to 2% of the reference value. Once the bus capacitor is charged, the control loop mode of operation is enabled and the connection to the grid performed.

- **Line voltage and frequency detection and anti-islanding**

The PLL continuously measures the line voltage and frequency in all operating states. If the voltage or frequency exceeds the high or low limits, the inverter ceases to deliver power to the grid. These conditions are also used to implement a passive method for island operation detection. An island operation occurs when the utility power is disconnected for maintenance or fault reasons while the inverter is still delivering power. With a passive method, detection of islanding from the utility grid is achieved via AC under/overvoltage and under/over-frequency detection functions.

- **Output overcurrent**

Due to fault conditions or AC line transient conditions, the maximum current may be exceeded. In this case, the inverter ceases to deliver power to the grid. The current threshold value is set to 1.2 A.

The demonstration board is provided with the components required to implement hardware short-circuit protection. However, this protection is disabled and may be activated by properly sizing the R11 and R14 which currently have a zero Ohm value.

- **Open loop operation**

This mode of operation has been implemented to allow system debug independently from grid operation. This mode, used for maintenance, test and debug, allows system operation only with manual control by acting on a set of pushbuttons on the board. The DC-DC converter power transfer can be adjusted by acting on the duty cycle parameter through the pushbutton placed on the microcontroller board. In the same way, the power transfer of the DC-AC converter can be modified acting on the modulating index.

- **LCD display**

The microcontroller board is equipped with a graphic LCD display. The selectable functions are:

1. open loop mode;
2. closed loop mode;
3. calibration;
4. DC-DC converter manual control;
5. DC-AC converter manual control;
6. PI parameters manual regulation.

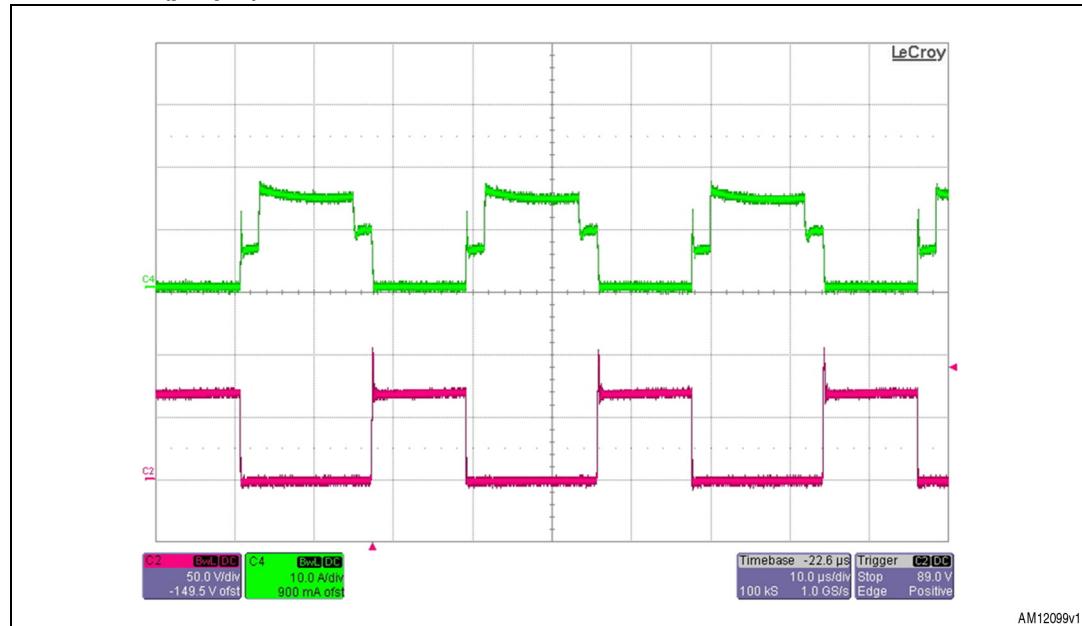
It is important to note that the calibration function must be performed by the operator when the system is first connected to the grid. In this way, any offset affecting the feedback signals used for control mode operation is compensated via firmware. When the calibration function is executed the display shows a grid current offset of about 1.7 V and a grid voltage offset of about 2.2 V.

The tuning of the PI regulators can be performed using the specific function implemented in the control algorithm. Acting on the two current regulators is very effective in order to adjust the quality of the output current both in terms of total harmonic distortion.

## 5 Experimental test results

The typical voltage and current waveforms of both the DC-DC and DC-AC converter are shown in this section. In particular, [Figure 22](#) shows the characteristic waveforms of the DC-DC converter MOSFETs, namely the drain to source MOSFET current (green track) and voltage (purple track).

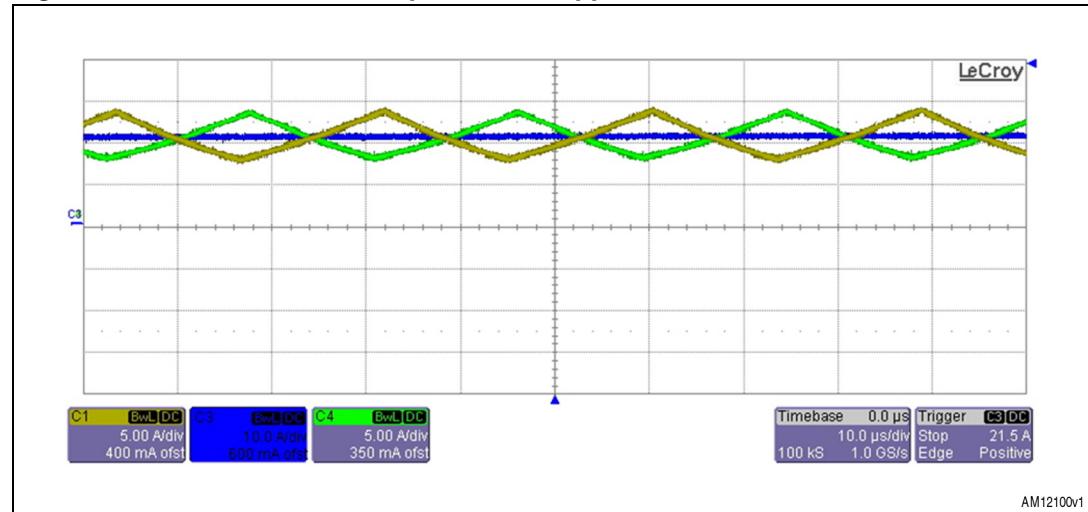
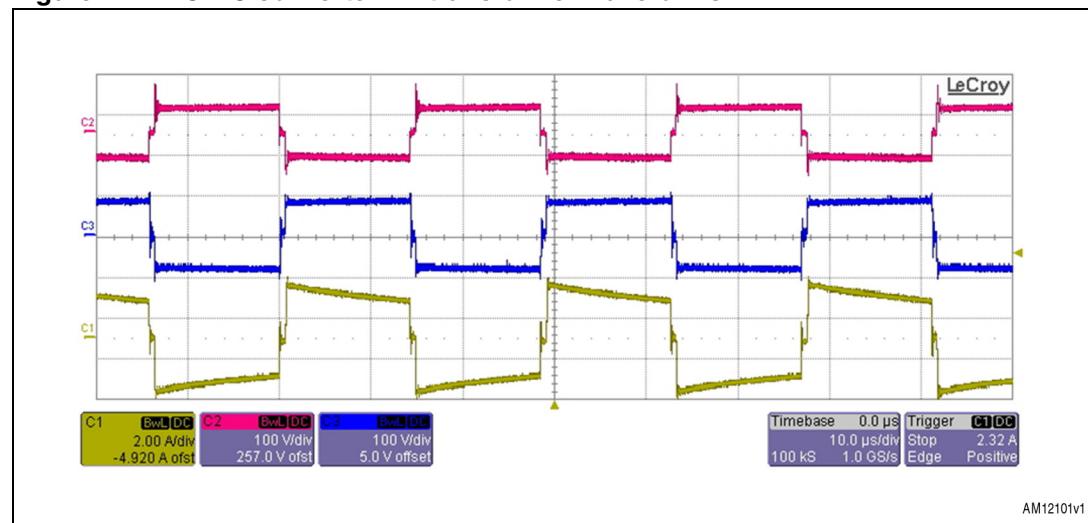
**Figure 22. DC-DC converter MOSFET current (green) and drain to source voltage (purple) @250 W**

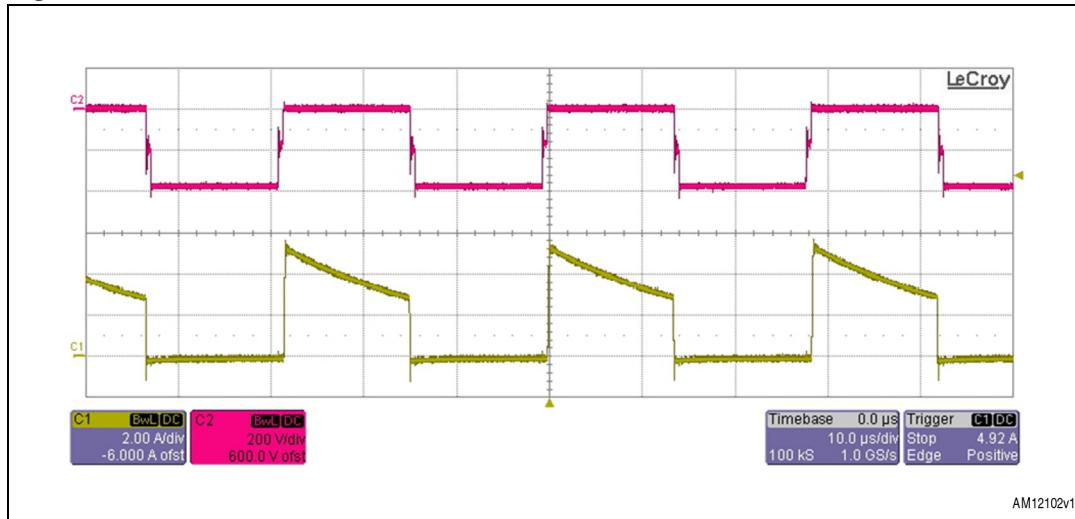
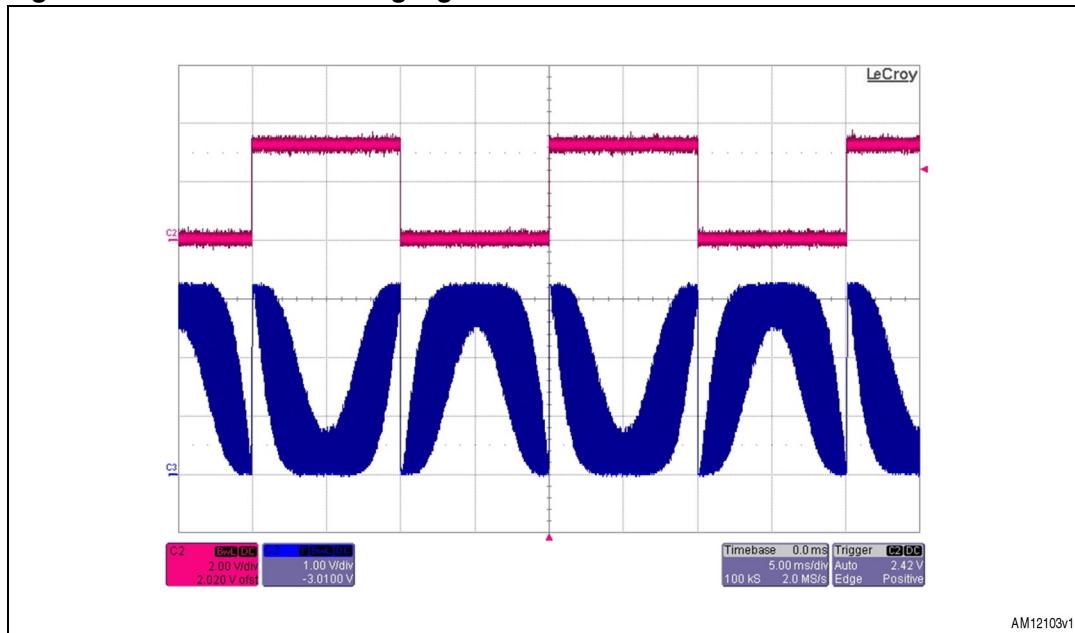


The transformer leakage inductance is the cause of the peak on the drain to source voltage at turn-off. This peak has a maximum value of 89 V, which was recorded when the microinverter was operating at 250 W of output power with an input voltage of 30 V.

[Figure 23](#) shows the current flowing through each of the two input inductors and the effect of current ripple cancellation that the interleaving has on the converter input current (blue track) when the system is operating at 30 V input and 250 W output power.

The HF transformer main waveforms are reported in [Figure 24](#), where the purple track is the transformer input voltage, the blue track is the transformer secondary voltage and the yellow track is the primary winding current. It is worth noting that the secondary voltage is only half of the total output voltage due to the presence of a voltage doubler connected downstream of the secondary winding. The current and voltage waveforms across one of the two rectifier diodes are shown in [Figure 25](#).

**Figure 23.** DC-DC converter input current ripple cancellation and inductor currents**Figure 24.** DC-DC converter HF transformer waveforms

**Figure 25.** DC-DC converter rectifier diode waveforms**Figure 26.** Inverter modulating signals

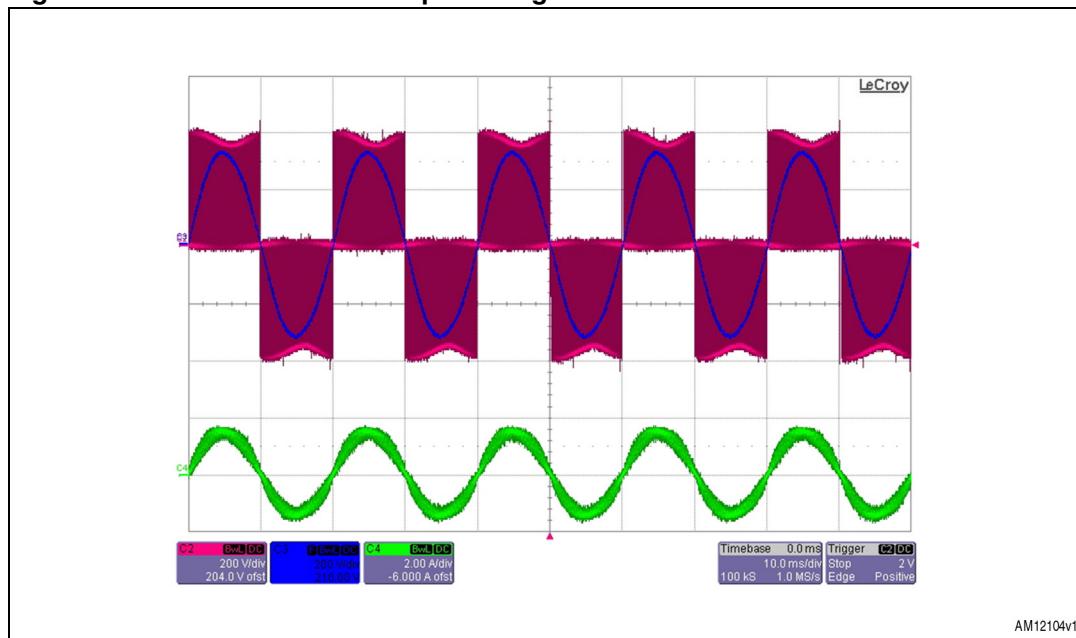
As already mentioned, the DC-AC converter has a hybrid modulation allowing one leg to switch at 17.4 kHz and one leg to switch at grid frequency. The image in [Figure 25](#) is a scope capture of the two modulating signals generated by the microcontroller and sent to the input pin of the L6390 driver. This device is then used to generate the two complementary signals controlling the gate of each STB11N65M5 MOSFET in the bridge.

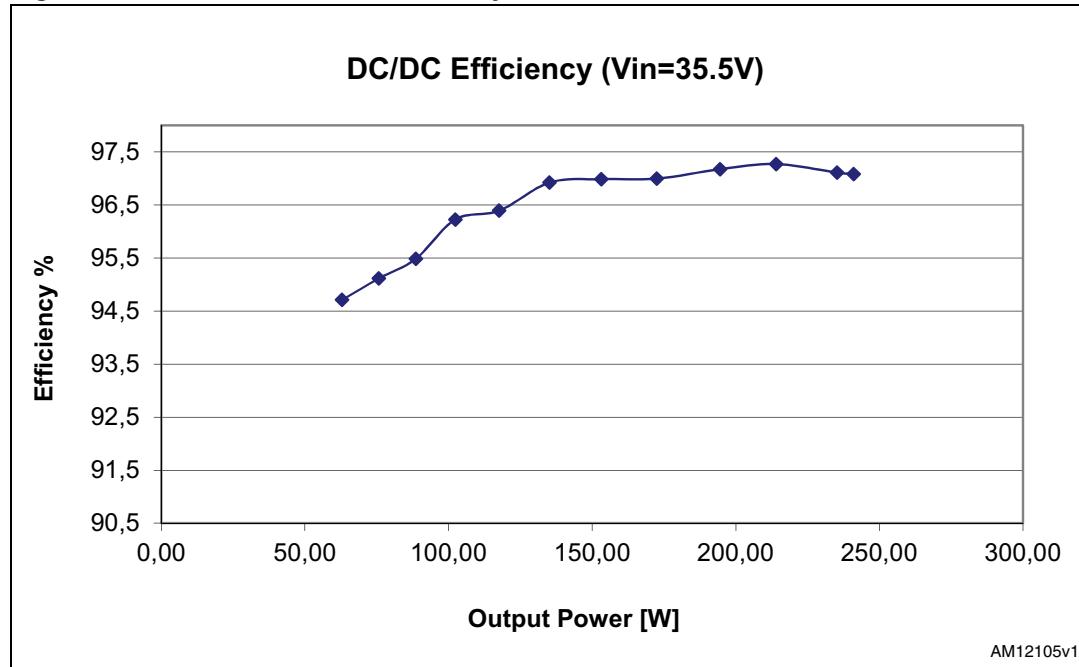
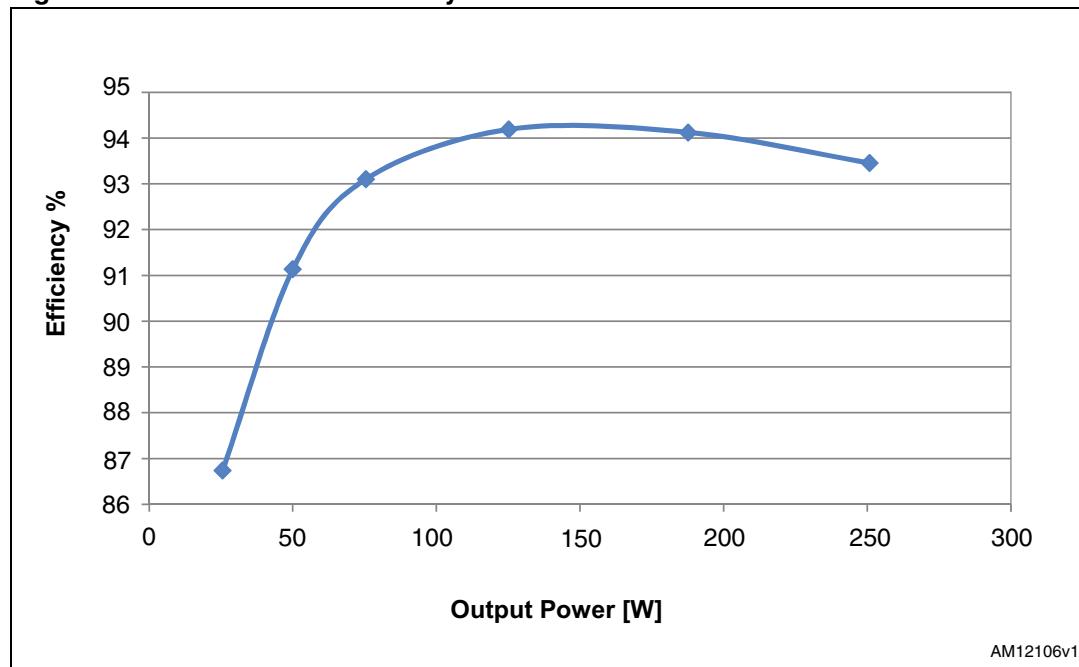
The resulting output voltage and current waveforms are shown in [Figure 27](#) where the purple track is the voltage between the mid points of each leg, the blue track is the system output voltage on the filter output and the green track is the system output current.

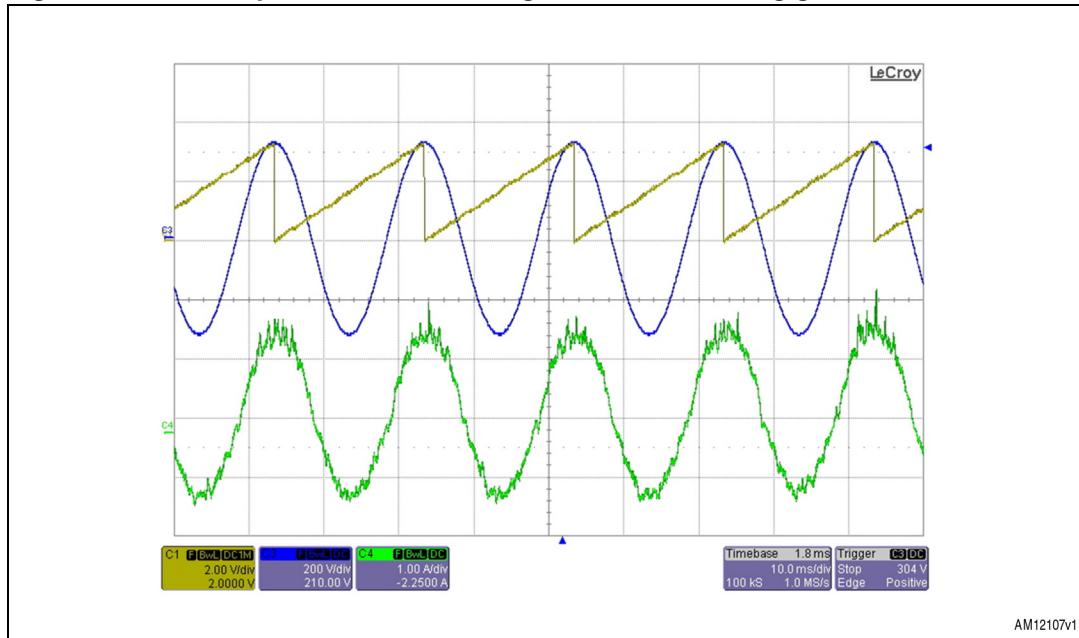
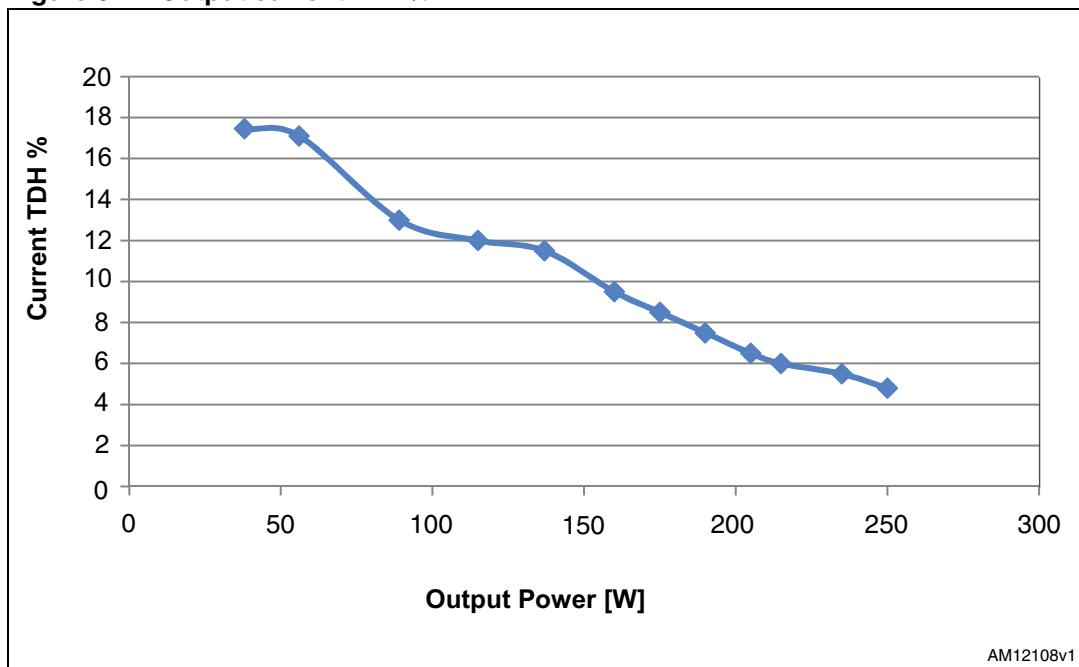
The efficiency of the system has been measured connecting the microinverter to a resistive load and adapting the ohmic value of the electrical load to the desired output power level. The open loop mode of operation allows the operating point of both the DC-DC converter

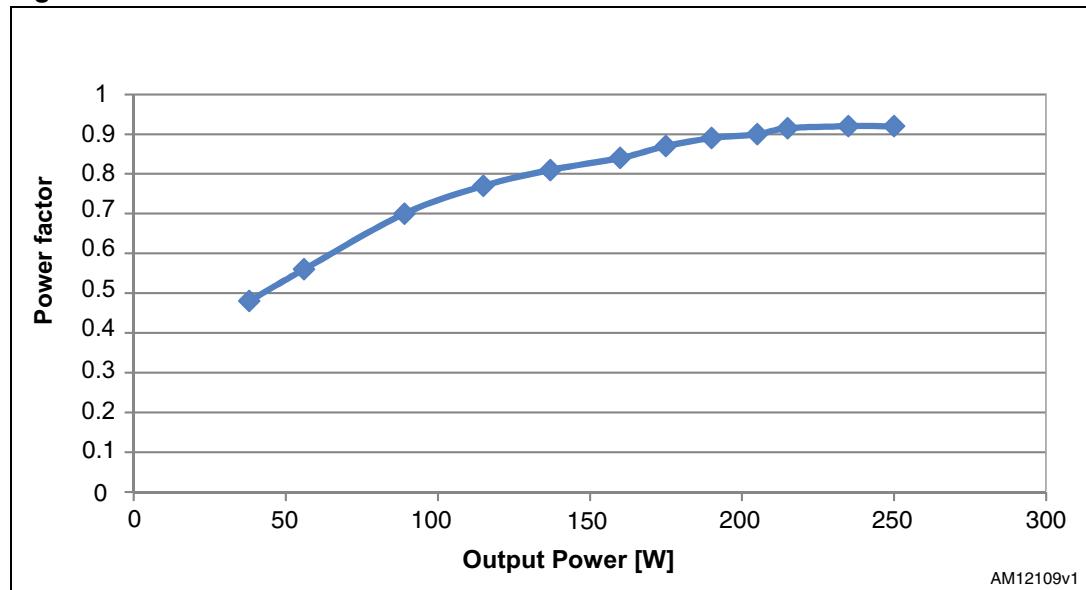
and the DC-AC converter to be adjusted by acting on the duty cycle and modulating index respectively. The duty cycle has been adjusted to obtain a DC bus voltage of 390 V and the modulating index in order to get 230 V AC on the output for each test point. The efficiency characterization of the DC-DC converter and of the system is shown in [Figure 28](#) and [29](#) respectively. The peak system efficiency is about 94% and the CEC efficiency is 93.4%. While [Figure 27](#) shows the MIC output waveforms when operating in open loop mode, [Figure 30](#) shows the same waveforms when the system is operating at nominal power in closed loop mode and grid connection. In these operating conditions the current THD is 2.8%. When operating in grid connection, the current THD is higher and equal to 4.8% at full load while the power factor is equal to 0.92. [Figure 30](#) shows the current and voltage waveforms during grid connected operation. It is worth noting that the PLL signal (yellow track) is synchronized with the peak of the grid voltage. Finally, [Figure 31](#) and [32](#) show the variation of output current THD and power factor across the operating profile of the system.

**Figure 27. DC-AC converter output voltage and current waveforms**



**Figure 28. DC-DC converter efficiency****Figure 29. Microinverter efficiency**

**Figure 30. MIC output current and voltage waveforms during grid connection****Figure 31. Output current THD%**

**Figure 32. Power factor**

## Appendix A Magnetic components datasheets

Figure 33. DC-DC boost converter inductors (part1)

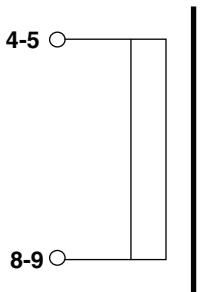
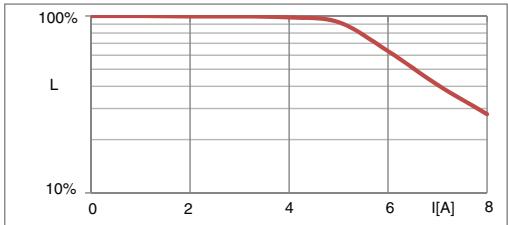
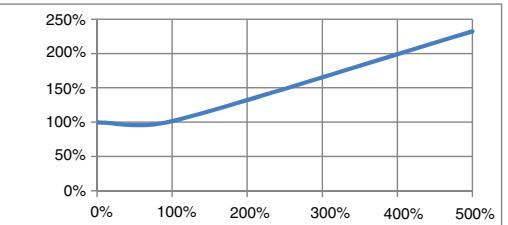
STP 04	Product Technical Specification	Code : <b>06103</b>	
<i>Product:</i> Inductor 600uH 4A		<i>Class Code:</i> <b>2162.0003</b>	
<i>Customer:</i> STMICROELECTRONICS		<i>Customer Code:</i>	
<i>Date :</i> 24.11.2010 <i>Revision:</i> 0		Page 1 of 2	
<b>TYPICAL APPLICATION</b> INDUCTOR FOR BUCK, BOOST AND BUCK-BOOST DC/DC CONVERTER, SUITABLE ALSO IN HALF-BRIDGE, PUSH-PULL AND FULL-BRIDGE APPLICATIONS		<b>TECHNICAL DATA</b>	
<b>CIRCUIT DIAGRAM</b>		<b>INDUCTANCE</b> (MEASURE 1KHZ, TA 20°C) 600 uH ±15%	
		<b>RESISTANCE</b> (MEASURE DC, TA 20°C) 81 mΩ MAX	
<b>OPERATING CURRENT</b> (MEASURE DC, TA 20°C) 4 A MAX		<b>SATURATION CURRENT</b> (MEASURE DC, L ≥ 50%NOM, TA 20°C) 6.5 A MAX	
<b>RESONANCE FREQUENCY</b> (TA 20°C) 637 KHZ NOM		<b>OPERATING TEMPERATURE RANGE</b> (IR 4A MAX) -10°C ±+65°C	
<b>THERMAL CLASS</b> B		<b>MAXIMUM DIMENSIONS</b> 35 x33 H 33 mm	
<b>WEIGHT</b> 90 g APPROX			
<b>INDUCTANCE VS CURRENT</b>		<b>INDUCTANCE VS FREQUENCY</b>	
			
<b>PIN DESCRIPTION</b>			
<i>PIN(*)</i>	<i>FUNCTION</i>	<i>PIN(*)</i>	<i>FUNCTION</i>
1	NOT CONNECTED	7	NOT CONNECTED
2		8 <sub>B</sub>	TO DRAIN MOSFET
3		9 <sub>B</sub>	NOT CONNECTED
4 <sub>A</sub>	TO VINPUT	10	
5 <sub>A</sub>		11	
6	NOT PRESENT	12	
(*)PIN WITH THE SAME SUBSCRIPT MUST BE CONNECTED TOGETHER ON PCB			
MOR&D0014-00	Rev.00	02/09/08	
	<b>MAGNETICA</b>		
			AM12160v1

Figure 34. DC-DC boost converter inductors (part2)

STP 04	Product Technical Specification	Code : <b>06103</b>
Product: Inductor 600uH 4A		Class Code: <b>2162.0003</b>
Customer: STMICROELECTRONICS		Customer Code:
Date : 24.11.2010 Revision: 0		Page 2 of 2

**DIMENSIONAL DRAWING**                                    DIMENSIONS IN MILLIMETERS, DRAWING NOT IN SCALE

35 MAX

33 MAX

33 MAX

5      7

30.5

5.1

12 11 10 9 8 7

1 2 3 4 5

Ø 0.8 (X11),  
RECOMMENDED PCB HOLE Ø 1.2 (X11)

MISSING PIN 6  
REFERENCE AS PCB ASSEMBLING

**BOTTOM VIEW (PIN SIDE)**

MOR&D0014-00

Rev.00

02/09/08

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Figure 35. AC voltage TV



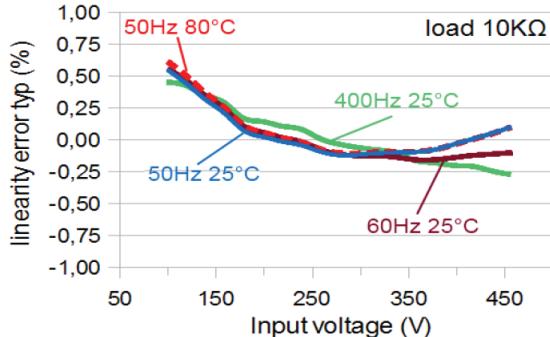
**SVL101801 - 180...440V** Voltage Measurement Transformer

- Low-cost, high precision, 50...400Hz measuring voltage transformer
- Multi output voltage level
- Max ambient temperature 80°C
- EN61558-1 and EN61558-2-6 safety requirement compliant up to 300Vac input<sup>a</sup>
- Short circuit proof on the whole permissible input voltage range
- Encapsulation in epoxy resin
- Tin-plated phosphor bronze pins



**ta80/B**  

Nominal	Input Voltage	Linearity error <sup>2</sup>		Rated Output Voltage (@nominal input)	Recommended Load	Pri/Sec Dielectric strength
Nominal	Precision range	Permissible range	Typical	Max		
400V <sup>a</sup>	180...440V	0...500V	/00.35%	/00.65%	2.5-5.0-7.5-10V	10KΩ
						5.0KV

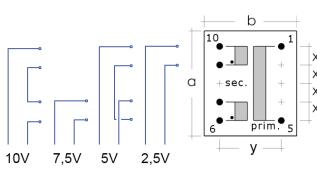


The graph shows linearity error (%) versus Input voltage (V) from 50 to 450V. Four curves are plotted: 50Hz 80°C (red), 400Hz 25°C (green), 50Hz 25°C (blue), and 60Hz 25°C (black). All curves show a minimum error around 250V.

**Dimensions mm**

a max	33.1
b max	28.6
h max	29.7
x typ	5.0
y typ	20.0

**Layout (bottom view)**



The layout diagram shows the bottom view of the transformer with dimensions a, b, and h. It includes a 10V scale bar and terminal numbers 1 through 10. Terminals 1, 2, 3, 4, 5, and 6 are labeled. A coordinate system (x, y) is shown at the bottom right.

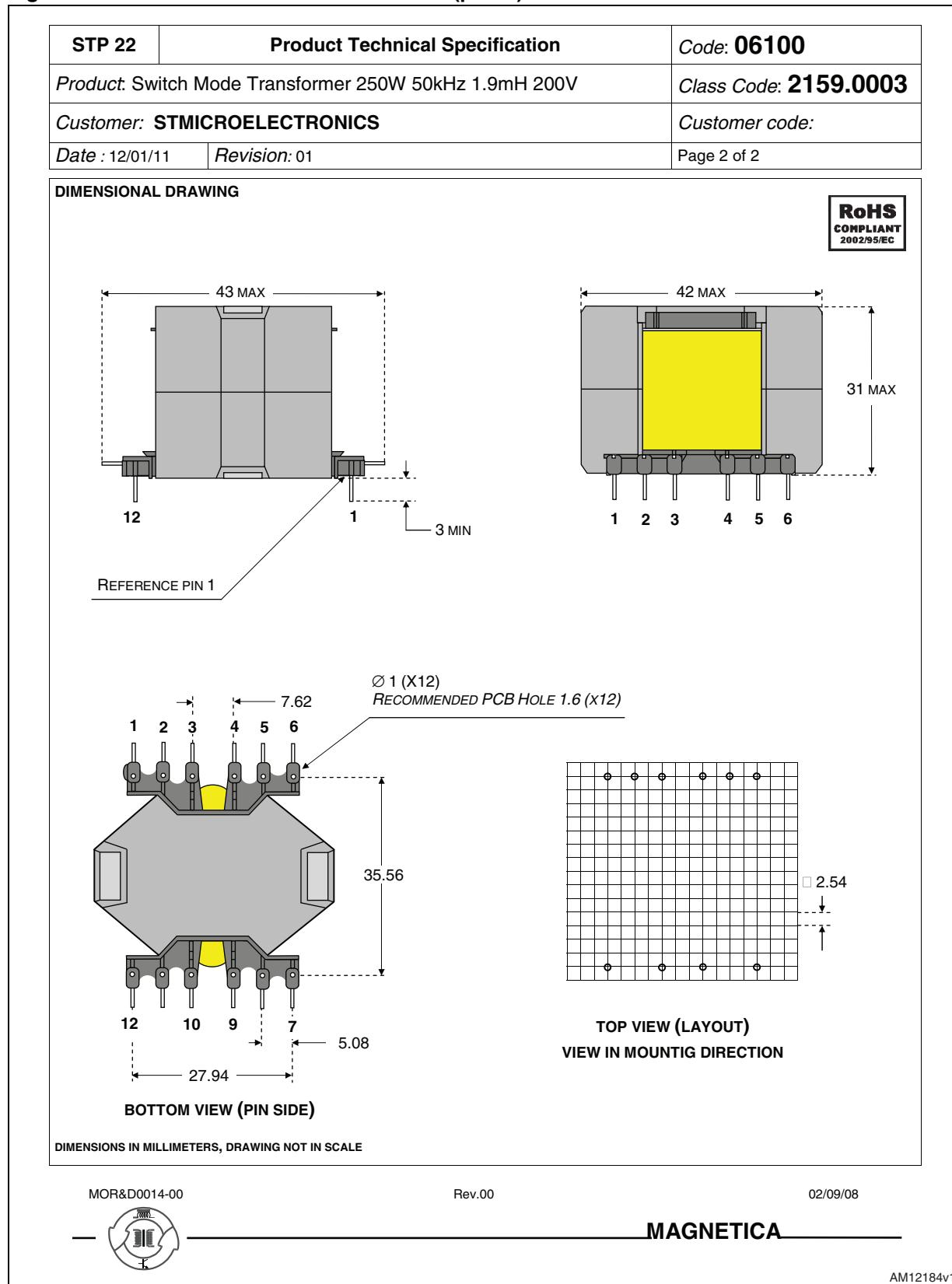
<sup>a</sup> This transformer, up to max 300Vac primary voltage, is compliant to the requirements for the inherently short-circuit proof safety transformers, as in EN61558-1 and EN61558-2-6 standard. Suitable for applications where SELV output voltage and short-circuit proof are required.  
<sup>b</sup> It can be used above 300Vac where the full compliance to EN61558-1 and EN61558-2-6 is not required.  
<sup>c</sup> 25°C ambient temperature, 50-60Hz.

AM12182v1

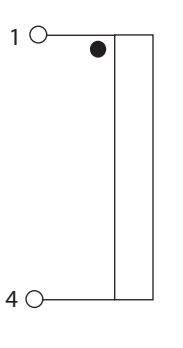
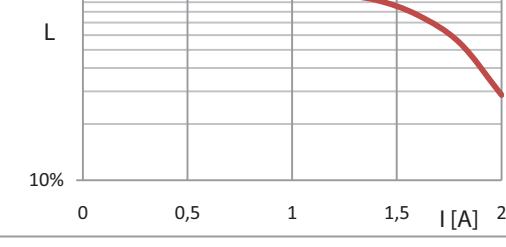
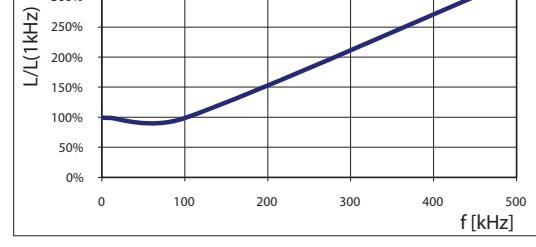
Figure 36. DC-DC converter HF transformer (part 1)

STP 22	Product Technical Specification		Code: 06100		
Product: Switch Mode Transformer 250W 50kHz 1.9mH 200V		Class Code: 2159.0003			
Customer: STMICROELECTRONICS		Customer code:			
Date : 12/01/11	Revision: 01		Page 1 of 2		
<b>TYPICAL APPLICATION</b> TRANSFORMER FOR HALF BRIDGE, PUSH-PULL AND FULL BRIDGE POWER SUPPLIES			<b>TECHNICAL DATA</b>		
<b>CIRCUIT DIAGRAM</b>			<b>INDUCTANCE</b> (MEASURE 1kHz, TA 20°C)		
			PIN 4,5,6-1,2,3      1.33 mH MIN PIN 12-10      2.4 mH MIN PIN 9-7      2.4 mH MIN		
			<b>RESISTANCE</b> (MEASURE D.C, TA 20°C)		
			PIN 4,5,6-1,2,3      25 mΩ MAX PIN 12-10      68 mΩ MAX PIN 9-7      83 mΩ MAX		
			<b>TRANSFORMER RATIO</b> (MEASURE 10kHz, TA 20°C)		
			PIN 12-10 ⇄ 4,5,6-1,2,3      1.33 ± 3% PIN 9-7 ⇄ 4,5,6-1,2,3      1.33 ± 3%		
			<b>LEAKAGE INDUCTANCE</b> 0.41 uH NOM (MEASURE 4,5,6-1,2,3 AND 7-9-10-12 IN S.C, F 10kHz, TA 20°C)		
			<b>PARASITIC CAPACITANCE</b> 13 pF NOM (MEASURE 4,5,6-1,2,3 WITH 7-9-10-12 IN OC, F 1MHz, TA 20°C)		
			<b>OPERATING CURRENT</b> 4 A <sub>p</sub> MAX (MEASURE 4,5,6-1,2,3, P <sub>MAX</sub> 250W ,F 50kHz, TA 20°C)		
			<b>OPERATING FREQUENCY</b> 50 KHz NOM (P <sub>MAX</sub> 250W , TA 20°C)		
			<b>OPERATING TEMPERATURE RANGE</b> -10°C ÷ +65°C (P <sub>MAX</sub> 250W , F 50kHz )		
			<b>THERMAL CLASS</b> B		
			<b>PRIMARY TO SECONDARY INSULATION</b> 1 kV (F 50Hz,DURATION TEST 2", TA 20°C)		
			<b>MAXIMUM DIMENSIONS</b> 43X43 H31 mm		
			<b>WEIGHT</b> 64 g APPROX		
<b>PIN DESCRIPTION</b>					
<b>PIN(*)</b>	<b>FUNCTION</b>	<b>PIN(*)</b>	<b>FUNCTION</b>		
1 <sub>A</sub>	PRIMARY DRAIN	7	SECONDARY GROUND		
2 <sub>A</sub>		8	NOT PRESENT		
3 <sub>A</sub>		9 <sub>C</sub>	SECONDARY CENTER TAP		
4 <sub>B</sub>	PRIMARY +VB 80V	10 <sub>C</sub>	SECONDARY +200V		
5 <sub>B</sub>		11	NOT PRESENT		
6 <sub>B</sub>		12	SECONDARY +200V		
(*)PIN WITH THE SAME SUBSCRIPT MUST BE CONNECTED TOGETHER ON PCB					
MOR&D0014-00	Rev.00		02/09/08		
	<b>MAGNETICA</b>				
			AM12183v1		

Figure 37. DC-DC converter HF transformer (part 2)



**Figure 38.** Inverter filter inductor (part 1)

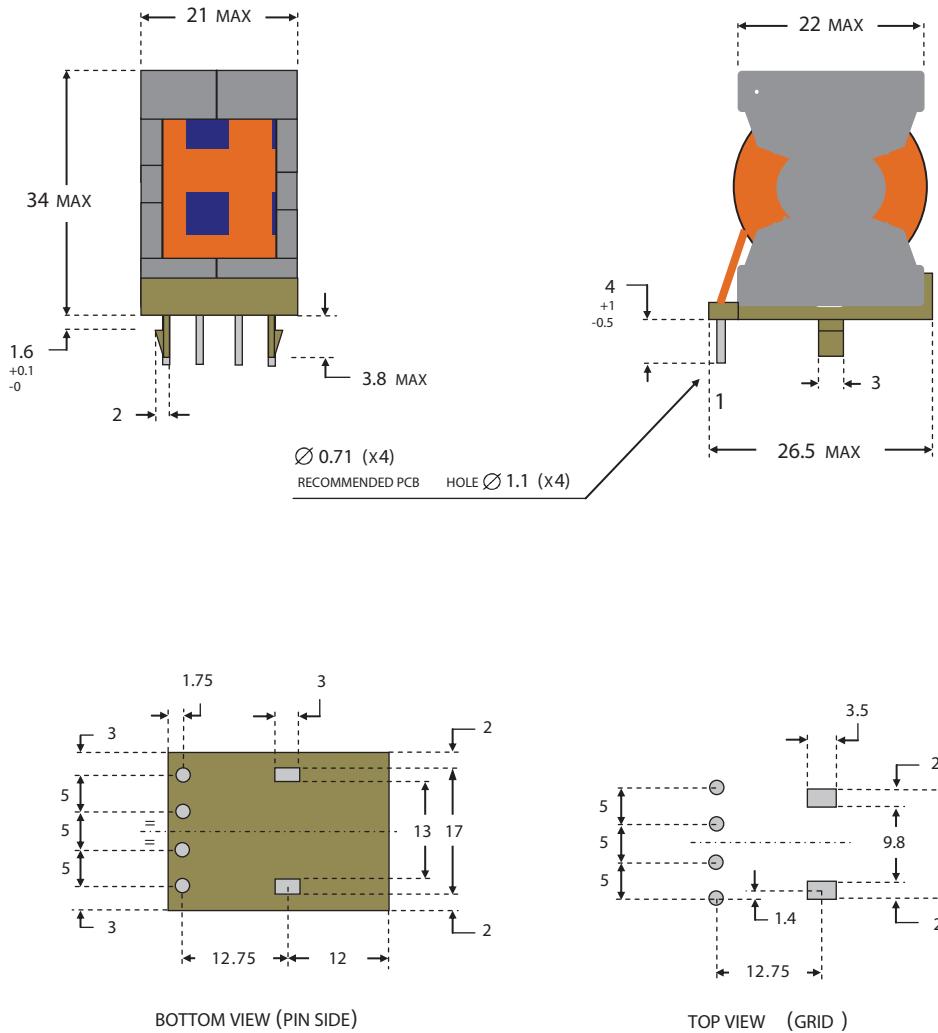
STP 04	Product Technical Specification	Code : 06272
Product: Inductor 3.6mH		Class Code: 2196.0001
Date : 24.05.2011	Revision : 0	Page 1 of 2
TYPICAL APPLICATION INDUCTOR FOR BUCK, BOOST AND BUCK-BOOST DC/DC CONVERTER, SUITABLE ALSO IN HALF-BRIDGE, PUSH-PULL AND FULL-BRIDGE APPLICATIONS		TECHNICAL DATA
CIRCUIT DIAGRAM		INDUCTANCE (MEASURE 1kHz, TA 20°C) PIN 1-4 3.6 mH ±15%
		RESISTANCE (MEASURED, TA 20°C) PIN 1-4 292 mΩ MAX
		OPERATING CURRENT (MEASURED DC, TA 20°C) 1.5 A MAX
		SATURATION CURRENT (MEASURED DC, L ≥ 50% NOM, TA 20°C) 1.77 A <sub>P</sub>
		RESONANCE FREQUENCY (TA 20°C) 589 kHz NOM
		AMBIENT TEMPERATURE RANGE (IR 1.5 A MAX, WITH SELF RISE 45°C) -20°C ÷ +85°C
		THERMAL CLASS B
		STORAGE TEMPERATURE RANGE -20°C ÷ +85°C
		MAXIMUM DIMENSIONS 21X27 H34 mm
		WEIGHT 60 g APPROX
INDUCTANCE VS CURRENT		INDUCTANCE VS FREQUENCY
		



**Figure 39. Inverter filter inductor (part 2)**

STP 04	Product Technical Specification	Code : 06272
Product: Inductor 3.6mH		Class Code: 2196.0001
Date : 24.05.2011	Revision : 0	Page 2 of 2

## DIMENSIONAL DRAWING



DIMENSIONS IN MILLIMETERS, DRAWING NOT IN SCALE



Rev.00

02/09/08

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## Appendix B Alternative DC-DC converter magnetic components with low profile

Figure 40. DC/DC inductor for 250 W microinverter

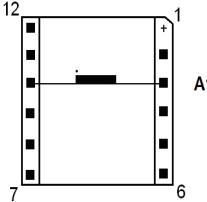
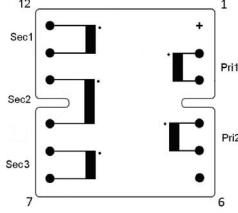
PRODUCT DATASHEET												
PRODUCT - REV	TLLPQ322001 00	DATE - REV.	25/05/12	00								
SAMPLING CODE	TLLPQ322001-220512A	CUSTOMER	ST Microelectronics									
<b>PRODUCT DESCRIPTION<sup>1</sup></b>												
DC/DC inductor for 250W microinverter												
Inductance (A1)	600uH± 5%											
DCR (A1)	118mΩ ±10%											
Saturation current	> 3.0A											
LAYOUT (BOTTOM VIEW)		DRAWING	DIMENSIONS (mm)									
			A	33,8	MAX							
			B	35,10	MAX							
			H	23,80	MAX							
			X	5,00	Typ							
			Y	30,00	Typ							
			D	0,80	Typ Ø							
			L	3,50	MIN							
All the items, except those defined "safety transformers in compliance to the European standards EN61558-1 and EN61558-2-6" in our catalogue, are supplied as a semi-finished component for specific use into electronic equipments designed by the client. Type testing and any other valuation necessary to verify the compliance of the characteristics of the transformer with the technical, safety and any other requirement have to be done by the user, before using. Each requirement and test has to be requested in writing ; without written instructions the product will be tested according to our Quality System standards.												
ST1 - ENG rev. 02 – 16/12/2011	confidential information			subject to change without notice								
1 Some data can be changed following type tests												
2 Only take into account materials actually present												
1 <sup>ST</sup> ITALIAN MANUFACTURER OF PCB TRANSFORMERS WITH ISO CERTIFIED QUALITY MANAGEMENT SYSTEM												
AM15526v1												

Figure 41. DC-DC transformer for 250 W microinverter

PRODUCT DATASHEET																																									
 <p><b>itacoil®</b> PCB INDUCTIVE COMPONENTS LOW PROFILE COUPLES</p>	PRODUCT - REV	TSLPQ322004 00	DATE - REV.	25/05/12 00																																					
	SAMPLING CODE	TSLPQ322004-220512A	CUSTOMER	ST Microelectronics																																					
PRODUCT DESCRIPTION <sup>1</sup>		DC/DC transformer for 250W microinverter																																							
Primary Inductance (P1+P2 series)	1,527mH ±28%																																								
Primary DCR (P1+P2 series)	48,5mΩ ±10%																																								
Secondary DCR (S1+S2+S3 series)	236,7" Ω ±10%																																								
Dielectric Strength (P1+P2/S1+S2+S3)	1,0KV/2sec.																																								
LAYOUT (BOTTOM VIEW)		DRAWING			DIMENSIONS (mm)																																				
					<table border="1"> <tr> <td>A</td><td>33,8</td><td>MAX</td></tr> <tr> <td>B</td><td>35,10</td><td>MAX</td></tr> <tr> <td>H</td><td>23,80</td><td>MAX</td></tr> <tr> <td>X</td><td>5,00</td><td>Typ</td></tr> <tr> <td>Y</td><td>30,00</td><td>Typ</td></tr> <tr> <td>D</td><td>0,80</td><td>Typ Ø</td></tr> <tr> <td>L</td><td>3,50</td><td>MIN</td></tr> <tr> <td></td><td></td><td></td></tr> <tr> <td></td><td></td><td></td></tr> <tr> <td></td><td></td><td></td></tr> <tr> <td></td><td></td><td></td></tr> <tr> <td></td><td></td><td></td></tr> </table>	A	33,8	MAX	B	35,10	MAX	H	23,80	MAX	X	5,00	Typ	Y	30,00	Typ	D	0,80	Typ Ø	L	3,50	MIN															
A	33,8	MAX																																							
B	35,10	MAX																																							
H	23,80	MAX																																							
X	5,00	Typ																																							
Y	30,00	Typ																																							
D	0,80	Typ Ø																																							
L	3,50	MIN																																							
COMPONENTS <sup>2</sup>		THERMAL CLASS		STANDARDS																																					
Magnet wire	T.I. 155°C (F)	IEC60172																																							
Bobbin material	T.I. 150°C (B)	UL94/V-0 - IEC 60695																																							
Insulation tape	T.I. 130°C (B)	IEC 60112																																							
Varnish	T.I. 155°C (F)																																								
All the items, except those defined "safety transformers in compliance to the European standards EN61558-1 and EN61558-2-6" in our catalogue, are supplied as a semi-finished component for specific use into electronic equipments designed by the client. Type testing and any other valuation necessary to verify the compliance of the characteristics of the transformer with the technical, safety and any other requirement have to be done by the user, before using. Each requirement and test has to be requested in writing ; without written instructions the product will be tested according to our Quality System standards.																																									
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AM15527v1																																									

## 6 Conclusions

This application note describes the design and performance of a dual stage 250 W microinverter characterized by maximum power point tracking and active and reactive power control capability. This is the main reason why the power conversion is based on a dual stage topology rather than the more common single-stage one. The converter performs MPPT and grid connection by means of an ARM Cortex-M3 based microcontroller (STM32F103xx), which is well proven to be perfectly suited for PV applications. Simulation and experimental results have confirmed the consistency of the proposed solution for single-panel PV generation systems.

## Revision history

**Table 8. Document revision history**

Date	Revision	Changes
12-Dec-2012	1	Initial release.

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