ELEC 204

Digital Design Preliminary

Lab Report

Pre Lab : 04

Name : Burhan Karahasan

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LED PING-PONG GAME

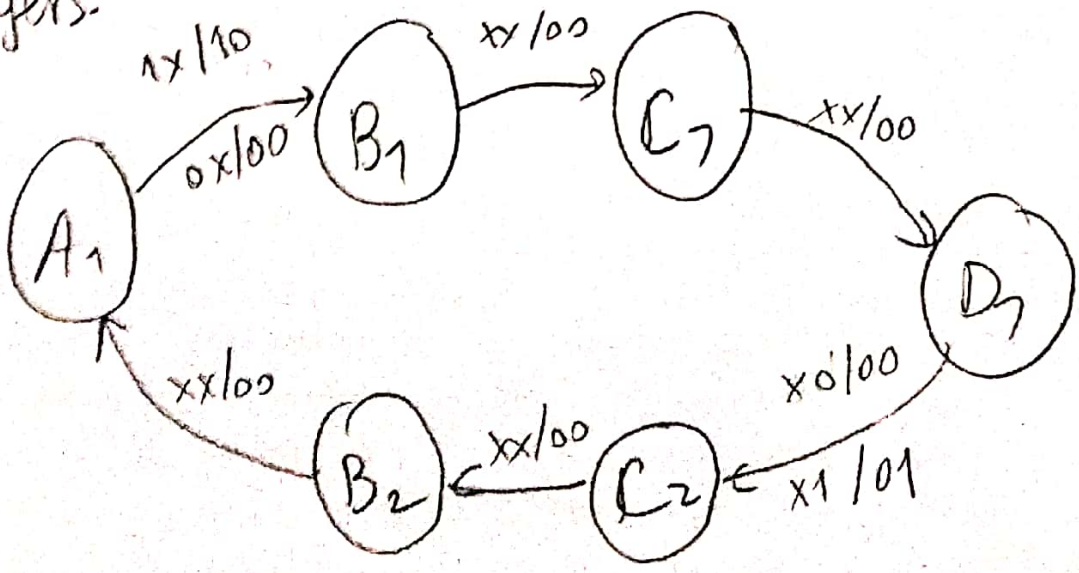
Qn.1 In the given code, there are two processes; one for clock dividing and another one demanded purpose. The clock divider process is sensitive to clock change and it increases a counter at the rising edges. When counter reaches to a previously assigned value, it causes an alternation in the output signal. In this code the clock divider decreases the frequency from 50MHz to $\frac{1}{2}$ Hz. The second process is sensitive to the alternating signal.

State Diagram

There are 4 LED outputs whose names are A, B, C and D respectively. I defined 6 different states called A_1, B_1, C_1, D_1, C_2 and B_2. Names indicate which LED is on, for example, B LED gives high when the present state is either B_1 or B_2.

I defined 2 inputs called Left and Right which are taking their values from two push buttons.

I defined two more outputs namely X and Y which represent the score earned for players.



State Table

Present State	Next State	Output (LR = 00 / 01 / 10 / 11)
A: 000001	000010	00 / 00 / 10 / 10
B_1: 000010	000100	00 / 00 / 00 / 00
C_1: 000100	001000	00 / 00 / 00 / 00
D: 001000	010000	00 / 01 / 00 / 01
C_2: 010000	100000	00 / 00 / 00 / 00
B_2: 100000	000001	00 / 00 / 00 / 00

L = Left Push
R = Right Push

X = catch for A
Y = catch for D

State Equations (D-type FF)

$D_6 = Q_6^+ = Q_5$

$D_5 = Q_5^+ = Q_4$

$D_4 = Q_4^+ = Q_3$

$D_3 = Q_3^+ = Q_2$

$D_2 = Q_2^+ = Q_1$

$D_1 = Q_1^+ = Q_6$

$X = Q_1 L$

$Y = Q_4 R$

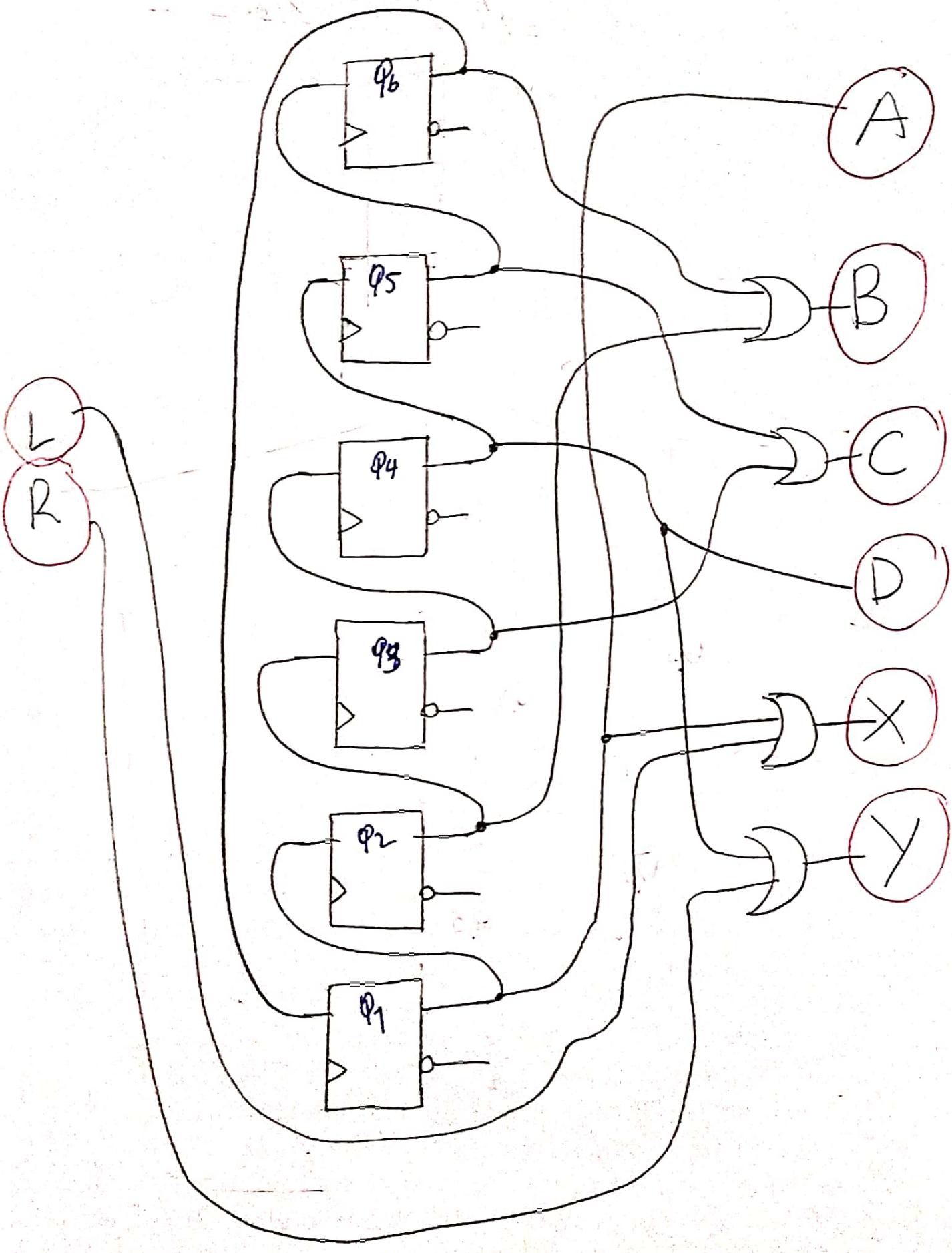
$A = Q_1$

$B = Q_2 + Q_6$

$C = Q_5 + Q_3$

$D = Q_4$

Circuit Design



Score Counter

X and Y will be the inputs of score counter component.

The circuit I use is normally a clock divider circuit whose last output gives the clock in demanded period. However, if we take all of the outputs as a vector then it becomes a binary counter clock. For the score counting purpose we define the first input as X (or Y). It utilizes 4 D type FFs.