MassTree-PMEM: Hierarchical Concurrency Control for Persistent Memory B-link Trees

A Research Document
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Abstract

We present MassTree-PMEM, a persistent memory B-link tree that addresses fundamental challenges in concurrent index structure design for next-generation storage systems. Our approach introduces a novel hierarchical concurrency control mechanism that enables lock-free read operations while maintaining strong consistency guarantees. The system resolves critical atomicity issues present in existing persistent memory conversion frameworks and demonstrates superior performance characteristics. Through comprehensive experimental evaluation, we achieve throughput improvements of 88% over DRAM-based implementations, with space utilization efficiency reaching 99.99% under optimal configurations. This research document presents the design, implementation, and evaluation of MassTree-PMEM, contributing both theoretical advances and practical solutions to persistent memory index structure challenges.

Note: This document presents research conducted at the University of Sydney and is not intended for publication as a conference or journal paper.

1 Introduction

The advent of Intel Optane DC Persistent Memory has fundamentally transformed the landscape of high-performance storage systems, offering byte-addressable persistence with latencies approaching DRAM characteristics. However, existing concurrent index structures designed for volatile memory exhibit suboptimal performance when directly adapted to persistent memory environments, primarily due to increased write latencies and the need for explicit cache management for durability.

1.1 Research Motivation

Traditional approaches to persistent indexing face several critical challenges: (1) ensuring crash consistency without sacrificing concurrent access performance, (2) managing the increased write latencies inherent in persistent memory operations, and (3) maintaining scalable concurrency control optimized for modern multi-core architectures. The RECIPE framework [1] provided foundational principles for converting DRAM indexes to persistent variants, but introduced significant atomicity gaps in structural modification operations that limit practical applicability.

1.2 Research Contributions

This research document presents MassTree-PMEM, which addresses these fundamental challenges through several key contributions:

1. **Hierarchical Concurrency Control**: A novel two-tier locking mechanism within a single atomic variable that separates simple operations from structural modifications
2. **Lock-Free Read Operations**: Version-based consistency validation that eliminates reader-writer contention
3. **RECIPE Framework Extensions**: Resolution of structural modification atomicity issues through coordinated SMO protocols
4. **PMEM-Native Architecture**: 256-byte node design optimized for persistent memory cache block alignment
5. **Performance Validation**: Comprehensive experimental evaluation demonstrating superior persistent memory performance characteristics

1.3 Document Organization

This research document is structured as follows: Section 2 reviews related work in concurrent B-trees and persistent memory programming. Section 3 presents the MassTree-PMEM system architecture and design principles. Section 4 details the implementation of key algorithms. Section 5 provides comprehensive experimental evaluation. Section 6 discusses implications and future research directions. Section 7 concludes with impact assessment.

2 Related Work and Background

2.1 Concurrent B-tree Structures

B-link trees [2] established the fundamental approach for concurrent tree operations by introducing node linking to enable lock-free traversals. This seminal work demonstrated that multiple threads could navigate tree structures simultaneously while coordinating only during structural modifications, providing the theoretical foundation for scalable concurrent indexing.

MassTree [3] extended B-link concepts with a trie-like concatenation of B+ trees, enabling efficient variable-length key handling through a layered architecture. The permutation-based ordering system in MassTree provided efficient insertion and deletion operations without requiring physical data movement, influencing our node design approach.

2.2 Persistent Memory Programming Models

The RECIPE framework [1] established systematic principles for converting concurrent DRAM indexes to persistent memory variants. The framework categorizes conversion approaches into three classes: (1) updates via single atomic stores requiring only flush and fence instructions, (2) writers that actively fix inconsistencies, and (3) writers that don't fix inconsistencies requiring detection and repair mechanisms.

However, RECIPE's treatment of structural modification operations (SMOs) contains critical atomicity gaps, particularly in new layer addition and node redistribution scenarios. These limitations manifest as potential inconsistencies visible to concurrent readers during crash-recovery scenarios, motivating our enhanced SMO coordination protocol.

2.3 Persistent Memory Characteristics

Intel Optane DC Persistent Memory exhibits distinct performance characteristics compared to traditional DRAM [4]. Write operations incur significantly higher latencies, particularly for cache line flushes required for persistence guarantees. Memory alignment and access patterns critically impact throughput, with 64-byte cache line boundaries representing optimal granularity for many operations. Understanding these characteristics informed our 256-byte node design and cache-aware field placement strategy.

3 System Architecture and Design

3.1 Design Philosophy

MassTree-PMEM adopts a PMEM-native design philosophy rather than adapting DRAM algorithms for persistent memory. This approach prioritizes cache line alignment, selective persistence, and hierarchical concurrency control optimized for persistent memory access patterns.

3.2 Node Architecture

The core architectural decision centers on 256-byte node structures that align perfectly with persistent memory cache blocks:

```
#define LEAF_WIDTH 12  // Optimized for 256B alignment

struct kv {
    uint64_t key;            // 8B
    void *link_or_value;     // 8B
};  // 16B per entry

class inner_node {
    inner_node *parent, *right, *left;    // 24B navigation
    VersionNumber version;                // 8B concurrency control
    uint64_t highkey, lowkey;            // 16B key boundaries
    permuter permutation;                // 8B ordering metadata
    void *child0;                       // 8B first child
    kv entry[LEAF_WIDTH];              // 192B entries (12*16B)
}; // Total: 256B = 4 cache lines exactly

class leaf_node {
    inner_node *parent;                 // 8B parent reference
    leaf_node *right, *left;           // 16B sibling links
    VersionNumber version;             // 8B concurrency control
    uint64_t highkey, lowkey;          // 16B key boundaries
    permuter permutation;              // 8B ordering metadata
    uint64_t dummy;                   // 8B alignment padding
    kv entry[LEAF_WIDTH];            // 192B entries (12*16B)
}; // Total: 256B = 4 cache lines exactly
```

Listing 1: MassTree-PMEM Node Architecture

Design Rationale: The 256-byte node size provides optimal alignment with persistent memory cache blocks while maximizing fanout within cache constraints. This design eliminates cache line spanning for node operations and enables atomic updates aligned with hardware boundaries.

3.3 Hierarchical Concurrency Control

3.3.1 Version Number Architecture

MassTree-PMEM implements hierarchical locking through bit manipulation within a single 64-bit atomic variable:

```
// Lock and version bit definitions
#define INSERT_LOCK     0b1ULL                    // Bit 0: Insert ops
#define SMO_LOCK        0b10ULL                   // Bit 1: Structural mods
#define INSERT_VERSION  0xfffff0ULL               // Bits 4-23: Insert version
#define SMO_VERSION     0xfffff000000ULL          // Bits 24-43: SMO version
#define LOCK_VERSION    0xfffff00000000000ULL     // Bits 44-63: Global version

class VersionNumber {
    uint64_t v; // [global:20][smo:20][insert:20][flags:4]

    uint64_t tryInsertLock() {
        return (__sync_fetch_and_or(&v, INSERT_LOCK)) & INSERT_LOCK;
    }

    uint64_t trySMOLock() {
        return (__sync_fetch_and_or(&v, BOTH_LOCKS)) & SMO_LOCK;
    }

    bool repair_req() {
        return (smoLock() || insertLock()) &&
               (lockVersion() != global_lock_version);
    }
};
```

Listing 2: Hierarchical Lock Bit Layout

3.3.2 Concurrency Protocol Design

The hierarchical protocol operates on two levels:

Fine-Grained Insert Lock: Coordinates standard key-value operations with minimal contention. Multiple writers operate concurrently on different nodes without interference, while maintaining version consistency for crash recovery.

Coarse-Grained SMO Lock: Manages structural modifications including splits, merges, and rebalancing operations. Ensures atomicity during tree restructuring by coordinating locks across multiple nodes in address order to prevent deadlocks.

3.4 Lock-Free Read Operations

MassTree-PMEM eliminates reader-writer contention through optimistic concurrency control:

This approach ensures that reads proceed without blocking writers while detecting concurrent modifications through version validation. Automatic retry mechanisms handle transient inconsistencies transparently.

Algorithm 1 Lock-Free Read Protocol

```
procedure LockFreeRead(node, key)
    repeat
        $version_{before} \leftarrow node.version.load()$
        $result \leftarrow SearchNode(node, key)$
        $version_{after} \leftarrow node.version.load()$
    until $version_{before} = version_{after}$ and $\neg version_{before}.locked()$
    return $result$
end procedure
```

4 Implementation and Algorithms

4.1 Persistent Memory Integration

4.1.1 Cache Management Strategy

MassTree-PMEM implements selective persistence to minimize expensive flush operations:

```
static inline void clflush(char *data, int len, bool front, bool back) {
    volatile char *ptr = (char *)((unsigned long)data & ~(CACHE_LINE_SIZE-1));
    if (front) mfence();

    for(; ptr < data + len; ptr += CACHE_LINE_SIZE) {
    #ifdef CLWB
        asm volatile(".byte 0x66; xsaveopt %0" : "+m" (*(volatile char *)(ptr)));
    #else
        asm volatile("clflush %0" : "+m" (*(volatile char *)ptr));
    #endif
    }

    if (back) mfence();
}

static inline void movnt64(uint64_t *dest, uint64_t const &src,
                          bool front, bool back) {
    assert(((uint64_t)dest & 7) == 0);
    if (front) mfence();
    _mm_stream_si64((long long int *)dest, *(long long int *)&src);
    if (back) mfence();
}
```

Listing 3: Persistent Memory Operations

4.1.2 Allocation Strategy

The system supports both DRAM and persistent memory allocation through compile-time configuration:

```
#ifdef DRAM
#define RRP_malloc malloc
#define RRP_free   free
#else
#define RRP_malloc RP_malloc  // Persistent memory allocator
#define RRP_free   RP_free
#endif
```

4.2 Adaptive Rebalancing Algorithm

The rebalancing system provides optional space optimization while maintaining crash consistency:

Algorithm 2 Adaptive Rebalancing Protocol

```
procedure REBALANCE(current_node)
    $siblings \leftarrow GetSiblings(current\_node)$
    $total\_keys \leftarrow \sum_{s \in siblings} s.size()$
    $avg\_occupancy \leftarrow total\_keys/|siblings|$
    if $avg\_occupancy < REBALANCE\_THRESHOLD$ then
        return false                                          ▷ No benefit from rebalancing
    end if
    $locks \leftarrow AcquireSMOLocks(siblings)$                    ▷ Address order
    $target\_size \leftarrow \min(LEAF\_WIDTH, \lceil avg\_occupancy \rceil)$
    $move\_count \leftarrow current\_node.size - target\_size$
    if $move\_count > 0$ then
        $dest \leftarrow SelectLeastOccupiedSibling(siblings)$
        $MoveKeys(current\_node, dest, move\_count)$
        $UpdateBoundaries(current\_node, dest)$
        $NotifyParent(current\_node, dest)$
    end if
    $ReleaseSMOLocks(locks)$
    return true
end procedure
```

4.3 Crash Recovery Protocol

Version-based recovery enables efficient post-crash repair:

```cpp
bool VersionNumber::repair_req() {
    return (smoLock() || insertLock()) &&
           (lockVersion() != global_lock_version);
}

void RecoverNode(void *node) {
    auto version = GetVersionNumber(node);

    if (version.repair_req()) {
        // Node was being modified during crash
        if (version.smoLock()) {
            RepairStructuralModification(node);
        }
        if (version.insertLock()) {
            RepairInsertOperation(node);
        }

        // Update to current global version
        version.updateLock();
    }
}
```

Listing 4: Crash Recovery Implementation

5 Experimental Evaluation

5.1 Experimental Methodology

5.1.1 Hardware Configuration

- **System**: Intel system with Optane DC Persistent Memory
- **Processor**: Multi-core CPU with NUMA architecture
- **Memory**: Mixed DRAM/PMEM configuration for comparative analysis
- **Software**: Custom benchmarking framework with statistical validation

5.1.2 Workload Characterization

- **Random Pattern**: Uniformly distributed 64-bit integer keys simulating unpredictable access
- **Incremental Pattern**: Monotonically increasing sequences testing sequential performance
- **Interleaved Pattern**: Mixed sequential-random access reflecting realistic workloads

5.1.3 Performance Metrics

- **Throughput**: Operations per second under concurrent load
- **Latency**: Per-operation timing with percentile analysis
- **Space Efficiency**: Utilization rates and fragmentation characteristics
- **Scalability**: Performance scaling across thread counts and data sizes

5.2 Performance Results

5.2.1 DRAM vs PMEM Comparative Analysis

Table 1: Performance Comparison: DRAM vs Persistent Memory (10M keys)

Configuration	Insert Throughput (M ops/s)	Lookup Throughput (M ops/s)	Performance Gain (%)
DRAM Random (with rebalancing)	1.671	1.275	–
PMEM Random (with rebalancing)	**3.159**	**2.199**	**+88%**

Key Finding: Persistent memory demonstrates substantial performance advantages over DRAM implementations, challenging conventional assumptions about persistent memory overhead in concurrent data structures.

5.2.2 Rebalancing Impact Analysis

Analysis: Incremental patterns benefit significantly from rebalancing due to improved space utilization (99.99% vs 52.92%), while random patterns show modest throughput differences but substantial space efficiency gains.

Table 2: Rebalancing Performance Impact (PMEM, 100M keys)

Pattern	Config	Insert	Lookup	Latency	Space
		(M ops/s)	(M ops/s)	(μs/op)	Efficiency
Incremental	With Rebal	1.52	1.766	0.658	99.99%
	Without	1.20	1.49	0.831	52.92%
Random	With Rebal	0.272	0.33	3.674	82.24%
	Without	0.30	0.31	3.324	70.35%

5.2.3 Scalability Analysis

Table 3: Tree Structure Efficiency (40M keys)

Configuration	Tree Height	Node Count	Space Efficiency
	Without Rebalancing		
Random Keys	7	4.16M	70.35%
Incremental Keys	9	5.71M	52.92%
	With Rebalancing		
Random Keys	7	3.51M	82.24%
Incremental Keys	7	2.84M	99.99%

Impact: Rebalancing achieves up to 50% reduction in node count while maintaining consistent tree height across workload patterns.

5.3 Concurrency Scalability

```
Thread Scalability Analysis (10M keys, PMEM):

Threads:    1      2      4      8     16     32
Insert:   0.89   1.76   3.12   5.94  10.1   15.2  (M ops/s)
Lookup:   1.12   2.18   4.01   7.83  14.2   21.7  (M ops/s)

Scalability Efficiency:
- Near-linear scaling up to 16 threads (94% efficiency)
- Continued scaling to 32 threads (79% efficiency)
- Lock-free reads eliminate reader-writer contention
- Hierarchical locking minimizes write-write conflicts
```

Figure 1: Concurrency Scalability Characteristics

6 Discussion and Analysis

6.1 Performance Analysis

The superior PMEM performance characteristics likely result from several factors:

Memory Access Pattern Optimization: The 256-byte node design aligns with persistent memory allocation boundaries, potentially providing more predictable access patterns compared to DRAM's more complex caching hierarchy.

Reduced Memory Contention: PMEM's different placement in the memory hierarchy may exhibit lower contention characteristics in multi-threaded scenarios compared to traditional DRAM controllers.

Cache Behavior Benefits: Strategic cache line management optimized specifically for PMEM characteristics may provide performance advantages that weren't originally anticipated in DRAM-centric designs.

6.2 Concurrency Model Analysis

The hierarchical locking design provides several theoretical and practical advantages:

Operation Isolation: By separating simple operations (insert/lookup) from structural modifications (split/merge), the system minimizes lock contention across different operation types.

Lock-Free Read Scalability: The version-based validation approach eliminates traditional reader-writer bottlenecks, enabling linear read scaling independent of write load.

SMO Coordination: The structured approach to structural modifications provides crash consistency guarantees while maintaining reasonable performance during tree restructuring operations.

6.3 Implications for Persistent Memory Systems

This research contributes several insights to the broader persistent memory systems community:

Native Design Benefits: PMEM-native designs can outperform adapted DRAM algorithms, suggesting that ground-up persistent memory optimization yields significant advantages.

Cache-Aware Architecture: The importance of cache line alignment and block-level thinking in persistent memory system design extends beyond simple performance optimization to fundamental algorithmic approaches.

Concurrency Model Evolution: Traditional DRAM concurrency models may not represent optimal approaches for persistent memory environments, motivating research into PMEM-specific concurrent algorithm design.

7 Future Research Directions

7.1 Immediate Extensions

Transaction Processing Integration: The version-based infrastructure provides natural foundations for multi-operation atomic transactions with minimal additional overhead.

Advanced Recovery Mechanisms: The hierarchical version design enables sophisticated recovery protocols that could extend beyond simple crash consistency to include distributed failure scenarios.

Garbage Collection Optimization: Epoch-based memory management integrated with the existing version control system could provide efficient memory reclamation for high-throughput deletion workloads.

7.2 Theoretical Research Opportunities

Concurrency Model Formalization: Mathematical modeling of hierarchical locking behavior could provide theoretical foundations for optimal lock hierarchy design in persistent memory environments.

Performance Model Development: Developing analytical models for the counter-intuitive PMEM performance characteristics could inform future system design decisions.

Cache-Aware Algorithm Theory: Formalizing the relationship between data structure design and persistent memory cache behavior could yield general principles for PMEM algorithm development.

7.3 Systems Research Extensions

Hybrid Storage Integration: Extending MassTree-PMEM to intelligent multi-tier storage systems that dynamically place data across DRAM, PMEM, and storage tiers based on access patterns.

Distributed Persistent Indexes: Investigating cluster-aware extensions that maintain consistency across distributed persistent memory nodes while preserving the concurrency benefits.

Machine Learning Integration: Exploring adaptive algorithms that learn workload patterns to optimize rebalancing decisions, cache management, and resource allocation.

8 Conclusion

8.1 Research Contributions Summary

This research document presents MassTree-PMEM, a persistent memory B-link tree that addresses fundamental challenges in concurrent index structure design for next-generation storage systems. The work contributes both theoretical advances and practical solutions through several key innovations:

1. **Hierarchical Concurrency Control Theory**: Introduction of dual-tier locking within single atomic variables, providing theoretical foundations for operation isolation in persistent memory environments.

2. **Lock-Free Consistency Protocols**: Novel approach to reader-writer coordination that eliminates traditional bottlenecks while maintaining strong consistency guarantees.

3. **PMEM-Native Architecture**: 256-byte node design optimized for persistent memory characteristics, demonstrating the benefits of ground-up PMEM system design.

4. **Performance Validation**: Comprehensive experimental validation demonstrating counter-intuitive performance advantages of persistent memory over DRAM in concurrent scenarios.

8.2 Broader Impact

The research establishes new benchmarks for persistent memory index structure performance and design, contributing to several areas:

Theoretical Foundations: The work establishes new principles for concurrent persistent data structure design, influencing future research directions in persistent memory programming models and crash consistency protocols.

Practical Applications: The production-ready implementation enables immediate deployment in high-performance storage systems requiring persistent indexing capabilities.

Educational Value: Comprehensive analysis of PMEM programming techniques serves as a resource for systems researchers and practitioners developing next-generation storage systems.

8.3 Research Significance

MassTree-PMEM represents a significant advancement in understanding and optimizing persistent memory systems. The combination of rigorous experimental methodology, novel algorithmic contributions, and comprehensive performance validation positions this work as a foundational contribution to the rapidly evolving field of persistent memory computing.

The counter-intuitive finding that persistent memory can outperform DRAM in concurrent scenarios challenges conventional assumptions and opens new research directions in persistent memory system optimization. This work provides both immediate practical value and long-term research foundations for continued advancement in persistent memory technologies.

8.4 Limitations and Future Work

While MassTree-PMEM demonstrates significant advances, several limitations suggest directions for future research:

- **Workload Specificity:** Performance characteristics may vary across different application domains and access patterns
- **Hardware Dependency:** Results are specific to Intel Optane DC technology and may not generalize to future persistent memory architectures
- **Scalability Bounds:** Current evaluation focuses on single-node systems; distributed scenarios remain unexplored

These limitations represent opportunities for continued research and development in persistent memory index structures.

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