PIM_9C32
Block Guide
V01.07

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Motorola, Inc.

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.00	20 AUG 2001	20 AUG 2001		Initial release of module specification in SRSv3 document format. Derived from module spec pim_9dp256.
V01.01	09 OCT 2001	09 OCT 2001		TPM replaced with PWM module, Timer extended => 16b8c, Module Routing Register MODRR added, reset values in PERS changed from %0011 to %1111
V01.02	12 OCT 2001	12 OCT 2001		- Section 1.1: Second sentence removed (related to design information) - Block Diagram updated (PW -> PWM, routing of PWM 5 removed) - Port T register naming changed (I/OCx -> IOCx) - Section "48 & 52 pin bond-out version" removed
V01.03	15 FEB 2002	15 FEB 2002		Section 3.3.1: Fuctional description changed, Table 3-3 added, Port AD: PERAD, PPSAD,RDRAD added
V01.04	26 JUL 2002	26 JUL 2002		Figure 3-39: PTIJ7, PTIJ6 replaced by PTIAD7, PTIAD6
V01.05	17 OCT 2002	17 OCT 2002		Added document number, syntax clean-up
V01.06	04 FEB 2003	04 FEB 2003		Changed end sheet, removed note on page 35
V01.07	27 OCT 2004	27 OCT 2004		Added Port AD subsection

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Section 1 Introduction

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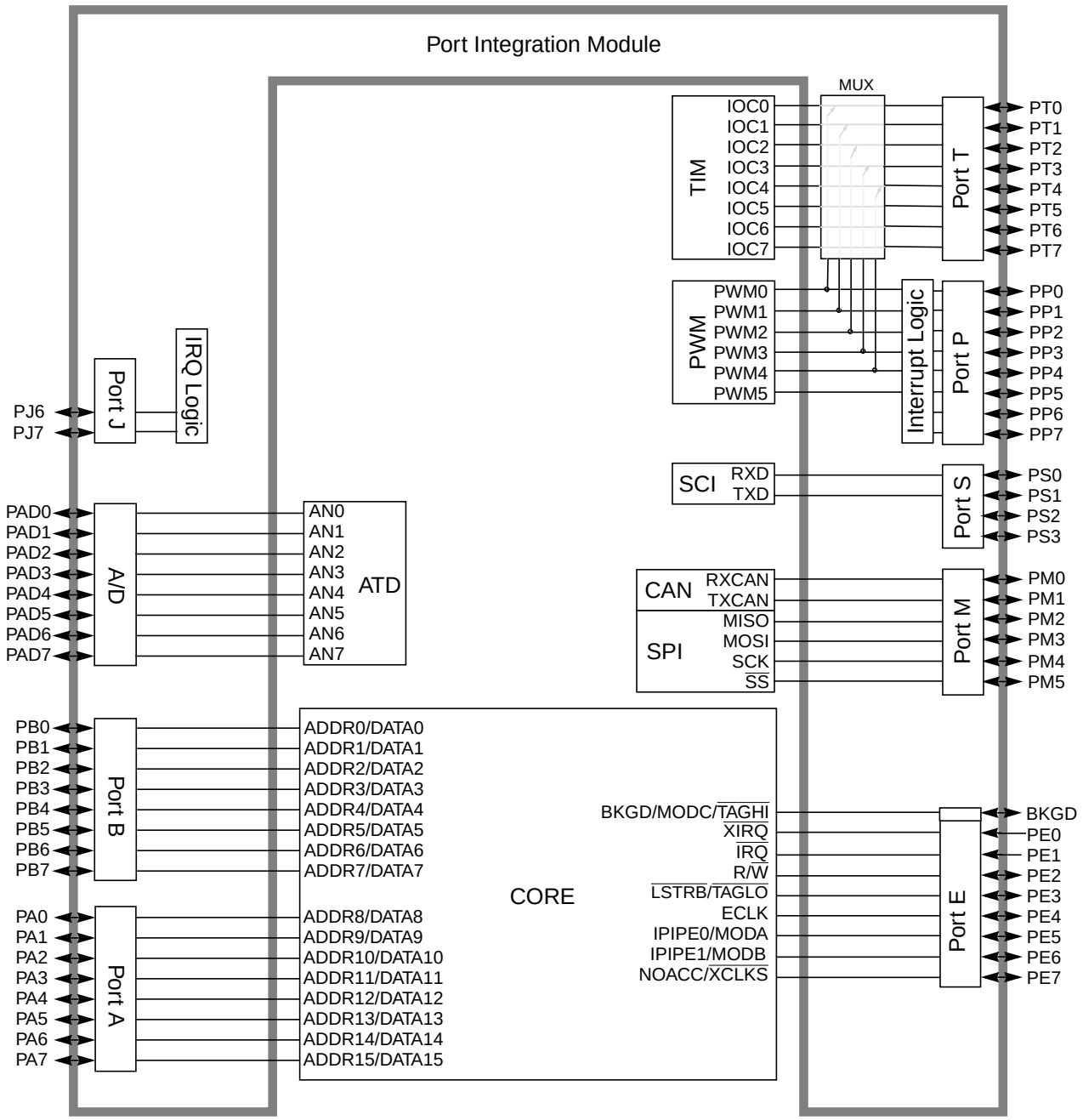

Figure 1-1 PIM_9C32 Block Diagram

1.1 Overview

The Port Integration Module establishes the interface between the peripheral modules and the I/O pins for all ports.

This section covers:

- Port A, B and E related to the core logic and the multiplexed bus interface,
- Port T connected to the TIM module (PWM module can be routed to port T as well),
- Port S connected to the SCI module,
- Port M associated to the MSCAN and SPI module,
- Port P connected to the PWM module, external interrupt sources available
- Port J pins can be used as external interrupt sources and standard I/O’s

The following I/O pin configurations can be selected:

Available on all I/O pins:

- Input/output selection
- Drive strength reduction,
- Enable and select of pull resistors,

Available on all Port P and Port J pins:

- Interrupt enable and status flags

The implementation of the Port Integration Module is device dependent.

A standard port has the following minimum features:

- Input/output selection
- 5V output drive with two selectable drive strength
- 5V digital and analog input
- Input with selectable pull-up or pull-down device

Optional features:

- Open drain for wired-or connections
- Interrupt inputs with glitch filtering

1.2 Features

A standard port has the following minimum features:

- Input/output selection
- 5V output drive with two selectable drive strength
- 5V digital and analog input
- Input with selectable pull-up or pull-down device

Optional features:

- Open drain for wired-or connections
- Interrupt inputs with glitch filtering

Section 2 External Signal Description

2.1 Overview

This section lists and describes the signals that do connect off-chip.

2.2 Signal properties

Table 2-1 shows all pins and their functions that are controlled by the PIM9C32 module. If there is more than one function associated to a pin, the priority is indicated by the position in the table from top (highest priority) to down (lowest priority).

Table 2-1 Pin Functions and Priorities

Port	Pin Name	Pin Function	Description	Pin Function after Reset
Port T	PT[7:0]	*PWM[4:0]*	*PWM outputs (only available if enabled in MODRR register)*	GPIO
		IOC[7:0]	Standard Timer Channels 7 to 0	
		GPIO	General-purpose I/O	
Port S	PS3	GPIO	General-purpose I/O	
	PS2	GPIO	General purpose I/O	
	PS1	TXD	Serial Communication Interface transmit pin	
		GPIO	General-purpose I/O	
	PS0	RXD	Serial Communication Interface receive pin	
		GPIO	General-purpose I/O	
Port M	PM5	SCK	SPI clock	
	PM4	MOSI	SPI transmit pin	
	PM3	$\overline{SS}$	SPI slave select line	
	PM2	MISO	SPI receive pin	
	PM1	TXCAN	MSCAN transmit pin	
	PM0	RXCAN	MSCAN receive pin	
Port P	PP[7:0]	PWM[5:0]	PWM outputs	
		GPIO[7:0]	General purpose I/O with interrupt	
	PP[6]	ROMON	ROMON input signal	
Port J	PJ[7:6]	GPIO	General purpose I/O with interrupt	
Port AD	PAD[7:0]	ATD[7:0]	ATD analog inputs	
		GPIO[7:0]	General purpose I/O	
Port A	PA[7:0]	ADDR[15:8]/ DATA[15:8]/ GPIO	Refer to MEBI in HCS12 Core User Guide.	
Port B	PB[7:0]	ADDR[7:0]/ DATA[7:0]/ GPIO	Refer to MEBI in HCS12 Core User Guide.	

Port	Pin Name	Pin Function	Description	Pin Function after Reset
Port E	PE7	NOACC/ $\overline{\text{XCLKS}}$/ GPIO	Refer to MEBI in HCS12 Core User Guide.	
	PE6	IPIPE1/ MODB/ GPIO		
	PE5	IPIPE0/ MODA/ GPIO		
	PE4	ECLK/GPIO		
	PE3	$\overline{\text{LSTRB}}$/ $\overline{\text{TAGLO}}$/ GPIO		
	PE2	R/$\overline{\text{W}}$/ GPIO		
	PE1	$\overline{\text{IRQ}}$/GPI		
	PE0	$\overline{\text{XIRQ}}$/GPI		

Section 3 Memory Map/Register Definition

3.1 Overview

This section provides a detailed description of all registers.

3.2 Module Memory Map

Table 3-1 shows the register map of the Port Integration Module.

Table 3-1 Module Memory Map

Address offset	Use	Access
$00	Port T I/O Register (PTT)	RW
$01	Port T Input Register (PTIT)	R
$02	Port T Data Direction Register (DDRT)	RW
$03	Port T Reduced Drive Register (RDRT)	RW
$04	Port T Pull Device Enable Register (PERT)	RW
$05	Port T Polarity Select Register (PPST)	RW
$06	Reserved	-
$07	Port T Module Routing Register (MODRR)	RW[1]
$08	Port S I/O Register (PTS)	RW[1]
$09	Port S Input Register (PTIS)	R

Table 3-1 Module Memory Map

$0A	Port S Data Direction Register (DDRS)	RW[1]
$0B	Port S Reduced Drive Register (RDRS)	RW[1]
$0C	Port S Pull Device Enable Register (PERS)	RW[1]
$0D	Port S Polarity Select Register (PPSS)	RW[1]
$0E	Port S Wired-Or Mode Register (WOMS)	RW[1]
$0F	Reserved	-
$10	Port M I/O Register (PTM)	RW[1]
$11	Port M Input Register (PTIM)	R
$12	Port M Data Direction Register (DDRM)	RW[1]
$13	Port M Reduced Drive Register (RDRM)	RW[1]
$14	Port M Pull Device Enable Register (PERM)	RW[1]
$15	Port M Polarity Select Register (PPSM)	RW[1]
$16	Port M Wired-Or Mode Register (WOMM)	RW[1]
$17	Reserved	-
$18	Port P I/O Register (PTP)	RW
$19	Port P Input Register (PTIP)	R
$1A	Port P Data Direction Register (DDRP)	RW
$1B	Port P Reduced Drive Register (RDRP)	RW
$1C	Port P Pull Device Enable Register (PERP)	RW
$1D	Port P Polarity Select Register (PPSP)	RW
$1E	Port P Interrupt Enable Register (PIEP)	RW
$1F	Port P Interrupt Flag Register (PIFP)	RW
$20-$27	Reserved	-
$28	Port J I/O Register (PTJ)	RW[1]
$29	Port J Input Register (PTIJ)	R
$2A	Port J Data Direction Register (DDRJ)	RW[1]
$2B	Port J Reduced Drive Register (RDRJ)	RW[1]
$2C	Port J Pull Device Enable Register (PERJ)	RW[1]
$2D	Port J Polarity Select Register (PPSJ)	RW[1]
$2E	Port J Interrupt Enable Register (PIEJ)	RW[1]
$2F	Port J Interrupt Flag Register (PIFJ)	RW[1]
$30	Port AD I/O Register (PTAD)	RW
$31	Port AD Input Register (PTIAD)	R
$32	Port AD Data Direction Register (DDRAD)	RW
$33	Port AD Reduced Drive Register (RDRAD)	RW
$34	Port AD Pull Device Enable Register (PERAD)	RW
$35	Port AD Polarity Select Register (PPSAD)	RW
$36-$3F	Reserved	-

NOTES:

1. Write access not applicable for one or more register bits. Please refer to detailed signal description.

3.3 Register Descriptions

The following table summarizes the effect on the various configuration bits - data direction (DDR), input / output level (I/O), reduced drive (RDR), pull enable (PE), pull select (PS) and interrupt enable (IE) for the ports. The configuration bit PS is used for two purposes:

1. Configure the sensitive interrupt edge (rising or falling), if interrupt is enabled.
2. Select either a pull-up or pull-down device if PE is active.

Table 3-2 Pin Configuration Summary

DDR	IO	RDR	PE	PS	IE[1]	Function	Pull Device	Interrupt
0	X	X	0	X	0	Input	Disabled	Disabled
0	X	X	1	0	0	Input	Pull Up	Disabled
0	X	X	1	1	0	Input	Pull Down	Disabled
0	X	X	0	0	1	Input	Disabled	falling edge
0	X	X	0	1	1	Input	Disabled	rising edge
0	X	X	1	0	1	Input	Pull Up	falling edge
0	X	X	1	1	1	Input	Pull Down	rising edge
1	0	0	X	X	0	Output, full drive to 0	Disabled	Disabled
1	1	0	X	X	0	Output, full drive to 1	Disabled	Disabled
1	0	1	X	X	0	Output, reduced drive to 0	Disabled	Disabled
1	1	1	X	X	0	Output, reduced drive to 1	Disabled	Disabled
1	0	0	X	0	1	Output, full drive to 0	Disabled	falling edge
1	1	0	X	1	1	Output, full drive to 1	Disabled	rising edge
1	0	1	X	0	1	Output, reduced drive to 0	Disabled	falling edge
1	1	1	X	1	1	Output, reduced drive to 1	Disabled	rising edge

NOTES:
1. Applicable only on ports P and J.

NOTE: *All bits of all registers in this module are completely synchronous to internal clocks during a register read.*

3.3.1 Port T Registers

Address Offset: $__00

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
TIM	IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0
PWM				*PWM4*	*PWM3*	*PWM2*	*PWM1*	*PWM0*
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-1 Port T I/O Register (PTT)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.

If a TIM-channel is defined as output, the related port T is assigned to IOC function.
In addition to the possible timer functionality of port T pins PWM channels [4:0] can be routed to port T[4:0]. For this the Module Routing Register (MODRR) needs to be configured.

Table 3-3 Port T[4:0] Pin Functionality Configurations

MODRR[x]	PWME[x]	TIMEN[x]	Port T[x] output
0	0	0	General Purpose I/O
0	0	1	Timer
0	1	0	General Purpose I/O
0	1	1	Timer
1	0	0	General Purpose I/O
1	0	1	Timer
1	1	0	PWM
1	1	1	PWM

NOTES:
1. TIMEN[x] means that the timer is enabled (TSCR1[7]), the related channel is configured for output compare function (TIOS[x] (or special output on a timer overflow event - configurable in TTOV[x][) and the timer output is routed to the port pin (TCTL1 / TCTL2).
2. All Fields they are don't shaded in grey are standard use cases.

Address Offset: $__01

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-2 Port T Input Register (PTIT)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.

Address Offset: $__02

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRT7	DDRT6	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-3 Port T Data Direction Register (DDRT)

Read:Anytime.

Write:Anytime.

This register configures each port T pin as either input or output.
The standard TIM / PWM modules forces the I/O state to be an output for each standard TIM / PWM module port associated with an enabled output compare. In these cases the data direction bits will not change.
The DDRT bits revert to controlling the I/O direction of a pin when the associated timer output compare is disabled.
The timer input capture always monitors the state of the pin.

DDRT[7:0] — Data Direction Port T
1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTT or PTIT registers, when changing the DDRT register.

Address Offset: $__03

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-4 Port T Reduced Drive Register (RDRT)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port T output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRT[7:0] — Reduced Drive Port T

1 = Associated pin drives at about 1/3 of the full drive strength.
0 = Full drive strength at output.

Address Offset: $__04

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-5 Port T Pull Device Enable Register (PERT)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

PERT[7:0] — Pull Device Enable Port T

1 = Either a pull-up or pull-down device is enabled.
0 = Pull-up or pull-down device is disabled.

Address Offset: $__05

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-6 Port T Polarity Select Register (PPST)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin.

PPST[7:0] — Pull Select Port T

1 = A pull-down device is connected to the associated port T pin, if enabled by the associated bit in register PERT and if the port is used as input.

0 = A pull-up device is connected to the associated port T pin, if enabled by the associated bit in register PERT and if the port is used as input.

Address Offset: $__07

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	MODRR4	MODRR3	MODRR2	MODRR1	MODRR0
Write:								
Reset:	-	-	-	0	0	0	0	0

= Reserved or unimplemented

Figure 3-7 Port T Module Routing Register (MODRR)

Read:Anytime.

Write:Anytime.

This register selects the module connected to port T.

MODRR[4:0] — Module Routing Register Port T

1 = Associated pin is connected to PWM module

0 = Associated pin is connected to TIM module

3.3.2 Port S Registers

Address Offset: $__08

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	PTS3	PTS2	PTS1	PTS0
Write:								
SCI	-	-	-	-	-	-	TXD	RXD
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-8 Port S I/O Register (PTS)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
The SCI port associated with transmit pin 1 is configured as output if the transmitter is enabled and the SCI pin associated with receive pin 0 is configured as input if the receiver is enabled. *Please refer to SCI Block User Guide for details*.

Address Offset: $__09

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	PTIS3	PTIS2	PTIS1	PTIS0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-9 Port S Input Register (PTIS)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This also can be used to detect overload or short circuit conditions on output pins.

Address Offset:$__0A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	DDRS3	DDRS2	DDRS1	DDRS0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-10 Port S Data Direction Register (DDRS)

Read:Anytime.

Write:Anytime.

This register configures each port S pin as either input or output.
If the associated SCI transmit or receive channel is enabled this register has no effect on the pins. The pin is forced to be an output if the SCI transmit channel is enabled, it is forced to be an input if the SCI receive channel is enabled.
The DDRS bits revert to controlling the I/O direction of a pin when the associated channel is disabled.

DDRS[3:0] — Data Direction Port S
1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTS or PTIS registers, when changing the DDRS register.

Address Offset: $__0B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	RDRS3	RDRS2	RDRS1	RDRS0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-11 Port S Reduced Drive Register (RDRS)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port S output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRS[3:0] — Reduced Drive Port S
1 = Associated pin drives at about 1/3 of the full drive strength.
0 = Full drive strength at output.

Address Offset: $__0C

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	PERS3	PERS2	PERS1	PERS0
Write:								
Reset:	0	0	0	0	1	1	1	1

= Reserved or unimplemented

Figure 3-12 Port S Pull Device Enable Register (PERS)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input or as output in wired-or (open drain) mode. This bit has no effect if the port is used as push-pull output. Out of reset a pull-up device is enabled.

PERS[3:0] — Pull Device Enable Port S

1 = Either a pull-up or pull-down device is enabled.

0 = Pull-up or pull-down device is disabled.

Address Offset: $__0D

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	PPSS3	PPSS2	PPSS1	PPSS0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-13 Port S Polarity Select Register (PPSS)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin.

PPSS[3:0] — Pull Select Port S

1 = A pull-down device is connected to the associated port S pin, if enabled by the associated bit in register PERS and if the port is used as input.

0 = A pull-up device is connected to the associated port S pin, if enabled by the associated bit in register PERS and if the port is used as input or as wired-or output.

Address Offset: $__0E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	WOMS3	WOMS2	WOMS1	WOMS0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-14 Port S Wired-Or Mode Register (WOMS)

Read:Anytime.

Write:Anytime.

This register configures the output pins as wired-or. If enabled the output is driven active low only (open-drain). A logic level of “1” is not driven. This bit has no influence on pins used as inputs.

WOMS[3:0] — Wired-Or Mode Port S

1 = Output buffers operate as open-drain outputs.

0 = Output buffers operate as push-pull outputs.

3.3.3 Port M Registers

Address Offset: $__10

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
Write:								
MSCAN/ SPI	-	-	SCK	MOSI	$\overline{SS}$	MISO	TXCAN	RXCAN
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-15 Port M I/O Register (PTM)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
The SPI pin configurations (PM[5:2]) is determined by several status bits in the SPI module. *Please refer to the SPI Block User Guide for details*.

Address Offset: $__11

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-16 Port M Input Register (PTIM)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This also can be used to detect overload or short circuit conditions on output pins.

Address Offset:$__12

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
Write:								
Reset:	-	-	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-17 Port M Data Direction Register (DDRM)

Read:Anytime.

Write:Anytime.

This register configures each port S pin as either input or output
If SPI or MSCAN is enabled, the SPI and MSCAN modules determines the pin directions. *Please refer to the SPI and MSCAN Block User Guides for details.*
If the associated SCI or MSCAN transmit or receive channels are enabled, this register has no effect on the pins. The pins are forced to be outputs if the SCI or MSCAN transmit channels are enabled, they are forced to be inputs if the SCI or MSCAN receive channels are enabled.
The DDRS bits revert to controlling the I/O direction of a pin when the associated channel is disabled.

DDRM[5:0] — Data Direction Port S
1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTM or PTIM registers, when changing the DDRM register.

Address Offset: $__13

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	RDRM5	RDRM4	RDRM3	RDRM2	RDRM1	RDRM0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-18 Port M Reduced Drive Register (RDRM)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port M output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRM[5:0] — Reduced Drive Port M

1 = Associated pin drives at about 1/3 of the full drive strength.
0 = Full drive strength at output.

Address Offset: $__14

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	PERM5	PERM4	PERM3	PERM2	PERM1	PERM0
Write:								
Reset:	0	0	1	1	1	1	1	1

= Reserved or unimplemented

Figure 3-19 Port M Pull Device Enable Register (PERM)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input or as output in wired-or (open drain) mode. This bit has no effect if the port is used as push-pull output. Out of reset a pull-up device is enabled.

PERM[5:0] — Pull Device Enable Port M

1 = Either a pull-up or pull-down device is enabled.
0 = Pull-up or pull-down device is disabled.

Address Offset: $__15

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	PPSM5	PPSM4	PPSM3	PPSM2	PPSM1	PPSM0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-20 Port M Polarity Select Register (PPSM)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin.

PPSM[5:0] — Pull Select Port M

1 = A pull-down device is connected to the associated port M pin, if enabled by the associated bit in register PERM and if the port is used as input.

0 = A pull-up device is connected to the associated port M pin, if enabled by the associated bit in register PERM and if the port is used as input or as wired-or output.

Address Offset: $__16

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	WOMM5	WOMM4	WOMM3	WOMM2	WOMM1	WOMM0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-21 Port M Wired-Or Mode Register (WOMM)

Read:Anytime.

Write:Anytime.

This register configures the output pins as wired-or. If enabled the output is driven active low only (open-drain). A logic level of “1” is not driven. This bit has no influence on pins used as inputs.

WOMM[5:0] — Wired-Or Mode Port M

1 = Output buffers operate as open-drain outputs.

0 = Output buffers operate as push-pull outputs.

3.3.4 Port P Registers

Address Offset: $__18

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
PWM	-	-	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-22 Port P I/O Register (PTP)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.

Address Offset: $__19

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIP7	PTIP6	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-23 Port P Input Register (PTIP)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can be also used to detect overload or short circuit conditions on output pins.

Address Offset: $__1A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRP7	DDRP6	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-24 Port P Data Direction Register (DDRP)

Read:Anytime.

Write:Anytime.

This register configures each port P pin as either input or output.
DDRP[7:0] — Data Direction Port P

1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTP or PTIP registers, when changing the DDRP register.

Address Offset: $__1B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRP7	RDRP6	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-25 Port P Reduced Drive Register (RDRP)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port P output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRP[7:0] — Reduced Drive Port P

1 = Associated pin drives at about 1/3 of the full drive strength.
0 = Full drive strength at output.

Address Offset: $__1C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERP7	PERP6	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-26 Port P Pull Device Enable Register (PERP)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

PERP[7:0] — Pull Device Enable Port P

1 = Either a pull-up or pull-down device is enabled.

0 = Pull-up or pull-down device is disabled.

Address Offset: $__1D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPSP7	PPSP6	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSP0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-27 Port P Polarity Select Register (PPSP)

Read:Anytime.

Write:Anytime.

This register serves a dual purpose by selecting the polarity of the active interrupt edge as well as selecting a pull-up or pull-down device if enabled.

PPSP[7:0] — Pull Select Port P

1 = Rising edge on the associated port P pin sets the associated flag bit in the PIFP register.A pull-down device is connected to the associated port P pin, if enabled by the associated bit in register PERP and if the port is used as input.

0 = Falling edge on the associated port P pin sets the associated flag bit in the PIFP register.A pull-up device is connected to the associated port P pin, if enabled by the associated bit in register PERP and if the port is used as input.

Address Offset: $__1E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PIEP7	PIEP6	PIEP5	PIEP4	PIEP3	PIEP2	PIEP1	PIEP0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-28 Port P Interrupt Enable Register (PIEP)

Read:Anytime.

Write:Anytime.

This register disables or enables on a per pin basis the edge sensitive external interrupt associated with port P.

PIEP[7:0] — Interrupt Enable Port P
1 = Interrupt is enabled.
0 = Interrupt is disabled (interrupt flag masked).

Address Offset: $__1F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PIFP7	PIFP6	PIFP5	PIFP4	PIFP3	PIFP2	PIFP1	PIFP0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-29 Port P Interrupt Flag Register (PIFP)

Read:Anytime.

Write:Anytime.

Each flag is set by an active edge on the associated input pin. This could be a rising or a falling edge based on the state of the PPSP register. To clear this flag, write a “1” to the corresponding bit in the PIFP register. Writing a “0” has no effect.

PIFP[7:0] — Interrupt Flags Port P
1 = Active edge on the associated bit has occurred (an interrupt will occur if the associated enable bit is set).
Writing a “1” clears the associated flag.
0 = No active edge pending.
Writing a “0” has no effect.

3.3.5 Port J Registers

Address Offset: $__28

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTJ7	PTJ6	0	0	0	0	0	0
Write:								
Reset:	0	0	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-30 Port J I/O Register (PTJ)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.

Address Offset: $__29

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIJ7	PTIJ6	0	0	0	0	0	0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-31 Port J Input Register (PTIJ)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can be used to detect overload or short circuit conditions on output pins.

Address Offset: $__2A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	DDRJ7	DDRJ6	0	0	0	0	0	0
Write:								
Reset:	0	0	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-32 Port J Data Direction Register (DDRJ)

Read:Anytime.

Write:Anytime.

This register configures port pins J[7:6] as either input or output.
DDRJ[7:6] — Data Direction Port J

1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTJ or PTIJ registers, when changing the DDRJ register.

Address Offset: $__2B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	RDRJ7	RDRJ6	0	0	0	0	0	0
Write:								
Reset:	0	0	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-33 Port J Reduced Drive Register (RDRJ)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port J output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRJ[7:6] — Reduced Drive Port J

1 = Associated pin drives at about 1/3 of the full drive strength.
0 = Full drive strength at output.

Address Offset: $__2C

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PERJ7	PERJ6	0	0	0	0	0	0
Write:								
Reset:	0	0	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-34 Port J Pull Device Enable Register (PERJ)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input or as wired-or output. This bit has no effect if the port is used as push-pull output.

PERJ[7:6] — Pull Device Enable Port J

1 = Either a pull-up or pull-down device is enabled.
0 = Pull-up or pull-down device is disabled.

Address Offset: $__2D

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PPSJ7	PPSJ6	0	0	0	0	0	0
Write:								
Reset:	0	0	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-35 Port J Polarity Select Register (PPSJ)

Read:Anytime.

Write:Anytime.

This register serves a dual purpose by selecting the polarity of the active interrupt edge as well as selecting a pull-up or pull-down device if enabled.

PPSJ[7:6] — Polarity Select Port J

1 = Rising edge on the associated port J pin sets the associated flag bit in the PIFJ register. A pull-down device is connected to the associated port J pin, if enabled by the associated bit in register PERJ and if the port is used as input.

0 = Falling edge on the associated port J pin sets the associated flag bit in the PIFJ register. A pull-up device is connected to the associated port J pin, if enabled by the associated bit in register PERJ and if the port is used as general purpose input.

Address Offset: $__2E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PIEJ7	PIEJ6	0	0	0	0	0	0
Write:								
Reset:	0	0	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-36 Port J Interrupt Enable Register (PIEJ)

Read:Anytime.

Write:Anytime.

This register disables or enables on a per pin basis the edge sensitive external interrupt associated with port J.

PIEJ[7:6] — Interrupt Enable Port J

1 = Interrupt is enabled.

0 = Interrupt is disabled (interrupt flag masked).

Address Offset: $__2F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PIFJ7	PIFJ6	0	0	0	0	0	0
Write:								
Reset:	0	0	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-37 Port J Interrupt Flag Register (PIFJ)

Read:Anytime.

Write:Anytime.

Each flag is set by an active edge on the associated input pin. This could be a rising or a falling edge based on the state of the PPSJ register. To clear this flag, write “1” to the corresponding bit in the PIFJ register. Writing a “0” has no effect.

PIFJ[7:6] — Interrupt Flags Port J

1 = Active edge on the associated bit has occurred (an interrupt will occur if the associated enable bit is set).
Writing a “1” clears the associated flag.

0 = No active edge pending.
Writing a “0” has no effect.

3.3.6 Port AD Registers

Address Offset: $__30

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTAD7	PTAD6	PTAD5	PTAD4	PTAD3	PTAD2	PTAD1	PTAD0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-38 Port AD I/O Register (PTAD)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.

Address Offset: $__31

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIAD7	PTIAD6	PTIAD5	PTIAD4	PTIAD3	PTIAD2	PTIAD1	PTIAD0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-39 Port AD Input Register (PTIAD)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can be used to detect overload or short circuit conditions on output pins.

Address Offset: $__32

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRAD7	DDRAD6	DDRAD5	DDRAD4	DDRAD3	DDRAD2	DDRAD1	DDRAD0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-40 Port AD Data Direction Register (DDRAD)

Read:Anytime.

Write:Anytime.

This register configures port pins AD[7:0] as either input or output.
DDRAD[7:0] — Data Direction Port AD

1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTAD or PTIAD registers, when changing the DDRAD register.

Address Offset: $__33

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRAD7	RDRAD6	RDRAD5	RDRAD4	RDRAD3	RDRAD2	RDRAD1	RDRAD0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-41 Port AD Reduced Drive Register (RDRAD)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port AD output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRAD[7:0] — Reduced Drive Port AD

1 = Associated pin drives at about 1/3 of the full drive strength.
0 = Full drive strength at output.

Address Offset: $__34

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERAD7	PERAD6	PERAD5	PERAD4	PERAD3	PERAD2	PERAD1	PERAD0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-42 Port AD Pull Device Enable Register (PERAD)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.
It is not possible to enable pull devices when a associated ATD channel is enabled simultaneously.

PERAD[7:0] — Pull Device Enable Port AD

1 = Either a pull-up or pull-down device is enabled.
0 = Pull-up or pull-down device is disabled.

Address Offset: $__35

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPSAD7	PPSAD6	PPSAD5	PPSAD4	PPSAD3	PPSAD2	PPSAD1	PPSAD0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-43 Port AD Polarity Select Register (PPSAD)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin.

PPSAD[7:0] — Pull Select Port AD

1 = A pull-down device is connected to the associated port AD pin, if enabled by the associated bit in register PERAD and if the port is used as input.

0 = A pull-up device is connected to the associated port AD pin, if enabled by the associated bit in register PERAD and if the port is used as input.

Section 4 Functional Description

4.1 General

Each pin can act as general purpose I/O. In addition the pin can act as an output from a peripheral module or an input to a peripheral module.

A set of configuration registers is common to all ports. All registers can be written at any time, however a specific configuration might not become active.

Example:

Selecting a pull-up resistor. This resistor does not become active while the port is used as a push-pull output.

4.1.1 I/O register

This register holds the value driven out to the pin if the port is used as a general purpose I/O.

Writing to this register has only an effect on the pin if the port is used as general purpose output. When reading this address, the value of the pins are returned if the data direction register bits are set to 0.

If the data direction register bits are set to 1, the contents of the I/O register is returned. This is independent of any other configuration (**Figure 4-1**).

4.1.2 Input register

This is a read-only register and always returns the value of the pin (**Figure 4-1**).

4.1.3 Data direction register

This register defines whether the pin is used as an input or an output.

If a peripheral module controls the pin the contents of the data direction register is ignored (**Figure 4-1**).

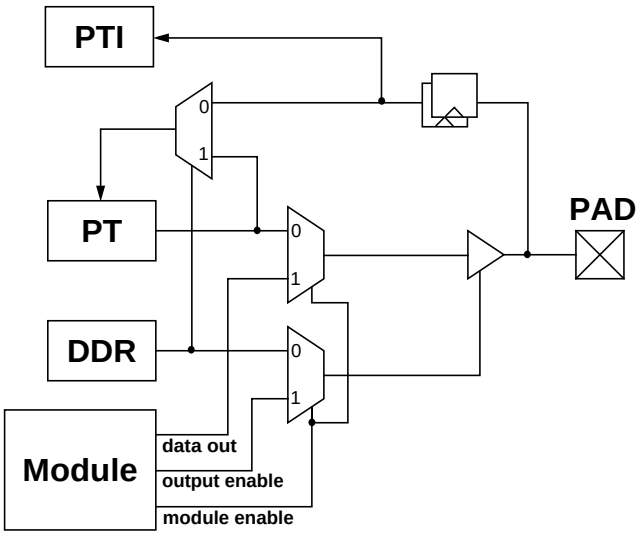

Figure 4-1 Illustration of I/O pin functionality

4.1.4 Reduced drive register

If the port is used as an output the register allows the configuration of the drive strength.

4.1.5 Pull device enable register

This register turns on a pull-up or pull-down device.

It becomes only active if the pin is used as an input or as a wired-or output.

4.1.6 Polarity select register

This register selects either a pull-up or pull-down device if enabled.

It becomes only active if the pin is used as an input. A pull-up device can be activated if the pin is used as a wired-or output.

4.2 Port T

This port is associated with the Standard Capture Timer. Port pins P[4:0] can be routed for PWM output on port T to port pins T[4:0].

In all modes, port T pins PT[7:0] can be used for either general-purpose I/O, Standard Capture Timer I/O or with the channels [4:0] of the PWM module, if enabled in MODRR.

During reset, port T pins are configured as high-impedance inputs.

4.3 Port S

This port is associated with the serial SCI module.

Port S pins PS[3:0] can be used either for general-purpose I/O, or with the SCI subsystem.

During reset, port S pins are configured as inputs with pull-up.

4.4 Port M

This port is associated with the MSCAN and SPI module.

Port M pins PM[5:0] can be used either for general-purpose I/O, with the MSCAN or SPI subsystems.

During reset, port M pins are configured as inputs with pull-up.

4.5 Port AD

This port is associated with the ATD module.

Port AD pins can be used either for general-purpose I/O, or for the ATD subsystem.

To use PortAD[n] as a standard input, the corresponding ATDDIEN[n] must be set. PortAD[n] can be used as a standard output independent of ATDDIEN[n]. *Please refer to ATD Block Guide for details.*

4.6 Port P

The PWM module is connected to port P.

Port P pins PP[5:0] can be used as PWM outputs. Further the Keypad Wake-Up function is implemented on pins P[7:0].

During reset, port P pins are configured as high-impedance inputs.

Port P offers 8 general purpose I/O pins with edge triggered interrupt capability in wired-or fashion. The interrupt enable as well as the sensitivity to rising or falling edges can be individually configured on per pin basis. All 8 bits/pins share the same interrupt vector. Interrupts can be used with the pins configured as inputs or outputs.

An interrupt is generated when a bit in the port interrupt flag register and its corresponding port interrupt enable bit are both set. This external interrupt feature is capable to wake up the CPU when it is in STOP or WAIT mode.

A digital filter on each pin prevents pulses (**Figure 4-3**) shorter than a specified time from generating an interrupt. The minimum time varies over process conditions, temperature and voltage (**Figure 4-2** and **Table 4-1**).

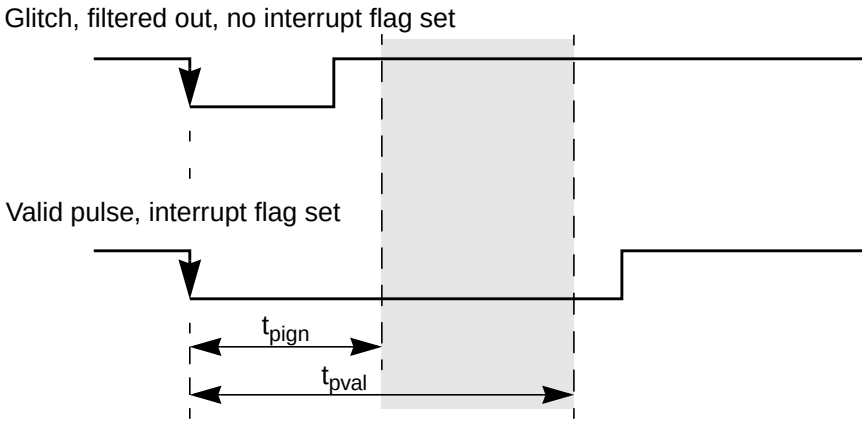

Figure 4-2 Interrupt Glitch Filter on Port P and J (PPS=0)

Table 4-1 Pulse Detection Criteria

Pulse	Mode			
	$\overline{STOP}$		STOP[1]	
		Unit		Unit
Ignored	t_{pign} <= 3	bus clocks	t_{pign} <= 3.2	µs
Uncertain	3 < t_{pulse} < 4	bus clocks	3.2 < t_{pulse} < 10	µs
Valid	t_{pval} >= 4	bus clocks	t_{pval} >= 10	µs

NOTES:
1. These values include the spread of the oscillator frequency over temperature, voltage and process.

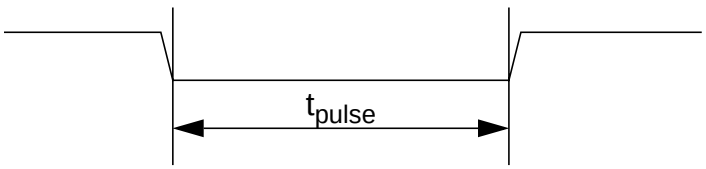

Figure 4-3 Pulse Illustration

A valid edge on input is detected if 4 consecutive samples of a passive level are followed by 4 consecutive samples of an active level directly or indirectly.

The filters are continuously clocked by the bus clock in RUN and WAIT mode. In STOP mode the clock is generated by a single RC oscillator in the Port Integration Module. To maximize current saving the RC oscillator runs only if the following condition is true on any pin:

Sample count <= 4 and port interrupt enabled (PIE=1) and port interrupt flag not set (PIF=0).

4.7 Port J

In all modes, port J pins PJ[7:6] can be used for general purpose I/O or interrupt driven general purpose I/O's. During reset, port J pins are configured as inputs.

Port J offers 2 I/O ports with the same interrupt features as on port P.

4.8 Port A, B, E and BKGD pin

All port and pin logic is located in the core module. Please *refer to S12_mebi Block User Guide for details.*

4.9 External Pin Descriptions

All ports start up as general purpose inputs on reset.

4.10 Low Power Options

4.10.1 Run Mode

No low power options exist for this module in run mode.

4.10.2 Wait Mode

No low power options exist for this module in wait mode.

4.10.3 Stop Mode

All clocks are stopped. There are asynchronous paths to generate interrupts from STOP on port P and J.

Section 5 Initialization/Application Information

5.1 General

The reset values of all registers are given in section **3.3. Register Descriptions**.

5.2 Reset Initialization

All registers including the data registers get set/reset asynchronously. **Table 5-1** summarizes the port properties after reset initialization.

Table 5-1 Port Reset State Summary

Port	Reset States				
	Data Direction	Pull Mode	Red. Drive	Wired-Or Mode	Inter-rupt
T	input	hiz	disabled	n/a	n/a
S	input	pull-up	disabled	disabled	n/a
M	input	pull-up	disabled	disabled	n/a
P	input	hiz	disabled	n/a	disabled
J	input	hiz	disabled	n/a	disabled
A	Refer to MEBI in HCS12 Core User Guide for details.				
B					
E					
BKGD pin	Refer to BDM in HCS12 Core User Guide for details.				

Section 6 Interrupts

6.1 General

Port P and J generate a separate edge sensitive interrupt if enabled.

6.2 Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Port P	PIFP[7:0]	PIEP[7:0]	I Bit
Port J	PIFJ[7:6]	PIEJ[7:6]	I Bit

Table 6-1 Port Integration Module Interrupt Sources

NOTE: *Vector addresses and their relative interrupt priority are determined at the MCU level.*

6.3 Recovery from STOP

The PIM_9C32 can generate wake-up interrupts from STOP on port P and J. For other sources of external interrupts please refer to the respective Block User Guide.

User Guide End Sheet

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