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CSCI 355
Fall Term
Digital Logic and Computer Organization

Lab #8
Synchronous Sequential Circuits

Date Due: Saturday, November ~~23~~ 30, 11:59 PM **Total Marks: 32**

General Instructions

- **This lab assignment is individual work. You may discuss questions and problems with anyone, but the work you hand in for this assignment must be your own work. Put your name, student number and instructor's name on the cover page of your report. Failure to follow these conventions will result in a deduction of grades for you. Do not submit folders, zip documents, even if you think it will help.**
- **Assignments must be submitted to VIULearn.**
- **VIULearn will not let you submit work after the assignment deadline. It is advisable to hand in each answer that you are happy with as you go. You can always revise and resubmit as many times as you like before the deadline; only your most recent submission will be graded.**
- **Partial credit will be given as appropriate, so hand in all attempts.**

1. Objectives

i. Implement behavioral Verilog HDL to realize Finite State Machine.

ii. Design Moore-type and Mealy-type machines using Verilog HDL

iii. Interpret waveforms generated with various input/output signals

2. Health and Safety

Any laboratory environment may contain conditions that are potentially hazardous to a person's health if not handled appropriately. Watch for posted information in and around the laboratories, and on the class website.
https://adm.viu.ca/sites/default/files/viu_safety_design_for_facilities_standard_draft.pdf

3. Background

Chapter 6, "Sequential Circuit/ Finite State Machine", from the lecture slides—Week 10 and Week 11.

4. Pre-Lab Tasks

2 Compare Moore and Mealy model (in terms of advantages and disadvantages).

5. Equipment Required

Cub machines running Linux

6. Lab Procedure

6.1 Simple Moore Module

7 Write the behavioral **Verilog code** for a Moore-type FSM that reads binary sequence w and sets z=1 if 11 pattern (with overlaps) is detected.
Draw **state diagram**.
Simulate using Icarus Verilog to verify the operation. Write **Verilog testbench** to simulate your design.
Show **screenshot of the Waveform** window indicating correct operation.

6.2 Moore-Type FSM

7

Write the behavioral **Verilog code** for a Moore-type FSM that reads binary sequence w and sets z=1 if either a 110 or 101 pattern (with overlaps) is detected.
Draw **state diagram**.
Simulate using Icarus Verilog to verify the operation. Write **Verilog testbench** to simulate your design.
Show **screenshot of the Waveform** window indicating correct operation.

6.3 Simple Mealy Module

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Write the behavioral **Verilog code** for a Mealy-type FSM that reads binary sequence w and sets z=1 if 11 pattern (with overlaps) is detected.
Draw **state diagram**.
Simulate using Icarus Verilog to verify the operation. Write **Verilog testbench** to simulate your design.
Show **screenshot of the Waveform** window indicating correct operation.

6.4 Mealy-Type FSM

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Write the behavioral **Verilog code** for a Mealy-type FSM that reads binary sequence w and sets z=1 if either a 110 or 101 pattern (with overlaps) is detected.
Draw **state diagram**.
Simulate using Icarus Verilog to verify the operation. Write **Verilog testbench** to simulate your design.
Show **screenshot of the Waveform** window indicating correct operation.

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REQUIRED: Demonstrate the gtkwave windows to your instructor to prove that your codes are working.
Make sure that the instructor records that you successfully demonstrated the experiments. Document your work properly in a lab report for submission!