Familiarization with Basic Combinatorial Logic

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CSCI 355 Digital Logic and Computer Organization

Submitted to

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1. Objectives

1. Investigate the basic logic elements (NOT, And, and OR)
2. Investigate the universal logic gates (NAND and NOR)
3. Build basic logic elements (NOT, And, and OR) using universal gates
4. Examine the input and output of the logic circuits

2. Components Required

Power supply, 1 x 7400 Quad 2-Input NAND Gate, 1 x 7402 Quad 2-Input NOR Gate, Breadboard, Digital Circuit Evaluator, Wiring Kit

3. Background

4. Pre-Lab

4.1 7400 Series

i. What is the difference between the 7400 series and the 5400 series?

The main difference is that the 5400 series was designed for military use, while 7400 was designed for commercial use

ii. Integrated circuits of the “HC” device family are popular nowadays. What does “HC” stand for?

High speed CMOS

iii. What is the maximum propagation delay (“T_P (max)”) for the “HC” device family?

15 nanaoseconds

4.2 Dual In-Line Package

i. When was the dual-inline format invented and by whom?

Invented in 1964 by Don Forbes.

ii. Which is PIN #1? How are the rest of the pins numbered?

Pin 1 is the top left pin, the rest of the pins are numbered counter clockwise

4.3 Datasheets

i. What is a 7474 IC?

Pasted from wikipedia: “

dual D positive edge triggered flip-flop, asynchronous preset and clear

“

ii. What is the number for a quad 2-input XOR gate?

74X2G86, which is number 7486

iii. Download and review the "datasheet" for the 7400 - quad 2-input NAND gate (you will need the “pinout” for the lab procedures below)

iv. Download and review the "datasheet" for the 7402 - quad 2-input NOR gate (you will need the “pinout” for the lab procedures below).

4.4 Number Conversion

i. Show a complete process of converting a binary number $(1011.101)_2$ to decimal.

Integer part

1011 = 1 * 2 ** 3 + 0 * 2 ** 2 + 1 * 2 ** 1 + 1 * 2 ** 0

= 8 + 0 + 2 + 1

= 11

Fraction part

101 = 1 * 2 ** (-1) + 0 * 2 ** (-2) + 1 * 2 ** (-3)

= 0.5 + 0 + 0.125

= 0.625

Together

1011.101 = 11 + 0.625 = 11.625

ii. Show a complete process of converting gray code (1011101) to normal binary.

Let b = 1011101

Let x be the converted binary number

i (bit index)

0	b[i] = 1	b[i - 1] = null	x[i] = 1
1	b[i] = 0	b[i - 1] = 1	x[i] = 1
2	b[i] = 1	b[i - 1] = 1	x[i] = 0

3	b[i] = 1	b[i - 1] = 0	x[i] = 1
4	b[i] = 1	b[i - 1] = 1	x[i] = 0
5	b[i] = 0	b[i - 1] = 0	x[i] = 0
6	b[i] = 1	b[i - 1] = 0	x[i] = 1

bianry number is x = 1101001

5. Debugging Techniques

6. Lab Procedure with Deliverables

6.1 AND Gate

Constructing AND gate circuit and verifying that it operates as expected.

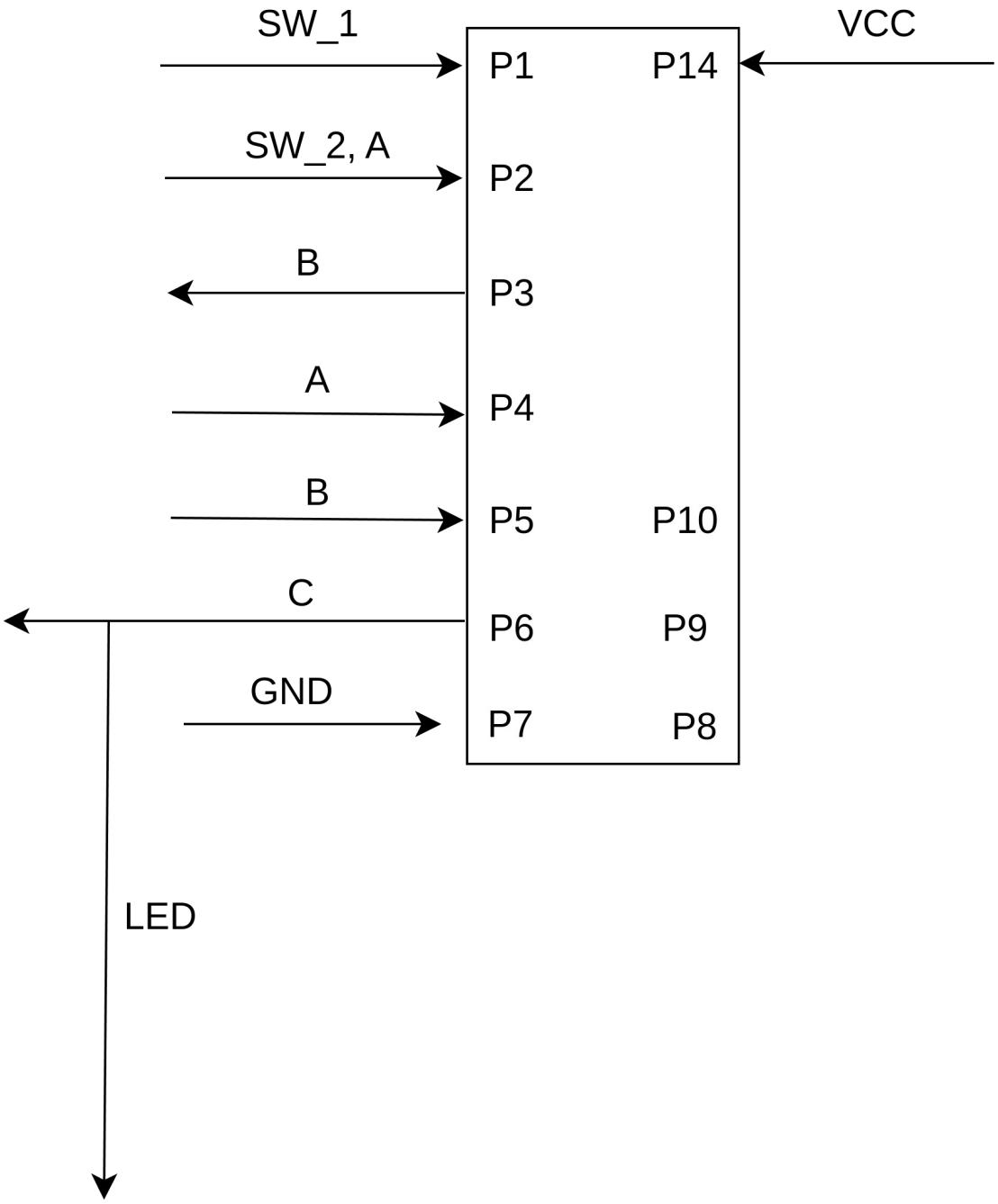
6.1.1 Construct the AND circuit on your breadboard using two NAND gates:

This circuit is created by two NAND gates with the second NAND gate functioning as an inverter.

A	B	C (intermediate output)	Y
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

The evidence for 6.1.1:

1. Circuit (Schematic) diagram as 6.1.1.AND_CIRCUIT_DIGRAM
2. The digital photo as 6.1.1.AND_DIGITAL
3. The PIN out diagram for this circuit



4. Pinning table

STUDENT NAME: Caleb Burke

EXPERIMENT NUMBER: 6.1.1

IC NUMBER: **SN7400**

Source	Destination		
Pin Number	**Alias Name**	**Pin Number**	**Alias Name**
P1			
P2			
P3	B		
P4	A		
P5	B		
P6	C		
P7	GND	+0V	
P14	VCC	+5V	

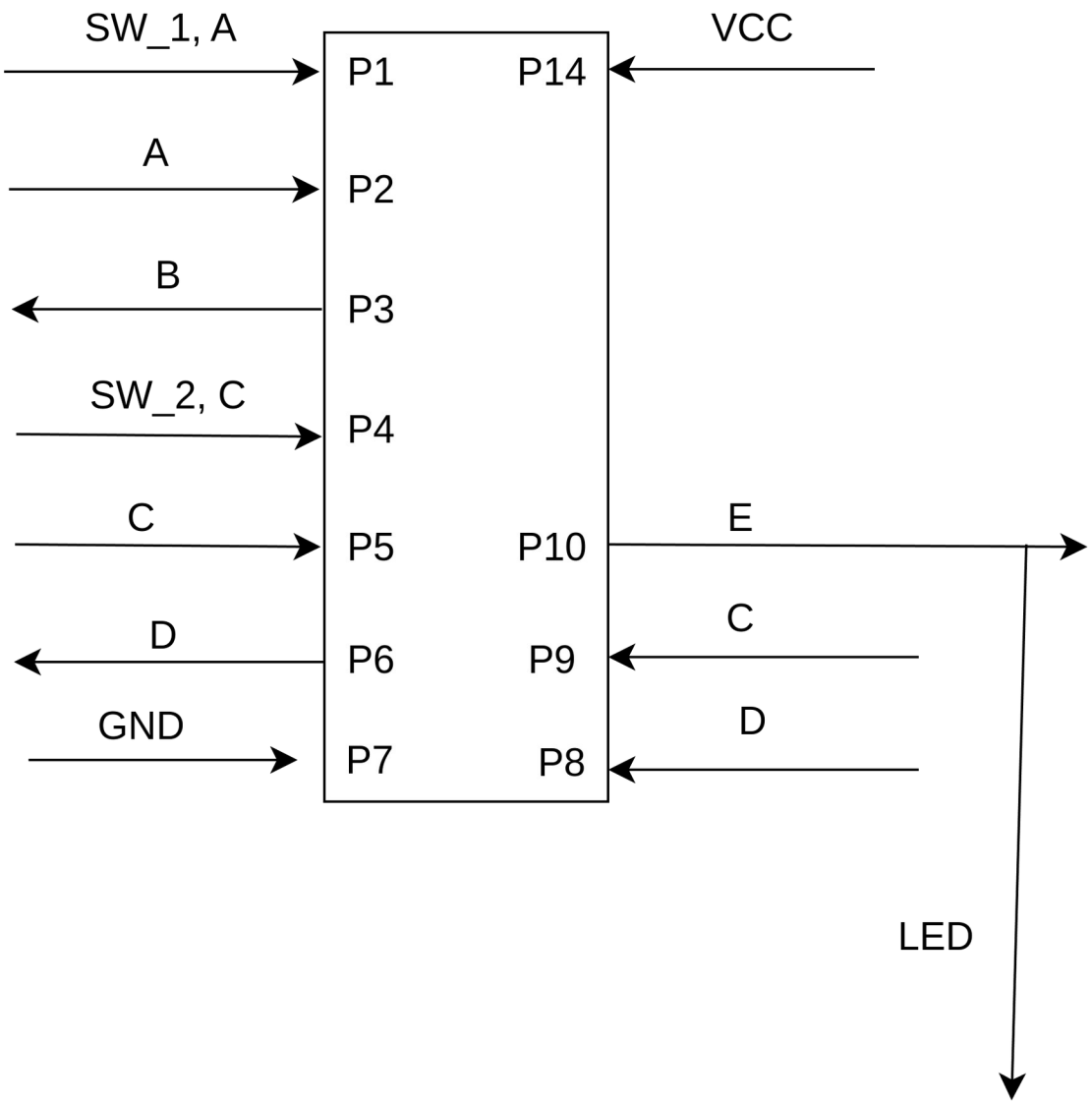
6.1.2 Construct the AND circuit on your breadboard using three NOR gates:

This circuit is created by two NOR gates functioning as inverters.

A	B	NOT A	NOT B	Y
0	0	1	1	0
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1

The evidence for 6.1.2:

1. Circuit diagram as 6.1.2.AND_CIRCUIT_DIAGRAM
2. The digital photo as 6.1.2.AND_DIGITAL
3. The PIN out diagram for this circuit



4. Pinning table

STUDENT NAME: Caleb Burke

EXPERIMENT NUMBER: 6.1.1

IC NUMBER: **SN7402**

Source	**Destination**		
Pin Number	**Alias Name**	**Pin Number**	**Alias Name**
P1			
P2			
P3	B		
P4	A		
P5	B		
P6	C		
P7	GND	+0V	
P14	VCC	+5V	

6.2 OR Gate

Constructing OR gate circuit and verify that it operates as expected.

6.2.1 Construct the OR circuit on your breadboard using two NOR gates:

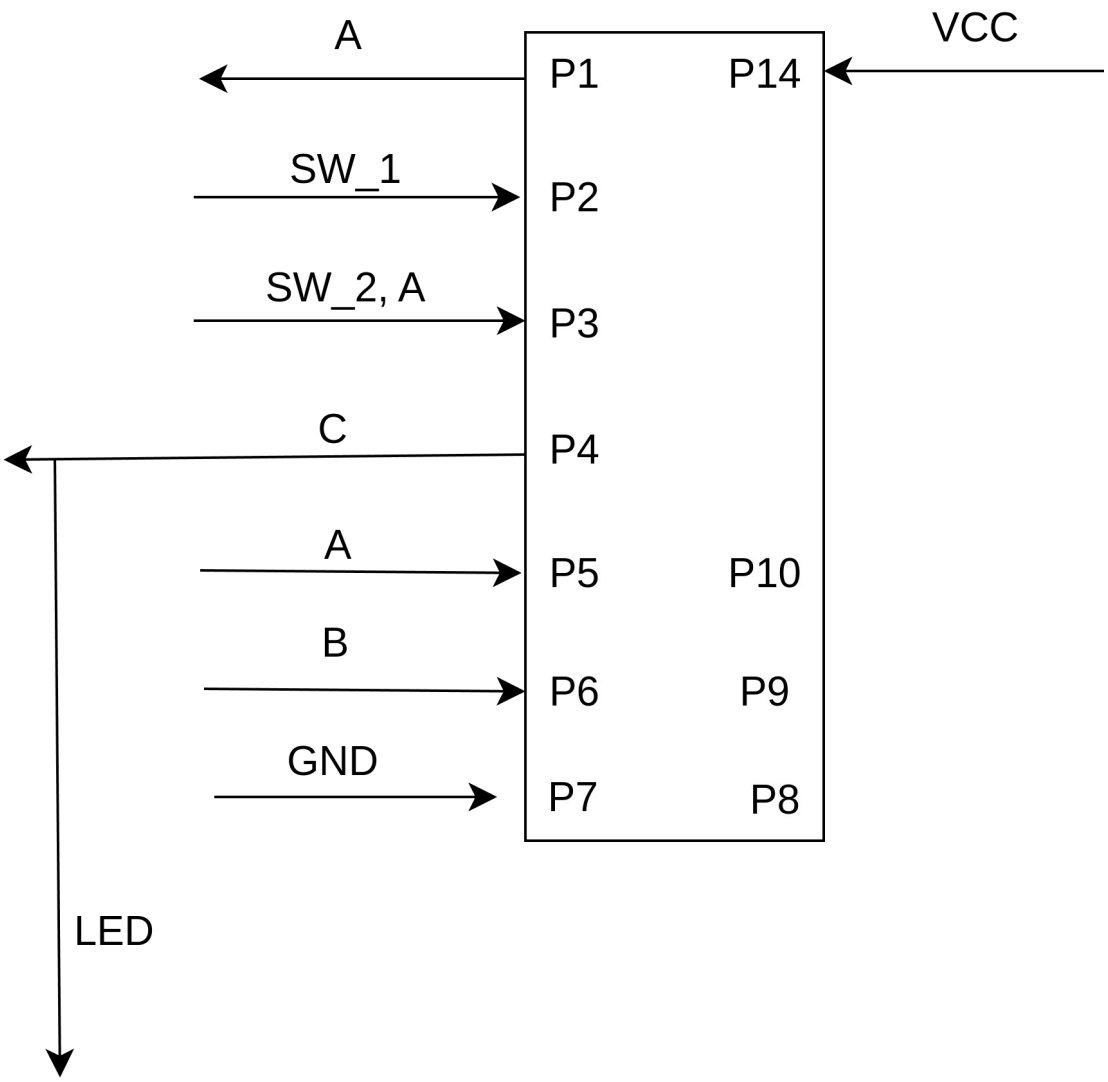
This circuit is created by two NOR gates with the second NOR gate functioning as an inverter.

A	**B**	**C(Intermediate Output)**	**Y**
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

The other evidence for 6.2.1 is:

1. Circuit (Schematic) diagram as 6.2.1.OR_CIRCUIT_DIAGRAM
2. The digital photo is as 6.2.1.OR_DIGITAL

3. The PIN out diagram for this circuit



4. Pinning table

STUDENT NAME: Caleb Burke

EXPERIMENT NUMBER: 6.1.1

IC NUMBER: **SN7402**

Source	**Destination**		
Pin Number	**Alias Name**	**Pin Number**	**Alias Name**
P1			
P2			

P3			
P4			
P5			
P6			
P7	GND	+0V	
P14	VCC	+5V	

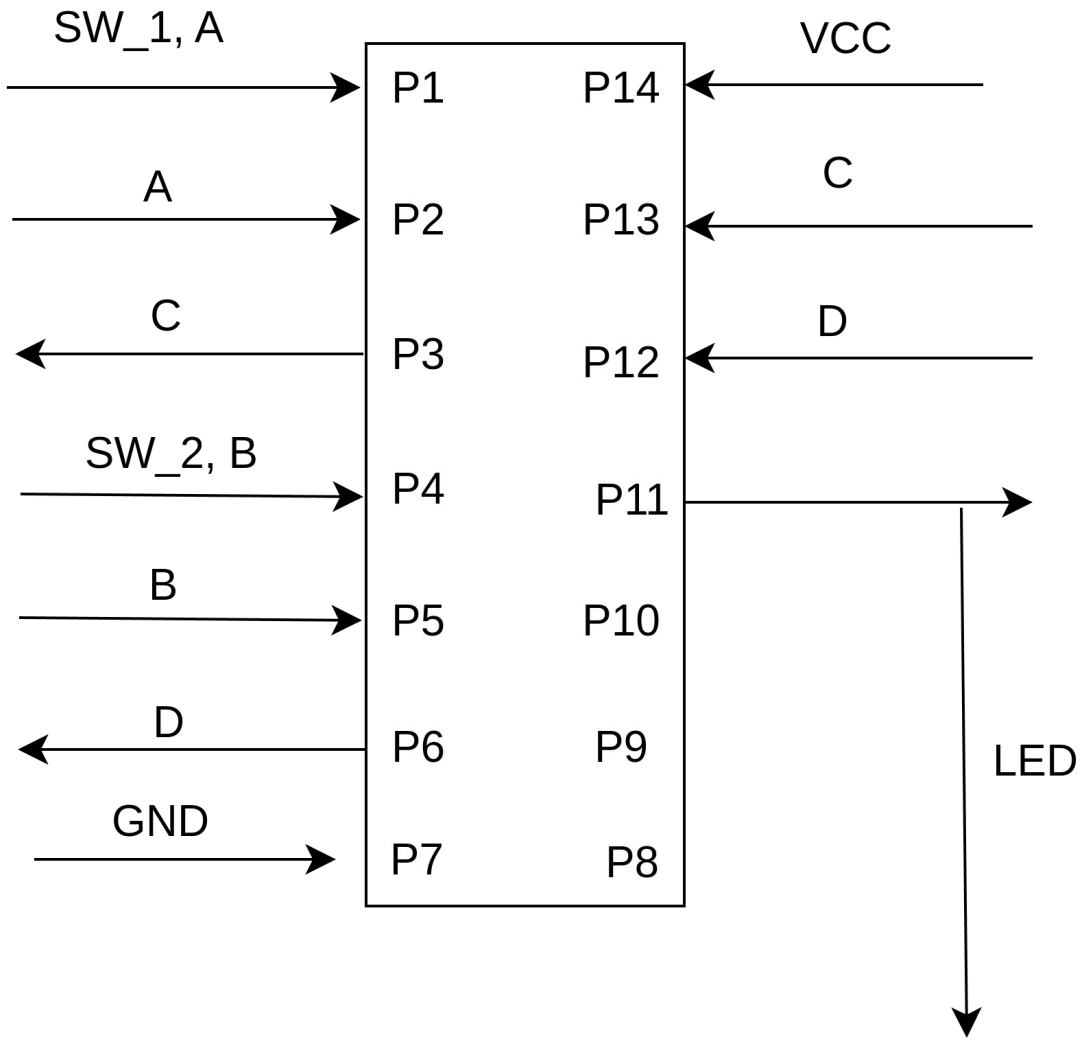
6.2.2 Construct the OR circuit on your breadboard using three NAND gates:

This circuit is created by three NAND gates with two NAND gates functioning as inverters.

A	B	NOT A	NOT B	Y
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

The other evidence for 6.2.2 :

1. Circuit diagram as 6.2.2.OR_CIRCUIT_DIAGRAM
2. The digital photo as 6.2.2.OR_DIGITAL
3. The PIN out diagram for this circuit



4. Pinning table

STUDENT NAME: Caleb Burke

EXPERIMENT NUMBER: 6.1.1

IC NUMBER: **SN7400**

Source	**Destination**		
Pin Number	**Alias Name**	**Pin Number**	**Alias Name**
P1			
P2			
P3			
P4			
P5			
P6			
P7	GND	+0V	
P14	VCC	+5V	

7. Conclusion

Any logical operation can be made from a combination of NOR and/or NAND gates.

References

https://en.wikipedia.org/wiki/List_of_7400-series_integrated_circuits

Appendix

Signature: Caleb Burke