

Combinational Logic and basics of Verilog HDL

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1. Objectives

1. Familiarization with Karnaugh Maps
2. Designing a minimum sum-of-products function with Karnaugh map
3. Designing a minimum product-of-sums function with Karnaugh map
4. Familiarization with the basics of Verilog HDL
5. Understanding waveforms generated with input/output signals

4. Pre-Lab

4.1 a. $F = x'yz' + xz' + xy + xz + y'z$

$z \backslash xy$	00	01	11	10
0	0	1	1	1
1	1	0	1	1

$F_{min} = x + yz' + y'z$

b. $F = xy' + wy' + xz' + wz' + y'z + w'x$

$z \backslash wy$	00	01	11	10
00	0	0	1	1
01	1	1	1	1
11	1	0	0	1
10	0	0	1	1

$F = xw' + z'w + xy'$

4.2 a) $F = \prod w, x, y, z (0, 1, 8, 9, 10, 12, 14)$

$yz \backslash wx$	00	01	11	10
00	0	0	0	0
01	0	1	1	0
11	1	1	0	0
10	0	0	1	1

group
 a: $w=0, 1 \quad x=0 \quad y=0 \quad z=0, 1$
 $F = x, y$
 b: $w=1 \quad x=1, 0 \quad y=1, 0 \quad z=0$
 $= w'z$

$F = (x+y)(w'z)$

b) $F = \prod w, x, y, z (0, 15)$

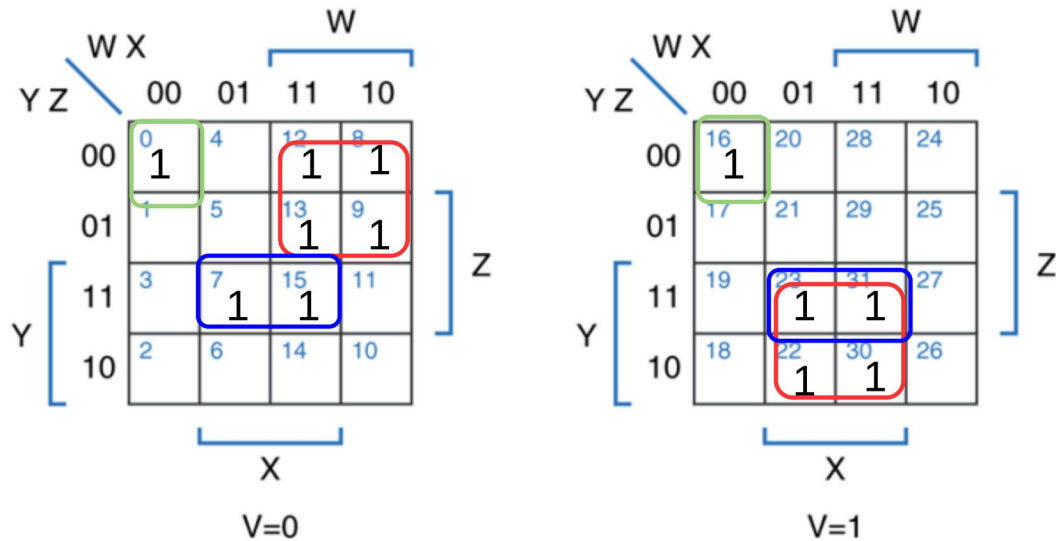
$yz \backslash wx$	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	0	0
10	0	0	0	0

group
 a: $w, x, y, z = 0$
 b: $w, x, y, z = 1$

$F = (w' + x' + y' + z')(w + x + y + z)$

4.3

$$F = \sum_{V,W,X,Y,Z} (0,7,8,9,12,13,15,16,22,23,30,31)$$



$$F = vxy + 'vw'y + 'w'x'y'z + xyz$$

4.4 b) $F = \sum w, x, y, z \ m(0, 3, 6, 9)$

Truth Table:

wxyz	BCD	yz \ wx
0000	0	00 01 11 10
0001	1	00 ① 0 0 d 0
0010	2	01 0 0 d 1
⋮	⋮	11 ① 0 d d
⋮	⋮	10 0 ① d d
1001	9	
⋮	⋮	
1111	15	

Grouping:

- a: $w, x, y, z = 0$
- b: $w = 1, x = 0, 1$
 $y = 0, 1, z = 1$
- c: $w = 1, 0, x = 0, y = 1, z = 1$
- d: $w = 0, 1, x = 1, y = 1, z = 0$

Don't care: 1001, 1111

Boolean Expression:

$$F = (w'x'y'z') + (wz) + (x'yz) + (xyz')$$

b) $F = \sum w, x, y, z \ m(0, 3, 6, 9)$

Truth Table:

yz \ wx	00	01	11	10
00	①	0	0	0
01	0	0	0	①
11	①	0	0	0
10	0	①	0	0

Boolean Expression:

$$F = (w'x'y'z') + (w'x'yz) + (w'xy'z') + (wx'y'z)$$

6. Lab Procedure with Deliverables

6.1 Three-Way Light Control using structural Verilog

Main code:

```
//Structural Specification
module threeWayLight (
    x1,x2,x3,f
);
    input wire x1,x2,x3;
    output wire f;
    wire nx1, nx2, nx3, a1, a2, a3, a4;

    not(nx1, x1); // ~x1
    not(nx2, x2); // ~x2
    not(nx3, x3); // ~x3

    and(a1, nx1, nx2, x3);
    and(a2, nx1, x2, nx3);
    and(a3, x1, x2, x3);
    and(a4, x1, nx2, nx3);
    or(f, a1, a2, a3, a4);

    assign o = (~x1 & ~x2 & x3) | (~x1 & x2 & ~x3) | (x1 & x2 & x3) | (x1 & ~x2 & ~x3);

endmodule
```

Test Bench:

```
`timescale 1ns/1ns
`include "threeWayLight.v"
module threeWayLight_tb (
);
    reg x1, x2, x3;
    wire f;

    threeWayLight ut(x1, x2, x3, f);

    initial begin
        $dumpfile("threeWayLight_tb.vcd");
        $dumpvars(0, threeWayLight_tb);

        x1 = 0;
        x2 = 0;
```

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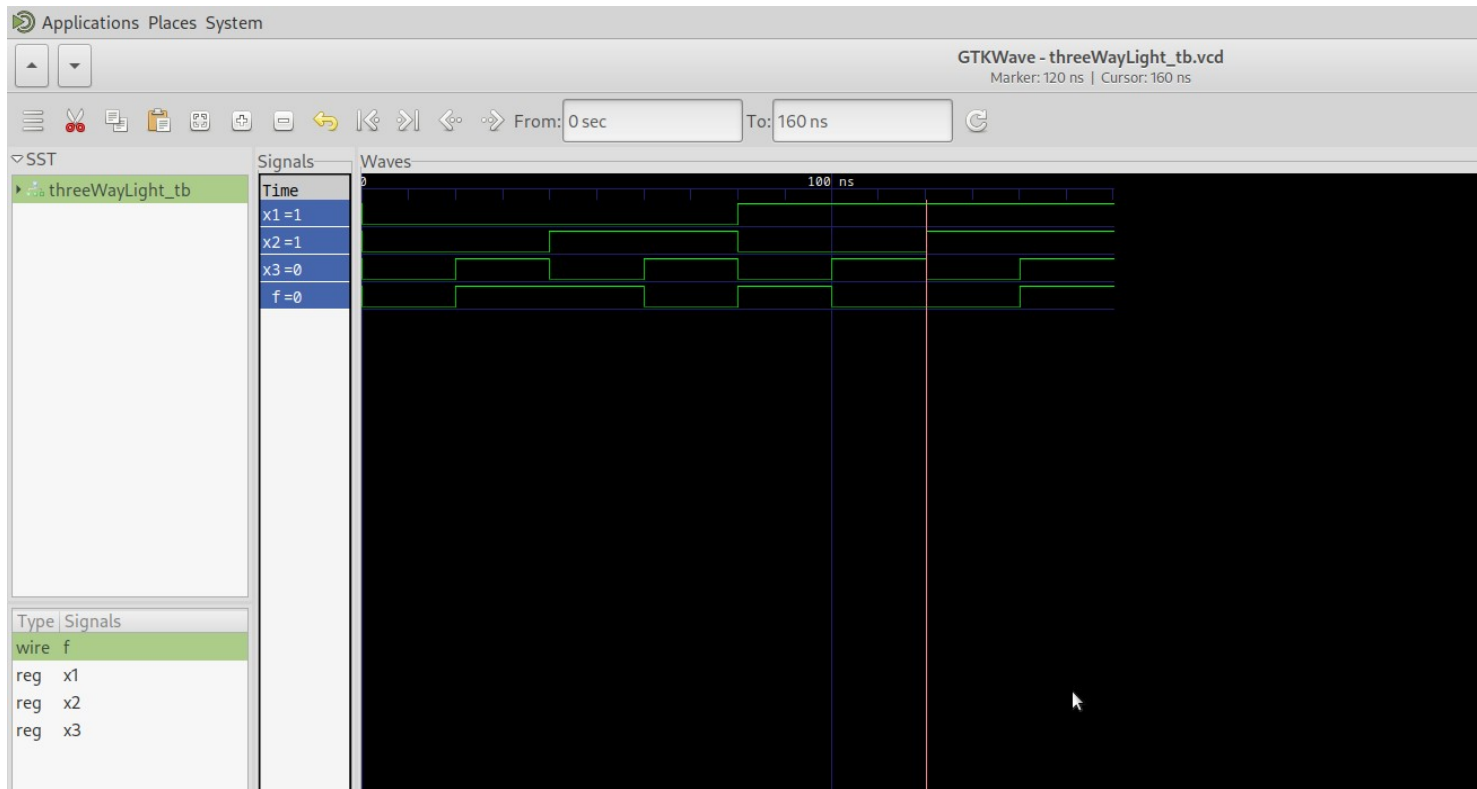
```
x3 = 0;
    #20;
x1 = 0;
x2 = 0;
x3 = 1;
    #20;
x1 = 0;
x2 = 1;
x3 = 0;
    #20;
x1 = 0;
x2 = 1;
x3 = 1;
    #20;
x1 = 1;
x2 = 0;
x3 = 0;
    #20;
x1 = 1;
x2 = 0;
x3 = 1;
    #20;
x1 = 1;
x2 = 1;
x3 = 0;
    #20;
x1 = 1;
x2 = 1;
x3 = 1;
    #20;

$display("Test complete");
```


end

endmodule

Timing diagram



Truth Table

x1	x2	x3	f
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0

1	1	0	0
1	1	1	1

Comparing the truth table and timing diagram, the code works as expected.

6.2 Three-Way Light Control using Behavioural Verilog

Main code:

```
//Structural Specification
module threeWayLightFunc (
    x1,x2,x3,f
);
    input wire x1,x2,x3;
    output wire f;
    assign f = (~x1 & ~x2 & x3) | (~x1 & x2 & ~x3) | (x1 & x2 & x3) | (x1 & ~x2 & ~x3);
endmodule
```

Testbench:

```
`timescale 1ns/1ns
`include "threeWayLightFunc.v"
module threeWayLightFunc_tb ();
    reg x1, x2, x3;
    wire f;

    threeWayLightFunc ut(x1, x2, x3, f);

    initial begin
        $dumpfile("threeWayLightFunc_tb.vcd");
        $dumpvars(0, threeWayLightFunc_tb);

        x1 = 0;
        x2 = 0;
        x3 = 0;
        #20;
        x1 = 0;
        x2 = 0;
        x3 = 1;
        #20;
```

CSCi 355: Lab 4

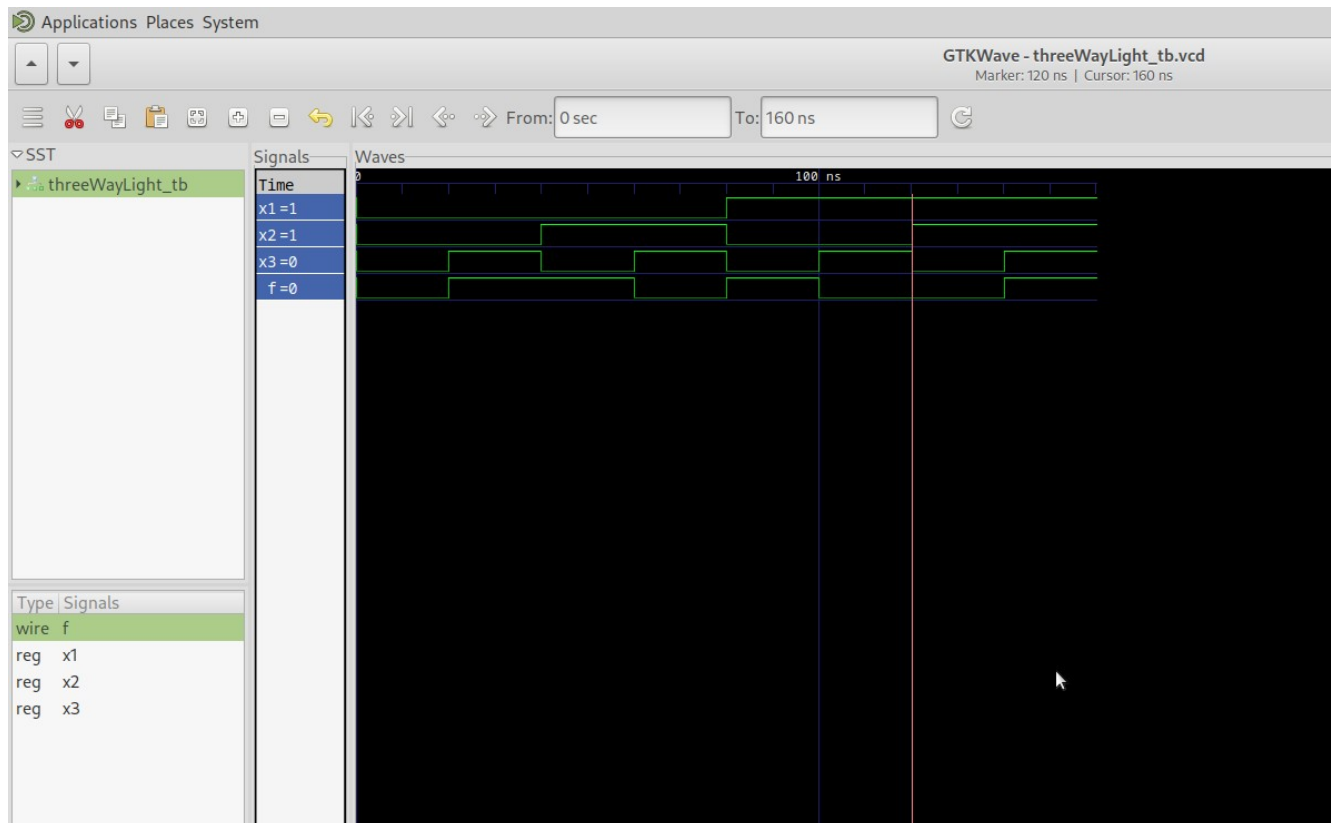
```
x1 = 0;
x2 = 1;
x3 = 0;
    #20;
x1 = 0;
x2 = 1;
x3 = 1;
    #20;
x1 = 1;
x2 = 0;
x3 = 0;
    #20;
x1 = 1;
x2 = 0;
x3 = 1;
    #20;
x1 = 1;
x2 = 1;
x3 = 0;
    #20;
x1 = 1;
x2 = 1;
x3 = 1;
    #20;

$display("Test complete");
end

endmodule
```

Timing Diagram

CSCi 355: Lab 4



Truth table

x1	x2	x3	f
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Comparing the truth table and timing diagram, the code works as expected.

Appendix

Signature: Caleb Burke