Combinatorial Logic

Submitted by

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Submitted to

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1. Objectives

1. Design multibit adder using Verilog HDL
2. Design multibit comparator using Verilog HDL
3. Interpret waveforms generated with input/output signals

2. Components Required

Power supply, 1 x 7400 Quad 2-Input NAND Gate, 1 x 7402 Quad 2-Input NOR Gate, Breadboard, Digital Circuit Evaluator, Wiring Kit

4. Pre-Lab

4.1 Why is a multi-bit adder processed from the least-significant bit to the mostsignificant bit while a multi-bit comparator is processed from the mostsignificant bit to the least-significant bit?

4.2 Write the decimal number 7129 in different representationsin Verilog HDL:

Binary = ?

Octal = ?

Hex = ?

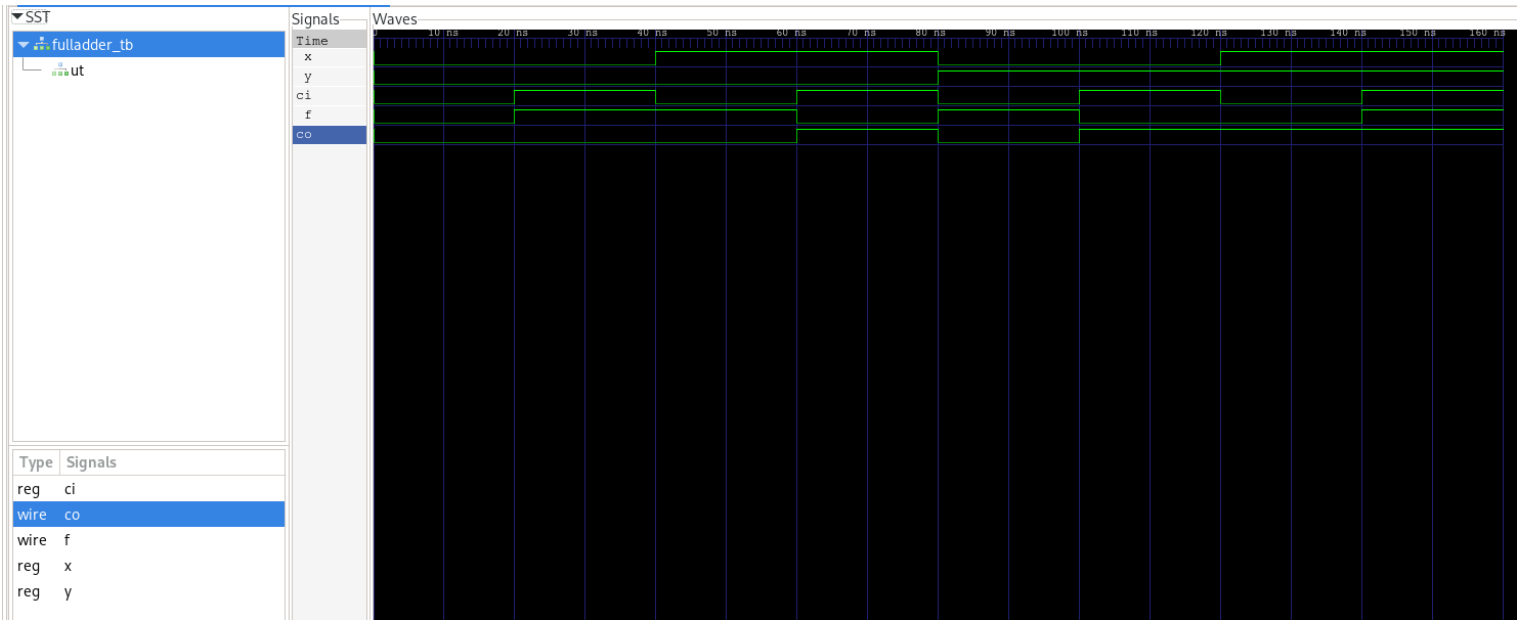
Decimal =

6. Lab Procedure

6.1 N-bit adder

1. fulladder

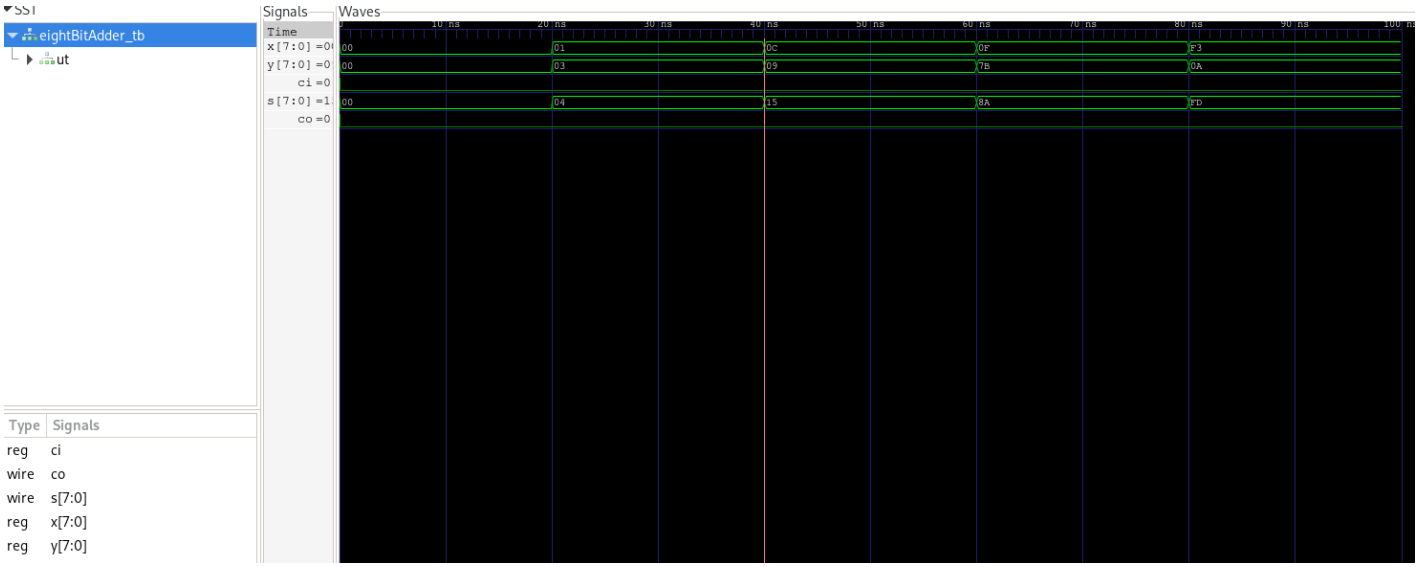
Verilog main code and testbench code attached.



Timing diagram

2. Eight bit adder

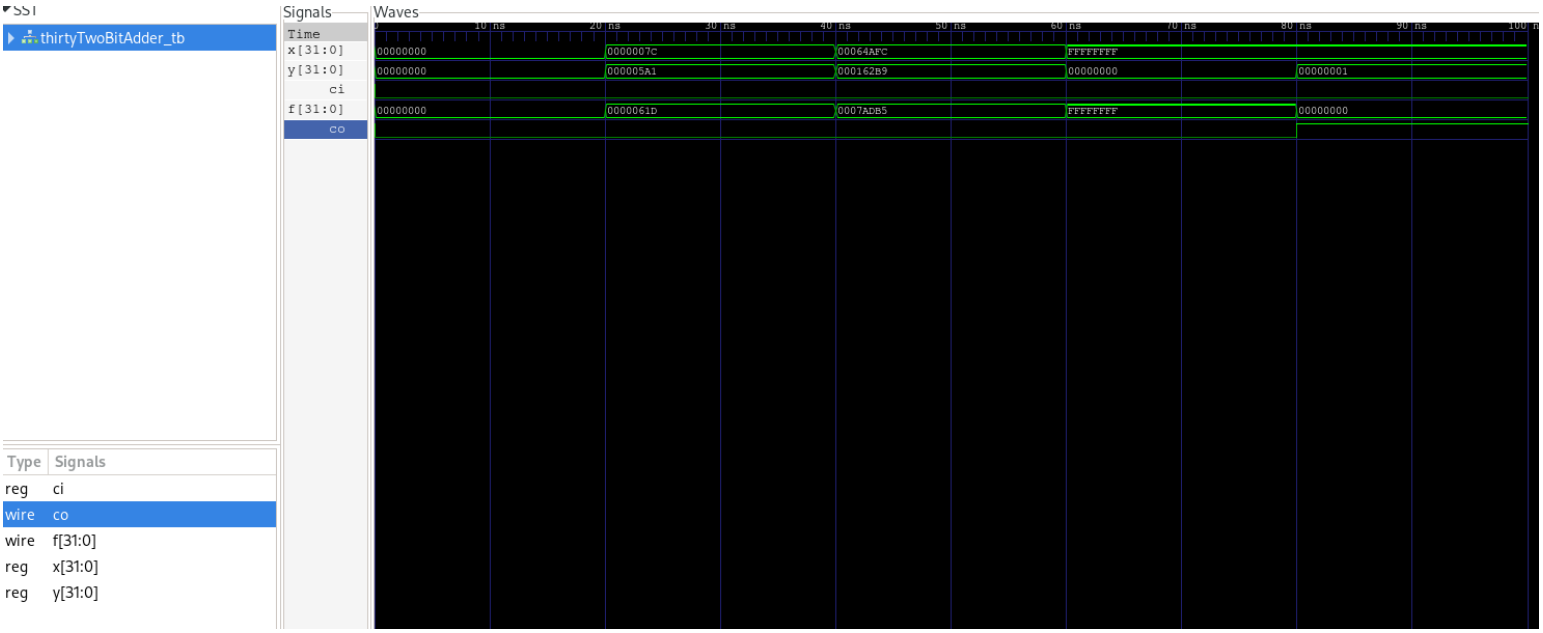
Verilog main code and testbench code attached.



Timing diagram

3. 32 bit adder

Verilog main code and testbench code attached.

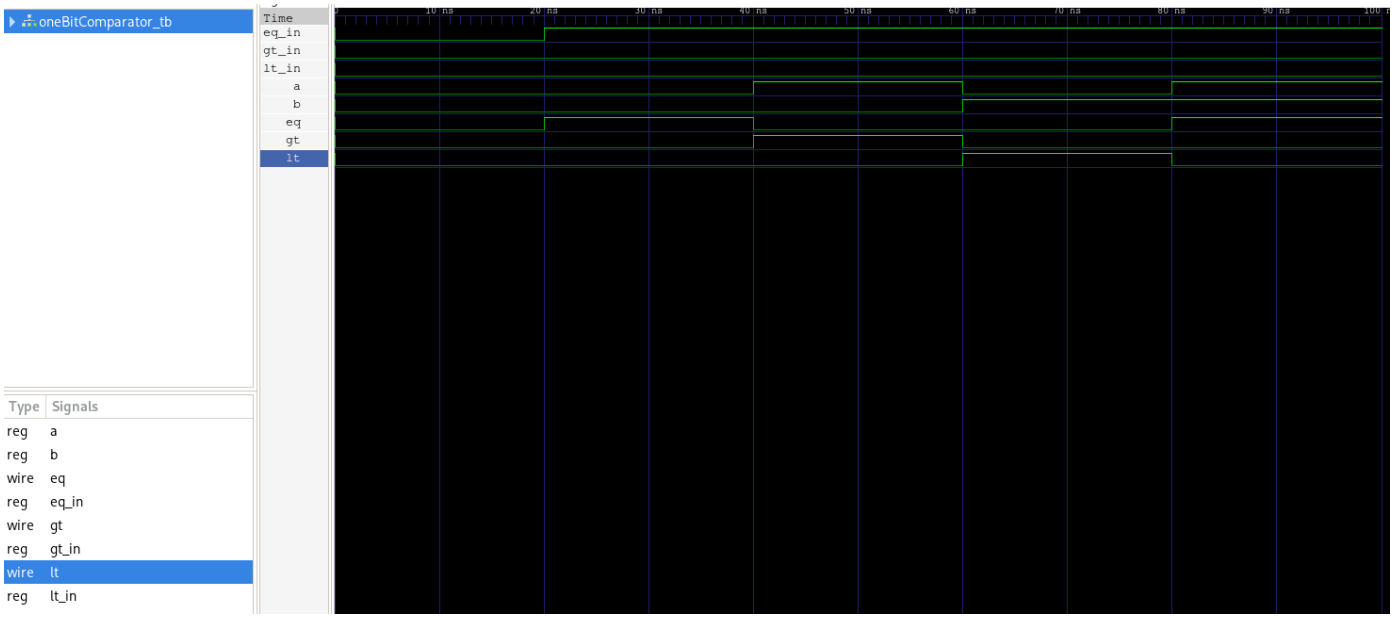


Timing diagram

6.2 Four bit comparator

1. One bit comparator

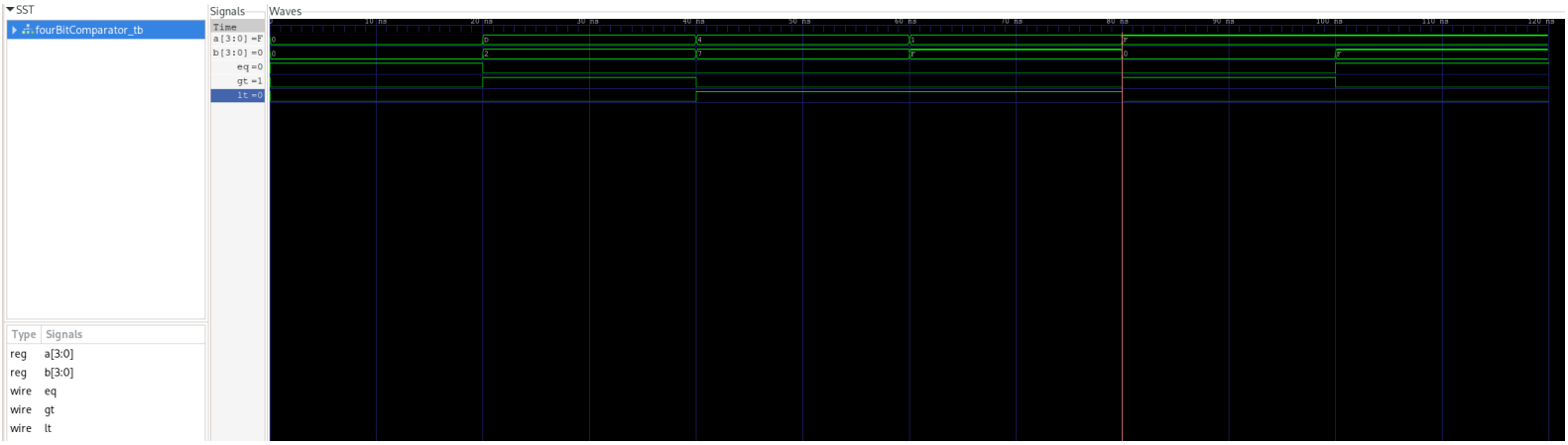
Verilog main code and testbench code attached.



Timing diagram

2. Four bit comparator

Verilog main code and testbench code attached.



Timing diagram

7. Conclusion

In this lab, I implemented and tested a multi-bit adder and comparator using Verilog HDL. Time diagrams confirmed functionality and reinforced core concepts.

Appendix

Signature: Caleb Burke