**Familiarization with Basic Combinatorial Logic**

Submitted by

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**CSCI 355 Digital Logic and Computer Organization**

Submitted to

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**Table of Contents**

Contents

[1. Objectives 1](#_Toc177490165)

[2. Components Required 1](#_Toc177490166)

[3. Background (You can remove this section) 1](#_Toc177490167)

[4. Pre-Lab 2](#_Toc177490168)

[4.1 7400 Series 2](#_Toc177490169)

[4.2 Dual In-Line Package 2](#_Toc177490170)

[4.3 Datasheets 2](#_Toc177490171)

[4.4 Number Conversion 3](#_Toc177490172)

[5. Debugging Techniques (You can remove this section) 3](#_Toc177490173)

[6. Lab Procedure with Deliverables 3](#_Toc177490174)

[6.1 AND Gate 3](#_Toc177490175)

[6.2 OR Gate 5](#_Toc177490176)

[7. Conclusion 6](#_Toc177490177)

[References 6](#_Toc177490178)

[Appendix 6](#_Toc177490179)

## 1. Objectives

1. Investigate the basic logic elements (NOT, And, and OR)

2. Investigate the universal logic gates (NAND and NOR)

3. Build basic logic elements (NOT, And, and OR) using universal gates

4. Examine the input and output of the logic circuits

## 2. Components Required

Power supply, 1 x 7400 Quad 2-Input NAND Gate, 1 x 7402 Quad 2-Input NOR Gate, Breadboard, Digital Circuit Evaluator, Wiring Kit

## 3. Background (You can remove this section)

## 4. Pre-Lab

### 4.1 7400 Series

1. What is the difference between the 7400 series and the 5400 series?
2. Integrated circuits of the “HC” device family are popular nowadays. What does “HC” stand for?
3. What is the maximum propagation delay (“TP (max)”) for the “HC” device family?

### Dual In-Line Package

1. When was the dual-inline format invented and by whom?
2. Which is PIN #1? How are the rest of the pins numbered?

### Datasheets

1. What is a 7474 IC?

1. What is the number for a quad 2-input XOR gate?
2. Download and review the "datasheet" for the 7400 - quad 2-input NAND gate (you will need the “pinout” for the lab procedures below)
3. Download and review the "datasheet" for the 7402 - quad 2-input NOR gate (you will need the “pinout” for the lab procedures below).

### Number Conversion

1. Show a complete process of converting a binary number (1011.101)2 to decimal.

* Either put it here or if you have it on a paper then put a picture of it here-do like this <<The conversion diagram is attached in appendix as CONVERSION\_BINARY\_FIG\_1. >>

1. Show a complete process of converting gray code (1011101) to normal binary.

## 5. Debugging Techniques (You can remove this section)

## 6. Lab Procedure with Deliverables

### 6.1 AND Gate

Constructing AND gate circuit and verifying that it operates as expected.

#### 6.1.1 Construct the AND circuit on your breadboard using two NAND gates:

This circuit is created by two NAND gates with the second NAND gate functioning as an inverter.

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | C (intermediate output) | Y |
| 0 | 0 |  |  |
| 0 | 1 |  |  |
| 1 | 0 |  |  |
| 1 | 1 |  |  |

The evidence for 6.1.1:

1. Circuit (Schematic) diagram as 6.1.1.AND\_CIRCUIT\_DIAGRAM
2. The digital photo as 6.1.1.AND\_DIGITAL
3. The PIN out diagram for this circuit as 6.1.1.AND\_PINOUT\_FIG
4. Pinning table as 6.1.1.AND\_PINOUT\_TABLE

6.1.1.AND\_PINOUT\_TABLE: <Example>

STUDENT NAME: John Doe

EXPERIMENT NUMBER: 6.1.1

IC NUMBER: **SN7400**

|  |  |  |  |
| --- | --- | --- | --- |
| **Source** | **Destination** | | |
| **Pin Number** | **Alias Name** | **Pin Number** | **Alias Name** |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

#### 6.1.2 Construct the AND circuit on your breadboard using three NOR gates:

This circuit is created by two NOR gates functioning as inverters.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | NOT A | NOT B | Y |
| 0 | 0 |  |  |  |
| 0 | 1 |  |  |  |
| 1 | 0 |  |  |  |
| 1 | 1 |  |  |  |

The evidence for 6.1.2:

1. Circuit diagram (Schematic) as 6.1.2.AND\_CIRCUIT\_DIAGRAM
2. The digital photo as 6.1.2.AND\_DIGITAL
3. The PIN out diagram for this circuit as 6.1.2.AND\_PINOUT\_FIG,
4. Pinning table as 6.1.2.AND\_PINOUT\_TABLE

### 6.2 OR Gate

Constructing OR gate circuit and verify that it operates as expected.

#### 6.2.1 Construct the OR circuit on your breadboard using two NOR gates:

This circuit is created by two NOR gates with the second NOR gate functioning as an inverter.

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | C(Intermediate Output) | Y |
| 0 | 0 |  |  |
| 0 | 1 |  |  |
| 1 | 0 |  |  |
| 1 | 1 |  |  |

The other evidence for 6.2.1 is:

1. Circuit (Schematic) diagram as 6.2.1.OR\_CIRCUIT\_DIAGRAM
2. The digital photo is as 6.2.1.OR\_DIGITAL
3. The PIN out diagram for this circuit as 6.2.1.OR\_PINOUT\_FIG,
4. Pinning table as 6.2.1.OR\_PINOUT\_TABLE

#### 6.2.2 Construct the OR circuit on your breadboard using three NAND gates:

This circuit is created by three NAND gates with two NAND gates functioning as inverters.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | NOT A | NOT B | Y |
| 0 | 0 |  |  |  |
| 0 | 1 |  |  |  |
| 1 | 0 |  |  |  |
| 1 | 1 |  |  |  |

The other evidence for 6.2.2 :

1. Circuit diagram as 6.2.2.OR\_CIRCUIT\_DIAGRAM
2. The digital photo as 6.2.2.OR\_DIGITAL
3. The PIN out diagram for this circuit as 6.2.2.OR\_PINOUT\_FIG
4. Pinning table as 6.2.2.OR\_PINOUT\_TABLE

## 7. Conclusion

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## References

## Appendix

Signature: \_\_\_\_\_\_\_\_\_\_\_