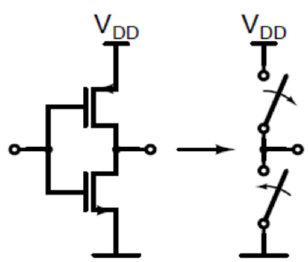
Lecture-3

→ In the last lecture we studied the possible amplification effect of a MOS Transistor.

→ It is different what MOS operation we see in Digital Circuits. In Digital circuits the Transistor is either ON or OFF.

MOSFET in Digital Circuits

- MOSFET is treated as a switch in digital design.
- Below threshold there is no current. Above threshold a sufficiently large V_{GS} can push the device into triode, where it is a resistor.
- This resembles a switch which has infinite resistance when off and finite resistance when on.
- Unlike analog where we use the device mostly in forward active region, in digital circuits the device toggles between off and linear regions.



M. Hekmat EE114S

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→ In Analog circuits we mostly operate in the saturation Region.

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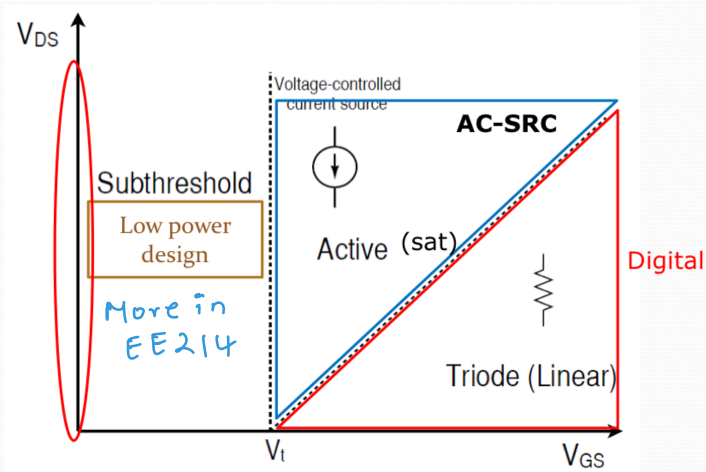
MOS regions usage



CHANNEL LENGTH MODULATION & Drain Current Saturation

Drain current Saturation and Channel Length Modulation

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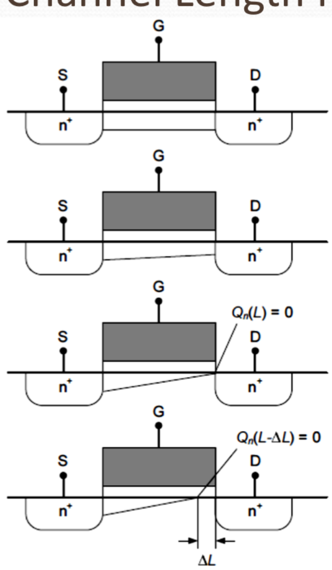
$V_{GS} > V_{th}$
Channel is formed



$V_{DS} = 0$

$0 < V_{DS} < V_{GS} - V_{Tn}$

$V_{DS} = V_{GS} - V_{Tn}$ (pinch off point)

$V_{DS} > V_{GS} - V_{Tn}$ (pinchoff point moves ~~left~~ left and channel length decreases)

$$Q_n(y) = C_{ox}[V_{GS} - V(y) - V_t]$$

- Channel pinch-off occurs for $V_{DS} \geq V_{GS} - V_t$ and the drain current saturates

Q How to Model the Impact of Channel length Modulation in the Saturation Region ?

For this we make use of concept Taylor's expansion

we have saturation current (I_D) given by

$$\boxed{I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2}$$

when we are in saturation as V_{DS} increases 'L' decreases.

→ and the new "length of channel" L' is a function of V_{DS}

$$\Rightarrow \quad L' = f(V_{DS})$$

∴ we can say that I_D will also be a function of V_{DS} in Saturation Region.

Taylor Series

If we a function $y = f(x)$

Then we can define the function as

$$\boxed{y = f(x_0) + (x - x_0)\frac{\partial f}{\partial x} + \cdots}$$

Here x_0 : operating point

→ In this case we can express I_D in terms of Taylor series expansion

$$\Rightarrow \quad I_D = I_{D_0} + \frac{\partial I_D}{\partial V_{DS}}\left(V_{DS} - \underbrace{V_{DS_0}}_{\text{operating point}}\right)$$

let us choose operating

$$\boxed{\begin{aligned} V_{DS_0} &= \text{Limit of the saturation Region} \\ &= V_{GS} - V_{th} \end{aligned}}$$

overdrive voltage.

→ ∴ we can write

$$\boxed{I_{D_0} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2}$$

(or)

$$\beta' \frac{W}{L}(V_{GS} - V_t)^2$$

→ we have I_{D_0} & V_{DS_0} what we need to find is the partial derivative $\frac{\partial I_D}{\partial V_{DS}}$

$$\boxed{\therefore \frac{\partial I_D}{\partial V_{DS}} = \frac{\beta'}{2} w (V_{GS}-V_t)^2 \frac{\partial \left(\frac{1}{L'}\right)}{\partial V_{DS}}}$$

$$\therefore \frac{\partial \left(\frac{1}{L'}\right)}{\partial V_{DS}} = \frac{\partial L'}{\partial V_{DS}} \cdot \frac{\partial \left(\frac{1}{L'}\right)}{\partial L'}$$

$$\boxed{\frac{\partial \left(\frac{1}{L'}\right)}{\partial V_{DS}} = \frac{\partial L'}{\partial V_{DS}} \cdot \frac{-1}{(L')^2}}$$

$$\Rightarrow \therefore \boxed{\frac{\partial I_D}{\partial V_{DS}} = \frac{-1}{(L')^2} \cdot \frac{\beta'}{2} \cdot w \cdot (V_{GS}-V_t)^2 \cdot \frac{\partial L'}{\partial V_{DS}}} \quad (1)$$

we have earlier that

$$I_D = \frac{\beta'}{2} \frac{w}{L'} (V_{GS}-V_t)^2$$

$$\Rightarrow \boxed{I_D L' = \frac{\beta'}{2} w (V_{GS}-V_t)^2} \quad (2)$$

put ② in ①

$$\Rightarrow \boxed{\frac{\partial I_D}{\partial V_{DS}} = -\frac{1}{(L')^2} I_D L' \cdot \frac{\partial L'}{\partial V_{DS}}}$$

$$\Rightarrow \boxed{\frac{\partial I_D}{\partial V_{DS}} = -\frac{I_D}{L'} \cdot \frac{\partial L'}{\partial V_{DS}}}$$

when $V_{DS} \uparrow$ $L' \downarrow$

$\therefore$ (as L' decreases as V_{DS} increases)

we can say that the the quantity is -ve

as $\boxed{\frac{\partial L'}{\partial V_{DS}} < 0}$

$$\Rightarrow \boxed{\frac{\partial I_D}{\partial V_{DS}} > 0}$$

which states that the saturation current Increases

→ Now lets call

$$\boxed{-\frac{1}{L'}\frac{\partial L'}{\partial V_{DS}} = \lambda}$$

→ Channel length modulation coefficient it is a parameter that depends mostly on technology and on Biasing Conditions

we would have

→ $\therefore$ $$\boxed{I_D = \frac{\beta'}{2}\cdot\frac{W}{L}(V_{GS}-V_t)^2(1+\lambda(V_{DS}-V_{DS0}))}$$

expression of 'I_D' including CLM.

usually this quantity is neglected because it will be of Range $0.1 - 0.2\ V$

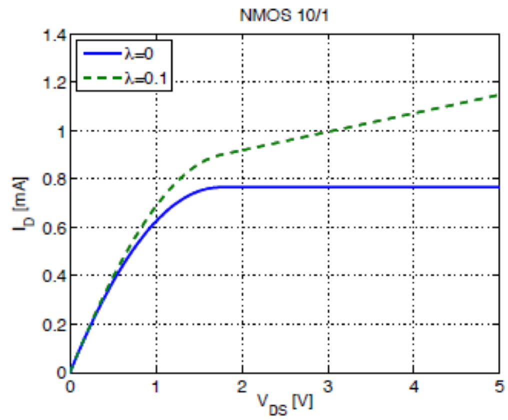
$\Rightarrow$ $$\boxed{I_D = \frac{\beta'}{2}\cdot\frac{W}{L}(V_{GS}-V_t)^2(1+\lambda V_{DS})}$$

$V_{DS_0} = V_{GS} - V_t$ (usually the V_{GS} is kept little higher than V_t)

$\therefore$ V_{DS_0} value is very small

Drain current Saturation and Channel Length Modulation

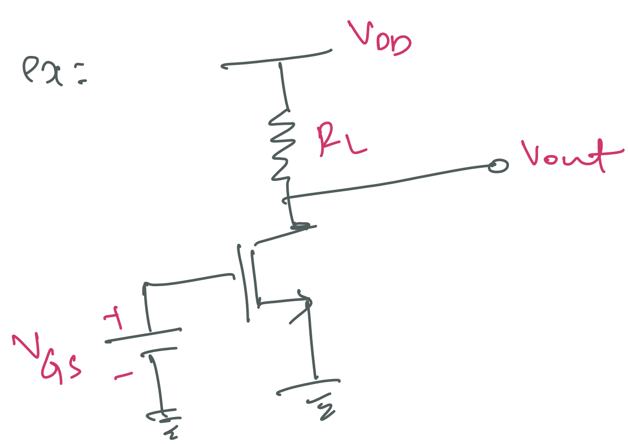
$$\Rightarrow I_D \simeq \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_t)^2)[1+\lambda V_{DS}]$$



(Channel length Modulation effect)

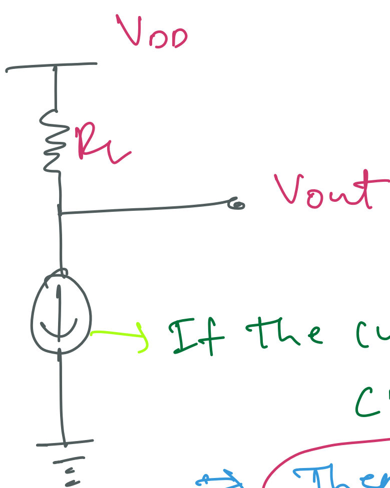
∴ The effect of CLM is that the current increases even in the saturation Region where it is ideally assumed to be constant.

∴ ex:



Here The MOS Transistor acts as a voltage dependent current source

⇒ Ideally we want the current source to remain constant.



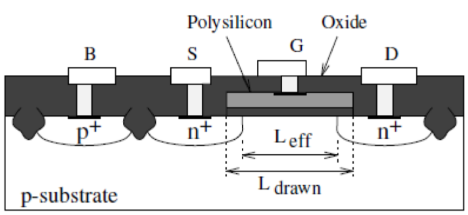
→ If the current increases because of CLM.

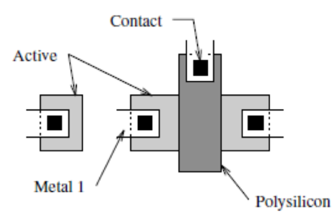
⇒ Then the current through R_L increases ↑

as $V_{out} = V_{DD} - I_D R_L$

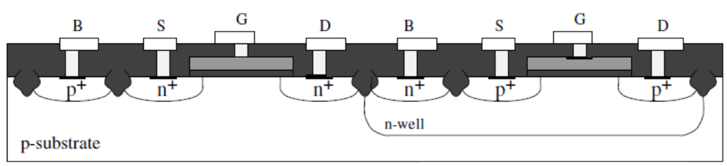
∴ Value of V_{out} ↓

MOSFET technology

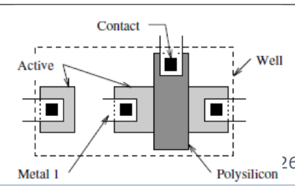




REAL device

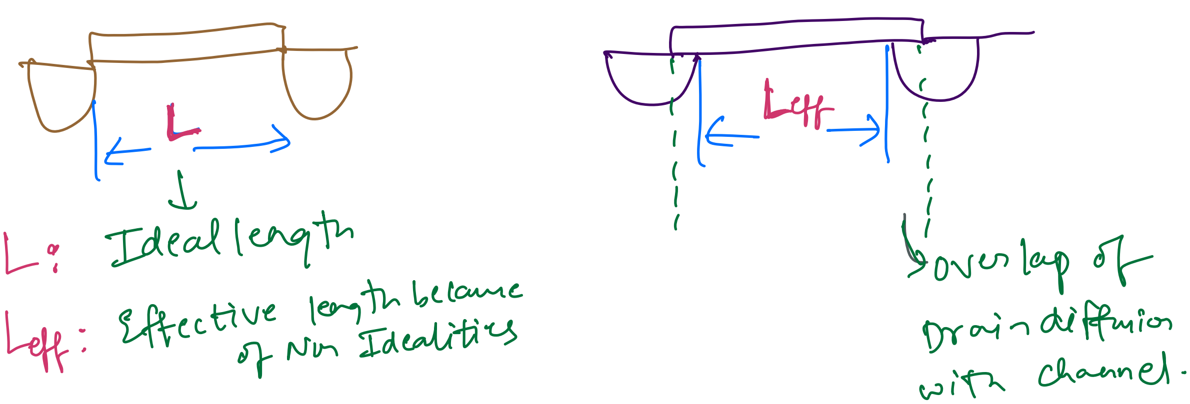


Transistor structure in a CMOS process with an n-well



→ The models that we have considered so far eventhough enriched with Channel length Modulation are very rough approximation of what a REAL device is.

→ An Idel device we see a perfectly divided channel Regions from source diffusion & Drain Diffusions may be without any overlap. b/w oxide Gate and Metalization of the Gate w.r.to the Source and Drain diffusion



→ There are several Non Idealities which are intrinsic to the Manufacturing Process of the Device.

→ On Top of That we have multiple Geometry connected effects which we cannot Neglect.

→ we should consider all these Non-Idealities before Analyzing the performance of the device in the Field.

→ **Note:-** Another important contact which is to be taken into effect is the Body Contact

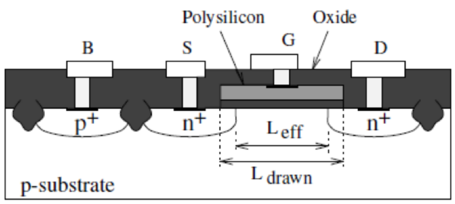
An important we should take into account is whether we have ~~(or)~~ not the possibility to keep the bulk to source voltage zero.

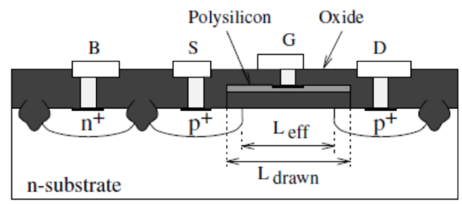
It is not always possible.

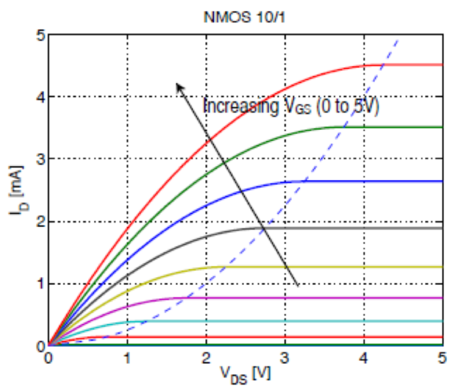
Note:- In our course we would consider the Bulk contact of all NMOS devices on a chip to be LOW.

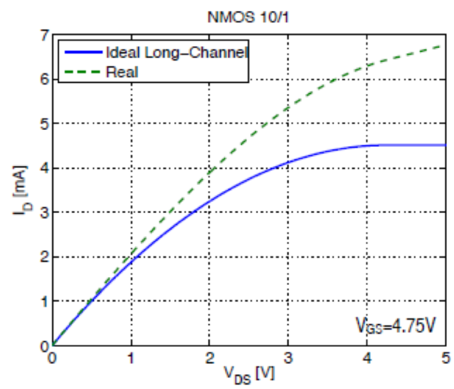
& Bulk contact of all PMOS devices on a chip to be High.

MOSFET: Id-Vds Curves





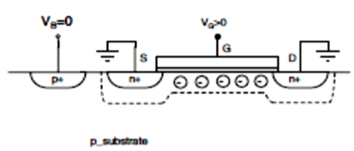


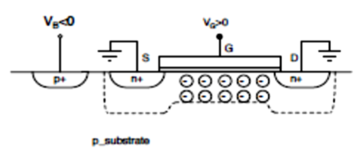


* Dashed blue line denotes the border between active and linear regions.

Substrate Voltage & MOS Device

Substrate Voltage and MOS Device





- Applying a voltage to bulk can modulate the depletion width.
- Positive V_{SB} draws more holes to the substrate, widening the depletion region.
- The increased amount of fixed negative ions in the depletion region, makes it harder for electrons to form the channel.
  - Larger V_{GS} is required to reach inversion.
  - V_t increases.

→ As introduced earlier the Substrate voltage (or) the Bulk voltage (or) the Body voltage plays a crucial Role in the operation of the MOSFET. Because, Essentially MOS is a 4 Terminal Device.

→ Bulk voltage plays an important Role because
(V_{SB})
Source to bulk voltage

Backgate Effect

- The backgate effect is the change in threshold voltage of the device due to change in the bulk potential.

$$V_t = V_{t0} + \gamma(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f})$$

- One can think of the substrate terminal as an additional gate for the transistor as it can control the channel in somewhat the same way.
- Change in V_t means change in I_D.
- Define small-signal backgate transconductance.
  - Remember that g_m embodied changes of I_D due to V_{GS} variations.

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = -\frac{\partial I_D}{\partial V_{SB}}$$
$$= \mu C_{ox}\frac{W}{L}(V_{GS} - V_t) \times (-\frac{\partial V_t}{\partial V_{BS}})$$

$$\frac{\partial V_t}{\partial V_{BS}} = -\frac{\gamma}{2\sqrt{(2\phi_f + V_{SB})}} \Longrightarrow g_{mb} = g_m \frac{\gamma}{2\sqrt{2\phi_f + V_{SB}}}$$

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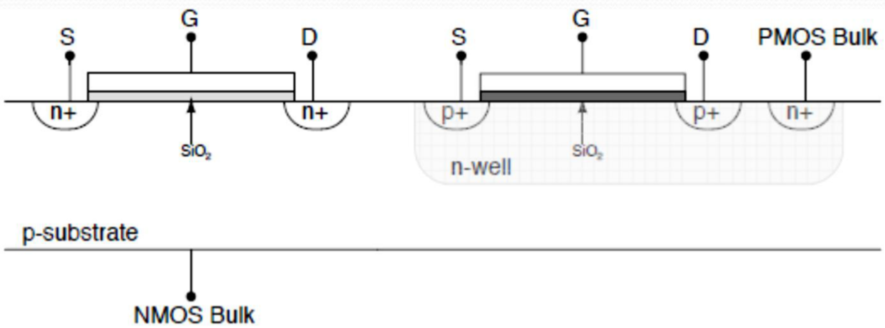
Bulk connections



The MOSFET is a 4-terminal device.

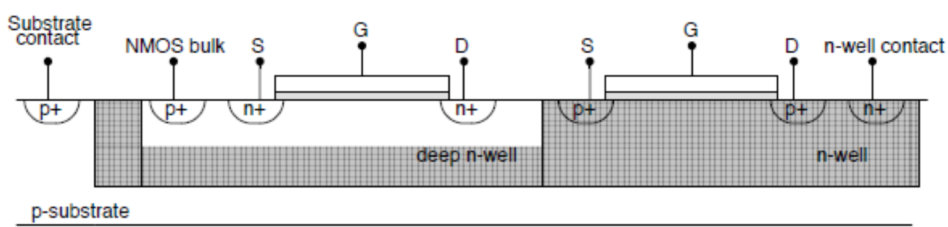
For NMOS

So far we have assumed that the p-substrate is grounded and all PMOS bulks are connected to V_{DD} but these assumptions are not binding.

The connection of the bulk can affect the behavior of the device.

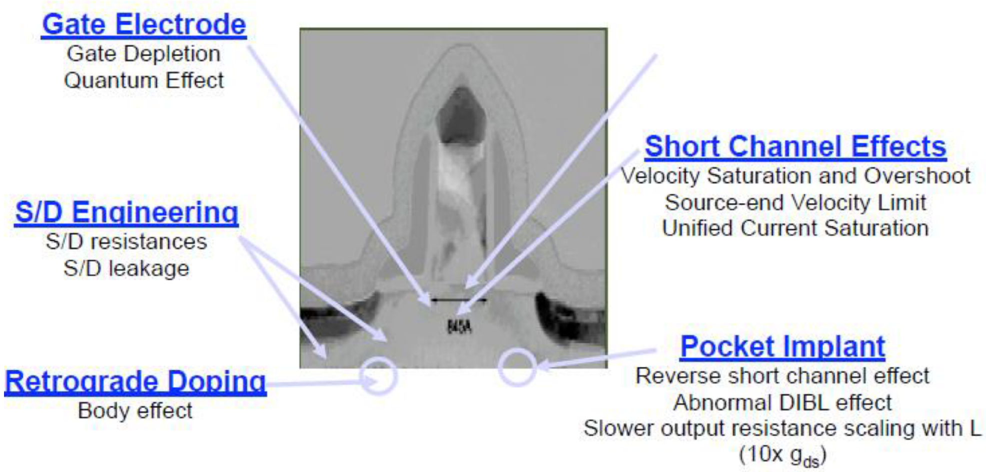
In our technology, PMOS devices have isolated bulk connections but all NMOS bulk nodes are connected through the substrate.

Triple-Well CMOS Technology



- More advanced technologies (e.g., 0.13µm and beyond) typically offer separate bulk connection for all devices.
- The separate connection of NMOS and p-substrate helps reducing noise coupling between different parts (specially between analog and digital sections).

A Real Transistor



Some additional complications…

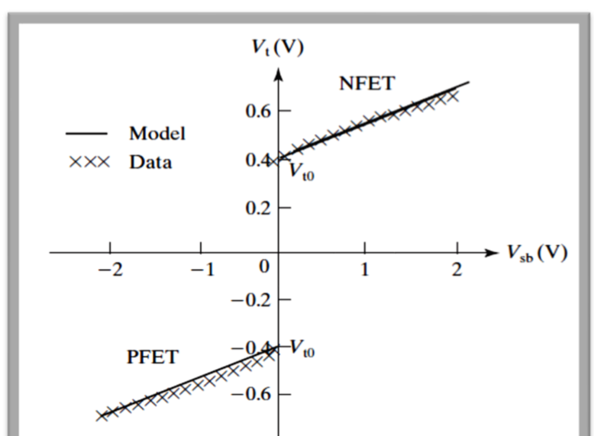
Effective mobility

$$\mu_{ns} = \frac{540\ \text{cm}^2/\text{Vs}}{1 + \left(\dfrac{V_{gs} + V_t + 0.2\ \text{V}}{5.4\,T_{oxe}}\right)^{1.85}}$$

Retrograde Doping

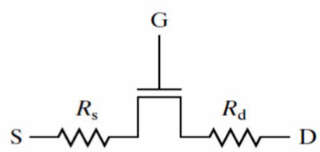
$$\boxed{V_t(V_{sb}) = V_{t0} + \frac{C_{dep}}{C_{oxe}} V_{sb} = V_{t0} + \alpha V_{sb}}$$

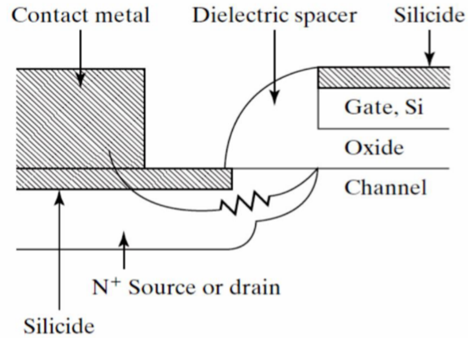
$$\alpha = C_{dep}/C_{oxe} = 3\text{T}_{oxe}/W_{dmax}$$

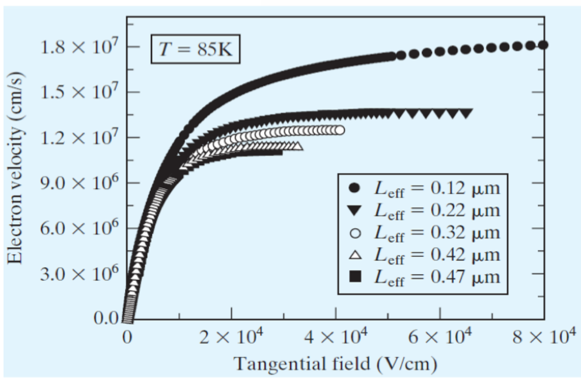


Some additional complications…

$$I_{dsat} = \frac{I_{dsat0}}{1 + R_s I_{dsat0}/(V_{gs} - V_t)}$$





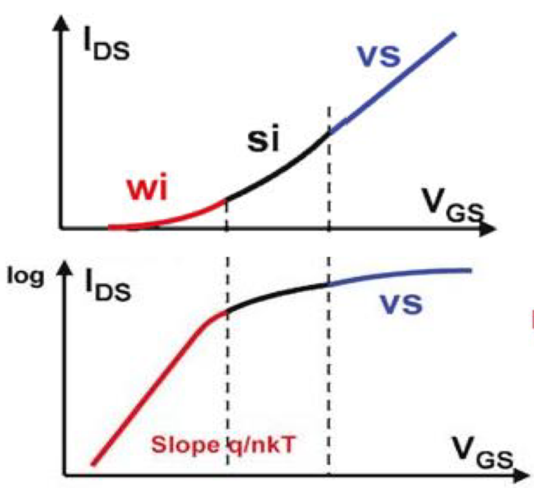


Velocity saturation

$$v = \frac{\mu_{ns}\mathscr{E}}{1 + \mathscr{E}/\mathscr{E}_{sat}}$$

Sub Threshold Conduction

Some additional complications…



$$I_{DSwi} = I_{D0}\frac{W}{L}\exp^{\frac{V_{GS}}{nkT/q}}$$

Current in Weak inversion

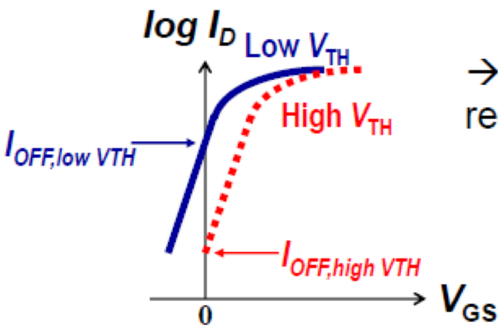
V_{TH} Design Trade-Off

- Low V_{TH} is desirable for high ON-state current:

$$I_{D,sat} \propto (V_{DD} - V_{TH})^{\eta} \qquad 1 < \eta < 2$$

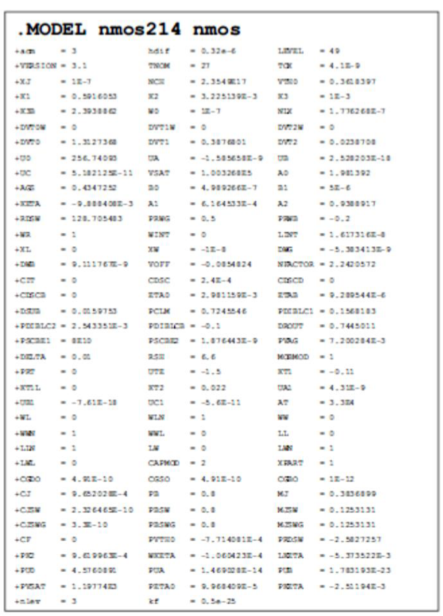
Velocity saturation

- But high V_{TH} is needed for low OFF-state current:



→ V_{TH} cannot be reduced aggressively.

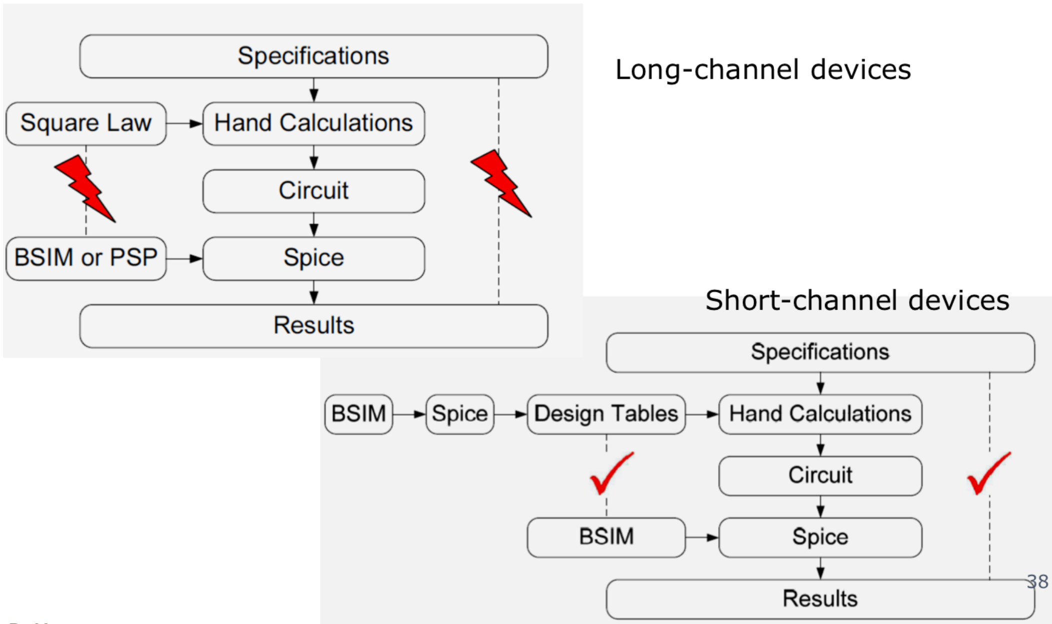
What are μC_{ox} ("KP") and λ ("LAMBDA") for our Technology?



```
.MODEL nmos214 nmos
+acm     = 3             hdif    = 0.32e-6       LEVEL   = 49
+VERSION = 3.1           TNOM    = 27            TOX     = 4.1E-9
+XJ      = 1E-7          NCH     = 2.3549E17     VTH0    = 0.3618397
+K1      = 0.5916053     K2      = 3.225139E-3   K3      = 1E-3
+K3B     = 2.3938862     W0      = 1E-7          NLX     = 1.776268E-7
+DVT0W   = 0             DVT1W   = 0             DVT2W   = 0
+DVT0    = 1.3127368     DVT1    = 0.3876801     DVT2    = 0.0238708
+U0      = 256.74093     UA      = -1.585658E-9  UB      = 2.528203E-18
+UC      = 5.182125E-11  VSAT    = 1.003268E5    A0      = 1.981392
+AGS     = 0.4347252     B0      = 4.989266E-7   B1      = 5E-6
+KETA    = -9.888408E-3  A1      = 6.164533E-4   A2      = 0.9388917
+RDSW    = 128.705483    PRWG    = 0.5           PRWB    = -0.2
+WR      = 1             WINT    = 0             LINT    = 1.617316E-8
+XL      = 0             XW      = -1E-8         DWG     = -5.383413E-9
+DWB     = 9.111767E-9   VOFF    = -0.0854824    NFACTOR = 2.2420572
+CIT     = 0             CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0             ETA0    = 2.981159E-3   ETAB    = 9.289544E-6
+DSUB    = 0.0159753     PCLM    = 0.7245546     PDIBLC1 = 0.1568183
+PDIBLC2 = 2.543351E-3   PDIBLCB = -0.1          DROUT   = 0.7445011
+PSCBE1  = 8E10          PSCBE2  = 1.876443E-9   PVAG    = 7.200284E-3
+DELTA   = 0.01          RSH     = 6.6           MOBMOD  = 1
+PRT     = 0             UTE     = -1.5          KT1     = -0.11
+KT1L    = 0             KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0             WLN     = 1             WW      = 0
+WWN     = 1             WWL     = 0             LL      = 0
+LLN     = 1             LW      = 0             LWN     = 1
+LWL     = 0             CAPMOD  = 2             XPART   = 1
+CGDO    = 4.91E-10      CGSO    = 4.91E-10      CGBO    = 1E-12
+CJ      = 9.652028E-4   PB      = 0.8           MJ      = 0.3836899
+CJSW    = 2.326465E-10  PBSW    = 0.8           MJSW    = 0.1253131
+CJSWG   = 3.3E-10       PBSWG   = 0.8           MJSWG   = 0.1253131
+CF      = 0             PVTH0   = -7.714081E-4  PRDSW   = -2.5827257
+PK2     = 9.619963E-4   WKETA   = -1.060423E-4  LKETA   = -5.373522E-3
+PU0     = 4.5760891     PUA     = 1.469028E-14  PUB     = 1.783193E-23
+PVSAT   = 1.19774E3     PETA0   = 9.968409E-5   PKETA   = -2.51194E-3
+nlev    = 3             kf      = 0.5e-25
```

- The HSpice model for an NMOS device in our technology is shown to the left
- This is a 110-parameter BSIM3v3 model
  - More recent models may require even more parameters (e.g. PSP, BSIM6)
  - KP and LAMBDA are nowhere to be found
- It turns out that the I-V characteristics of a modern MOSFET cannot be accurately described by the square law

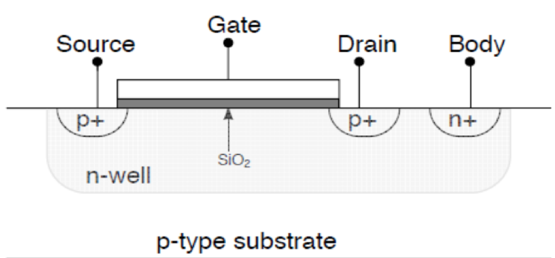
Design strategies



B. Murmann

PMOS vs NMOS

If we reverse all voltages and switch all dopings their opposite type, we will have a PMOS.



Body should be connected to the highest potential in the circuit.

For PMOS, V_t is negative.

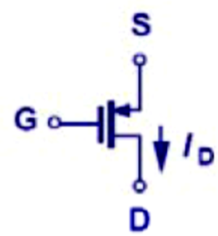
Typically, provides lower current for the same voltage due to holes having a smaller μ than electrons.

Everything we have derived so far is equally applicable to PMOS. You only need to put absolute values around every term in all our equations.

PMOS *I-V* Equations

$$I_{D,tri} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left[2(V_{SG}-V_{TH})V_{DS}-V_{DS}^2\right] \qquad DS \leftrightarrow SD \quad GS \leftrightarrow SG$$

$$= \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left[2(|V_{GS}|-|V_{TH}|)|V_{DS}|-V_{DS}^2\right]$$



Long Channel:

$$I_{D,sat} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{SG}-V_{TH})^2\left[1+\lambda\left(V_{SD}-V_{SD,sat}\right)\right]$$

$$= \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(|V_{GS}|-|V_{TH}|)^2\left[1+\lambda\left(|V_{DS}|-|V_{D,sat}|\right)\right]$$

Short Channel:

$$I_{D,sat} = v_{sat}WC_{ox}(V_{SG}-V_{TH})\left[1+\lambda\left(V_{SD}-V_{SD,sat}\right)\right]$$

$$= v_{sat}WC_{ox}(|V_{SG}|-|V_{TH}|)\left[1+\lambda\left(|V_{DS}|-|V_{D,sat}|\right)\right]$$

Note: $V_{GS}<0, V_{DS}<0, V_{D,sat}<0, V_{TH}<0$ in PMOS

Taylor series

- Single variable:

$$f(x)=\sum_{k=0}^{\infty}\frac{f^{(k)}(a)}{k!}(x-a)^k = f(a)+f'(a)(x-a)+\frac{f''(a)}{2!}(x-a)^2+\cdots$$

$$f(x)\approx f(a)+f'(a)(x-a) \quad \text{linear approximation}$$

- Multiple variables (linear approximation):

$$\boxed{f(x,y)=f(a,b)+f_x(a,b)(x-a)+f_y(a,b)(y-b)}$$

→ lets try to apply this concept to the saturation current that we have in our MOSFET device.

* $y = f(x)$ → If we have a function like this

$$\boxed{y_0 + \Delta y = f(x_0) + f'(x_0)\Delta x}$$

for small variations

where

$$y_0 = f(x_0)$$

$$\Delta y = f'(x_0)\Delta x$$

what if $\boxed{y = f(x, z)}$

then

$$\boxed{y_0 + \Delta y = f(x_0, z_0) + \frac{\partial f}{\partial x}\Delta x + \frac{\partial f}{\partial z}\Delta z}$$

→ Applying this concept of Multivariable calculus to the saturation current Equation

$$\boxed{I_D = \frac{\beta'}{2}\frac{W}{L}(V_{GS} - V_t)^2(1 + \lambda V_{DS})}$$

$$\boxed{V_T = V_{T0} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right)}$$

$\rightarrow$ $\therefore$ The saturation current is dependent on $\boxed{3}$ quantities V_{GS}, V_{DS}, V_{SB}

Gate Source voltage

Drain-Source voltage

Source Bulk voltage

$$\therefore \boxed{I_D = I_D(V_{GS}, V_{DS}, V_{SB})}$$

According to Taylor's Series Expansion

$$I_D = \underbrace{I_{D_0}}_{\text{Nominal Value}} + \underbrace{\text{variations w.r.to 3 quantities}}_{\text{w.r.to } V_{GS}, V_{DS}, V_{SB}}$$

$$\therefore I_D = I_{D_0} + i_d$$ $\rightarrow$ variation of current around Nominal value

Similarly

$$V_{GS} = V_{GS_0} + v_{gs}$$ $\rightarrow$ variation of Gate-Source

These are called Small Signal Variations

$$V_{DS} = V_{DS_0} + v_{ds}$$

$$V_{BS} = V_{BS_0} + v_{bs}$$

→ If we combine all this using Taylor series Expansion.

$$\boxed{I_{D_0} = I_D(V_{GS0}, V_{DS0}, V_{SB0})}$$

$$\boxed{i_d = \frac{\partial I_D}{\partial V_{GS}} \cdot v_{gs} + \frac{\partial I_D}{\partial V_{DS}} \cdot v_{ds} + \frac{\partial I_D}{\partial V_{BS}} \cdot v_{bs}}$$

This formula is the most important in our course

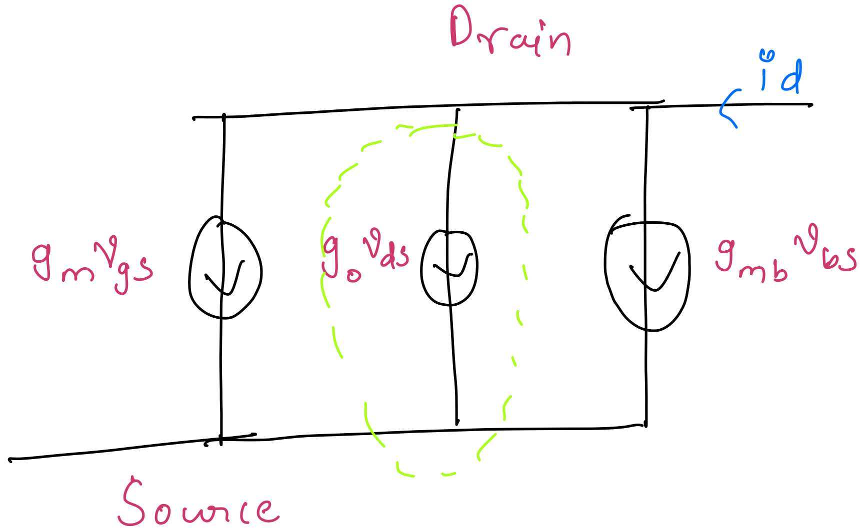
Because the small signal Model is derived from the taylor Expansion.

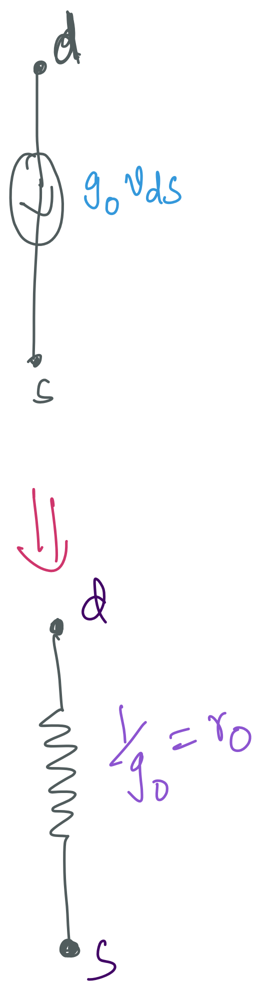
$$i_d = \underbrace{\frac{\partial I_D}{\partial V_{GS}}}_{g_m} \cdot v_{gs} + \underbrace{\frac{\partial I_D}{\partial V_{DS}}}_{g_o} \cdot v_{ds} + \underbrace{\frac{\partial I_D}{\partial V_{BS}}}_{g_{mb}} \cdot v_{bs}$$

g_m (Transconductance) (Ω^{-1})

g_{mb} Bulk Transconductance

→ We can turn this Algebraic expression into a circuit Equivalent. Small Signal Model because it maps small changes in the Drain current with respect to variations in V_{GS}, V_{DS}, V_{BS}





∵ the current through this C.S is controlled by voltage across V_{DS}.

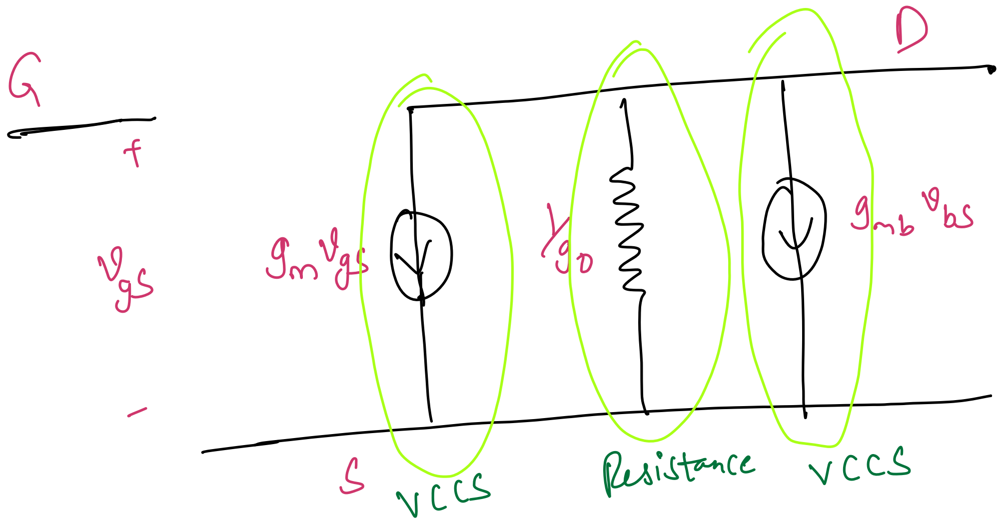
∴ It can be Replace by a Resistor with Resistance

$$\boxed{r_o = \frac{1}{g_o}}$$

"But this is not the case for $g_m v_{gs}$, $g_{mb} v_{bs}$

Because they appear b/w DS and are dependent on v_{gs} and v_{bs} not v_{DS}

∴ The the small signal Model would be



∴ If we are in the Neighbourhood of our Quiescent point or operating point, That variation are small. Then we can transform our Non linear circuit into combination of linear elements.

→ The above simple Sub-Circuit describes the behaviour of Transistor. we have drawn a linearised circuit based on the partial differential equation

$$\boxed{\hat{i}_d = \underbrace{\frac{\partial I_D}{\partial V_{GS}}}_{g_m} i_{gs} + \underbrace{\frac{\partial I_D}{\partial V_{DS}}}_{g_o} v_{ds} + \underbrace{\frac{\partial I_D}{\partial V_{SB}}}_{g_{mb}} v_{SB}}$$

→ we know that g_m, g_o, g_{mb} play a critical role in the function of the MOSFET.

Q How can we play with g_m, g_o, g_{mb} possibly with the tools we have as a designer?

→ First of all lets compute this quantity so that we can infer how can these quantities define the operation of MOSFET.

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

This derivative must be calculated at a specific operating point in saturation region.

∴ we have $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS})$

or

$$I_D = \frac{\beta'}{2}\frac{W}{L}(V_{GS}-V_T)^2\underbrace{(1+\lambda V_{DS})}$$

For the sake of calculation of g_m we neglect this term.

usually $0.1 \leq \lambda \leq 0.2$

$$\therefore \quad g_m = \frac{\partial I_D}{\partial V_{GS}}$$

if we compute this derivative we get

$$\boxed{g_m = 2(V_{GS}-V_T)\,\frac{\beta'}{2}\,\frac{W}{L}}$$

$$\therefore \quad g_m = \beta' \frac{W}{L}(V_{GS}-V_T)$$

$$\boxed{g_m = \beta(V_{GS}-V_T)}$$

g_m can also be written as using I_D expression

$$\Rightarrow \quad g_m = \beta(V_{GS}-V_T)$$

from $I_D = \frac{1}{2}\beta(V_{GS}-V_T)^2$

$$\Rightarrow \quad \sqrt{\frac{2I_D}{\beta}} = V_{GS}-V_T$$

$$\Rightarrow \quad g_m = \beta\sqrt{\frac{2I_D}{\beta}}$$

$$\boxed{g_m = \sqrt{2I_D\beta}}$$

we can also write

$$\beta = \frac{2I_D}{(V_{GS}-V_T)^2}$$

If we substitute β in $g_m = \sqrt{2I_D\beta}$

then

$$g_m = \sqrt{2I_D\beta}$$

$$= \sqrt{2I_D\left(\frac{2I_D}{(V_{GS}-V_T)^2}\right)}$$

$$\boxed{g_m = \frac{2I_D}{V_{GS}-V_T}}$$

$$\therefore \boxed{g_m = (V_{GS}-V_T)\beta = \sqrt{2I_D\beta} = \frac{2I_D}{V_{GS}-V_T}}$$

Here we have

$$\left.\begin{array}{c} g_m \propto \sqrt{I_D} \\ \& \\ g_m \propto I_D \end{array}\right\}$$

Q which one is correct ?

Ans:- Both are correct and it depends on the other variables which ones are constant which ones are Not.

→ To calculate $g_O = \frac{\partial I_D}{\partial V_{DS}}$

$\Rightarrow \quad I_D = I_{D0}(1+\lambda V_{DS})$

$$\Rightarrow \boxed{\frac{\partial I_D}{\partial V_{DS}} = I_{D0} \cdot \lambda}$$

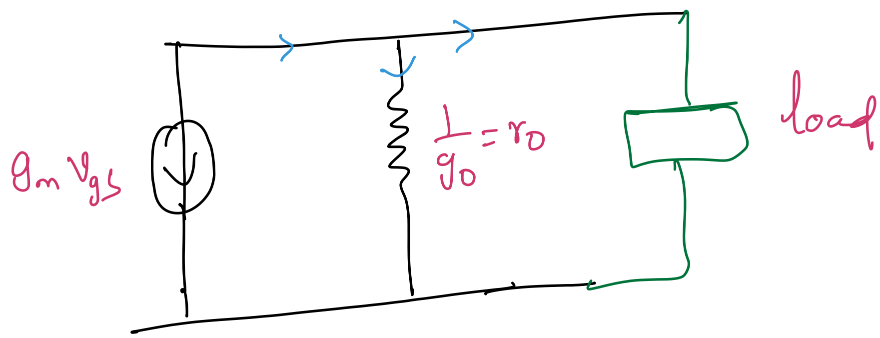
The units of λ is $\frac{1}{\text{volt}}$

→ The calculation of $g_{mb} = \frac{\partial I_D}{\partial V_{SB}}$ is in the slide above Back gate Effect

$$\boxed{g_{mb} = g_m \frac{\gamma}{2\sqrt{2\phi_F + V_{SB}}}}$$

g_{mb} is order of the magnitude $\frac{1}{10}$ of g_m ∴ g_{mb} is mostly Ignored.

→ ∴ The New small signal can be drawn as

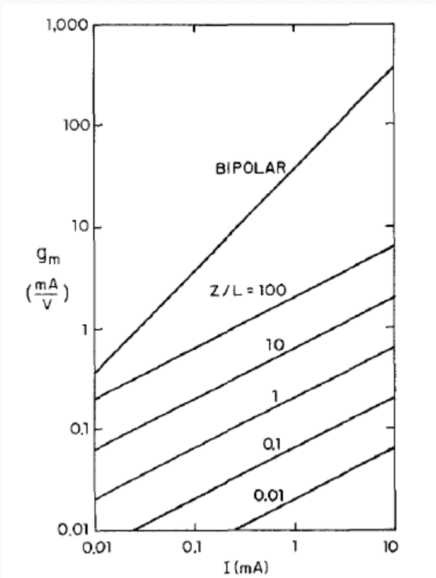


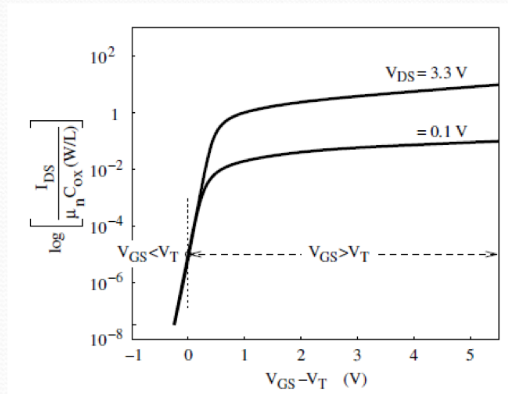
→ Ideally we would like all the current generated by the VDCS to the load and for this to happen g_o should be low so that the r_o will be high (CLM parameter). And all the current flows to the Load.

∴ g_m should be Larger

g_o should be as Low as possible

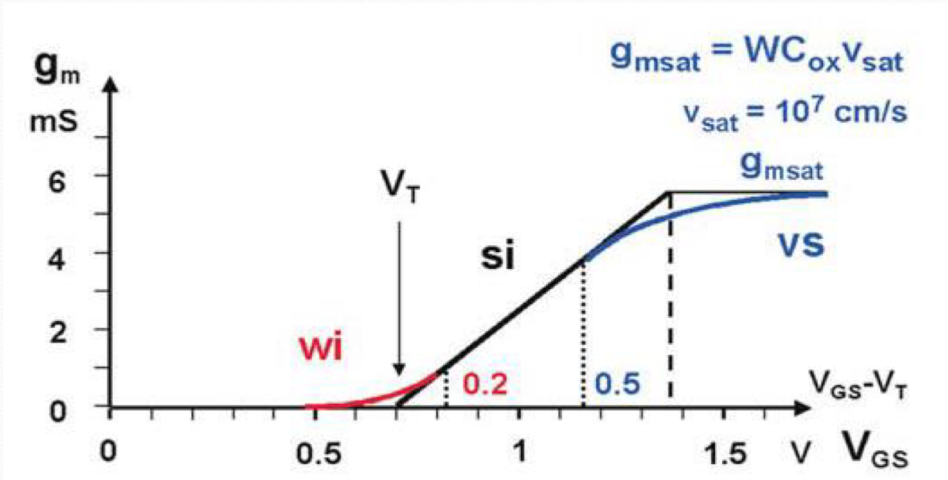
MOS vs BJT transconductance





→ In case of BJT we have large Transconductance when compared to MOSFET

Transconductance and MOS non-idealities



→ g_m saturates and can't Increase further because of velocity saturation.

$$g_m \propto (V_{GS} - V_T)$$

But as V_{GS} ↑ the g_m increase but after certain point it saturates.

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