

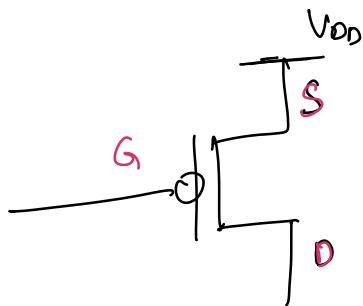
## Lecture-5

→ we have already discussed the small signal model of NMOS.

The modelling of the device, <sup>in saturation</sup>, can be arranged in terms of 3 subcomponents related to the

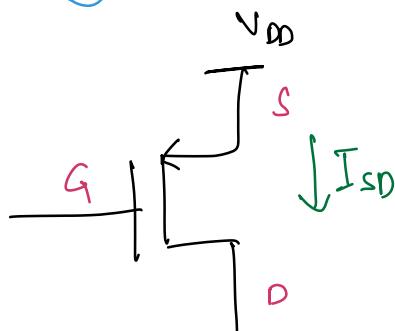
- i) Transconductance  $g_m$
- ii) o/p conductance  $g_o$
- iii) Body Effect  $g_{mb}$

→ Now let's see what happens with the PMOS



↑ con

In many configurations, source of the PMOS is directly connected to the supply voltage.



we know that when the PMOS is on the current flows from source to the drain

→  $I_{SD}$  is given by this expression  
 $\rightarrow$  Source is more negative than Gate when compared to Drain

$$I_{SD} = \frac{B_p}{2} \cdot \frac{W}{L} \left[ (V_{SG} - |V_{TP}|) \right]^2 (1 + \gamma_p \frac{|V_{SD}|}{V_{SD}})$$

→ we also have an expression for the threshold

$$|V_{TP}| = |V_{TP_0}| + \gamma_p \sqrt{2\phi_F + V_{BS} - \sqrt{2\phi_F}}$$

→ So, How to get small signal Analysis of PMOS ?

Ans It's pretty much like we did in NMOS case. so what we have to do is to find partial derivative of the current w.r.t different voltages applied to the PMOS Transistor.

$$(i) \quad \frac{\partial I_{SD}}{\partial V_{SD}} = \gamma_p \left[ \frac{B_p}{2} \cdot \frac{W}{L} (V_{SG} - |V_{TP}|)^2 \right]$$

$$\hat{=} \boxed{\gamma_p I_{SD}} = g_o$$

$$\frac{B_p^1 W}{P_p L} = B_p$$

(ii)  $\frac{\partial I_{SD}}{\partial V_{SG}} = \beta_p (V_{SG} - V_{TP})$

↓

$\sqrt{2\beta_p I_{SD}} = g_m$

by neglecting effect  
of channel length  
Modulation.  
as an approximation.

(iii)  $\frac{\partial I_{SD}}{\partial V_{BS}} = \frac{\partial I_{SD}}{\partial |V_{TP}|} \frac{\partial |V_{TP}|}{\partial V_{BS}} = -g_m \cdot n = -g_{mb}$

Here we have  $V_{BS}$  as in PMOS where  $n = \frac{\gamma_p}{2\sqrt{2\phi_p + V_{BS}}}$

Bulk should be connected most positive terminal

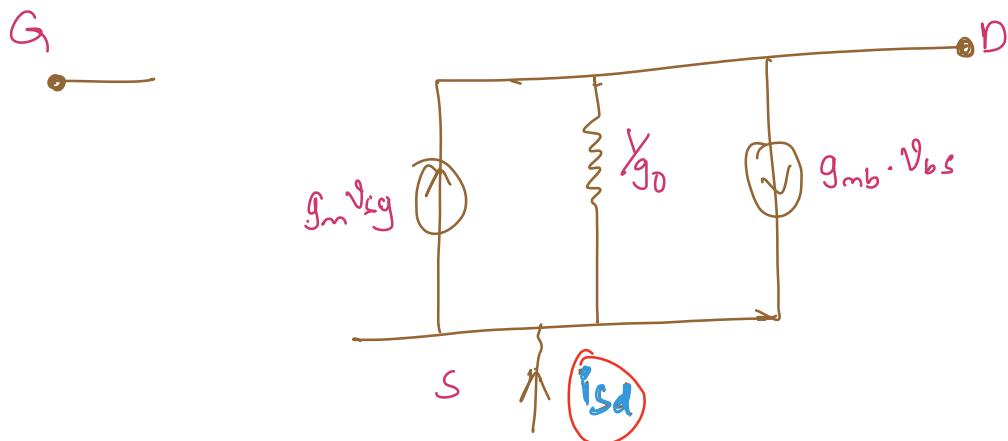
→  $i_{sd} = \frac{\partial I_{SD}}{\partial V_{SG}} V_{SG} + \frac{\partial I_{SD}}{\partial V_{SD}} \cdot V_{SD} + \frac{\partial I_{SD}}{\partial V_{BS}} \cdot V_{BS}$

Small variation in saturation current in PMOS

⇒  $i_{sd} = g_m V_{SG} + g_o V_{SD} - g_{mb} V_{BS}$

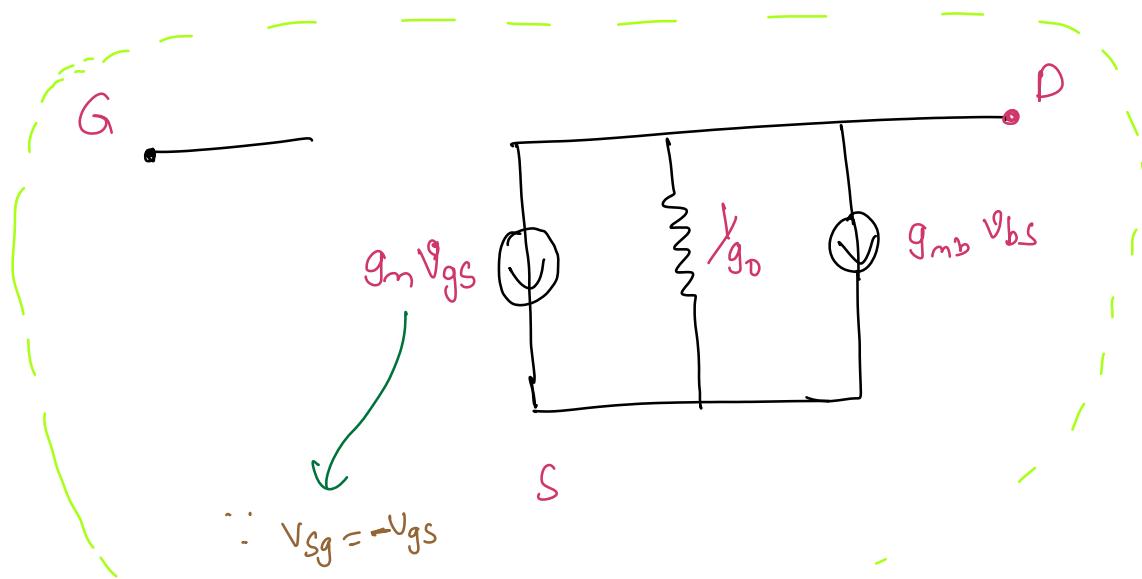
We can Translate this Analytical expression  
into circuit

→  $i_{sd} = g_m V_{SG} + g_o V_{SD} - g_{mb} V_{BS}$



→ If we are more interested in describing the opposite current i.e

$$i_{ds} = -i_{sd}$$



Note:- Interacting thing related to small signal circuit of PMOS is

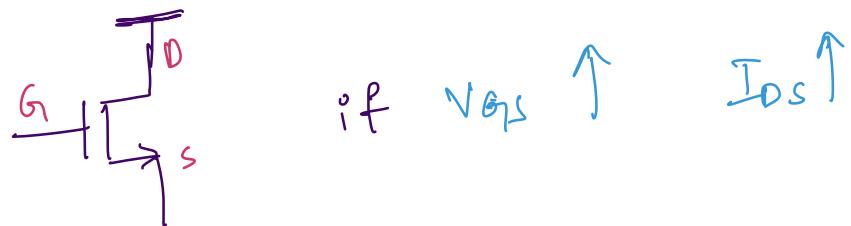
The small signal circuit of PMOS is equivalent to small signal circuit of NMOS

This is very useful for circuit analysis.

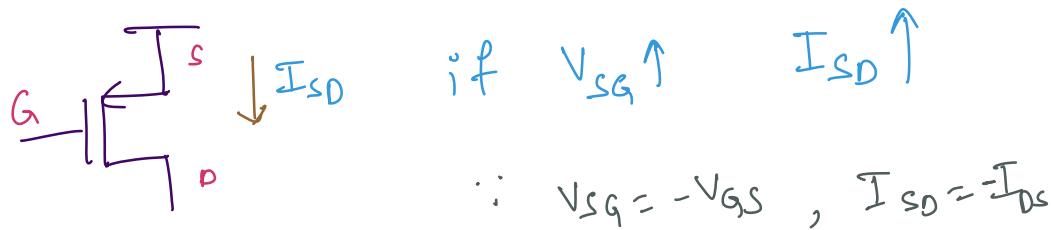
The equivalence is nothing the behaviour to variation is exactly the same.

→ This can be a bit counter intuitive.

If we look at an NMOS



If we look at PMOS



→ we can also say for PMOS



This is similar to what happens in NMOS.

∴ Bottomline is that in terms of variations both

PMOS & NMOS have same effect.

→ If we look at PMOS & NMOS from the perspective of Total current and Total voltage applied both are rather different.

→ But if we look at these devices from small signal perspective which is interested in variations induced by voltages to currents & vice versa then both look similar.

→ It is very important to understand this because we are going to transform very complicated circuit from Large signal to small signal one and it must be very clear what we are doing for both PMOS & NMOS.

### Analysis of PMOS in Linear & Triode Region

For NMOS we have

$$I_{DS} = \beta \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

if we calculate partial derivative of  $I_D$  w.r.t  $V_{GS}$ ,  $V_{BS}$ ,  $V_{DS}$

(i) Then

$$g_m \text{Triode} = \frac{\partial I_{DS}}{\partial V_{GS}} = \boxed{\beta V_{DS} \neq g_{m\text{sat}}}$$
  

(ii)

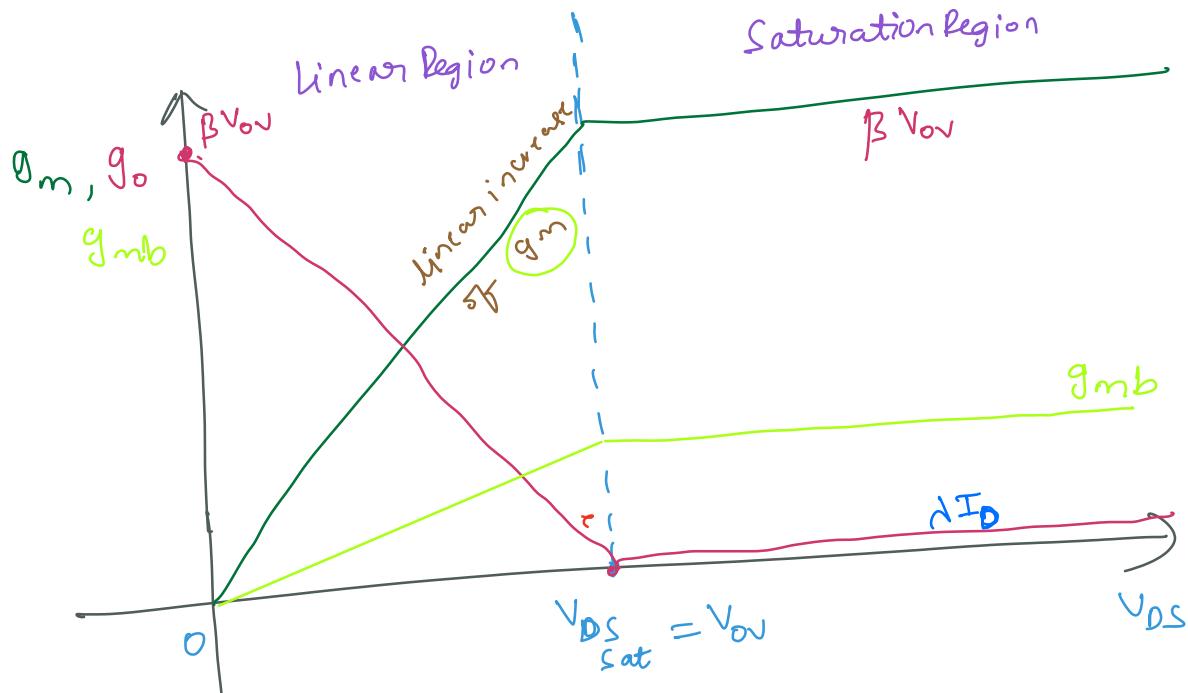
$$g_{mb} \text{Triode} = \frac{\partial I_{DS}}{\partial V_{BS}} = \boxed{g_m \downarrow} \quad \eta = \frac{\gamma}{2\sqrt{\phi_F + V_B}}$$
  

(iii)

$$g_o \text{Triode} = \frac{\partial I_{DS}}{\partial V_{DS}} = \boxed{\beta V_{ov} - \beta V_{DS} = \beta [V_{ov} - V_{DS}]}$$

→ Here in Triode Region we can see that

$g_m$  &  $g_o$  both depend on  $V_{DS}$



→ This is the trend of  $g_m$  &  $g_o$  in linear & saturation region of operation of MOSFET  
That is we operate mostly in saturation region of MOSFET for Analog Circuits.  
Because we expect a stable amplification.

Note: In the above graph we did not mention  $g_{mb}$  because  $g_{mb}$  is related to  $g_m$ .

$$g_{mb} = g_m \eta$$

where  $\eta = \frac{1}{10}$   
usually

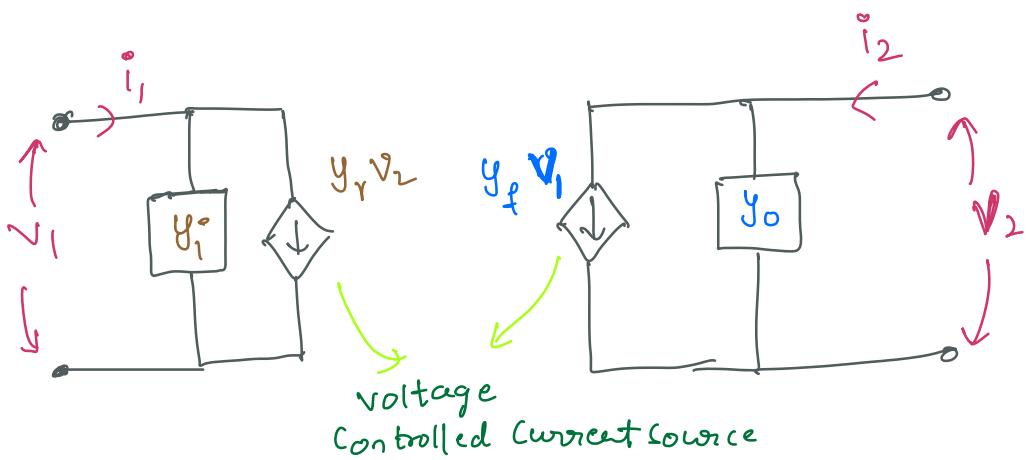
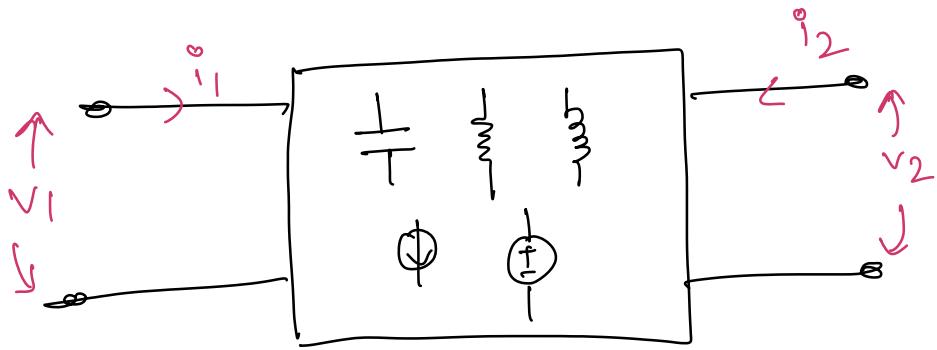


### 2-port Networks

Important tool in the Analysis of Complex circuit Behaviour

→ whenever we a circuit consisting of linear components. It can be capacitors, resistors, Inductors, linearly controlled current generator & voltage generators. No matter how complex.

In this case we can neglect what is Inside the complex circuit and just characterize the circuit from the Port perspective.



$y_i^o$  : Input Admittance

$y_o$  : output Admittance

→ According to KCL

$$i_1 = y_i^o v_1 + y_r v_2$$

$$i_2 = y_f v_1 + y_o v_2$$

} we can study this system of linear equations with Linear Algebra tools

we would be particularly interested in the

## "Admittance Matrix"

$$Y = \begin{bmatrix} y_1 & y_{\gamma} \\ y_{\gamma} & y_0 \end{bmatrix}$$

Q How to determine  $\gamma$ -parameters of the Admittance Matrix in general for complex circuit?

Ans

If we look at admittance matrix

$$y_1^o = \frac{\overset{\circ}{i}_1}{v_1} \quad \text{for } v_2 = 0 \text{ i.e. } v_{out} = 0$$

o/p port short circuited

similarly

$$y_{\gamma} = \frac{\overset{\circ}{i}_1}{v_2} \quad \text{for } v_1 = 0 \text{ i.e. } v_{in} = 0$$

i/p port short Circuited

$$y_f = \frac{\overset{\circ}{i}_2}{v_1} \quad \Big|_{v_2=0}$$

$$y_0 = \frac{\overset{\circ}{i}_2}{v_2} \quad \Big|_{v_1=0}$$

∴ whenever we have complex circuit, if we want  $y_i^*$  then we have short circuit the o/p port and investigate simply the relationship b/w  $v_i + i_i$

→ Let's see how we use these parameters in circuit Representations in practice.

$$Y_i^* = \frac{i_i}{v_i^*} = \frac{1}{z_i} \neq y_i^*$$

generic input Admittance

$$y_i^* = Y_i^* \text{ only when } v_2 = 0$$

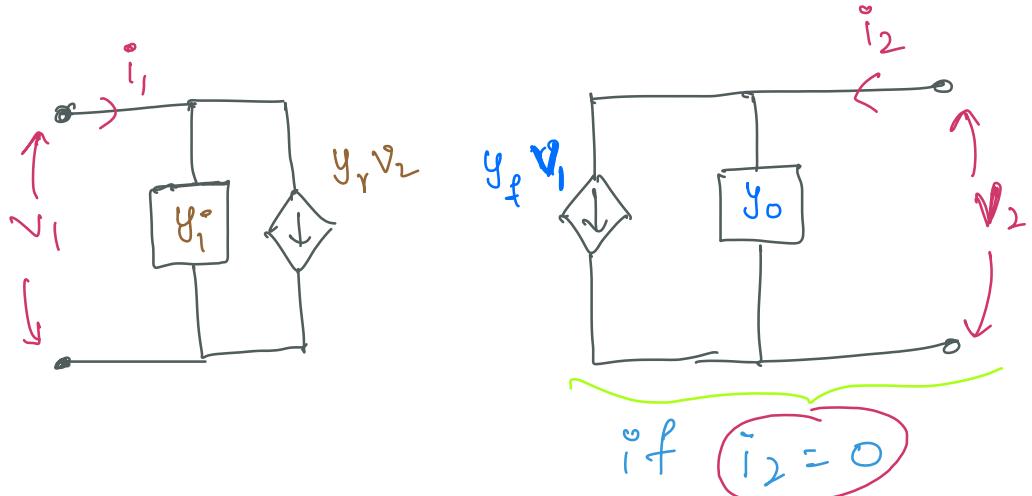
Q what is  $y_i^*$  when o/p is open circuit, i.e.  $i_2 = 0$ ?

$$Y_i^*|_{i_2=0}$$

(open circuit) ?

Ay





\*then the current in  $y_o$ , should be equal to the current in the voltage controlled current source

$$y_f v_1$$

$$\Rightarrow v_2 y_o = -y_f v_1$$

$$\Rightarrow v_2 = -\frac{y_f}{y_o} v_1$$

if we plug this value to the i/p End.  
Then we will have.

$$i_1 = y_i v_1 + y_r v_2$$

$$i_1 = y_i v_1 + y_r \left( -\frac{y_f}{y_o} v_1 \right)$$

$$\Rightarrow i_1 = \left( y_i - \frac{y_r y_f}{y_o} \right) v_1$$

$$\Rightarrow \boxed{\frac{i_1}{v_1} = y_i - \frac{y_r y_f}{y_o}}$$

$$\Rightarrow Y_{i1} \Big|_{i_2=0} = \frac{i_1}{v_1} = y_i - \frac{y_r y_f}{y_o}$$

$$\Rightarrow \boxed{Y_i = \frac{y_i y_o - y_r y_f}{y_o}}$$

Detourineet  
of  $Y$   
matrix

$$\Rightarrow \boxed{Y_i \Big|_{i_2=0} = \frac{\Delta Y}{y_o}} \quad \text{--- } 1$$

$$Y = \begin{bmatrix} y_i & y_r \\ y_f & y_o \end{bmatrix}$$

\* earlier we had  $v_2 = -\frac{y_f}{y_o} v_1$

Voltage Gain  $\Rightarrow$

$$\boxed{\frac{v_2}{v_1} = \text{Gain} = A_v = -\frac{y_f}{y_o}} \quad \text{--- } 2$$

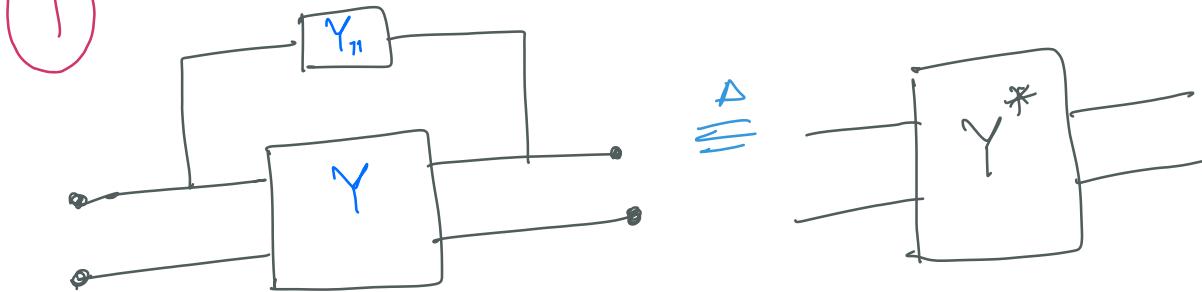


Similarly

$$Y_o \Big|_{i_2=0} = \frac{\Delta Y}{y_i} \quad \xrightarrow{*} \quad ③$$

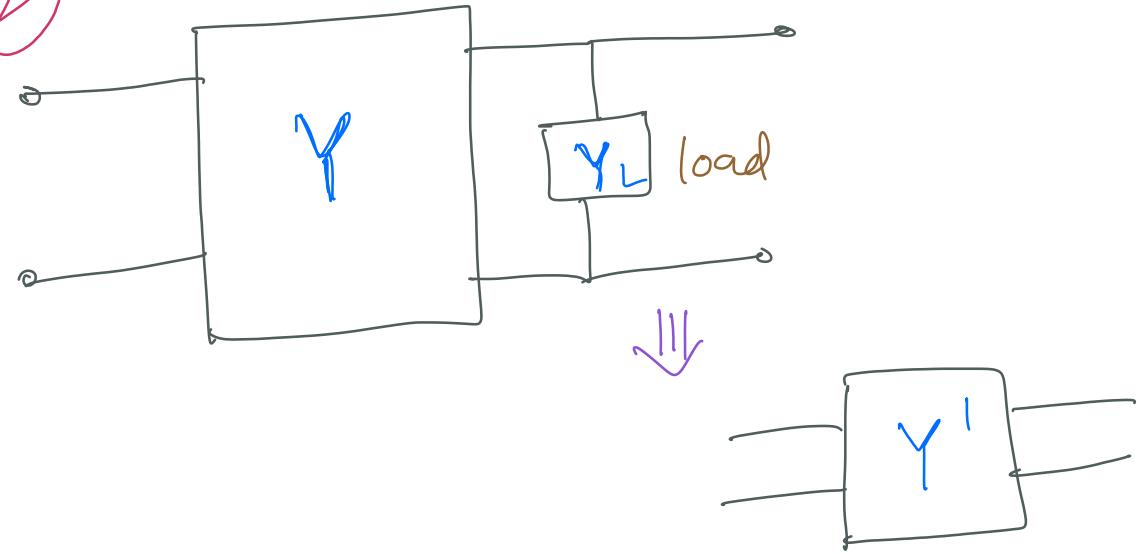
→ Current Gain :  $A_i = \frac{y_f}{y_i}$   $\rightarrow Y$

\* If we have two circuits in parallel.



$$\begin{array}{|l|l|} \hline & Y_i^* = y_i + Y_{11} \\ \hline & Y_f^* = y_f - Y_{11} \\ \hline \end{array} \quad \begin{array}{|l|} \hline Y_r^* = y_r - Y_{11} \\ \hline Y_o^* = y_o + Y_{11} \\ \hline \end{array}$$

\* ②

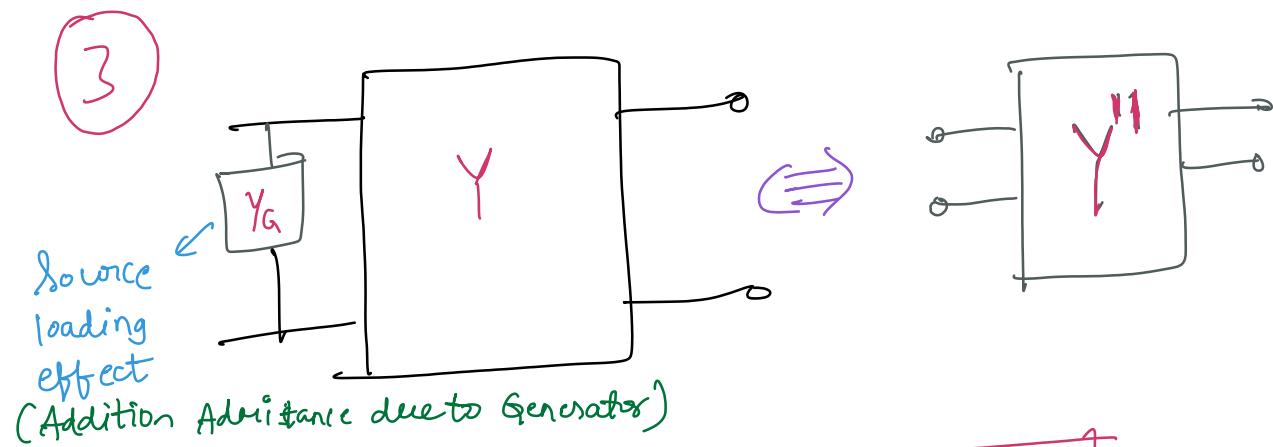


|              |                    |
|--------------|--------------------|
| $y_1' = y_1$ | $y_r' = y_r$       |
| $y_f' = y_f$ | $y_o' = y_o + Y_L$ |

This result is quite interesting because basically it allows you to calculate the voltage gain of the Transistor where

$Y_L$  is the load.

$$\Rightarrow A_v = \frac{v_2}{v_1} = -\frac{y_f'}{y_o'} = \frac{-y_f}{y_o + Y_L}$$



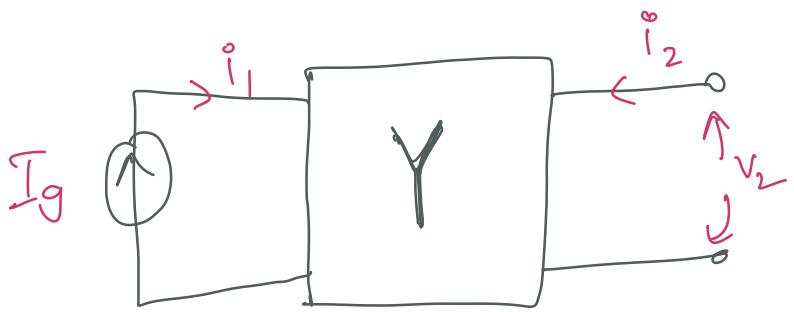
|                     |               |
|---------------------|---------------|
| $y_i'' = y_i + Y_G$ | $y_y'' = y_y$ |
| $y_f'' = y_f$       | $y_o'' = y_o$ |

∴ The current Gain  $A_i$  can be written  
for a circuit source loading.

⇒

$$A_i = \frac{i_2}{i_1} = \frac{y_f''}{y_i''} = \frac{y_f}{y_i + Y_G}$$

④ Circuit Configuration



$$\left. \frac{V_2}{I_g} \right|_{i_2=0} = ? = \text{It is called Trans Resistance of Circuit}$$

$\Rightarrow \frac{V_2}{I_g} = \left. \frac{V_2}{V_1} \cdot \frac{V_1}{I_g} \right|_{i_2=0}$

$$\because I_g = i_1$$

But

$$\left. \frac{V_1}{I_g} \right|_{i_2=0} = \frac{V_1}{i_1}$$

$$\boxed{\frac{V_2}{I_g} = \left. \frac{V_2}{V_1} \right|_{i_2=0} \cdot \left. \frac{V_1}{i_1} \right|_{i_2=0}}$$

$$\frac{V_2}{V_1} = A_V \quad \text{for } i_2 = 0$$

$$\frac{V_1}{I_1} = \frac{1}{Y_i} \quad \text{for } i_2 = 0$$

⇒

$$\frac{V_2}{I_g} = A_V \cdot \frac{1}{Y_i} \quad \text{for } i_2 = 0$$

$$\frac{V_2}{I_g} = -\frac{y_f}{y_o} \cdot \frac{y_o}{\Delta Y}$$

$$\frac{V_2}{I_g} \rightarrow -\frac{y_f}{\Delta Y} \quad \text{for } i_2 = 0$$

\*

Transresistance

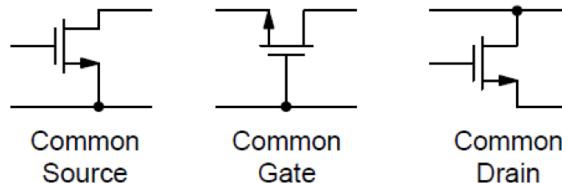
These are the Basic Circuit Analysis  
 Techniques that are need for the Course  
 and many more we will learn in  
 Future.

### Amplifier stages

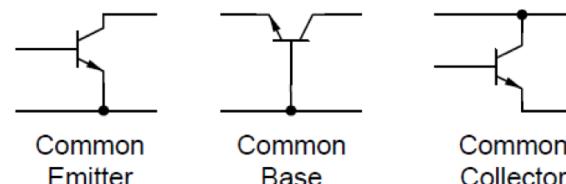


## Basic Single-Stage Amplifier Configurations

MOS



Bipolar



Transconductance Stage

Current Buffer

Voltage Buffer

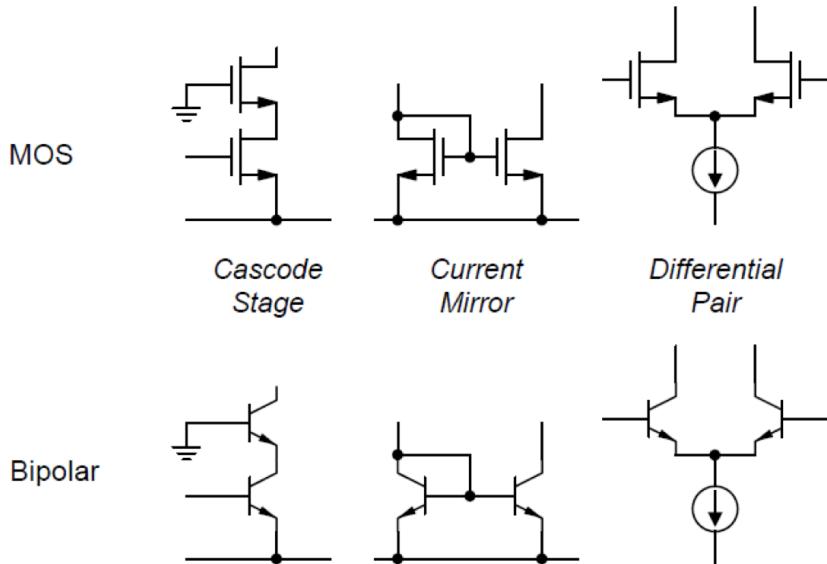
Amplification stage  
→ Input voltage is  
Translated into o/p  
current.

Current Buffer  
needs to have  
very low i/p impedance  
and very high output  
impedance

Voltage Buffer

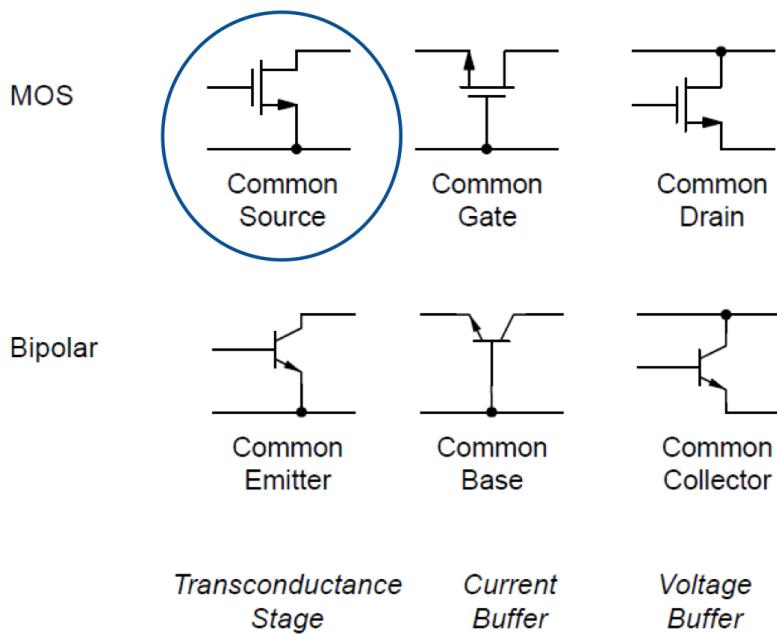
Has very high i/p  
impedance  
and very low o/p impedance  
Because voltage needs to  
directly transferred to load.

## Widely Used Two-transistor Circuits

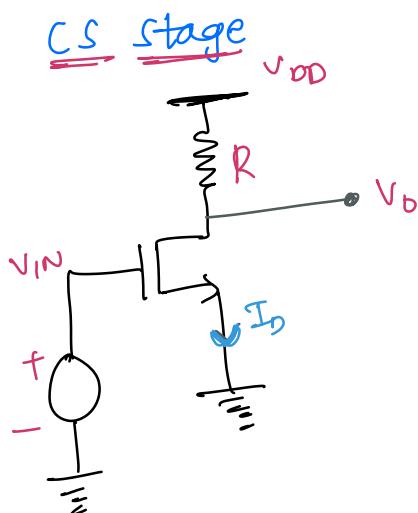
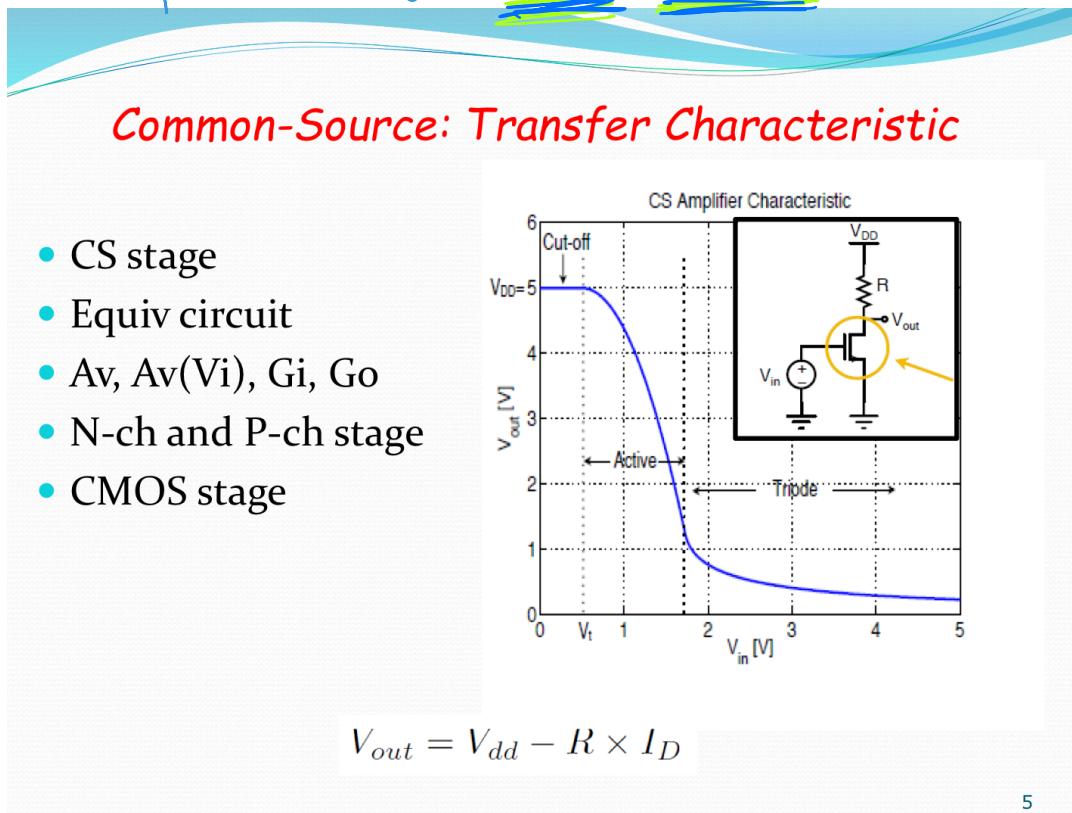


The circuits we will study in this course

## Basic Single-Stage Amplifier Configurations



→ Before getting into 2 Transistor circuit, It's good to get familiarize with single Transistor Amplifier stage. common source



This is the large signal model of the circuit.

where,

$$V_{IN} = V_{GS}$$

$$V_O = V_{DD} - R I_D$$

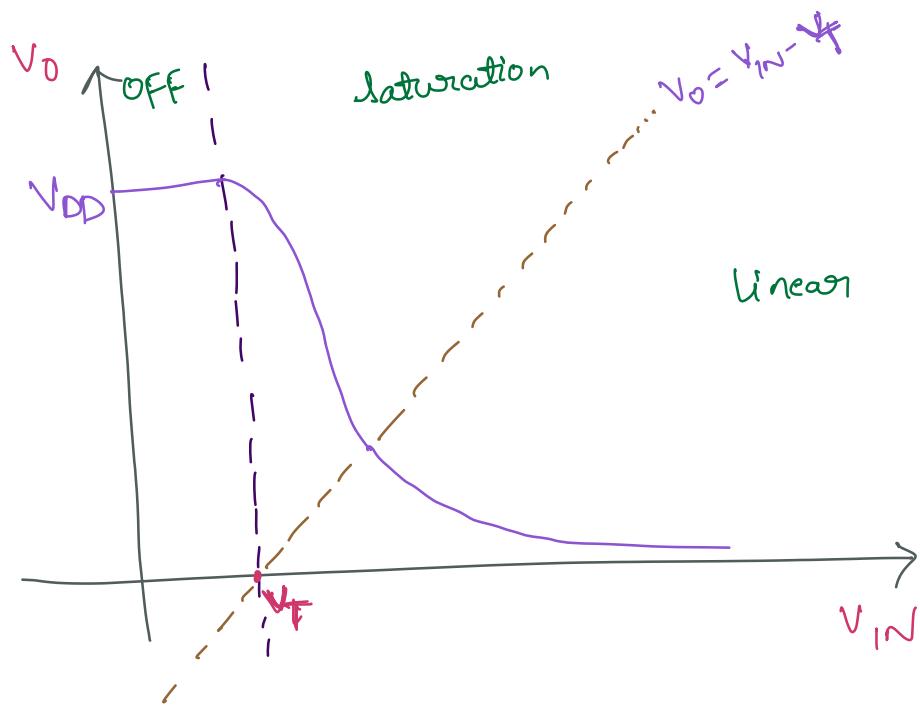
when device is in saturation

\*  $I_D = \frac{1}{2} (V_{GS} - V_T)^2 \rightarrow \text{saturation}$

$$I_D = B \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

↳ linear

I/p - o/p characteristics of common source stage



In Saturation

If  $V_{GS}$  ↑ then  $I_D$  ↑

If  $I_D$  ↑ then  $V_o = V_{DD} - I_D R \downarrow$

In Linear Region

If  $V_{GS}$  ↑  $I_D$  ↑  $\Rightarrow V_o \downarrow$

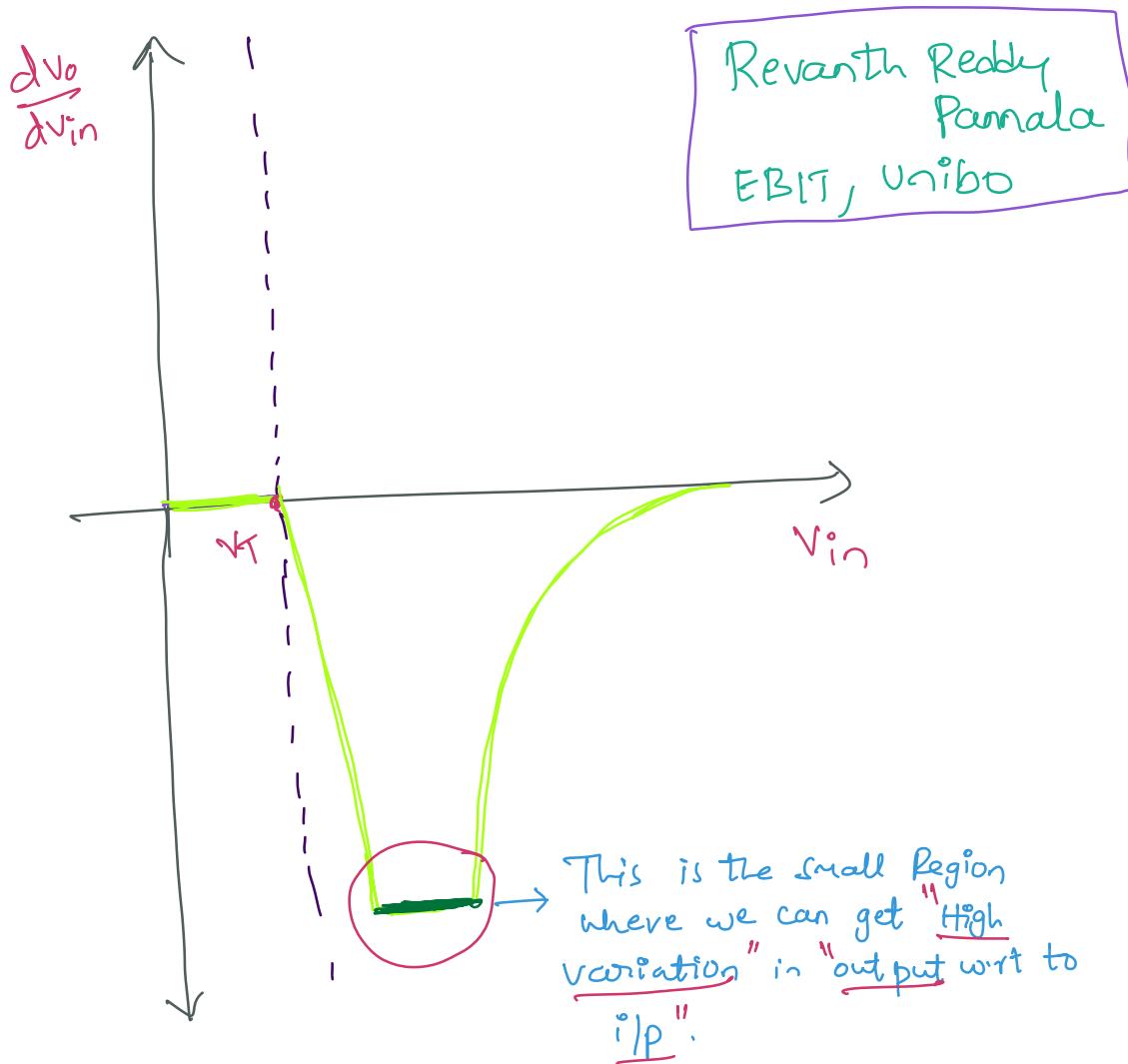
but not as steeply as in saturation region

This is Qualitative analysis of I/p-o/p Relationships

→ But what we are mostly interested in is the derivative of the relationship b/w o/p-i/p curve.

Because derivative is the one which is used in linearization process.

Because derivative links the variation of i/p to the variation of the o/p.



$\therefore$  To have a Good Amplification induced by our CMOS configuration with common source connection, we need to Bias the circuit in the above Highlighted Region

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