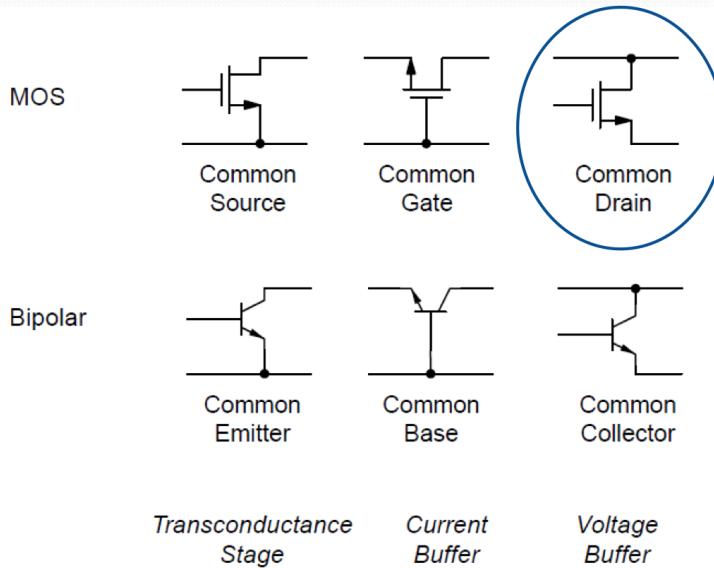


Lecture - 7

Rexanith Reddy
Pannala

Basic Single-Stage Amplifier Configurations



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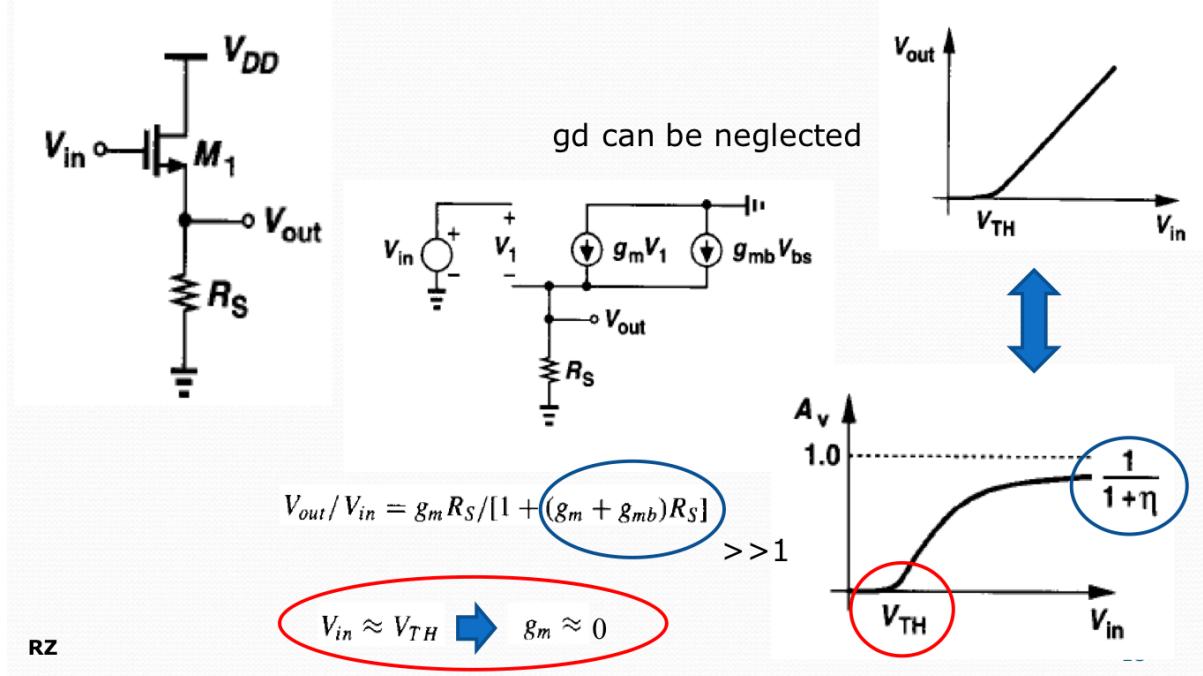
- In The earlier class we studied about the CS Amplifier and Analyzed its small signal Model. It is good for Amplification of signal
- But the only draw back it had was the opf Resistance of the CS-stage was on the Higher side.
- This would be an issue because if we were to Interfacing the CS stage with a subsequent stage with Relatively Low P/P Resistance.

Because we will have partitioning effect now
Two stages -

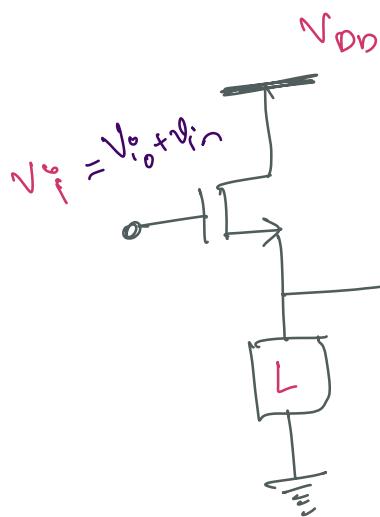
→ So, in order to be compliant with subsequent stages with low i/p Impedance a viable solution is to interpose CS configuration with an other configuration called Common Drain

In this case the Drain terminal is common to i/p port and o/p port and as a consequence of that the information flow is from Gate to source.

Common Drain



* Now let's try and Analyze the "Common Drain" stage both for "Biasing" & "Small Signal Model"



→ Here we can see that the drain should always be connected to the true terminal.

→ The i/p is $V_i = V_{i0} + v_{in}$

V_{i0} = DC operating Voltage for Biasing the Gate Source Junction

v_{in} = Actual small signal that is being applied to the device

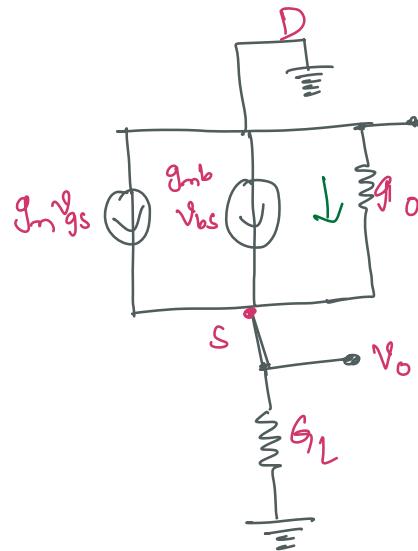
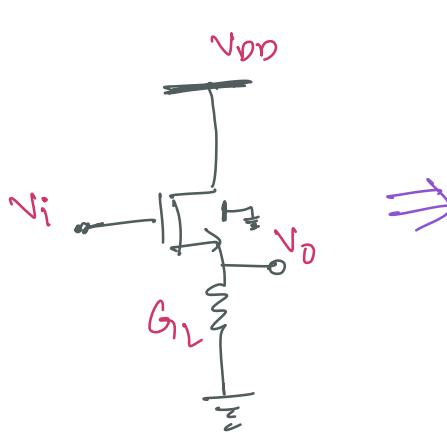
$$\rightarrow \text{IIP} \quad V_o = V_{o0} + v_o$$

Dc operating voltage (Bias voltage)

Variations small signal along the Dc operating point which actually represent the signal.

→ Then we will have a Load value characterised by it's conductance (G_L).

→ Small Signal Analysis of Common Drain



→ Here in the Small Signal Model all the constant voltage sources are Grounded.

→ Now we can write certain equations for the small signal Model.

→ Here source is not connected to the ground directly ∴

$$V_{GS} = V_G - V_S$$

where V_S = "Voltage across the load" = V_D

$$\Rightarrow \boxed{V_{GS} = V_i - V_D}$$

Note:- whenever we are writing equations for a small signal Model we are considering

small signal variations only-

→ Assuming Back Gate (or) Bulk contact connected to the Ground $\Rightarrow V_b = 0$

$$\begin{aligned}\therefore V_{BS} &= V_b - V_S \\ &= 0 - V_0 \\ \therefore V_{BS} &= -V_0\end{aligned}$$

→ By looking at the source node of the LCM.

we can observe that the current flowing through the load is flowing through the transistor itself.

$G_L V_o$: The current flowing through the Load.

$$\nexists G_L V_o = g_m V_{GS} + g_{mb} V_{BS} + g_o (0 - V_0)$$

Assuming current is flowing into the source node.

$$\Rightarrow G_L V_o = g_m(v_i - V_o) + g_{mb}(-V_o) - g_o V_o$$

$$\Rightarrow V_o [G_L + g_m + g_{mb} + g_o] = g_m v_i$$

$$\Rightarrow \frac{V_o}{v_i} = \frac{g_m}{G_L + g_m + g_{mb} + g_o}$$

These are all small signal parameters of NMOS transistor which can be represented as

$$G_T$$

$$\Rightarrow \frac{V_o}{v_i} = \text{Voltage Gain} = \frac{g_m}{G_L + G_T} < 1$$

$$G_T = g_m + g_{mb} + g_o > g_m$$

which signifies that the gain is less than one.

$$A_v = \frac{g_m}{\frac{1}{R_L} + G_T} \Rightarrow$$

$$\frac{g_m R_L}{1 + G_T R_L}$$

Another form of the gain

Q What about the "Input Resistance"?

If we look at the input terminal of small signal Model. It is an open circuit only voltage is applied to the Gate, current won't flow through the gate because of oxide barrier between Gate & Body.

$$\therefore i_i^o = 0$$

$$\Rightarrow \left(\frac{i_i^o}{v_i^o} \right) = 0 \Rightarrow G_i^o = 0 \quad (\text{Input conductance is ZERO})$$

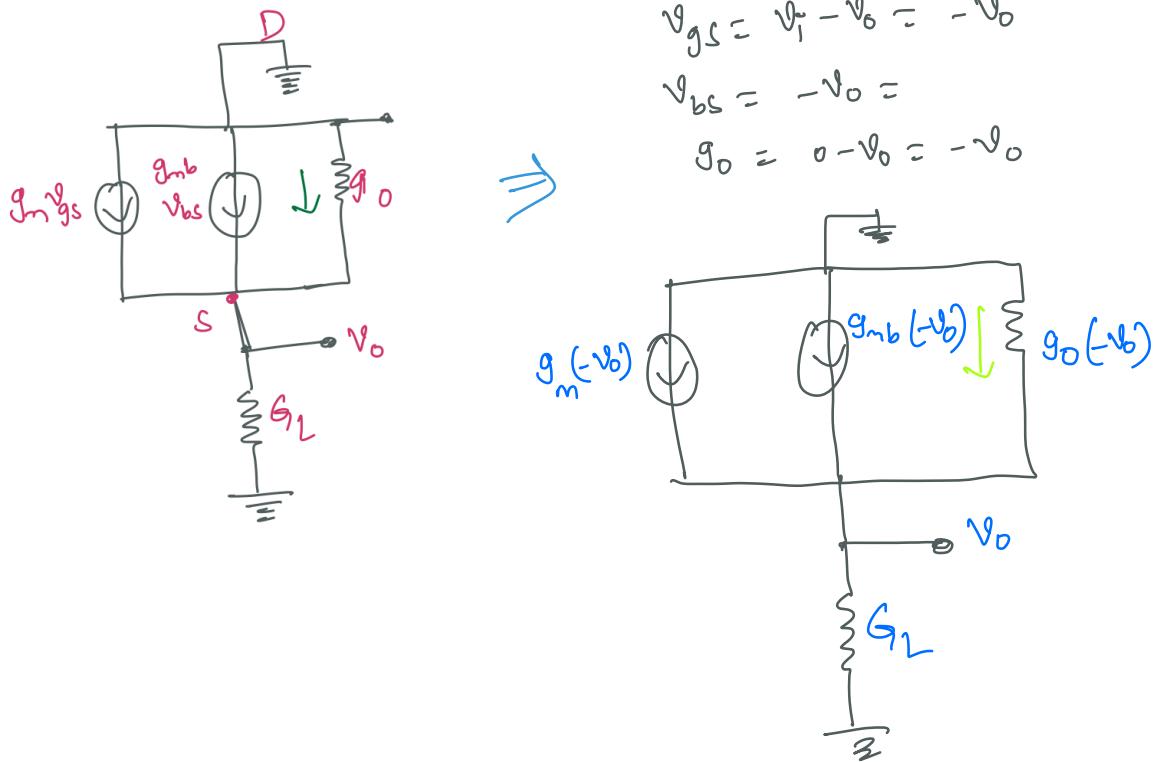
for $v_o = 0$

$$\therefore R_i^o = \infty = \frac{1}{G_i^o}$$

Q What about Output Impedance of Common Drain?

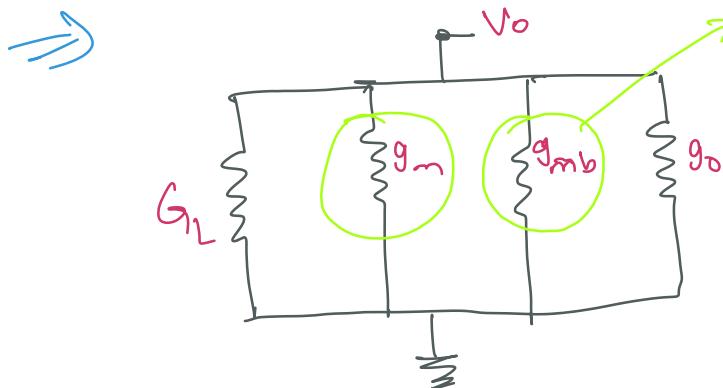
If we look at the op end of small signal Model. Let op conductance = $G_o = \left(\frac{i_o^o}{v_o^o} \right)$

$$v_i^o = 0$$



→ To calculate o/p Impedance we assume
 $v_i=0$.

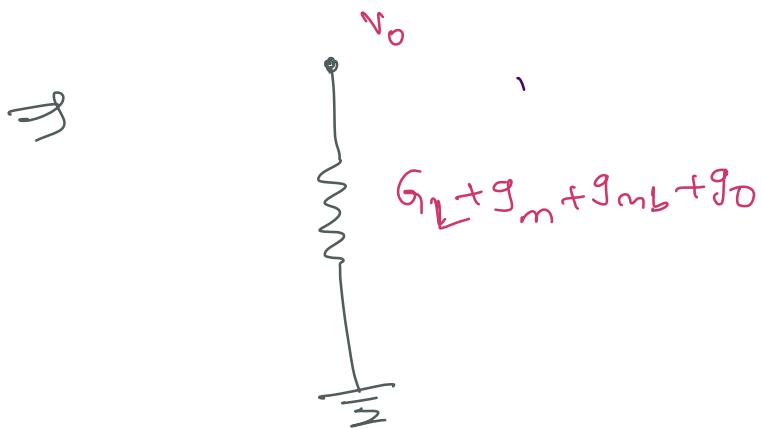
∴ The SLM transforms it to the above
 circuit where the small signal parameters
 are driven by v_o .



These voltage controlled
 current sources are
 replaced by Resistance
 because they are
 controlled by the voltage
 directly applied to
 them -

All these effects are in parallel when we are

Studying The Olp Impedance.



$$\Rightarrow G_o = \frac{i_o}{v_o} \Big|_{v_i=0} = G_L + g_m + g_{mb} + g_o$$

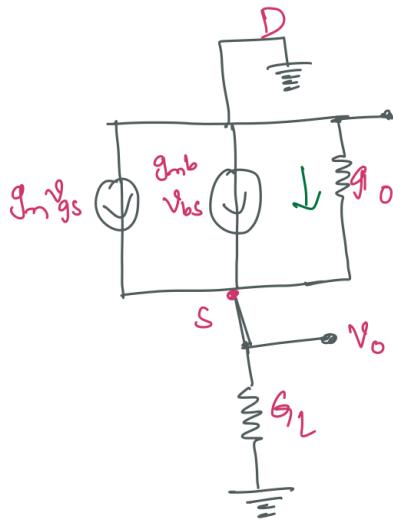
$$\Rightarrow R_o = \frac{1}{G_o} = \frac{1}{G_L + g_m + g_{mb} + g_o}$$

Small Quantity

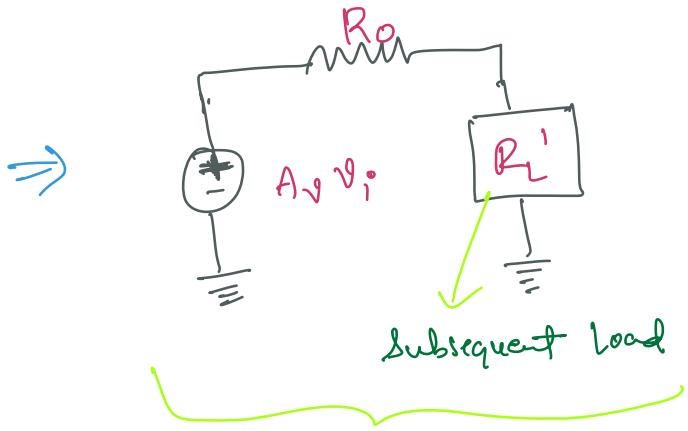
Here we can clearly say that "Olp Impedance of the Common Drain is low."

→ Since the olp Impedance of Common Drain stage is low we can use it as a

Voltage Buffer



Thermin Equivalent



Here the gain upto this point is divided by the voltage divider if the R_0

is less than the voltage gain can be efficiently transferred to the subsequent load R_L'

$$\Rightarrow V_{R_L'} = \frac{R_L'}{R_L' + R_0} (A_v v_i)$$

Must be small for efficient transmission of gain to subsequent load.

if R_0 is small then

$$V_{R_L'} = \frac{R_L'}{R_L} A_v v_i$$

→ we have also seen

$$\text{Gain} = A_v = \frac{g_m}{G_T + g_L} \approx \frac{g_m R_L}{1 + G_T R_L}$$

$$\therefore G_T = g_m + g_{mL} + g_o$$

$$G_T \approx g_m$$

Then

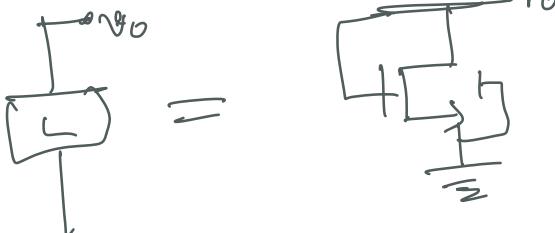
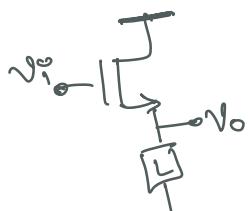
$$A_v \approx \frac{g_m R_L}{1 + g_m R_L} \approx 1$$

If $g_m R_L$ is larger than '1' then Gain can be approximated as '1'.

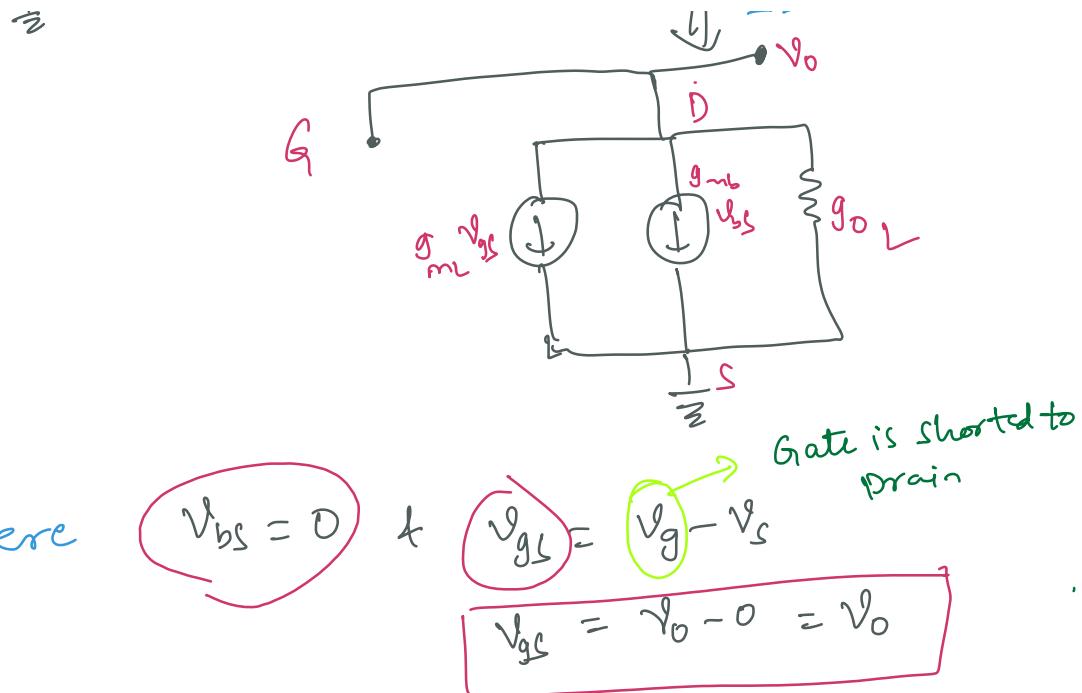
→ Ex:- If the Load  can be

a Diode connected Load

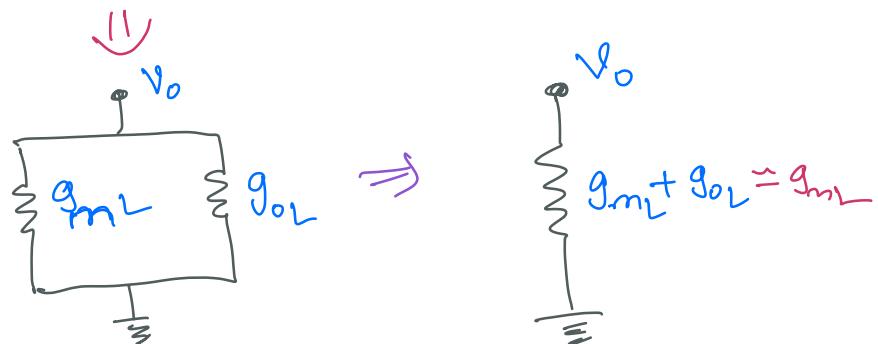
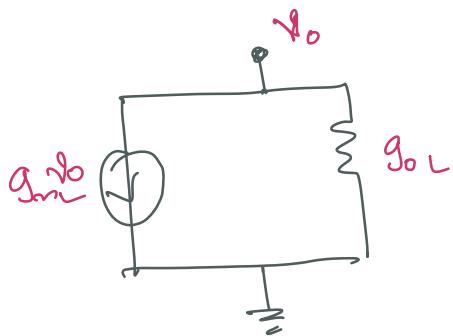
i.e



|| CCM



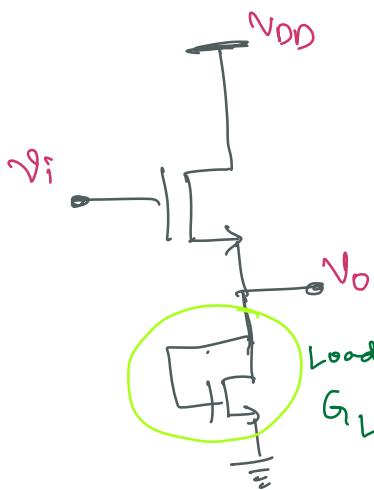
\therefore Then the circuit transforms to



\therefore

\therefore For a diode connect load the conductance

$$G_L \approx g_{mL}$$



Then
 $(Av) \text{ Gain} = \frac{g_m R_L}{1 + g_m R_L}$

$$Av \Rightarrow \frac{g_m / g_{mL}}{1 + g_m / g_{mL}}$$

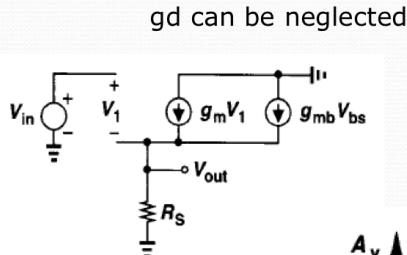
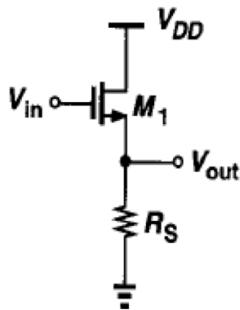
if $g_m \approx g_{mL}$ Then

$$\Rightarrow Av = \frac{1}{1+1} = \frac{1}{2}$$

$\therefore G_L \approx g_{mL}$ is taken sufficiently low to have a unitary gain.

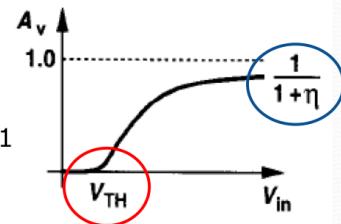
Ans 3 So Be

Common Drain



$$V_{out}/V_{in} = g_m R_S / [1 + (g_m + g_{mb}) R_S] \gg 1$$

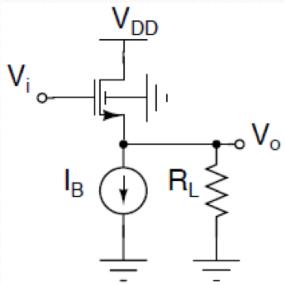
$$V_{in} \approx V_{TH} \rightarrow g_m \approx 0$$



RZ

The Gain can reach unity when the over drive voltage is increased.

CD: Some Practical Issues



- Several sources of nonlinearity:
 - (i) – V_t being a function of V_o in the presence of the backgate effect.
 - (ii) – I_D (and thus V_{ov}) being a function of V_o .
 - (iii) – Gets worse as R_L gets smaller.
- Reduced input and output voltage swing:
 - E.g. $V_{DD}=1V$, $V_t=0.3V$, $V_{ov}=0.2V$
 - CD buffer stage consumes 50% of supply headroom!
 - Often not feasible in low- V_{DD} applications.
 - More frequently used when the required swing is small.
 - E.g. pre-amplifiers or LNAs that turn μV into mV at the output.

→ (i) V_t being a function of V_b in the presence of the back-gate effect

→ we have seen that in CD stage

$$V_{BS} = -V_b \stackrel{= -V_s}{\approx} \text{in the SSM}$$

we also know that V_t is dependent on the Bulk to source voltage V_{SB} .

→

$$V_{th} = V_{th0} + \frac{\gamma}{2\sqrt{2\phi_F + N_{SB}}} \Rightarrow V$$

This is a function of V_b which will have potential side effects when V_b is very low.

→ we can see that CD stage performance are strongly influenced by the operating point.

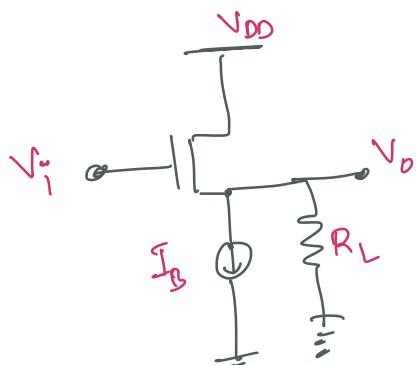
we have seen that $V_b = V_s$ is a varying quantity which depends on the characteristic source voltage

V_i .
of the input.

while back gate voltage should be kept constant in typical technology, but as V_{bs} is dependent on V_o .

$\therefore V_t$ is undoubtedly a function of the V_o as explained above.

→ And as V_{th} varies according to $V_s = V_o$
we can say current I_D varies with variation in $N_s = V_o$ and thus V_o also varies
 $\therefore V_{bv} = V_{gs} - V_{th}$



Here the input voltage V_i cannot have large swings because we have to keep the transistor ON.

$$\begin{aligned}\therefore V_{gs} &= V_g - V_s \\ &= V_i - V_o\end{aligned}$$

* Reduced ip and op voltage swing

e.g:- if $V_{DD} = 1V$, $V_t = 0.3V$, $V_{ov} = 0.2V$
 DC operating values

$$V_{GS} = V_t = V_{ov}$$

$$\Rightarrow V_{GS} - 0.3 = 0.2$$

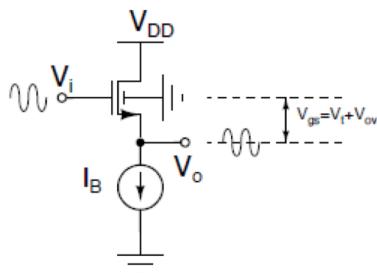
$$\Rightarrow V_{GS} = 0.5V$$

∴ for a typical CD stage with $V_{DD} = 1V$
 the allowable voltage swing is 0.5



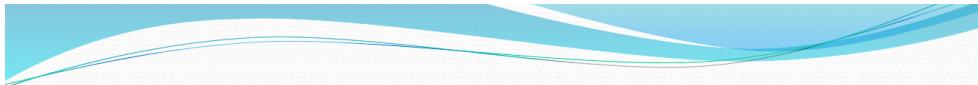
CD as a Level Shifter

- Frequently, we need to change DC levels without changing the AC signal.
- In an NMOS CD stage, the output DC level is lower than the input by V_{GS} .
- V_{GS} is almost constant.



- Likewise, to increase the DC level, one can use a PMOS CD stage.

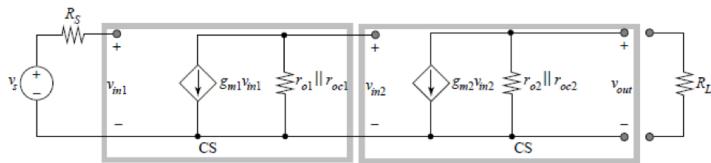
* Another important application of CD amplifiers
as in CASCODE Amplifier stage.



Cascaded Voltage Amplifier

- Want $R_{in} \rightarrow \infty$, $R_{out} \rightarrow 0$, with high voltage gain.

Try CS as first stage, followed by CS to get more gain ... use 2-port models

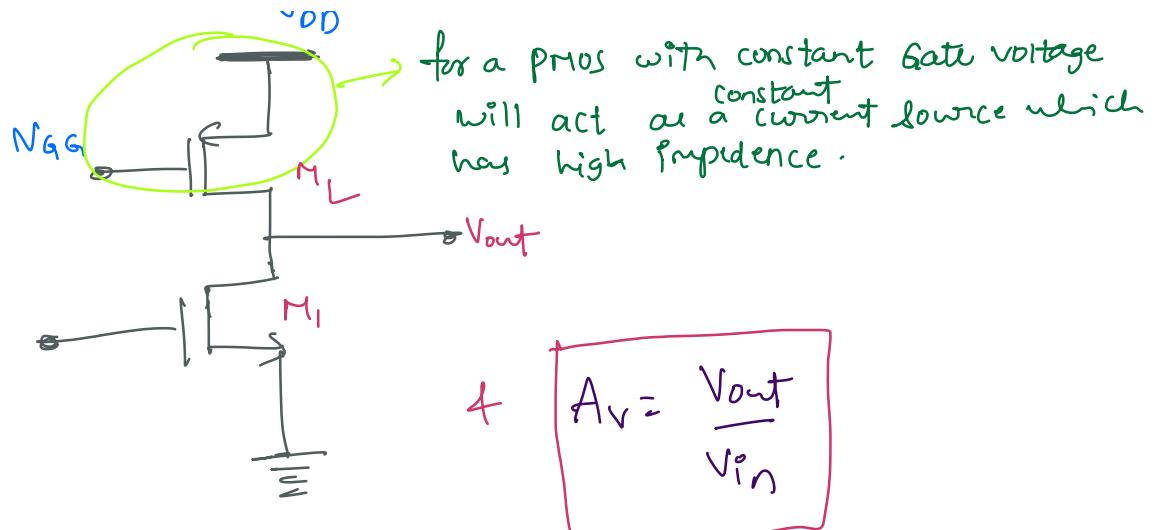


- solve for overall voltage gain ... higher, but $R_{out} = R_{out2}$ which is too large

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** Let suppose we want to implement relatively High voltage Gain and low o/p resistance we can achieve this using CD as the interface b/w the CS and the load.

i.e To "achieve High Gain" we rely on CS topology.
and to achieve "low o/p impedance" we rely on "CD stage".

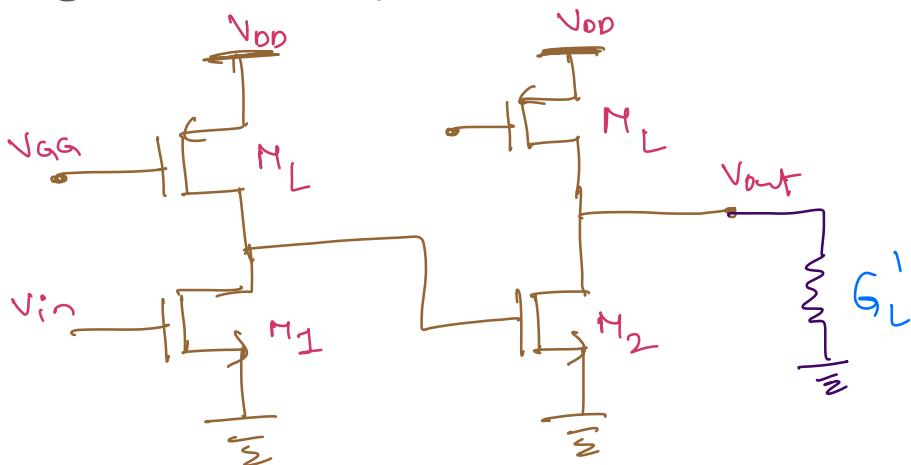


$$\boxed{A_V = \frac{-g_m 1}{g_{o1} + g_{o2}}}$$

" we have seen
that g_o is almost
100 times smaller
than g_m "

∴ This gain can be easily around 50

→ If we want more gain we can connect a second CS stage in cascade to the first CS stage.



The Gain we get from this configuration is

$$A_V = A_{V_{CS2}} \cdot A_{V_{CS2}}$$

$$\Rightarrow A_V = \frac{g_{m1}}{g_{o1} + g_{oL}} \cdot \frac{g_{m2}}{g_{o2} + g_{oL}}$$

$$\Rightarrow A_V = 50 \times 50 \quad \text{for example}$$

This gain is excellent but

Q what happens if we have a actual load of the combination G_L^1 ?

Solⁿ

$$\text{i.e } A_V = \frac{g_{m1}}{g_{o1} + g_{oL}} \cdot \frac{g_{m2}}{g_{o2} + g_{oL} + G_L^1}$$

If this conductance

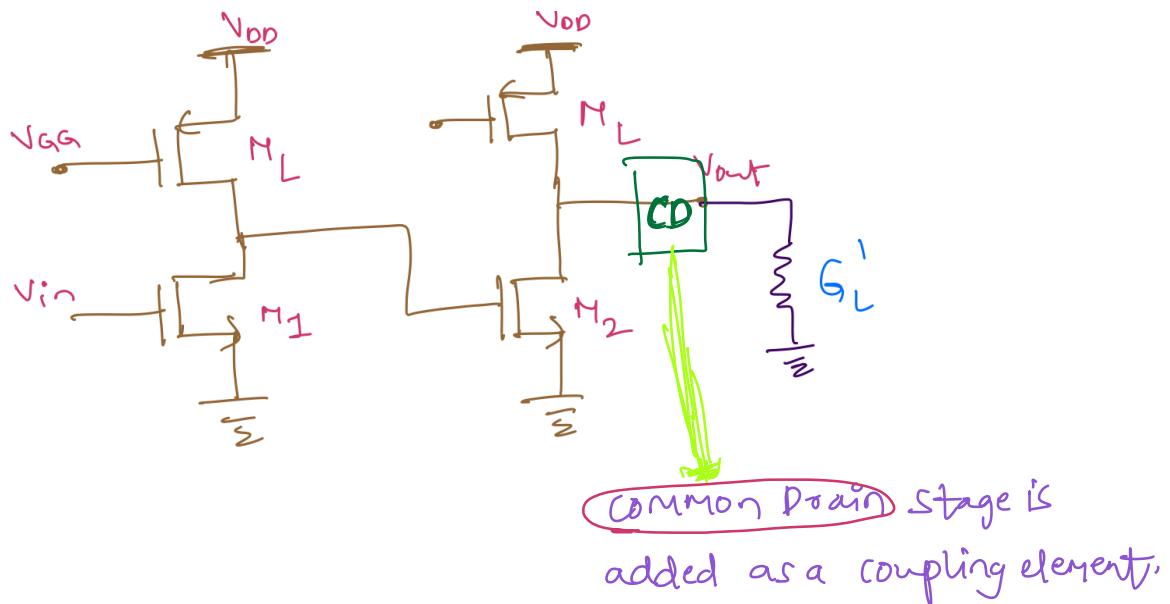
is high we cancel out all the beneficial effects of the 2nd stage.

Q

How can we AVOID the impact of

the G_L' on the overall gain of the cascade stage?

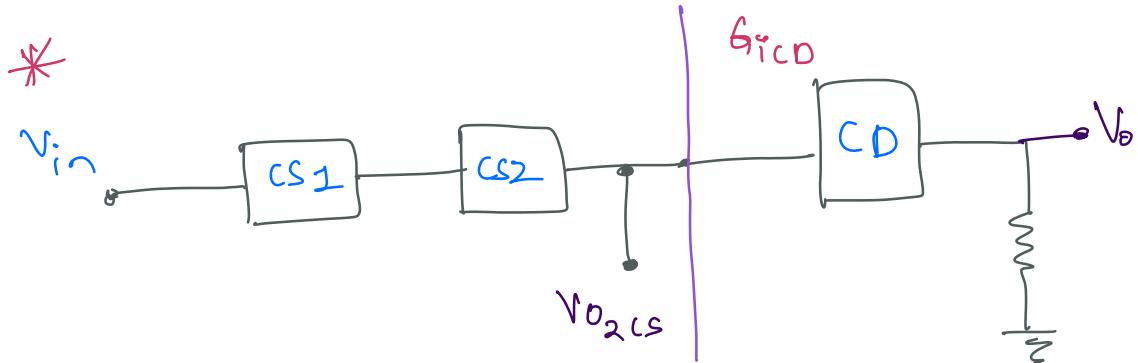
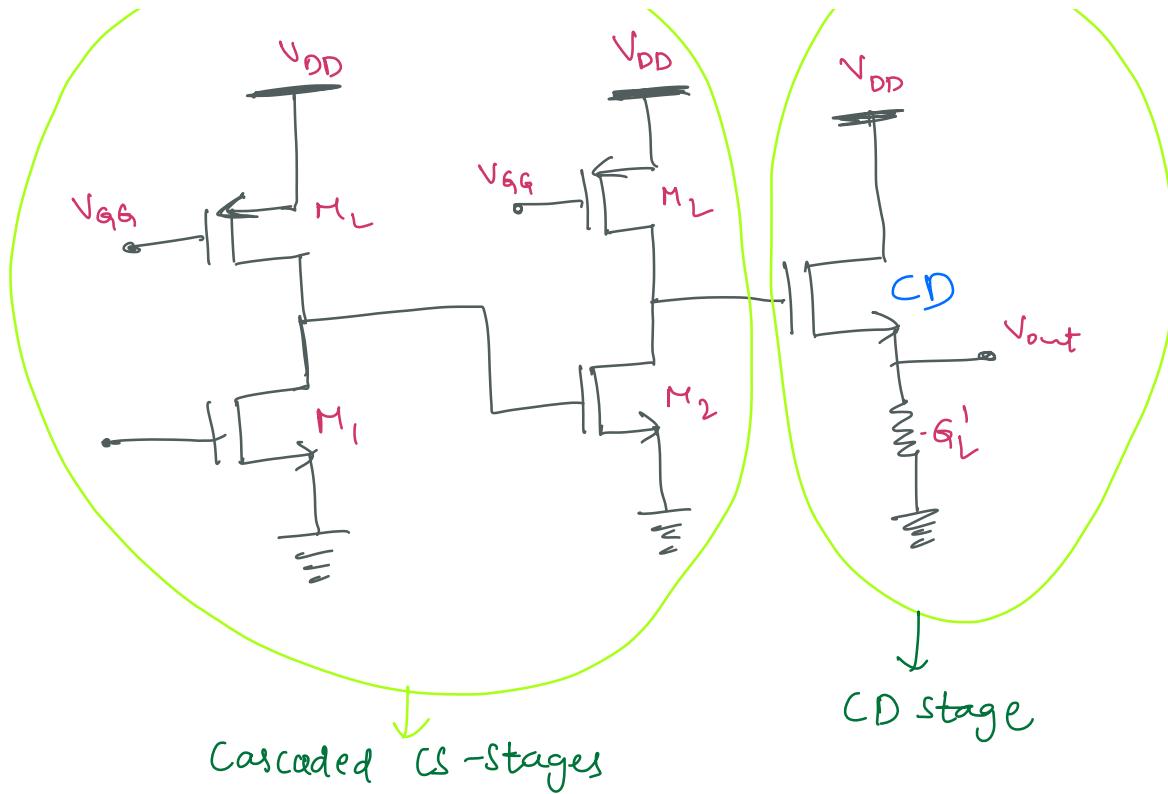
Ans we add Common drain stage



The bottom line is if G_L' is large quantity then the global gain is going to decrease.

\therefore If we place CD stage b/w o/p of 2nd CS stage and loading conductance of CD amplifier.





Here it is that the cascade common
source stage is loaded by the the input
conductance of the CD stage i.e G_{icd}



$$\therefore \frac{V_{o2CS}}{V_{in}} = \frac{g_{m1}}{(g_{m1} + g_{m2})} \cdot \frac{g_{m2}}{(g_{o2} + g_{o1} + G_{icd})}$$



Q How large is the ip conductance is CD stage?

Ans we know $R_{CD} = \infty$ because current cannot flow through the Gate.

$$\therefore G_{CD} = \frac{1}{R_{CD}} = \frac{1}{\infty} = 0$$

Op of 2 CS stages

$$\therefore \frac{V_o}{V_{in}} = \frac{g_{m1} \cdot g_{m2}}{(g_{o1} + g_{o2})(g_{o2} + g_{o1})}$$

$$\Rightarrow V_o = A_{CD} \cdot V_{o,2CD}$$

Vout of whole stage

$$\Rightarrow V_o = \frac{g_{mCP}}{G_T + g_L} \cdot V_{o,2CD}$$

The gain of CD-stage is almost

equivalent to (1)
 \therefore somehow the gain of the
 Two CS stages is still maintained.

Three-Stage Voltage Amplifier

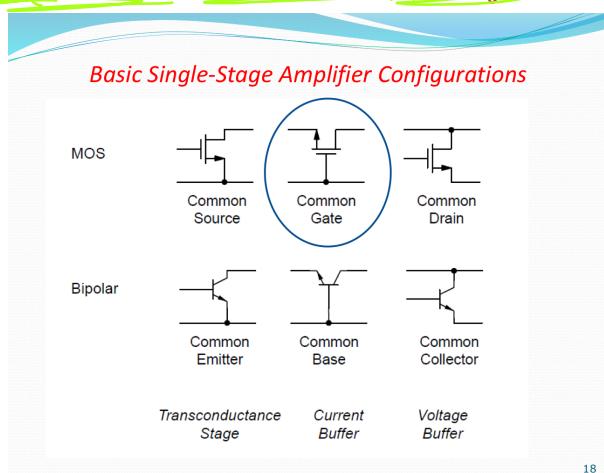
- Fix output resistance problem by adding a common drain stage (voltage buffer)

The circuit diagram shows a three-stage voltage amplifier. Stage 1 is a Common Source stage (CS-CS) with input voltage v_s and source resistance R_S , outputting v_{in} . Stage 2 is another CS stage with transconductance $A_v v_m$ and load resistor $(r_{o2} \parallel r_{oc2})$, outputting v_{in3} . Stage 3 is a Common Drain stage (CD) with transconductance $\frac{1}{(g_{m3} + g_{mb3})}$ and load resistor R_L , outputting v_{out} .

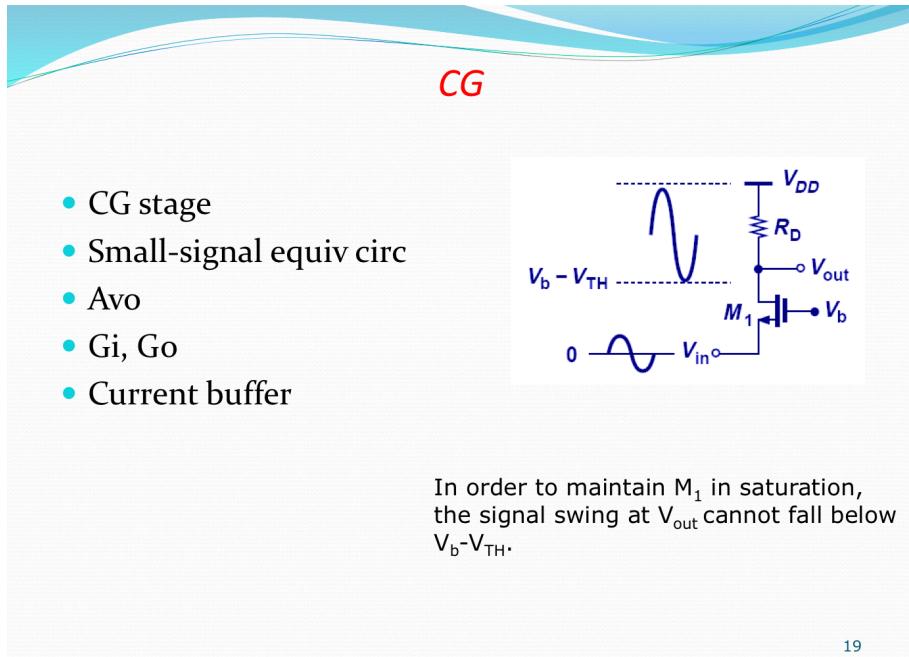
- Output resistance is not that low ... few kΩ for a typical MOSFET and bias --> could pay an area penalty by making (W/L) very large to fix.

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* Common Gate Amplifier Stage (current Buffer)



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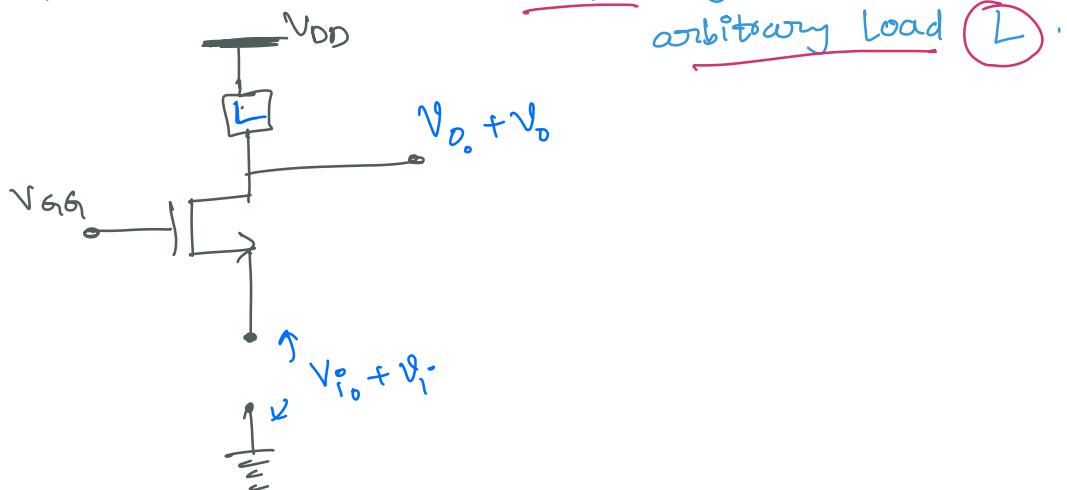


In CD stage we have studied Voltage Buffers-

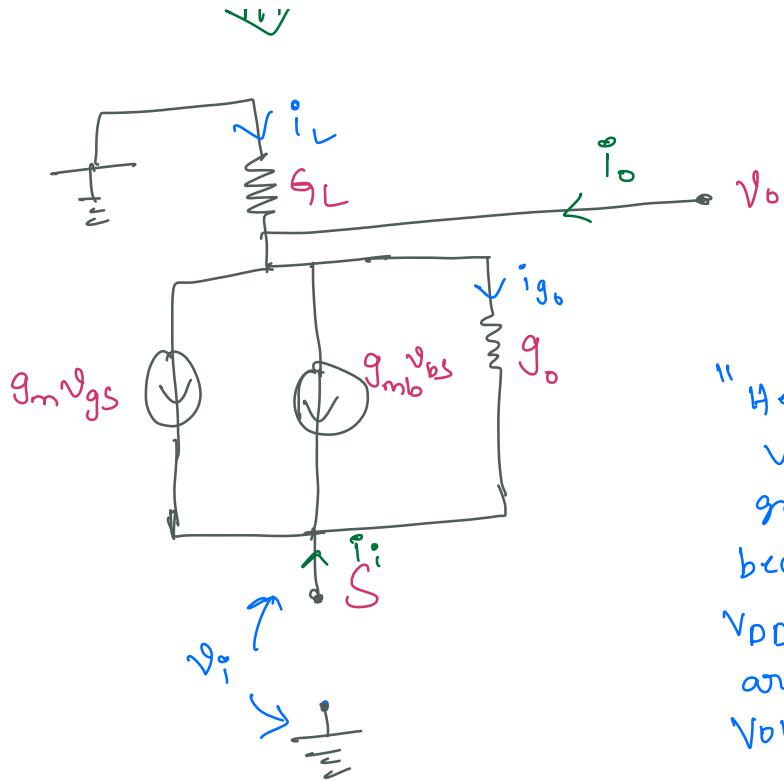
But in many cases it is beneficial to model the information flow by means of currents -
 \therefore we make use of "Common Gate" configuration.



let's start with "CG" configuration with arbitrary load L.



III. Small signal Equivalent



"Here Gate and VDD are grounded because VDD + VGS are constant voltages"

* Using Kirchoff's law write equations

$$i_L = -V_o \cdot g_{LV}$$

$$\rightarrow i_L = g_m V_{GS} + g_{mB} V_{BS} + i_{g_o}$$

$$-V_o G_L = g_m V_{GS} + g_{mB} V_{BS} + (V_o - V_i) g_o$$

$$\Rightarrow -V_o G_L = g_m (V_g - V_s) + g_{mB} (V_b - V_s) + V_o g_o - V_i g_o$$

$$V_g = 0, V_s = V_i$$

$$V_b = 0, V_s = V_i$$

$$\Rightarrow -V_o G_L = -g_m v_i^o - g_{mb} v_i^o + V_o - V_i g_o$$

$$\Rightarrow V_o + V_o G_L = (g_m + g_{mb} + g_o) v_i^o$$

$$\Rightarrow V_o (g_o + G_L) = (g_m + g_{mb} + g_o) v_i^o$$

\Rightarrow

$$\frac{V_o}{v_i^o} = \frac{g_m + g_{mb} + g_o}{g_o + G_L}$$

$$A_V = \frac{V_o}{v_i^o} = \frac{G_T}{g_o + G_L}$$

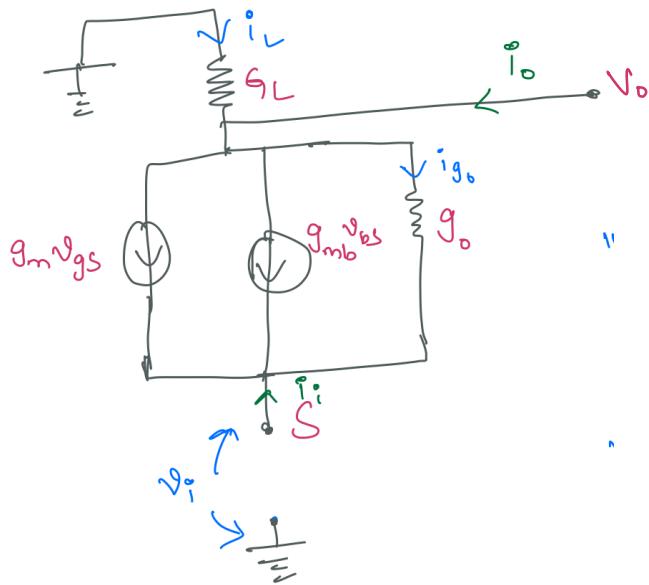
* Let's calculate i/p Conductance

$$G_i = \frac{v_i^o}{v_i} \Big|_{i_o=0}$$

$$\rightarrow v_i^o = -g_m v_{gs} - g_{mb} v_{bs} + g_o (v_i - V_o)$$

$$\Rightarrow -g_m(0 - v_i) - g_{mb}(0 - v_i) + g_o (v_i - V_o)$$

$$v_i^o \Rightarrow g_m v_i + g_{mb} v_i + g_o (v_i - V_o)$$



$$\therefore \overset{o}{i}_i = (g_m + g_{mb} + g_o) \overset{o}{v}_i - g_o \overset{o}{v}_o$$

$$\boxed{\overset{o}{i}_i = G_T \overset{o}{v}_i - g_o \overset{o}{v}_o}$$

$$\Rightarrow \overset{o}{i}_i = G_T \overset{o}{v}_i - g_o \left(\frac{\overset{o}{v}_o}{\overset{o}{v}_i} \right) \overset{o}{v}_i$$

$$\Rightarrow G_T \overset{o}{v}_i - g_o A_V \overset{o}{v}_i$$

$$\boxed{\overset{o}{i}_i \Rightarrow (G_T - g_o A_V) \overset{o}{v}_i}$$

$$G_I \Big|_{\overset{o}{i}_o=0} = \frac{\overset{o}{i}_i}{\overset{o}{v}_i} = G_T - g_o A_V$$

$$G_I \Big|_{i_0=0} = G_T - g_0 \frac{G_T}{(G_L + g_0)}$$

$$\exists \quad G_T \left(1 - \frac{g_0}{G_L + g_0} \right)$$

$$G_I = G_T \left(\frac{G_L + g_0 - g_0}{G_L + g_0} \right)$$

$$G_I \exists G_T \left(\frac{G_L}{G_L + g_0} \right)$$

This is almost equal to
(1)

(i) $G_L > g_0$

$$G_I \approx G_T$$

case 1

(ii) $G_L \sim g_0$

$$G_I \approx \frac{G_T}{2}$$

case 2

(iii) $G_L \ll g_0$

$$G_I = \frac{G_T \cdot G_L}{g_0}$$

case 3

$$G_I = \frac{G_T \cdot G_L}{G_L + g_0}$$

Unlikely Configuration

$$G_I = G_T \quad \text{in case 1 ,}$$

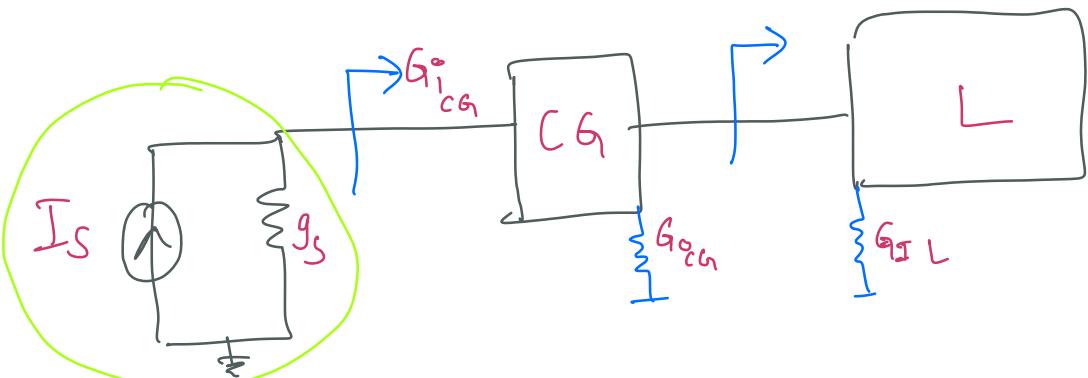
(input
conductance of
CG stage)

$$G_I = \frac{G_T}{2} \quad \text{in case 2}$$

$\rightarrow G_T = g_m + g_{mb} + g_o$ g_m is generally very high

$\Rightarrow G_I = G_T = \text{High conductance}$
 i.e low i/p Resistance

which is the prime requirement for current Buffer.



Current source with Internal Resistance

\therefore for maximum current to flow the i/p conductance of CG stage should be

" High)

* The other important aspect is if you want to transfer the current to the load.

" The o/p conductance of CG stage should be low i.e o/p Resistance should be high."

" and the conductance of o/p load should be high i.e Resistance should be low"

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