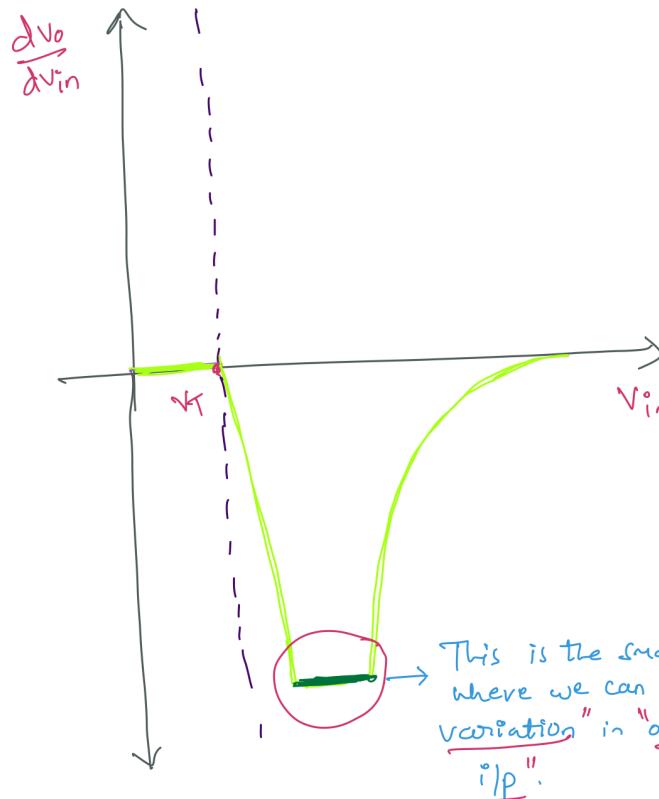


Lecture-6

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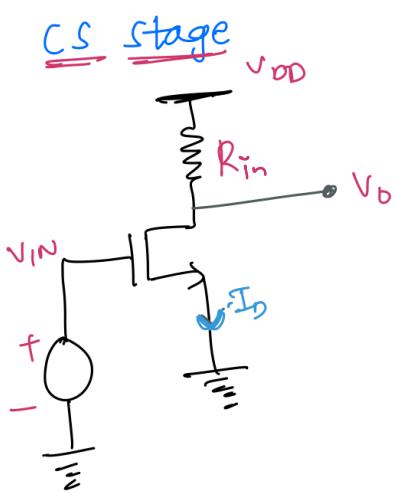
→ choosing operating point in the highlighted region gives us High gain.

∴ The CS-stage should be Biased properly.

→ So, in order Better study the circuit we need make use of Small Signal Analysis..

Q) How can we turn the Large signal schematic into small signal schematic?

Ans



→ we have to transform each circuit component into its small circuit equivalent.

LSC	SSC
<u>Large signal Component</u> ① NMOS PMOS	<u>Small signal Component</u> G_o
② For constant Voltage source 	short circuit Because for constant voltage $\frac{dV}{dt} = 0$

③ For constant current sources



open circuit

$$\frac{di}{dt} = 0 \therefore \text{open circuit}$$

④ Resistor (R)



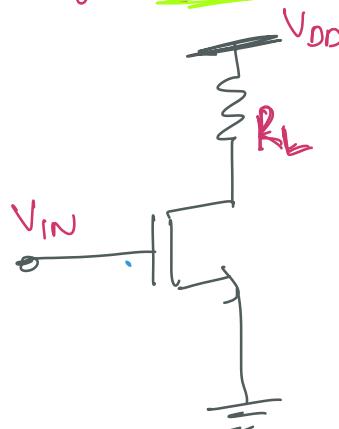
⑤ Inductor



⑥ Capacitor



Large signal Model

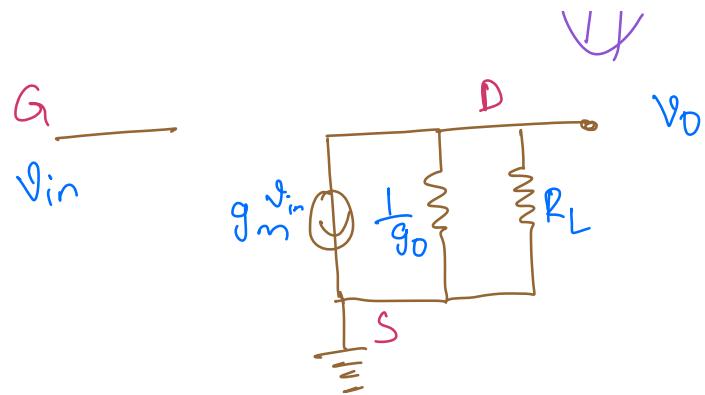


Small signal Model



Virtual
Ground
Related
to V_{DD}

i/p is shorted



We have ignored g_{mb} because Body & Source are Grounded Together.

\Rightarrow Let $\frac{1}{g_0} = r_0$ (resistance due to channel Length Modulation)

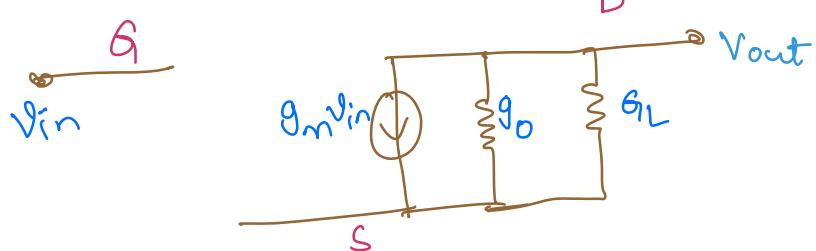
$$r_0 = \frac{1}{d I_D}$$

$$\therefore g_0 = d I_D$$

$\because r_0 + R_L$ are parallel we can calculate the equivalent resistance

$$R_{eq} = \frac{R_L r_0}{r_0 + R_L}$$

\rightarrow or we can indicate the resistances in terms of their conductances (g_0, g_L) $G_L = \frac{1}{R_L}$



When two conductances are in parallel.
they are supposed to be Added.

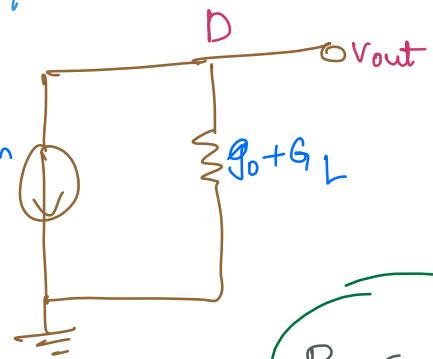
\therefore

$$g_{eq} = g_o + g_L$$

→ If the current through VCCS is made to flow through the parallel we have

$$V_o = -\left(g_m V_{in}\right) \frac{1}{g_o + g_L}$$

Resistance



$$R_{eq} = \frac{1}{g_o + g_L}$$

$$\therefore V_o = -\frac{g_m}{g_o + g_L} V_{in}$$

$$\Rightarrow A_V = \frac{V_o}{V_{in}} = -\frac{g_m}{g_o + g_L} = \text{Gain of the Circuit}$$

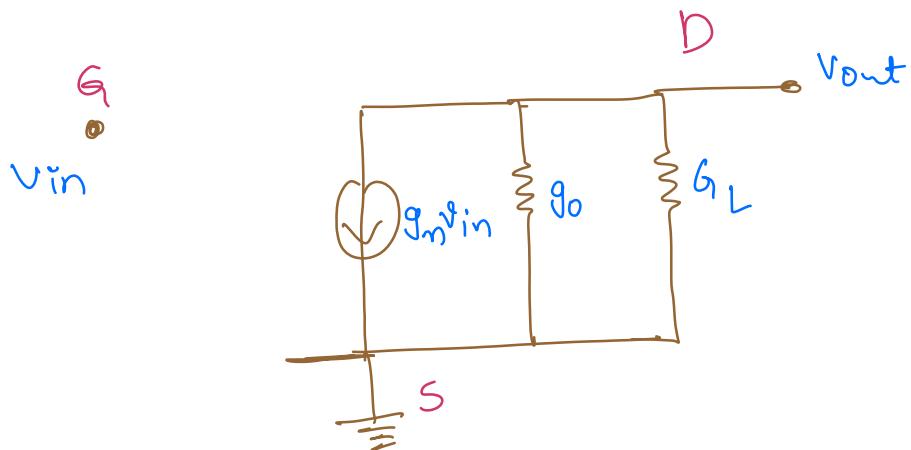


Let's see some results from the perspective of

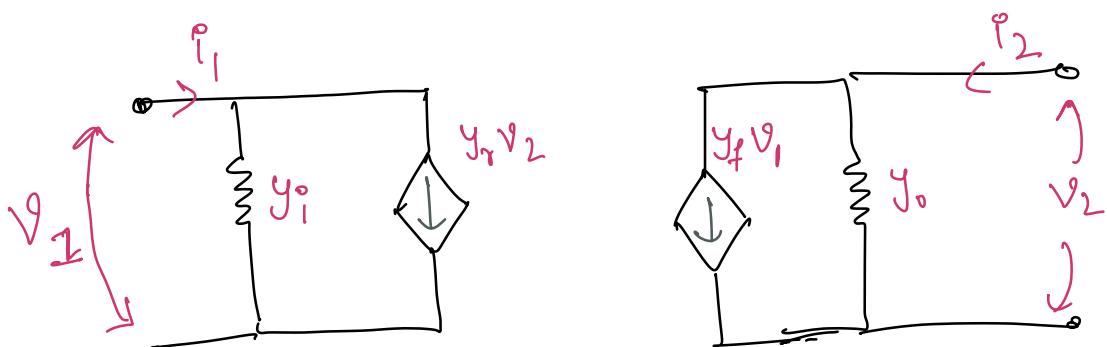
**

Admittance Matrix.

Just to verify the coherence of the Results we found out in the past class.



→ In order to study the Behaviour of the circuit we need to study the parameter of the Matrix in terms of 2-ports



From the definition of Admittance parameter

we know $y_i = \frac{i_1}{v_1} \Big|_{v_2=0}$

In common source configuration since i/p terminal is connected to the Gate. Because of presence of oxide layer b/w Gate and the Body.

The i/p Impedance is High and ∴ NO Current will flow.

$$\therefore \boxed{i_1 = 0}$$

$$\therefore \boxed{y_1 = \frac{\overset{\circ}{i}_1}{v_1} \Big|_{v_2=0} = 0}$$

Admittance Matrix $Y = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}$

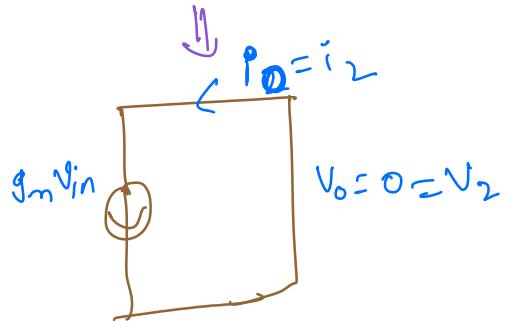
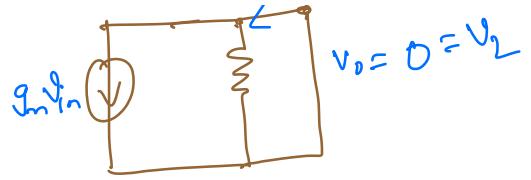
$$||| \quad \boxed{y_{12} = \frac{\overset{\circ}{i}_1}{v_2} \Big|_{v_1=0} = 0}$$

$$\boxed{y_{21} = \frac{\overset{\circ}{i}_2}{v_1} \Big|_{v_2=0} = \frac{g_m v_{in}}{v_{in}} = g_m}$$

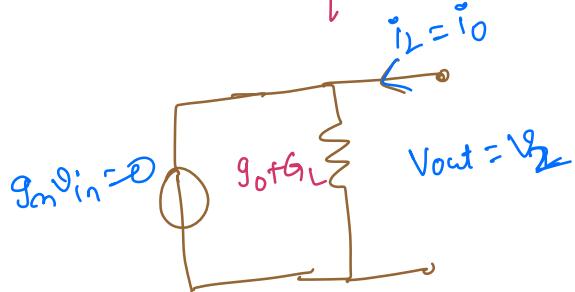
for CS stage $\underline{i_0 = i_2}$

$$v_1 = v_{in}$$

$$i_2 = g_m v_{in}$$



$$y_0 = \frac{i_2}{v_2} \quad | \quad v_1 = 0$$



In CS stage

$$v_1 = v_{in} = 0$$

\Rightarrow if $v_{in} = 0$

then $g_m v_{in} = 0$

then no current flows through the opamp.

$$\therefore i_2 = \frac{V_{out}}{R_{eq}} = V_{out} \cdot (G_L + g_o)$$

$$\Rightarrow y_0 = \frac{V_{out} \cdot (G_L + g_o)}{V_{out}} \Rightarrow G_L + g_o$$

When we studied Admittance matrix

we found Gain voltage is $A_V = -\frac{y_f}{y_o}$

$$\therefore A_V = \frac{-y_f}{y_o} = \frac{-g_m}{(G_L + g_o)}$$

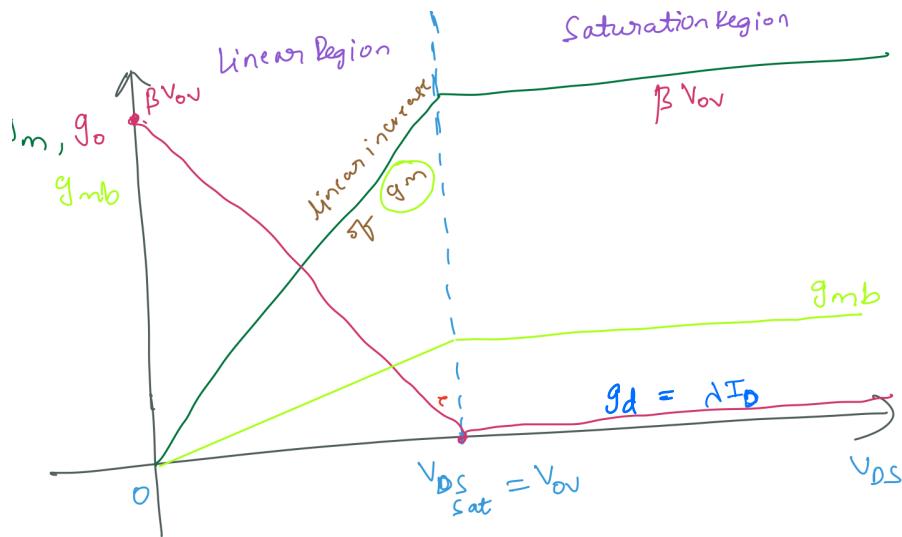
↓
Calculating the voltage is dependent on the region in which the Transistor is operating.

→ In order to achieve higher gain
 G_L should be low $\Rightarrow R_L$ should be high

∴ If $G_L = 0$ then

$$A_V = \frac{-g_m}{g_o}$$
 → Intrinsic Gain of the Transistor

→ By look at the below picture it is evident that the best possible region to achieve high gain is Saturation Region.



Because in Saturation Region g_m is much larger than g_d

$$g_m \approx 100 g_d$$

$$\Rightarrow \frac{g_m}{g_0} = \frac{\frac{2 I_D}{V_{OV}}}{\frac{d I_D}{d V_{DS}}} \Rightarrow \frac{2 I_D}{V_{OV}} \cdot \frac{1}{\frac{d I_D}{d V_{DS}}}$$

$$\boxed{\frac{g_m}{g_0} \Rightarrow \frac{2}{V_{OV} \beta}} \rightarrow \text{Intrinsic Gain}$$

$$g_m = \frac{2 I_D}{V_{OV}} = \sqrt{2 \beta I_D}$$

$$\Rightarrow \underline{g_m} = \sqrt{2 \beta I_D} \Rightarrow \sqrt{2 \beta}$$

$$g_o \quad \frac{1}{\lambda I_D} - \frac{1}{\lambda \sqrt{I_D}}$$

$$\Rightarrow \boxed{\frac{g_m}{g_o} = \frac{\sqrt{2\beta}}{\lambda \sqrt{I_D}}} \Rightarrow \boxed{\frac{g_m}{g_o} \propto \frac{1}{\lambda \sqrt{I_D}}}$$

→ we know

$$\lambda \propto \frac{1}{L} \Rightarrow L \uparrow \quad \lambda \downarrow \Rightarrow \left(\frac{g_m}{g_o} \right) \uparrow$$

$$L \downarrow \quad \lambda \uparrow$$

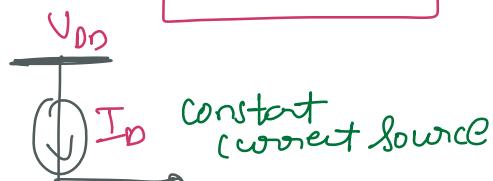
∴ If channel length Increases, λ decreases which intern increases the Intrinsic Gain of the MOSFET.

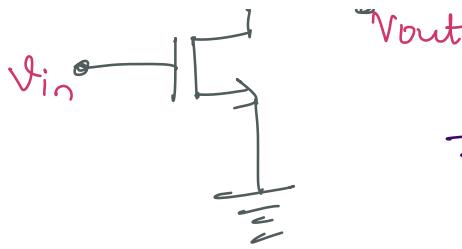
→

$$\therefore \boxed{\frac{g_m}{g_o} \propto \frac{1}{\lambda \sqrt{I_D}}}$$

if current is constant, because of a current generator source loading the circuit.

$$\boxed{\frac{g_m}{g_o} \propto \frac{1}{\lambda}}$$





$$\Rightarrow \frac{g_m}{g_0} = \frac{\sqrt{2B I_D}}{\gamma I_D}$$

$$\frac{g_m}{g_0} \propto \sqrt{2 \frac{W}{L} B}$$

\therefore we have a constant current I_D

$$\therefore \boxed{\frac{g_m}{g_0} = \sqrt{2 \frac{W}{L} B}}$$

\downarrow

\therefore 'd' is dependent on 'L'

$$\Rightarrow \frac{g_m}{g_0} \propto \sqrt{L}$$

Because
 $d \approx L$

$\rightarrow \therefore$ If we want High Intrinsic Gain

	V_{out}	L	I_D	
High Gain	\downarrow	\uparrow	\downarrow	
High Frequency	\uparrow	\downarrow	\uparrow	

Challenges in
Analog Ckt Design

Q What are the Requirements for Transit Frequency ?

Ans we have already derived the expression for Transit frequency.

$$f_T = \frac{3}{2} \frac{\mu}{2\pi L^2} \cdot V_{OV}$$

→ It is clearly visible that Transit Frequency is looking for Large over Drive voltage & Small channel length.

which is in contrast to the requirements for voltage gain.

we also know that in saturation Region

$$V_{OV} \propto \sqrt{I_D}$$

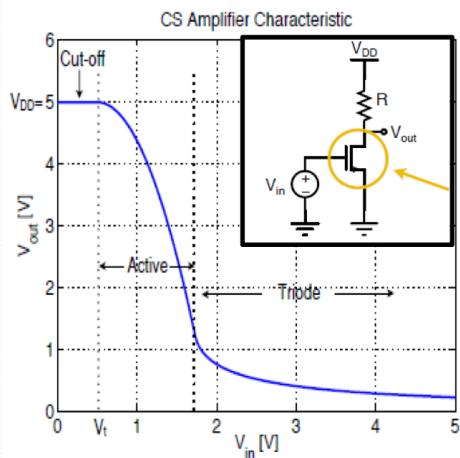
, ∴ we also need high I_D for high frequency operation.

→ The contrast between Gain & Frequency

requirements is what makes Analog circuit Design challenging.

Common-Source: Transfer Characteristic

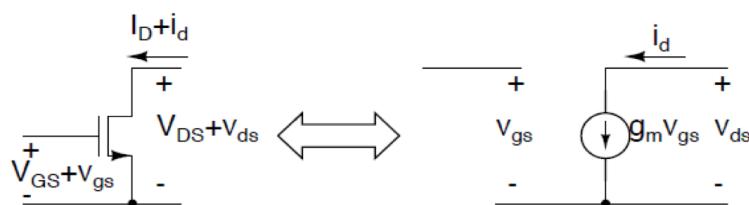
- CS stage
- Equiv circuit
- $A_v, A_v(V_i), G_i, G_o$
- N-ch and P-ch stage
- CMOS stage



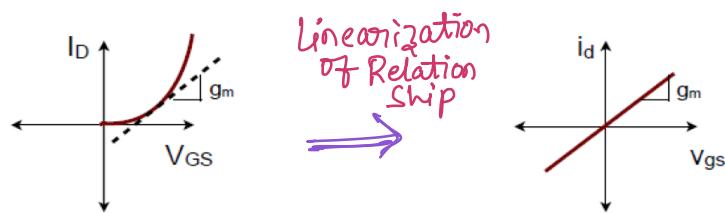
$$V_{out} = V_{dd} - R \times I_D$$

5

Small signal simplified model



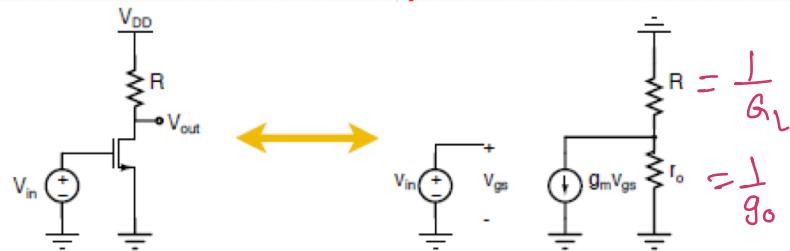
Most relevant effect of the Transistor in CS stage is Transconductance



$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

Assuming that the device is in active region ($V_{GS} > V_t$ and $V_{DS} > V_{GS} - V_t$).

CS: Voltage Gain



$$v_{out} = -g_m v_{gs} \times (R \parallel r_o) = -g_m v_{in} \times (R \parallel r_o)$$

$$\Rightarrow A_v = \frac{v_{out}}{v_{in}} = -g_m \times (R \parallel r_o)$$

- With r_o even if R is infinite the gain will still be finite ($g_m r_o$).
- $g_m r_o$ is called the "intrinsic gain" of the MOSFET and is a measure of maximum achievable voltage gain by a given device.

$$g_m r_o = \frac{g_m}{g_{ds}} = \frac{g_m}{\lambda I_D} = \frac{2}{\lambda V_{OV}}$$

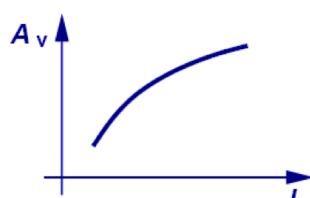
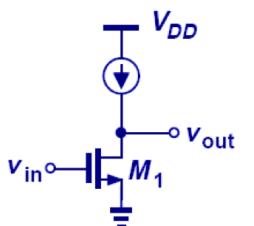
maximum achievable gain is inversely proportional to V_{OV} .

$$g_{ds} = g_o$$

EK

7

CS: Voltage-Gain vs Channel-Length



$$|A_v| = \frac{\sqrt{2\mu_n C_{ox} \frac{W}{L}}}{\lambda \sqrt{I_D}} \propto \sqrt{\frac{2\mu_n C_{ox} WL}{I_D}}$$

Since λ is inversely proportional to L , the voltage gain actually becomes proportional to the square root of L .

8



Figures of Merit for Design

- Transconductance efficiency
 - Want large g_m , for as little current as possible

$$\frac{g_m}{I_D}$$

Square Law

$$= \frac{2}{V_{OV}}$$

- Transit frequency
 - Want large g_m , without large C_{gg}

$$C_{GS} -$$

$$\approx \frac{3}{2} \frac{\mu V_{OV}}{L^2}$$

- Intrinsic gain
 - Want large g_m , but no g_o

$$\frac{g_m}{g_o}$$

$$\approx \frac{2}{\lambda V_{OV}}$$

$$\propto$$

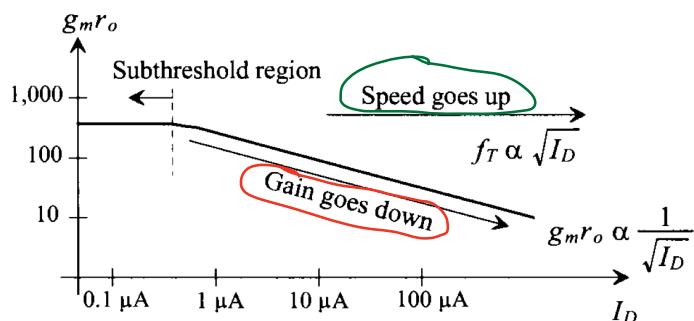
9



High Frequency, High Gain, High Transconductance Efficiency

are the qualities that cannot be achieved together.

Gain and Speed as functions of I_D

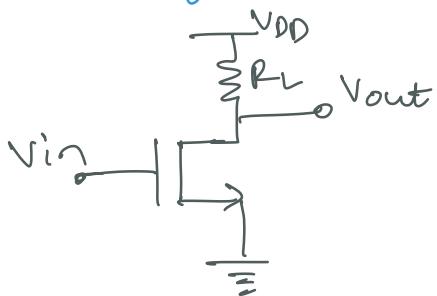


$$f_T = 1.5 \frac{\mu_n}{2\pi L^2} (V_{GS} - V_t)$$

Transit Frequency

10

→ If we have look at the Gain expression of CS stage



$$A_v = -g_m (R_L || r_o)$$

Here the gain depends on intrinsic op resistance r_o of own MOS component.

→ But "Loading Resistance" R_L plays an important role.

$$g_o = \frac{1}{r_o} \quad g_L = \frac{1}{R_L}$$

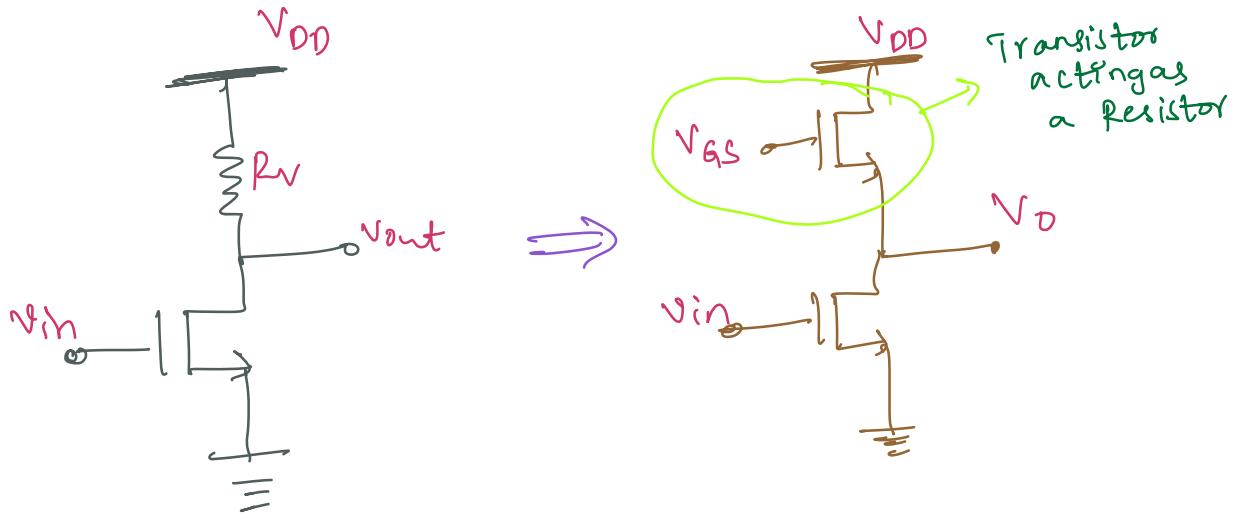
→ Ideally we would love the Loading Resistance to be infinite which provides for Maximum "gain(Av)".

But this is not the case in most situations because, we also need Biasing current for the device.

→ Now, let's toy an Analyze possible circuit configurations.

It is fact that it is not easy to implement Resistance on our MOS Technology.

\therefore "Resistors are Replaced by Transistors with Proper Biasing."



We found Gain of this configuration to be in terms of Admittance Matrix, as R_L is a Loading Resistor

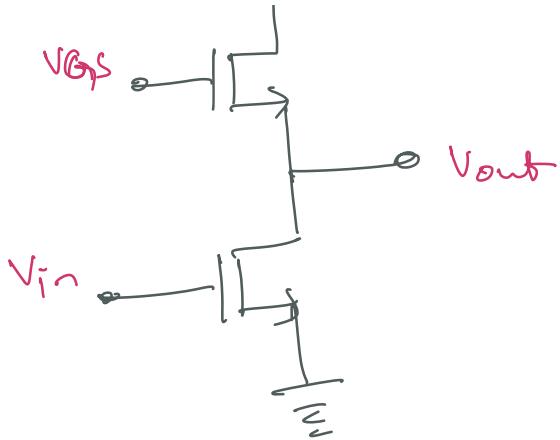
$$AV = \frac{-Y_f}{Y_0 + Y_L}$$



$$\therefore Y_L = \frac{1}{R_L}$$

Q: But what is the Resistance of the transistor which is acting a load?

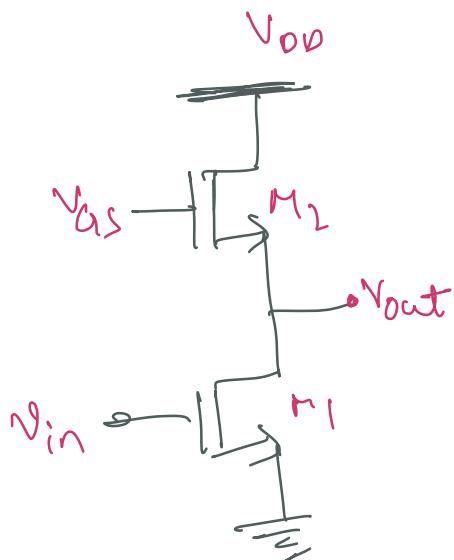




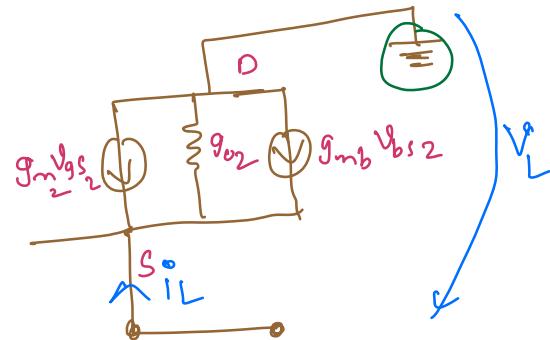
$$Y_L = ? = \frac{V_{IL}}{V_L}$$

Remember we are interested in small signal variations

\Rightarrow As a consequence we can turn the NMOS into its small signal equivalent.



Virtual Ground



V_L : Voltage Applied
 i_L : Current flowing into the ckt.

$\because V_{GS}$ is biasing voltage which is constant \therefore it is grounded in SCE

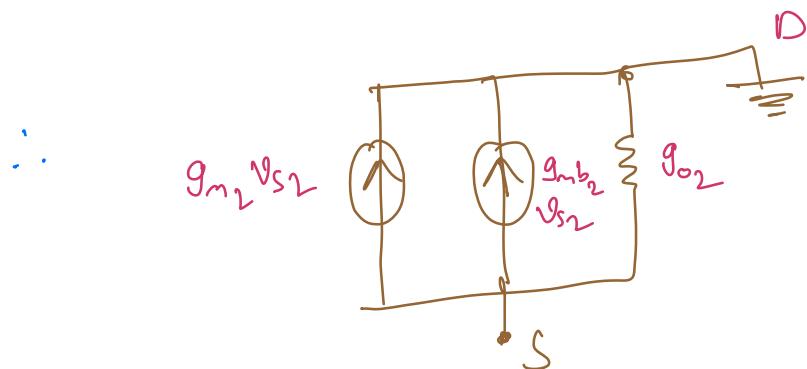
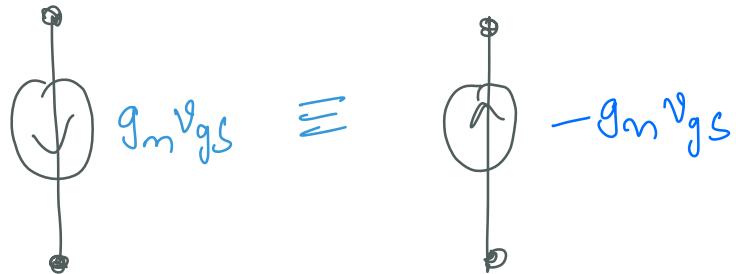
Here we have,

$$(i) V_{GS2} = (V_{G2} - V_{S2}) \\ \Rightarrow 0 - V_{S2}$$

$$V_{GS2} = -V_{S2}$$

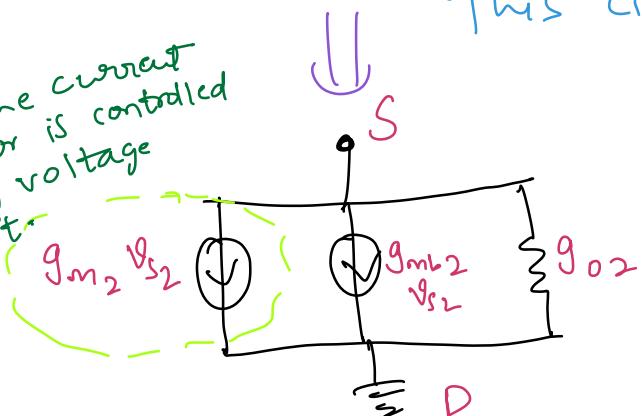
$$(ii) V_{BS2} = V_{B2} - V_{S2} \\ = 0 - V_{S2}$$

(Generally bulk voltage is considered to be zero)



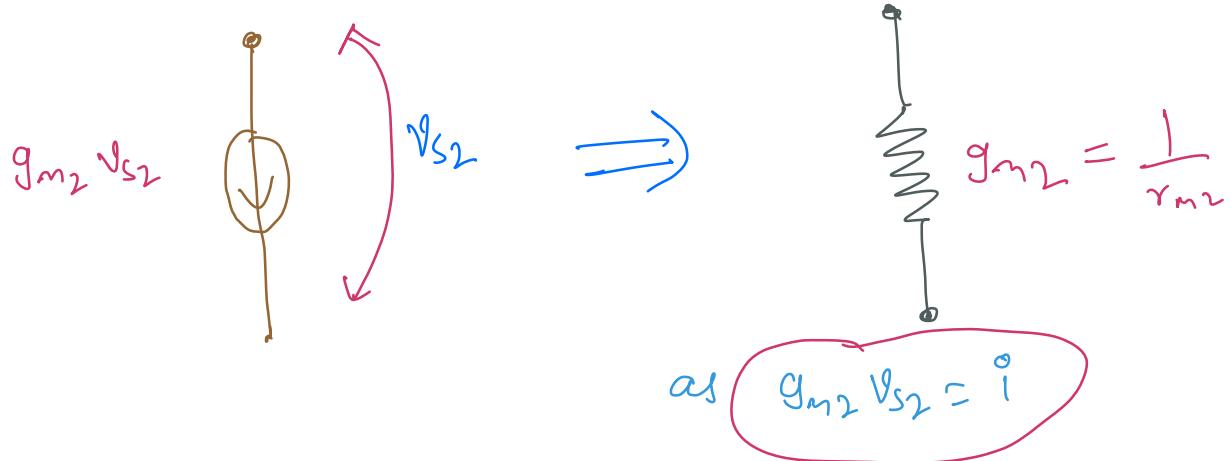
This circuit can be flipped

Here the current generator is controlled by very voltage across it.

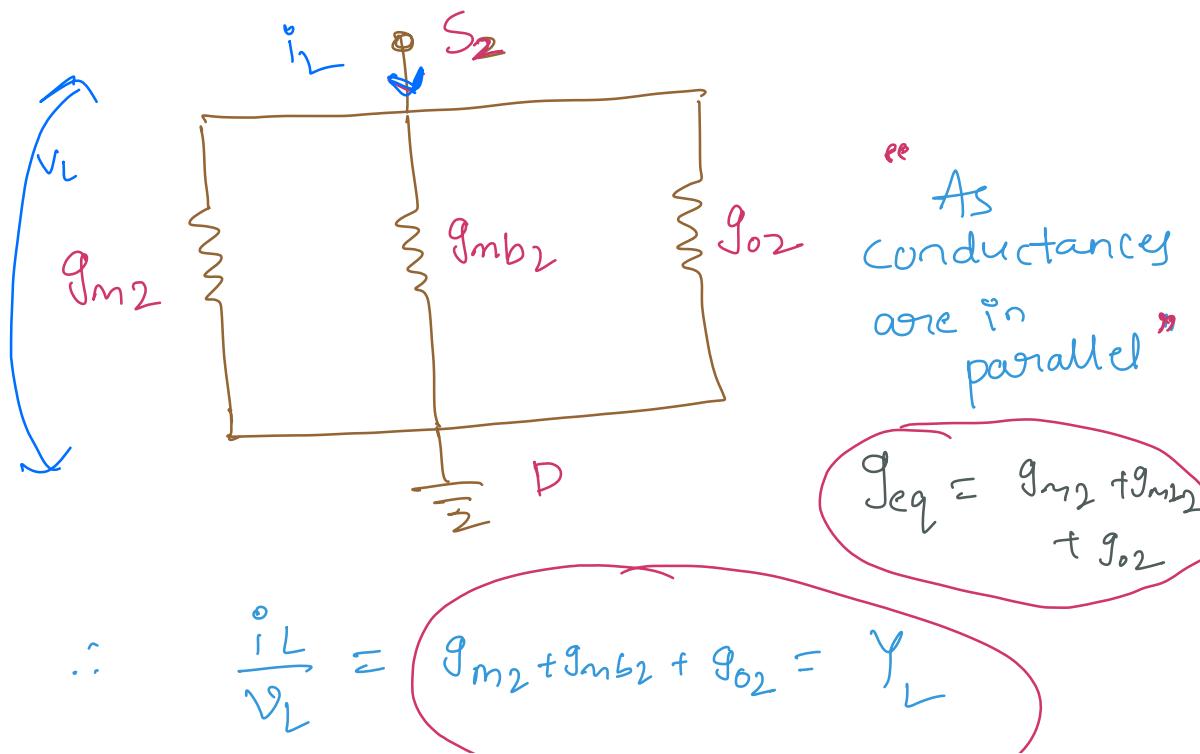


→ we know that a current source which is controlled by the very voltage across it, then

the current source can be replaced by
a Resistor.



\therefore The circuit is equivalent to



∴ The gain of the CS stage with Transistor Load is.

$$A_V = \frac{-Y_f}{Y_o + Y_L}$$

$$\text{Here } Y_L = g_{m2} + g_{mb2} \\ + g_{o2}$$

$$A_V = \frac{-Y_f}{Y_o + g_{m2} + g_{mb2} + g_{o2}}$$

Gain of Transistor Load acting as Resistor

**

$$A_V = \frac{-g_{m1}}{g_{o1} + g_{m2} + g_{mb2} + g_{o2}}$$

In this expression $g_{m2} \gg g_{o1}, g_{o2}, g_{mb2}$

∴ $A_V \approx \frac{-g_{m1}}{g_{m2}}$

Good Approximation

$$\Rightarrow A_V = -\frac{\sqrt{2\beta_1 I_d}}{\sqrt{2\beta_2 I_d}}$$

The Bias current is same

$$\therefore A_V = -\sqrt{\frac{\beta_1}{\beta_2}} = \frac{\beta' (\gamma_L)_1}{\beta' (\gamma_L)_2}$$

As $\beta' = \text{intrinsic conductivity}$ is same for a Given Technology

$$\therefore A_V = -\frac{(\gamma_L)_1}{(\gamma_L)_2}$$

\therefore The Bottom line is Gain is equal to Ratios of (γ_L) of two transistors

\therefore To have High Gain size of Transistor 1 Should be High than Transistor 2.

This not so easy to achieve.

→ Instead there are other configurations for which High Gain can be achieved.

ex: Using PMOS for loading Resistor
& NMOS for CS stage.

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