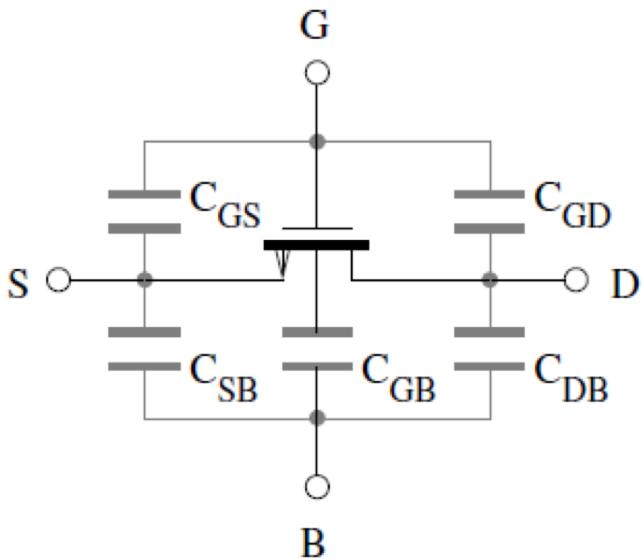


Lecture-4

- In the previous classes we have seen the Modelling of DC Behaviour of the MOSFET.
- But indeed one of the most important aspects is also to characterize the MOSFET in terms of Frequency Behaviour. and in particular to do that we need to estimate the Parasitic Capacitances which are somehow intrinsically connected to device.



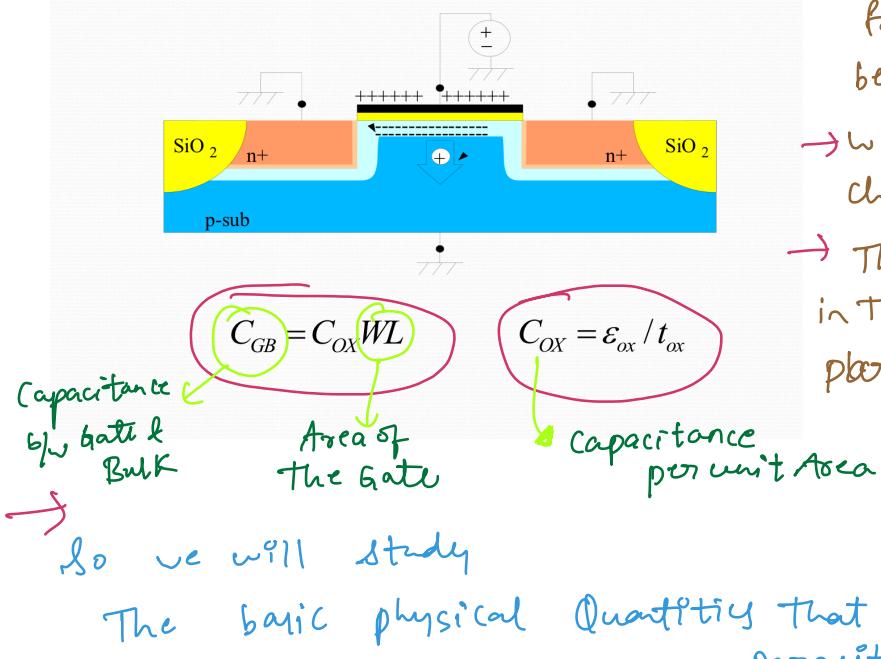
MOSFET Capacitances



→ Basically the MOSFET behaviour is based on complex charge distribution, across Gate region, Channel regions and all these charge and discharge effects can be related to Capacitive Behaviour.

→ So the Model which we see above includes all these additional parasitic effects. So let's try and understand this behaviour in detail.

Capacitance in Cut-off



→ In case of Cut-off Region we don't have free charge carriers below the Gate.

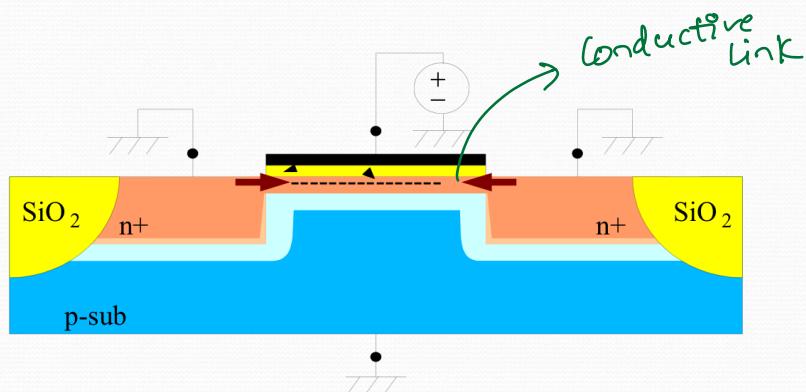
→ We have just fixed charge (i.e. space charge)

→ The mechanism we have in this case is similar to parallel plate capacitance.

- First of all The Capacitive Effect of the device depends on The Working Region of the device itself.
- In short, we will not experience same capacitive behaviour in Saturation w.r.t what we have in Linear Region or in Cut off. Because different phenomenon occurs consequently the charge redistribution mechanism is different for different regions.

Capacitance in Triode on linear Region

Capacitance in Triode



$$C_{GS} = C_{GD} = \frac{1}{2} C_{ox} WL$$

In Triode Region, there is a conductive link b/w Source.

∴ Instead of the capacitance b/w Gate & Bulk,
we focus on Gate-Source & Gate-^{Drain} Effects.

∴ It is splitting the former capacitance C_{GB}
into two part one is related to Source
and another to Drain.

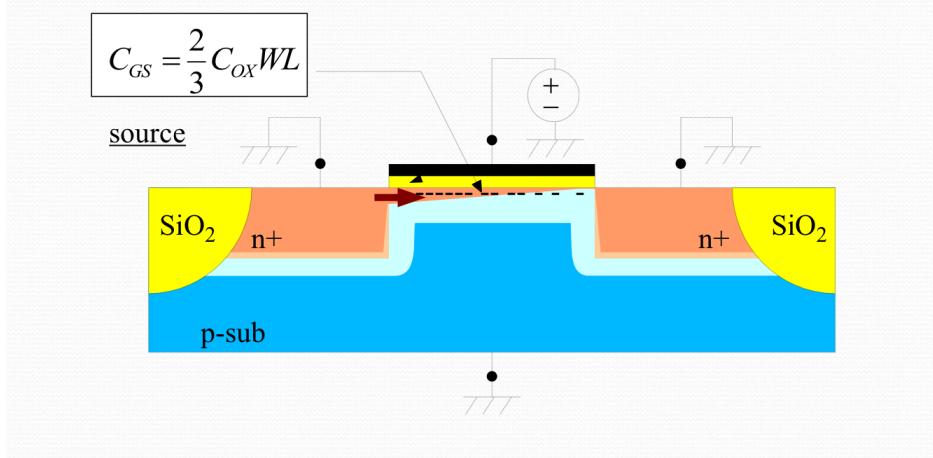
We know that if the capacitances are in
parallel they must be added.

$$\therefore C_{GS} = C_{GD} = \frac{1}{2} C_{ox} WL$$

Q What happens to Capacitance in Saturation ?

$$\text{i.e } V_{DS} \geq V_{GS} - V_T$$

Capacitance in Active Region



→ In saturation region for a sufficient value of $V_{DS} > V_{GS} - V_T$ i.e. pinch off voltage, the conductive link b/w Source & Drain would be interrupted.

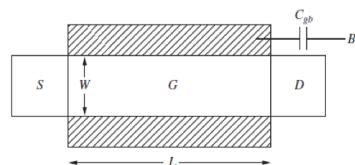
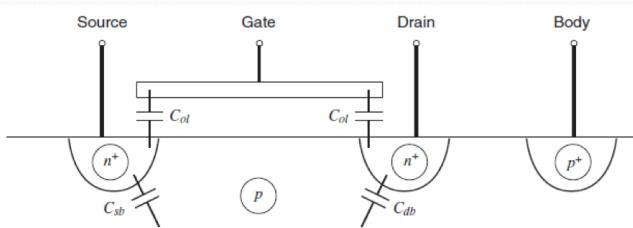
So, in saturation we have C_{GS} equal to.

$$C_{GS} = \frac{2}{3} C_{ox} WL$$

In saturation C_{GD} effect is cancelled out

i.e. $C_{GD} \approx 0$

MOSFET: Extrinsic Capacitances

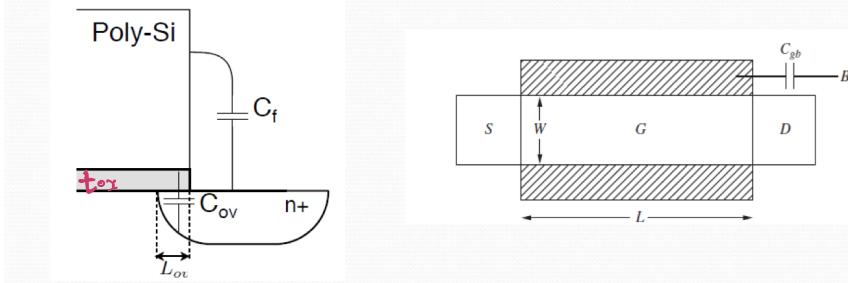


- Two main sources of extrinsic capacitances:
 - Overlap and fringing C_{ol}
 - Gate to source and drain
 - Junction capacitance C_{sb}, C_{db}
 - Drain and source to bulk
- These capacitances are merely parasitics that have nothing to do with device's operation.

Extrinsic Capacitances:-

There are other capacitances apart from Intrinsic capacitances called Extrinsic Capacitances.

MOSFET: Gate Extrinsic Capacitances



C_{ov} is directly proportional to the overlap area:

$$C_{ov} = WL_{ov}C_{ox}$$

C_f is due to fringing electric fields to source and drain through sidewalls:

- Increasingly more important in modern technologies because poly-Si thickness can be much larger than t_{ox} .

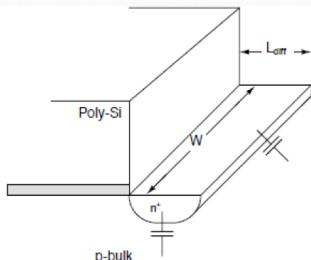
Can lump these two capacitors together:

$$C_{G,ex} = WC'_{G,ex}$$

$C'_{G,ex}$ is 0.5fF/ μm for both NMOS and PMOS.

In this case the only thing that is under design control is the channel width (W).

MOSFET: Junction Capacitances

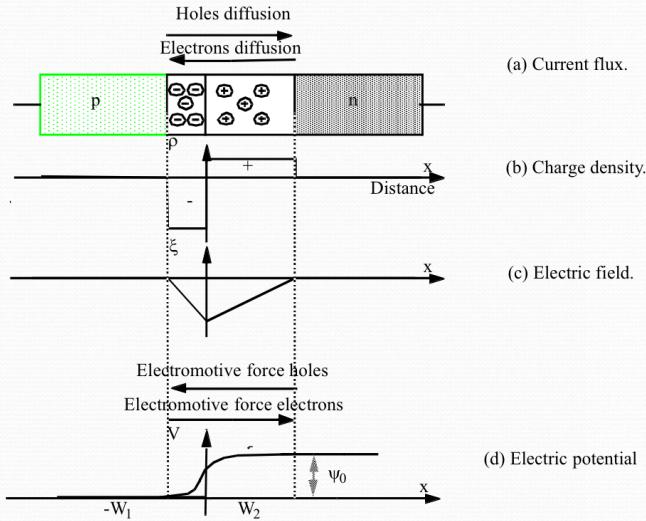


- Junction capacitances are calculated based on the bottom-plate area and sidewall perimeter of the source and drain diffusions.
- Note that L_{diff} doesn't have to be the same on both source and drain sides.
- Junction capacitances depend on the bias voltage:

$$C_j \propto \frac{1}{(1 + \frac{V_R}{\phi_B})^m}$$

- V_R is the reverse voltage, Φ_B is junction built-in potential, Φ_B and m are technology-dependent.

pn junctions



→ Junction capacitance C_{SB} & C_{DB} are similar to what happens in PN Junction Diode, because of Built in potential.

Junction capacitance

$$C_{SB} = \frac{C_{SB0}}{\left(1 + \frac{V_{SB}}{\psi_0}\right)^{MJ}}$$

$$C_{DB} = \frac{C_{DB0}}{\left(1 + \frac{V_{DB}}{\psi_0}\right)^{MJ}}$$

Typical of Technology

Built in potential equal for both source & drain

Dependent on Area of Diffusion for Source Area

$$C_{SB0} = C_{SB0}(Area)$$

$$C_{DB0} = C_{DB0}(Area)$$

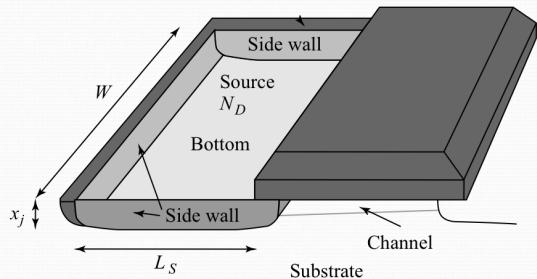
$$\psi_0 = V_t \ln \left(\frac{N_A N_D}{n_i^2} \right)$$

$$kT/q$$



Built in potential of
a PN Junction

Diffusions' Capacitance



$$C_{diff} = C_{bottom} + C_{sw} = C_j \times \text{AREA} + C_{jsw} \times \text{PERIMETER}$$

$$= C_j L_S W + C_{jsw}(2L_S + W)$$

This is because the transistor is generally a 3D device and we have to calculate Diffusion capacitance w.r.t to that.

In perimeter we consider $2L_s$ but not $2W$
Twice length

$2L_s$

because

the other end of source or drain diffusion there is a channel.

- At the boundary b/w source & drain diffusion to channel a whole different physics happens which is beyond this course

$\therefore \text{perimeter} = 2L_s + \text{fw}$

MOSFET: Junction Capacitance Expressions

Bottom Area of Diffusion

Perimeter of Diffusion

Junction capacitance

Sidewall capacitance

$$C_{jdb} = \frac{AD \times CJ}{\left(1 + \frac{V_{DB}}{PB}\right)^{MJ}} + \frac{PD \times CJSW}{\left(1 + \frac{V_{DB}}{PBSW}\right)^{MJSW}}$$

$$C_{jsb} = \frac{AS \times CJ}{\left(1 + \frac{V_{SB}}{PB}\right)^{MJ}} + \frac{PS \times CJSW}{\left(1 + \frac{V_{SB}}{PBSW}\right)^{MJSW}}$$

$$AD = W \times L_{diff}, \quad PD = W + 2L_{diff}$$

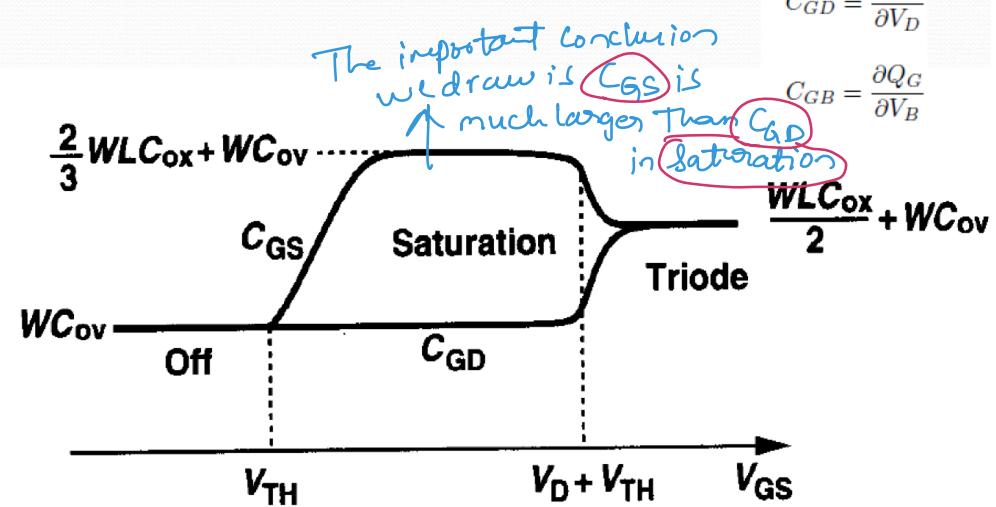
Parameter	(0.18μm)	
	NMOS	PMOS
C_{ox}	8.42 fF/μm ²	8.42 fF/μm ²
C_{oi}	0.491 fF/μm	0.657 fF/μm
C_J	0.965 fF/μm ²	1.19 fF/μm ²
C_{JSW}	0.233 fF/μm	0.192 fF/μm
PB	0.8 V	0.8 V
MJ	0.38	0.40
MJSW	0.13	0.33
LDIF	0.64 μm	0.64 μm

	CJ	CJSW	MJ	MJSW	PB & PBSW
NMOS	0.1 fF/μm ²	0.5 fF/μm	0.5	0.33	0.95V
PMOS	0.3 fF/μm ²	0.35 fF/μm	0.5	0.33	0.95V

→ The parameters above mentioned are SPICE parameters which are used to design actual devices.

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MOSFET: c) Gate Capacitances: Intrinsic+ Extrinsic

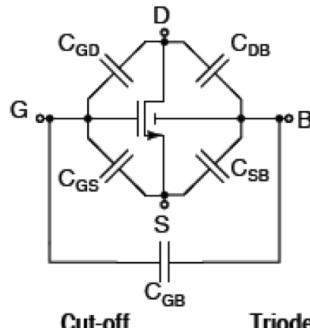


$$C_{GS} = \frac{\partial Q_G}{\partial V_S}$$

$$C_{GD} = \frac{\partial Q_G}{\partial V_D}$$

$$C_{GB} = \frac{\partial Q_G}{\partial V_B}$$

MOSFET: Capacitance Summary



	Cut-off	Triode	Active
C_{GS}	C_{ov}	$\frac{1}{2}WLC_{ox} + C_{ov}$	$\frac{2}{3}WLC_{ox} + C_{ov}$
C_{GD}	C_{ov}	$\frac{1}{2}WLC_{ox} + C_{ov}$	C_{ov}
C_{GB}	$\left[\frac{1}{C_{CB}} + \frac{1}{WLC_{ox}} \right]^{-1}$	0	0
C_{SB}	C_{jdb}	$C_{jdb} + \frac{C_{CB}}{2}$	$C_{jdb} + \frac{2}{3}C_{CB}$
C_{DB}	C_{jdb}	$C_{jdb} + \frac{C_{CB}}{2}$	C_{jdb}

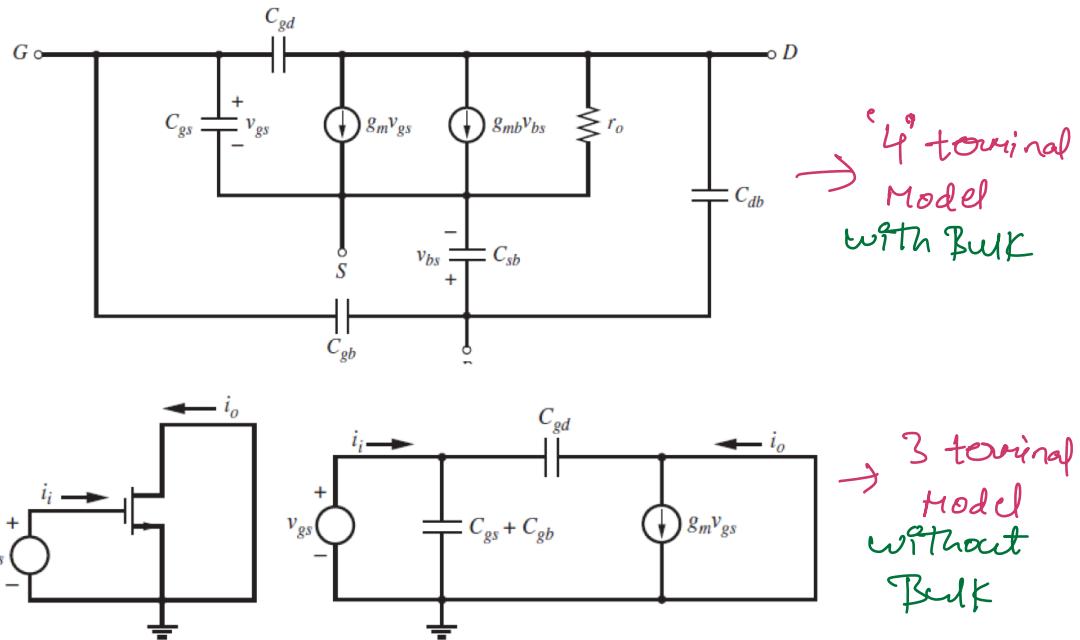
Terms in black are intrinsic capacitances

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Note:- Next we will see how these capacitances effect the Frequency behaviour of the device.

- To do that we will compute an important parameter to characterize the Behaviour for specific Technology called "TRANSIT FREQUENCY"
- So, what we see in the below picture is basically linearized model of the MOSFET Transistor enriched with parasitic effect.
- This is the model we are going to use to analyze small variations around an operating point.

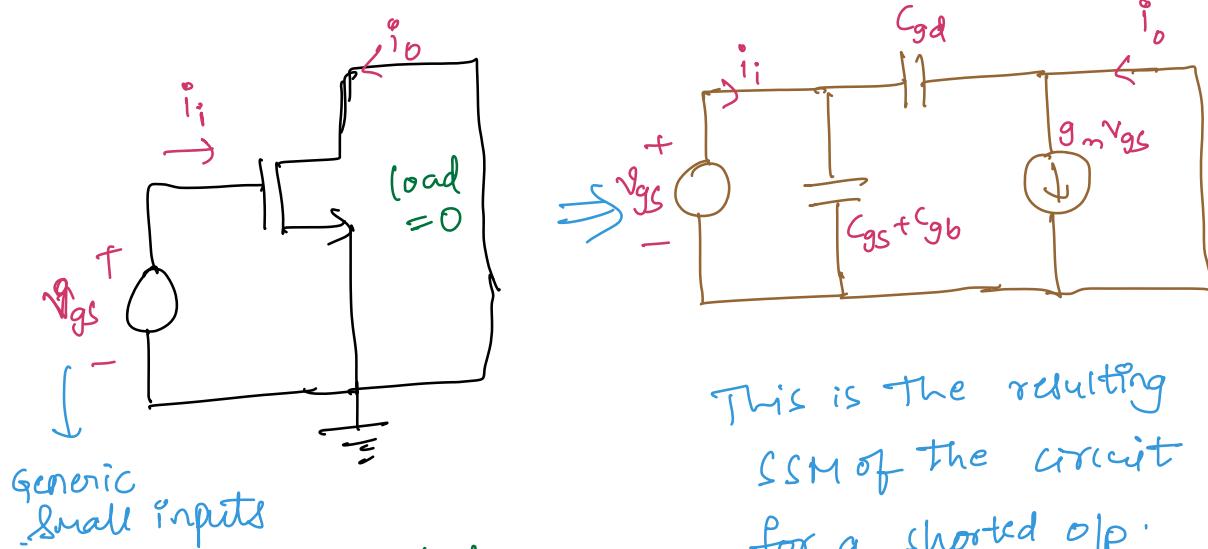
MOSFET: Transit Frequency Calculation



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- what is important is, when we are interested in parasitics, i.e. AC Frequency behaviour of the MOSFET device is influenced by the parasitic capacitances.
- one interesting observation is that the small signal model of the circuit is calculated in the saturation region. So, the parasitic capacitances must be calculated in saturation region.
- But, one of the most interesting configuration of generic NMOS device is when we apply

an input signal at the Gate and study the effects of the Device intrinsic o/p current.



Here we want to study the intrinsic effect of the device so the load is considered to be ZERO.

i.e. drain is Grounded to the source.

→ Now, to analyze the SCM for shorted o/p we can say

i_i : O/p Current

(In DC $i_i=0$, but at Higher frequencies i_i is not zero, due to Capacitive path b/w Gate & Source Through $(C_{gs} + C_{gb})$)
→ Gate & Drain Through C_{gd}

* So, we can say AC current is present.

→ Now, in saturation region MOSFET acts as an Amplifier i.e. input i_i can vary the current i_o in the o/p Branch.

→ The most important point is:
we are interested in determining Frequency at which the o/p quantity will be equal to the i/p quantity.

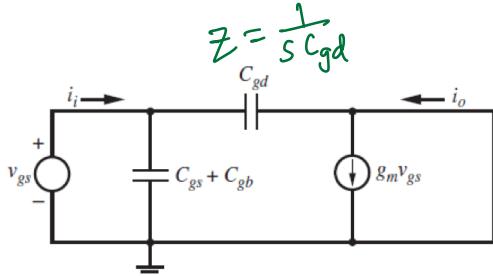
i.e. $i_o = i_i$

This is the case when we won't have any current gain.

∴ The Frequency at which we no longer have current gain is called Transit Frequency.

→ Derivation of Transit Frequency is given below

MOSFET: Transit Frequency Calculation



$i_i = s(C_{gs} + C_{gb} + C_{gd})v_{gs}$ because Drain & Source are Shorted

$$i_o \simeq g_m v_{gs}$$

$\text{H} = 1 \text{ when } \omega = \omega_T$

$$\frac{i_o}{i_i} \simeq \frac{g_m}{s(C_{gs} + C_{gb} + C_{gd})} \quad \frac{i_o}{i_i} \simeq \frac{g_m}{j\omega(C_{gs} + C_{gb} + C_{gd})} \quad \omega_T = \frac{g_m}{C_{gs} + C_{gb} + C_{gd}}$$

$$f_T = \frac{1}{2\pi} \omega_T = \frac{1}{2\pi} \frac{g_m}{C_{gs} + C_{gb} + C_{gd}}$$

Assume the intrinsic device capacitance C_{gs} is much greater than $(C_{gb} + C_{gd})$

$$f_T = 1.5 \frac{\mu_n}{2\pi L^2} (V_{GS} - V_t)$$

(especially when we are in saturation.)

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Note:- we also need to take into account of Miller Effect when the out is not grounded. But, in this case as the out is Grounded the Miller effect has a minor role.

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