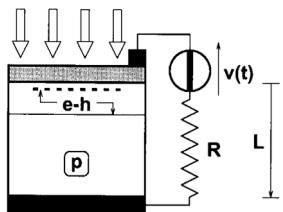


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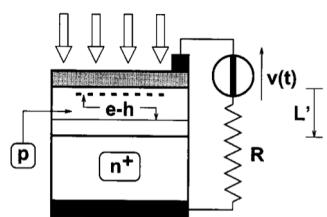
Lecture-17

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MOS photocapacitor

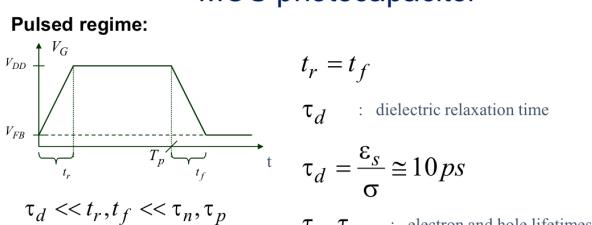


MOS photocapacitor (epitaxial)



→ MOS Photo capacitor is a simple device. Assume that we Bias the MOS capacitor by applying a voltage to the Gate s.t. The capacitor goes into the Strong Inversion condition. However, the applied voltage is a **PULSE**

Initially the MOS capacitor is in a **flatband condition** (Electric potential is uniform everywhere and no net charge anywhere in the semiconductor)

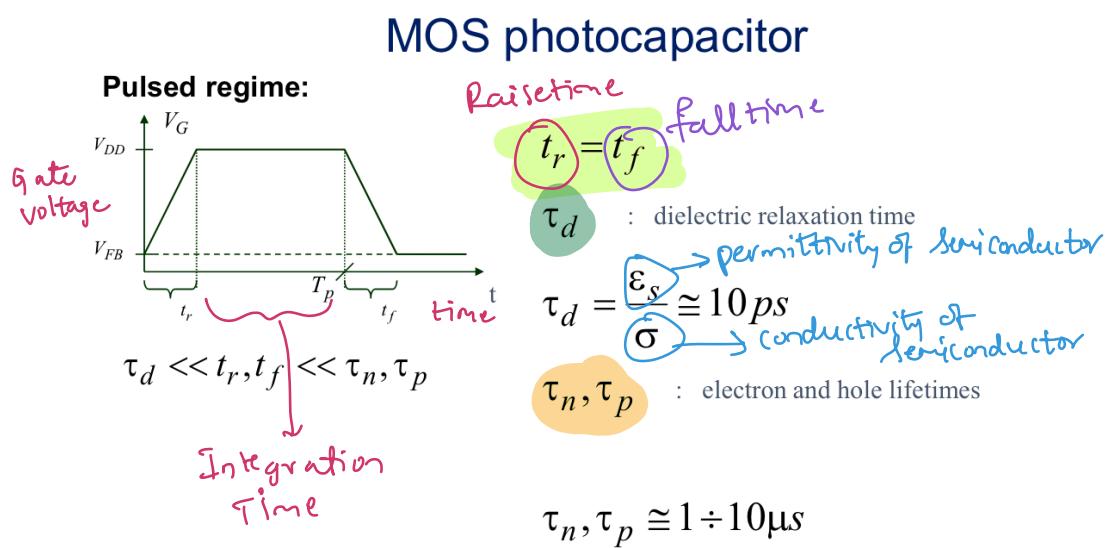


- From the condition of flat band we apply a pulse that brings the voltage applied to the semiconductor to the strong inversion situation if we wait for enough time for strong inversion to be established. This is a Dynamic Situation.
- We apply the Pulse at the time of application

of pulse (considering that the MOS photo capacitor has a p-type substrate, we apply a large positive voltage to the Gate) This **+ve voltage** pushes holes away from the surface and there is a formation of Depleted Region but for formation of Inversion layer it takes time.

- In the above case if we keep the large +ve Gate voltage and if there is no impinging light. The only phenomenon that would occur in the Depleted Region is the generation of e^-H pairs because of Thermal generation.
- If the material is good and lifetime of generated e^-H pairs is long enough we can have an inversion layer.
- Assume instead the case in which we also have photons impinging on the Device and the no. of photons is relatively large. In this case the generation of e^-H pairs is because of Thermal & optical reasons. We may also expect e^-H pairs generated by photony is dominant and after the Integration Time we can see a layer of e^-s near the surface as shown in the MOS capacitor figure.

- In This case we have charge that is proportional to the no. of charges that arrived in the semiconductor. In this way we transform the Optical signal into an Electrical signal.
- MOS Photo Capacitors are simple devices that's why they are very successful in the fabrication of optical sensors.



T_d : Dielectric Relaxation time is the typical time taken for the holes to be pushed away from the surface upon the application of the gate voltage i.e. for the formation of a Depleted Region.

Capacitance of the MOS Structure — IV

The surface potential φ_s given by

$$\sqrt{\varphi_s} = \sqrt{V_i + \gamma^2/4 - \gamma/2}, \quad V_i = V'_G - |Q_i|/C_{ox},$$

increases with V_i , hence it increases as $|Q_i|$ decreases. If V_G is rapidly brought from V_{FB} to a value above the threshold voltage, initially $|Q_i|$ is much smaller than in equilibrium. As a consequence,

$$\sqrt{\varphi_s} \approx \sqrt{V'_G + \gamma^2/4 - \gamma/2} \doteq \sqrt{\varphi_G}$$

is larger than the equilibrium value. In conclusion, a large depleted region is formed in the semiconductor, of width

$$x_d = \sqrt{\frac{2\epsilon_{sc}}{qN_A}} \sqrt{\varphi_G},$$

while no inversion layer is present. As the inversion layer is generated, $|Q_i|$ increases and the surface potential decreases towards the equilibrium value. The time necessary to reach the equilibrium condition is determined by the thermal-generation processes.

This is the analysis of capacitor.

- It is very easy to calculate the value of the surface potential we simply invert the charge per unit area in the inverted layer i.e Q_i

- When we apply the pulse at $t=0$

$Q_i = 0$. when

$$Q_i = 0 \quad V_i = \text{maximum} \\ = V'_G$$

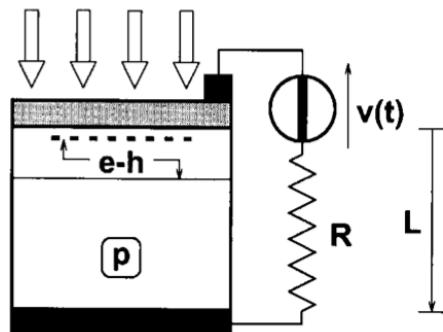
Q) Now, what is the difference b/w a Capacitor and a Photo capacitor?

Ans

- In Capacitor the generation of e-H pair is determined by Thermal Generation
- In photo capacitor the generation of e-H pairs is because of Thermal & optical generation.
- If the optical generation is dominant the majority of e⁻s near the surface is because of

optical generation.

- After the Integration time when the Gate voltage returns to V_{FB} we practically eliminate the vertical field in the SCR so the holes go back and flood the SCR and layer of e^- s are not attracted anymore near the surface because there is no EF any more so these e^- s start diffusing into the substrate and recombine with the holes.
- This mechanism of Diffusing e^- s into the substrate produces a current and we can read the current through the Resistor.



• The Sampling Time is the time required for e^- s to diffuse it may be long in this Device.

Q) How long is the Sampling Time?

MOS Photocapacitor — I

For a p -type substrate, the electron-continuity equation reads

$$\frac{\partial n}{\partial t} + U - \frac{1}{q} \operatorname{div} \mathbf{J}_n = G.$$

At $t = 0$ the gate voltage V_G is suddenly brought from $V_G(0^-) > V_T$ to $V_G(0^+) = V_{FB}$. In one dimension it is $G = G_0 \exp[-k(s + x)] = G_s \exp(-kx)$, with $s = t_{ox}$. Taking the weak-injection case and observing that $J_n(0) = 0$, $J_n(L) \simeq J_n(\infty) = 0$, the above yields

$$\frac{d}{dt} \int_0^\infty q(n - n_{p0}) dx + \frac{1}{\tau_n} \int_0^\infty q(n - n_{p0}) dx = q \frac{G_s}{k},$$

$$\frac{d}{dt} (Q \exp(t/\tau_n)) = q \frac{G_s}{k} \exp(t/\tau_n),$$

with $Q(t) \doteq \int_0^\infty q(n - n_{p0}) dx$. It follows

$$Q(t) - q\tau_n \frac{G_s}{k} = [Q(0) - q\tau_n \frac{G_s}{k}] \exp(-t/\tau_n),$$

showing that the approach to the asymptotic condition is dominated by the minority-carrier lifetime τ_n .

Arg This is relatively easy because we solve the e^- continuity eqⁿ

$$\frac{\partial n}{\partial t} + U - \frac{1}{q} \operatorname{div} \mathbf{J}_n = G$$

Thermal Recombination
and we assume
the weak
injection
condition

optical generation

→ We integrate continuity eqⁿ over one dimension of the device $x=0$ (Interface b/w Semiconductor & oxide layer)

$x=\infty$ (The Bulk is at the infinity)

$$\frac{\partial n}{\partial t} = \frac{\partial(n - n_{p0})}{\partial t} \quad \text{because } n_{p0} \text{ is a constant}$$

$$\int_0^\infty \frac{d}{dt} q(n - n_{p0}) dx +$$

$$\frac{1}{\tau_n} \int_0^\infty q(n - n_{p0}) dx = q \frac{G_s}{k}$$

$\therefore J_n(0) = J_n(\infty) = 0 \quad \therefore$ we don't have
 "J_n" term in the above integral eq?
 → because there is no current because NO current
 can cross from Oxide layer into the semiconductor
 "J_n" is not zero in the bulk but the current
 is because of Diffusion of the population of
 e^-s becomes lesser and lesser because of
 recombination and at some point this current
 is Negligible $\therefore J_n(L) \approx J_n(\infty) = 0$

$$\rightarrow RHS = q \frac{G_s}{K}$$

$G_s(0) = G_s$
 $G_s(\infty) = 0$

$\therefore G = G_s e^{-Kx}$

\rightarrow In conclusion, we obtain a Differential eq[?]
 w.r.t time which is Integrable

i.e.

$$\frac{d}{dt} \left(Q \exp \left(\frac{t}{\tau_{n_s}} \right) \right) = q \frac{G_s}{K} \exp \left(\frac{t}{\tau_{n_s}} \right)$$

Lifetime of e^-s

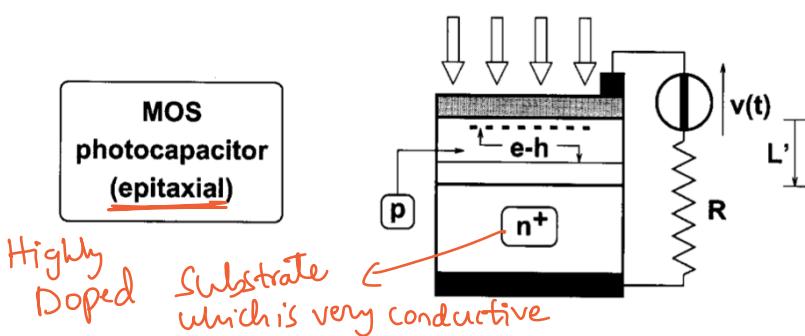
$$Q(t) = \int_0^{\infty} q(n - n_{p_0}) dx$$

with this eq we obtain that the charge per unit Area \propto associated with excess electrons concentration decays w.r.t time

Conclusion: The approach to Asymptotic condition is dominated by Minority-Carrier lifetime T_n . T_n is generally of the order 10μs i.e Sampling Time is long ∵ photocapacitor by itself is a slow sensor.

Q) Can we improve upon the Photo capacitor? Any

Mos Photocapacitor
Epitaxial



$$5\mu\text{m} \leq L' \leq 10\mu\text{m}$$

$$L \geq 200\mu\text{m}$$

The Highly Doped N^+ substrate almost acts like a contact at practically low voltage. It has lifted the contact from Bulk to the edge of PN Junction.

- Apart from the above changes the rest of the functionality remains unchanged.
- Because of N^+ the Boundary conditions change i.e. we don't have $T(x)$ anymore. So we must solve Continuity eq with a Different Boundary Condition.

$$J_n = q D_n \frac{dn}{dx}$$

Consider a photocapacitor built in a p -type epitaxial layer of thickness $L' = a$. To determine the time decay of the excess charge per unit area $Q(t) = q \int_0^a [n(x, t) - n_{p0}] dx$ one must solve the continuity equation

$$\frac{\partial n}{\partial t} + \frac{n - n_{p0}}{\tau_n} - \frac{1}{q} \frac{\partial}{\partial x} q D_n \frac{\partial n}{\partial x} = G_s \exp(-kx),$$

Photocapacitor within an Epitaxial Layer — I

- Consider a photocapacitor built in a p -type epitaxial layer of thickness $L' = a$. To determine the time decay of the excess charge per unit area $Q(t) = q \int_0^a [n(x, t) - n_{p0}] dx$ one must solve the continuity equation

$$\frac{\partial n}{\partial t} + \frac{n - n_{p0}}{\tau_n} - \frac{1}{q} \frac{\partial}{\partial x} q D_n \frac{\partial n}{\partial x} = G_s \exp(-kx),$$

- where the one-dimensional case has been considered. The drift term of the current can be neglected due to the bias condition. The boundary and initial conditions are

$$\left(\frac{\partial n}{\partial x} \right)_{0,t} = 0, \quad n(a, t) = n_{p0}, \quad n(x, 0) - n_{p0} = 2Q(0)\delta(x)$$

(the condition $J_n = 0$ at the bottom boundary does not hold here). One sees that $Q(0) \equiv \int_0^a 2Q(0)\delta(x) dx$. Letting $f \doteq (n - n_{p0}) \exp(t/\tau_n)$ yields

$$\frac{\partial f}{\partial t} = D_n \frac{\partial^2 f}{\partial x^2} + G_s \exp(-kx + t/\tau_n),$$

$$\left(\frac{\partial f}{\partial x} \right)_{0,t} = 0, \quad f(a, t) = 0, \quad f(x, 0) = 2Q(0)\delta(x).$$

→ Q) what are the new Boundary conditions?

A) The Heavily doped n imposes a condition of Equilibrium to the concentration

i.e $n(a, t) = n_{p0}$

'n' at 'a' at every instant of time is equal to n_{p0}

Initial condition: at $t=0$ (when we switch from V_{DD} to V_{FB})

$$n(x, 0) - n_{p0} = 2Q(0)\delta(x)$$

at $t=0$ in this case, we have a layer of e^-s and this is indicated by a Dirac Delta condition which is centered at origin and we take only half of it on the side of semiconductor and the integral of it must be equal to the excess charge at $t=0$.

\therefore The eqⁿ wrt space has a second derivative we need another condition.

$$\left(\frac{\partial n}{\partial x} \right)_{0,t} = 0 \quad \Rightarrow \text{Derivative at any instant of time wrt the surface}$$

\therefore The Differential eqⁿ is linear

$$\frac{\partial n}{\partial t} + \frac{n - n_{p0}}{\tau_n} - \frac{1}{q} \frac{\partial}{\partial x} q D_n \frac{\partial n}{\partial x} = G_s \exp(-kx),$$

For this we can find an integrating factor

$$\exp(t/T_n)$$

\therefore We can define an Auxiliary function

$$f = (n - n_0) \exp(t/T_n)$$

$$\Rightarrow \frac{\partial f}{\partial t} = D_n \frac{\partial^2 f}{\partial x^2} + G_s \exp(-kx + t/T_n)$$

and New Boundary Condition

$$\left(\frac{\partial f}{\partial x}\right)_{0,t} = 0$$

$$f(a, t) = 0,$$

$$f(x, 0) = 2 \Phi(0) f(x)$$

Q) We have to solve the Diff eqⁿ from 0' to 'a', can we express Φ in terms of Fourier series?

Any

Yes

Photocapacitor within an Epitaxial Layer — II

- To solve the above equation it is convenient to consider the function \hat{f} defined in $-2a \leq x \leq 2a$ and such that, for all t :

$$\begin{cases} \hat{f}(x, t) = f(x, t) & 0 \leq x \leq a \\ \hat{f}(-x, t) = \hat{f}(x, t) & -2a \leq x \leq +2a \end{cases}$$

namely, \hat{f} is even on the interval of length $4a$ centered at $x = 0$.

Also, \hat{f} is chosen so that it can be expanded in Fourier series over $-2a \leq x \leq +2a$, with $\hat{g}_k = \cos[k\pi x/(2a)]$:

$$\hat{f} = \sum_{k=0}^{\infty} \hat{c}_k(t) \hat{g}_k(x), \quad \hat{c}_k = \frac{1}{2a} \int_{-2a}^{+2a} \hat{g}_k \hat{f} dx.$$

- Clearly \hat{f} fulfills the boundary condition $(\partial \hat{f} / \partial x)_0 = 0$, but not the boundary condition $\hat{f}(a) = 0$. For this, one must restrict the choice to those \hat{f} such that $\hat{f}(2a - x) = -\hat{f}(x)$, $0 \leq x \leq a$, namely, that are odd in the interval of length $2a$ centered at $x = a$. Letting $\hat{g}_k(2a - x) = -\hat{g}_k(x)$ it is found $\cos(k\pi) = -1$, that is $k = 2i + 1$, $i = 0, 1, 2, \dots$. Defining $g_i \doteq \cos[(i + 1/2)\pi x/a]$ yields

$$c_i \doteq \frac{1}{2a} \int_{-2a}^{+2a} g_i \hat{f} dx = \frac{1}{a} \int_0^{2a} g_i \hat{f} dx = \frac{2}{a} \int_0^a g_i \hat{f} dx.$$

Photocapacitor within an Epitaxial Layer — III

- The equalities above are due to the properties of \hat{f} and g_i . As $f = \hat{f}$ in the interval $0 \leq x \leq a$, the Fourier expansion of f reads

$$f = \sum_{i=0}^{\infty} c_i(t) g_i(x), \quad c_i = \frac{2}{a} \int_0^a f \cos\left(\frac{x}{L_i}\right) dx,$$

with $1/L_i \doteq (i + 1/2)\pi/a$. One sees that $g'_i(0) = 0$, $g(a) = 0$, $g''_i = -g_i/L_i^2$. It can also be shown that g_i is the Green function of the equation to be solved. Now,

$$\int_0^a g_i \frac{\partial f}{\partial t} dx = \frac{d}{dt} \int_0^a g_i f dx = \frac{a}{2} \frac{dc_i}{dt}$$

and, integrating by parts and using the boundary conditions,

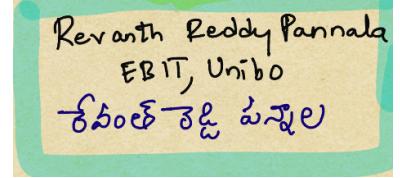
$$\int_0^a g_i \frac{\partial^2 f}{\partial x^2} dx = \int_0^a \frac{d^2 g_i}{dx^2} f dx = -\frac{1}{L_i^2} \int_0^a g_i f dx = -\frac{a}{2} \frac{c_i}{L_i^2}.$$

Defining

$$\alpha_i \doteq \frac{2}{a} \int_0^a g_i G_s \exp(-kx) dx,$$

the equation for $c_i(t)$ finally reads

$$\frac{dc_i}{dt} + \frac{c_i}{\tau_i} = \alpha_i \exp(t/\tau_n), \quad \tau_i \doteq \frac{L_i^2}{D_n}.$$



Photocapacitor within an Epitaxial Layer — IV

- The initial condition is

$$c_i(0) = \frac{2}{a} \int_0^a g_i f(x, 0) dx = \frac{2}{a} \int_0^a g_i 2Q(0) \delta(x) dx = \frac{2}{a} Q(0),$$

independent of i . Integrating yields $c_i(t) \exp(t/\tau_i) - c_i(0) = \alpha_i \tau_i^* [\exp(t/\tau_i^*) - 1]$, with $1/\tau_i^* \doteq 1/\tau_n + 1/\tau_i$ whence, using $n - n_{p0} = f \exp(-t/\tau_n)$,

$$n - n_{p0} = \sum_{i=0}^{\infty} g_i [\alpha_i \tau_i^* + (c_i(0) - \alpha_i \tau_i^*) \exp(-t/\tau_i^*)].$$

Note that the excess charge per unit area $Q(t) = q \int_0^a (n - n_{p0}) dx = q \sum_{i=0}^{\infty} (-1)^i L_i [\alpha_i \tau_i^* + (c_i(0) - \alpha_i \tau_i^*) \exp(-t/\tau_i^*)]$ does not vanish when $t \rightarrow \infty$ as long as $G_s \neq 0$. Using $\tau_i = L_i^2/D_n$ and the definition of the minority-carrier diffusion length $L_n = \sqrt{\tau_n D_n}$ one finds

$$\tau_i = \tau_n L_i^2 / L_n^2 = \tau_n a^2 / [\pi L_n (i + 1/2)]^2.$$

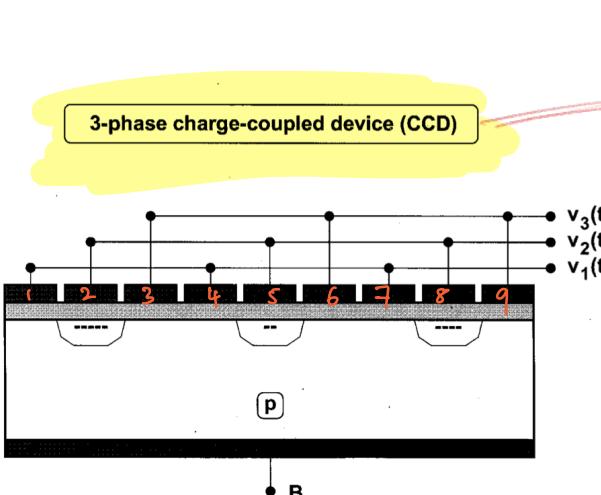
- By way of example one may take $\tau_n = 10 \mu s$, $D_n = 10 \text{ cm}^2/\text{s}$, whence $L_n = 100 \mu \text{m}$. As $\tau_{i+1} < \tau_i$ and, in particular, $\tau_1 = \tau_0/9$, the slowest decay rate corresponds to the term with $i = 0$, whereas the terms with $i > 0$ are less important. Taking by way of example $a = 10 \mu \text{m}$ yields $\tau_0 \simeq \tau_n/100$, $\tau_0^* \simeq \tau_0$.

Note: If we use MOS epitaxial layer photo capacitor over a MOS photo capacitor we gain a factor of atleast 100 in the **sampling time**.

→ We know Photo Capacitor is a simple device ∵ many of the complicated arrays of optical Sensors are made of putting Photo Capacitors one near the other. To build Matrices for Arrays made of Photo Capacitors.

At this point it is much convenient to talk about possible Architectures that are used to build arrays of Photo sensors.

ex: Cameras , Cell phones
(Field of Optical sensors)



* They are a sub class of larger class of Devices called Charge Transfer Devices

- Assume we have 1D Array of MOS photocapacitors one near the other. The first observation Metal Gate seem to cover almost completely the device so light cannot enter it.
- However, in this device Gate contacts are not necessarily made of metals. It is possible to manufacture the **Contacts** in a way that they are practically **Transparent to Radiation**
- The Gates are separated from each other and are independently controlled by applied voltages but they are very close to each other
- If you look from left to right

Gates 1, 4, 7 have same voltage $V_1(t)$

Gates 2, 5, 8 $V_2(t)$

Gates 3, 6, 9 $V_3(t)$

and so on...

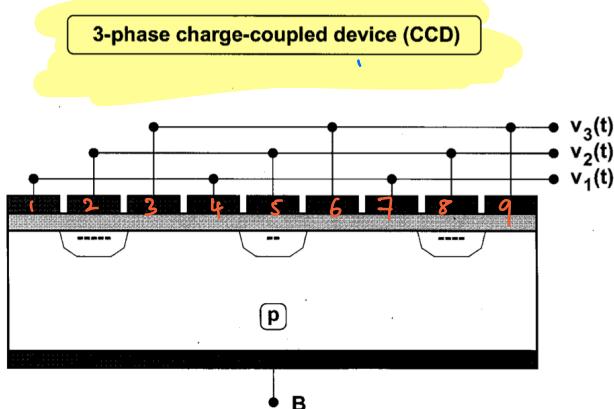
This is called **3-phase CCP**

→ These phases have an evolution in Time
i.e they go from V_{FB} to V_{DD}

e.g. $v_2(t)$ is at High Voltage

$v_1(t), v_3(t)$ are at Low Voltage

∴ under Gates 2, 5, 8 we have
depleted Regions as shown in the figure.



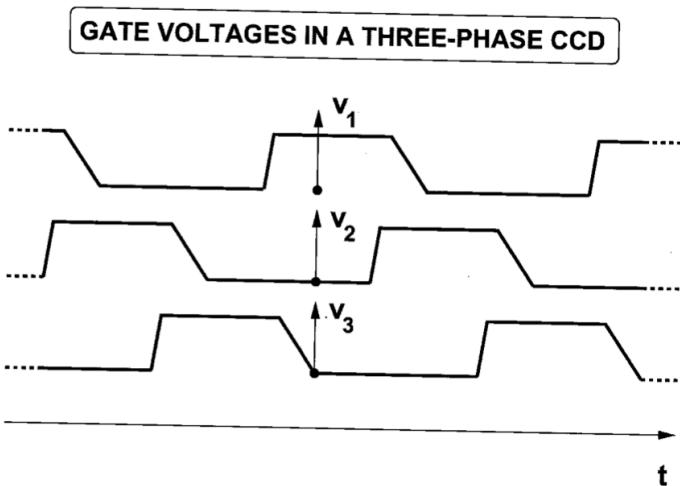
→ ∴ During Integration time some charge is accumulated in these three photo capacitors 2, 5, 8 depending on illumination.

Of course light enters the whole semiconductor and there is optical generation under all the photo capacitors (i.e. everywhere). But if

don't have High Gate voltage then there is no field \rightarrow $e^- - h$ pairs that are optically generated simply diffuse away and recombine

Q) How can we read these package of e^- s?

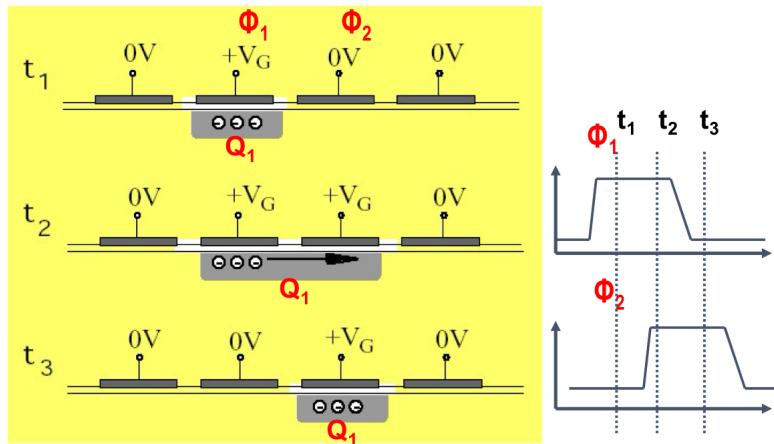
Ans The idea in CCD is in the phary to move the package of e^- s along the CCD and bring them for instance to PTS of the device and Read them with a reading device.



T. 34.18: Andamento delle tensioni di gate in un CCD a tre fasi.



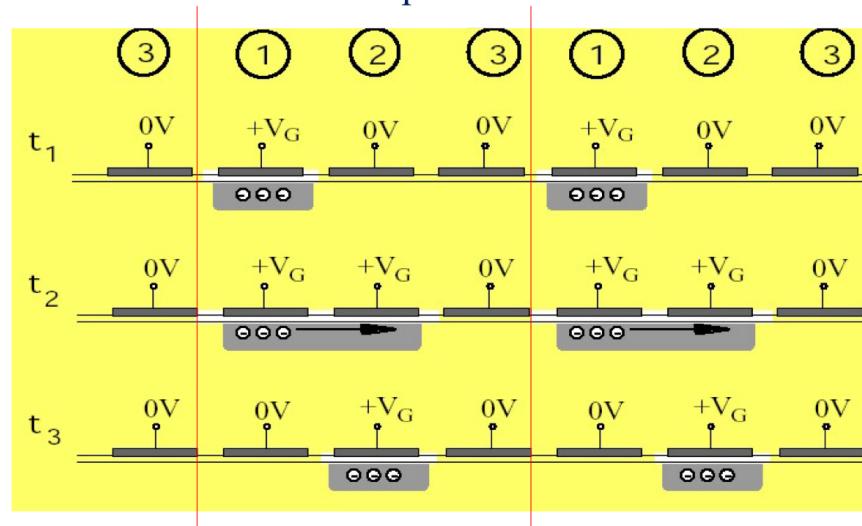
Charge transfer mechanism (is both Diffusion & Drift)



Note: minimum of 3 phases are necessary to ensure one dimensional motion of weight packets. (charge)



Three phase CCD





Charge Transfer Devices

CTD – Charge Transfer Devices

CCD – Charge Coupled Devices

Technology evolution:

1967: photodiodes and MOS phototransistors (passive pixel arrays) → charge is read out using row and column decoders

1970: CCD image sensors → charge is shifted out

1980: technology scaled to 0.5um → CMOS sensors with active pixel arrays → voltage is read out using row and column decoders (current technology of choice)

CCD - The History of CCDs or Charge Coupled Devices
George Smith and Willard Boyle invented the first CCDs or charge coupled devices



The Nobel Prize in Physics 2009

“for the invention of an imaging semiconductor circuit – the CCD sensor”

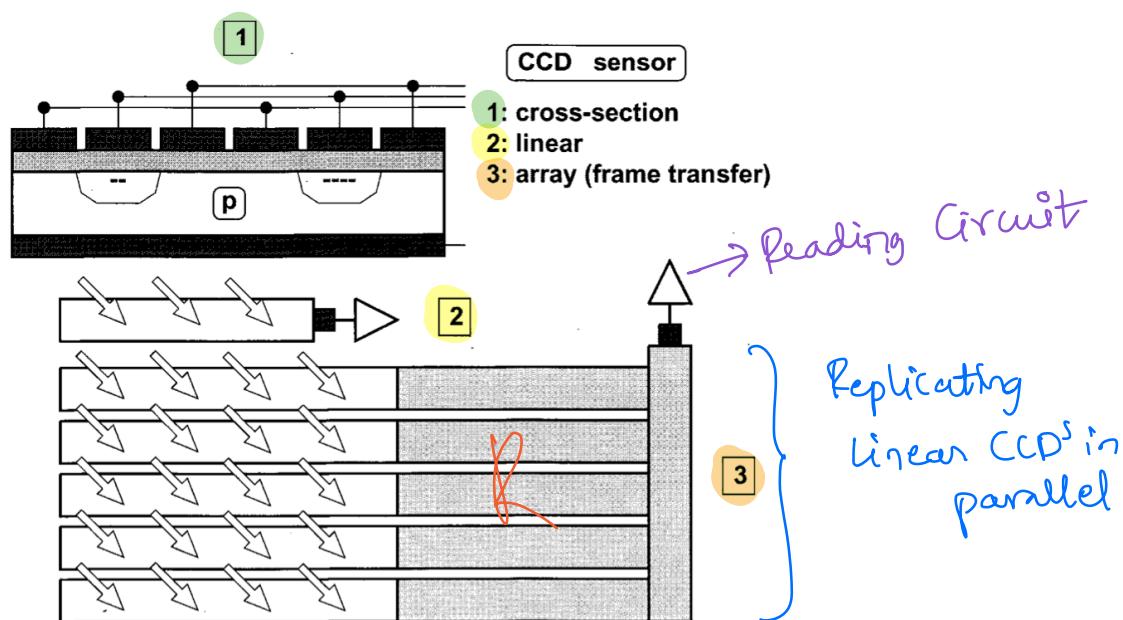
Willard S. Boyle George E. Smith

Bell Laboratories
Murray Hill, NJ, USA

W.S. Boyle and G.E. Smith, 49 (1970) 587; Bell Systems Technical Journal



Bell Labs researchers Willard Boyle (left) and George Smith (right) with the charge-coupled device, which transforms patterns of light into useful digital information and is the basis for many forms of imaging, including camcorders and satellite surveillance. Photo taken in 1974.

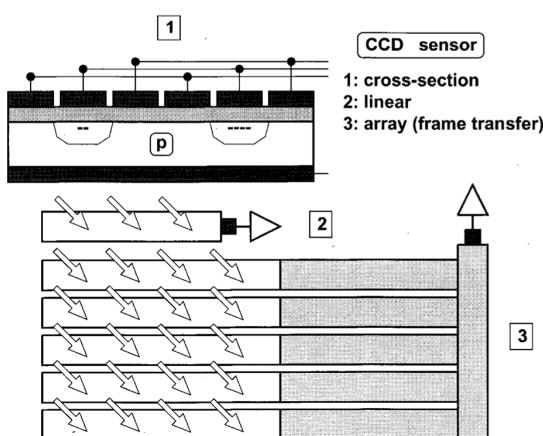


- The only problem here is when we are moving the charge packets there is still generation of $e^- - h^+$ pairs because of impinging light which in a way pollutes the existing packets.
 - ∴ We must transfer the packets as fast as possible into this region They are also CCD which are protected for the light they have a layer on top that prevents the radiation to cross into the semiconductor. This architecture is called Train Transfer Architecture.

09/04/25

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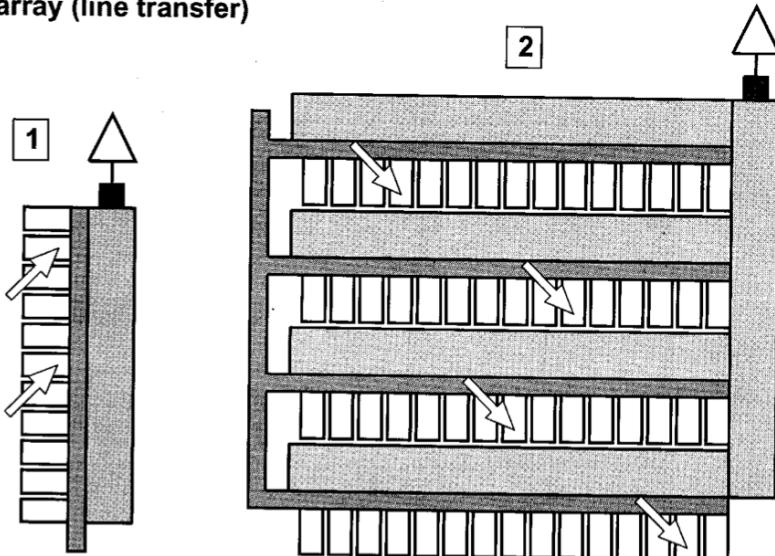
If you want to build a display for a TV or computer. Any screen for that matter where we want to provide a succession of frames one present one after the other in order to provide illusion of motion.

- If the frames are presented at a time distance shorter than 50 ms the human brain has a retention of image that there is an illusion of movement.
- Typically video screens are scanned row by row, there is also another format called Interlaced format in which rows of odd index ex: 1, 3, 5... are scanned first and followed by even index. This is called Interlaced format. With this essentially one can divide the frequency of frames by 2. This is more relaxed when compared to original one.

CCD sensor

1: linear

2: array (line transfer)



Q) How can we use interlaced format when we use Frame Transfer CCD ?

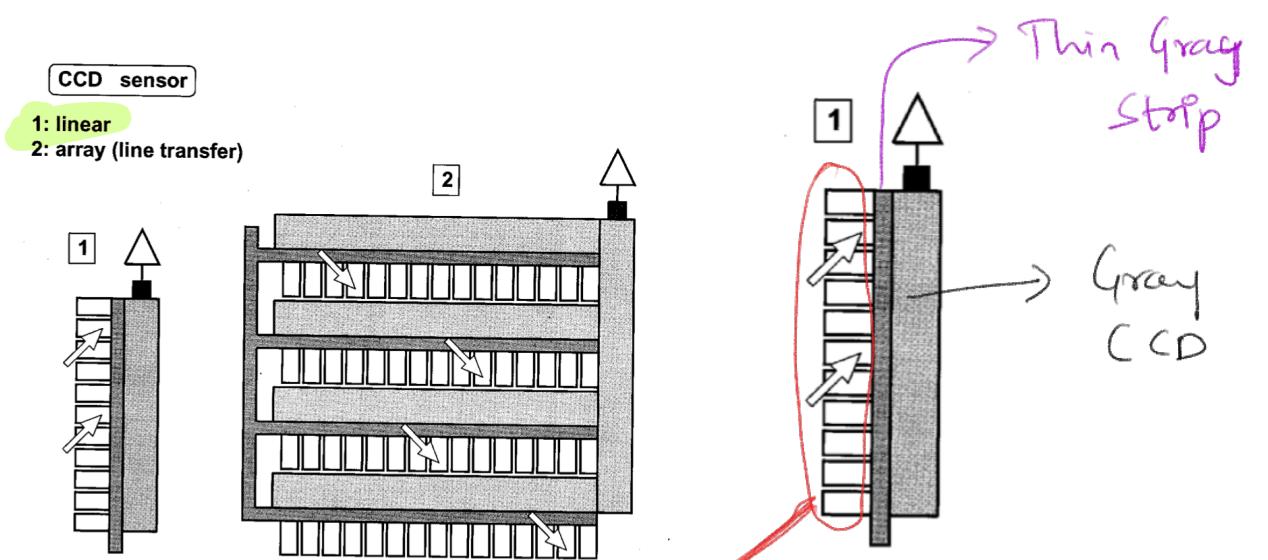
Ans This is easy because, simply during One Integration Time we keep the Gate operate at High voltage the Gate of ODD index .

In the next Integration time we operate the Gate of even Index . This dramatically provides for interlaced format to the signal (i.e it can be achieved by changing The control of the clocks)

→ Another advantage of solid state sensors like FTA (Frame Transfer Arrays) and CCD's which are used in the implementation of video displays is in the possibility of obtaining colour signals.

- It is sufficient to use instead of single array three arrays. (one for each fundamental colour)
- The incoming optical signal is split into THREE fundamental colours & each fundamental colour is oriented into '3' different arrays - and they are combined later into a single signal.
This implementation is simple }

→ Another possible implementation of 2D optical device - we consider first linear array indicated on the left -



- Individual photo capacitors, unusual here photo capacitors are operated alternatively during Integration Time. So photo capacitors integrate the charge band on the optical signal
- The Thin Gray strip is a gate and one can transfer the charge that has been integrated in each photo capacitor from left to right into the vertical CCD (\therefore Charge after integration is transferred parallelly into the ^{Gray}CCD because it protected from radiation)
- So the Duty cycle of this device is very good because charge transfer happens pretty quickly.

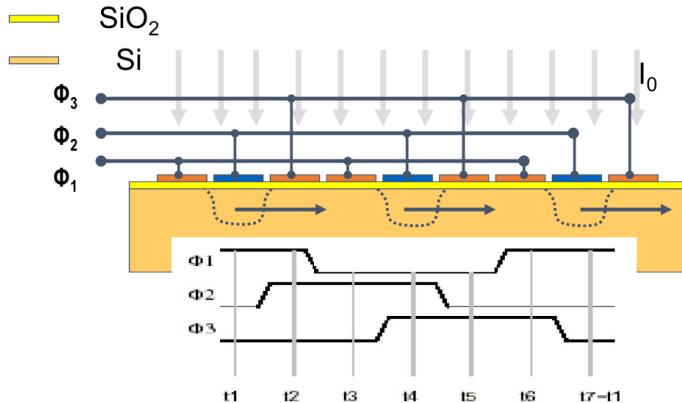


2. Charge transfer

A CCD is a dynamic analog (charge) shift register;

Charge transfer must occur at high enough rate to avoid corruption by leakage
but slow enough to ensure high charge transfer efficiency

A three-phase is typically implemented.



Charge transfer efficiency

- $\eta = (1-\varepsilon) \leq 1$, CCD charge transfer efficiency
Is the fraction of signal charge transferred from one CCD stage to the next.
(ε is the charge transfer inefficiency).

- Must be made very high since charge is transferred up to $p \times (n+m)$ stages,
with p number of phases, n number of columns, m number of rows.
Example: An array of $N=1000$ pixels and $p=3$ phases with $\varepsilon=10^{-4}$ gives:

$$\eta_{\text{tot}} = \eta^{pN} = (1-\varepsilon)^{pN} = 74\%$$

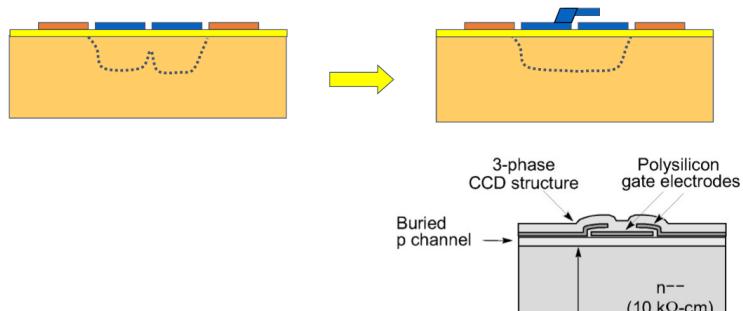
The charge transfer efficiency of a 1024 x 1024 CCD image sensor is:

η	Fraction at output
0.999	0.1289
0.9999	0.8148
0.99999	0.9797

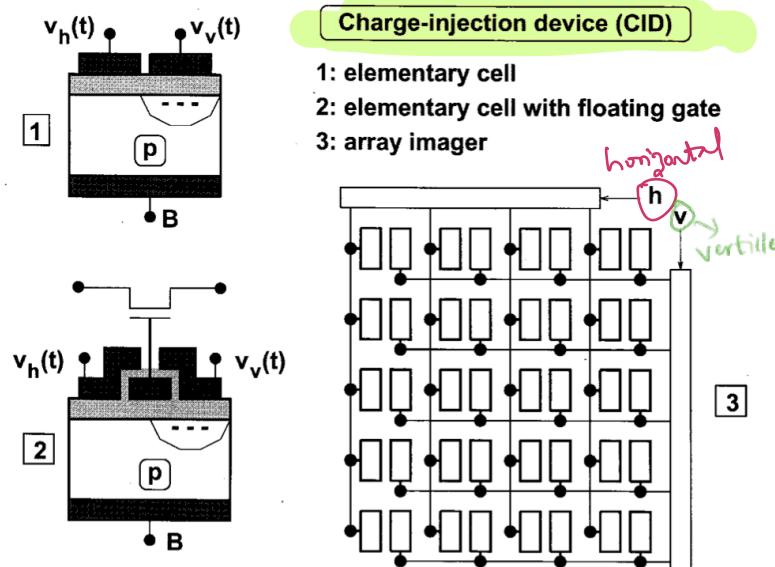
Optimization of charge transfer

Fringing fields can be increased by:

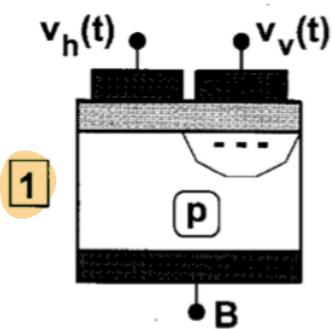
- increasing the gate voltage difference
- reducing the spacing between capacitors and overlapping the poly gates
- Use low-doped substrate



Now we are learning
→ Another type of charge Transfer Device
i.e CID Charge Injection Device



operation principle is similar to that of CCD but final operation is different.



- Here we can observe that each individual pixel has Two Gate voltages. Therefore there are '4' possible combinations

$v_h(t)$ Horizontal voltage	$v_v(t)$ vertical voltage
L	L
L	H
H	L
H	H

- Here voltages are low & high & the light impinges on there "charge accumulation under v_v "
- Now if we also make v_h high. in this way we will succeed in forming a unique potential well underneath the Two Gates.
 \therefore Inverted charge distributes uniformly between the two gates
- In the next stage we keep v_h high & v_v low in this case the charge that was uniformly distributed by two Gates shifts to the left.

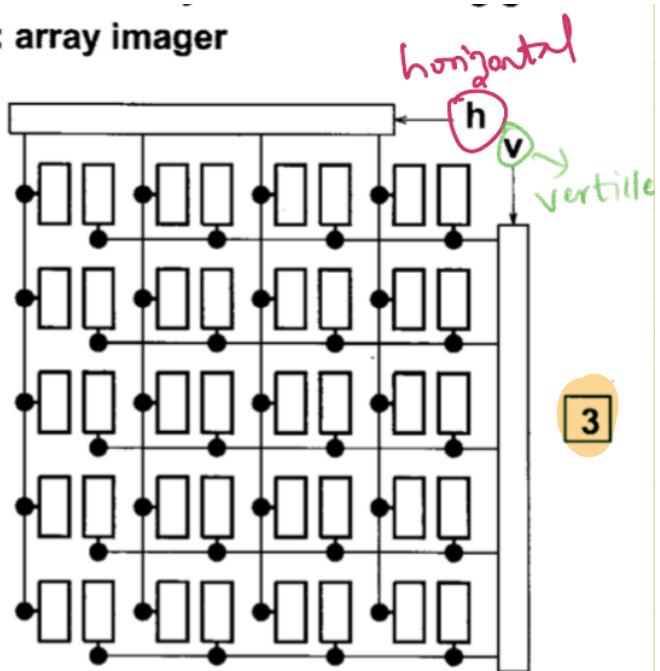
In principle we can repeat the above operation several times. If we want to Read the Charge

packet we put both the Gate voltages Low
in this case the Inverted charge starts
Diffusing into the Bulk and we produce a
current that is readable by a reading Device

Q) can we replicate the above phenomenon to
form a Two Dimensional Device?

Ans YES

3: array imager



- This shows Top view of an Array of Charge injection device
- All the gates that are on the right in the same Row are connected together to the vertical control
- Similarly the Gates that are on the left in the same Row are connected to the horizontal control.

- Assume All The Gates are kept High the one integrating during Integrating time the Charge accumulated will equally distribute under each pair of Gate

- If now we want to read one individual pixel that is in the Upper left. So we operate vertical control of 1st column to low & at the same time vertical control of control of same row to low. In this case each charge will be pushed into the substrate & will be read by the reading device.
- At the same time all the pixels in the same first row will have the left Gate high but the right gate kept low.

They will keep the charge under the left Gate

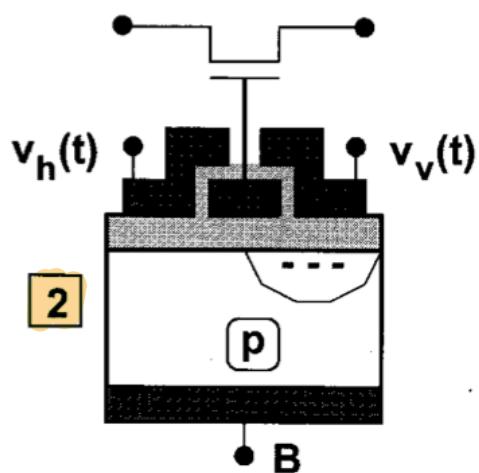
- Similarly in the left most column will have the Right Gate kept High & Left Gate kept low

And all the remaining Pixels ^{will} have both Gates High so they keep the charge. So this allows us to address each individual pixel.

→ In this case a single reading device is used
 so this device is very efficient, but
 The reading activity destroys the information.

8) Can we make the CID device better?
 i.e. Reading without losing information?

Ans Yes, we can !



- This is shown in the figure which is slightly modified

Here in addition to

v_h & v_v There is an additional Gate which is connected to the Gate of an MOS Transistor.

- Since the additional Gate is not connected to any generator, that means value of the electric potential of the additional Gate is determined by Electro static induction. This Gate is also called a Floating Gate

→ Now assume we are operating C1D as described before i.e Inverted layer present under the Right Gate and Then make the Left Gate High so the charge distributes Uniformly

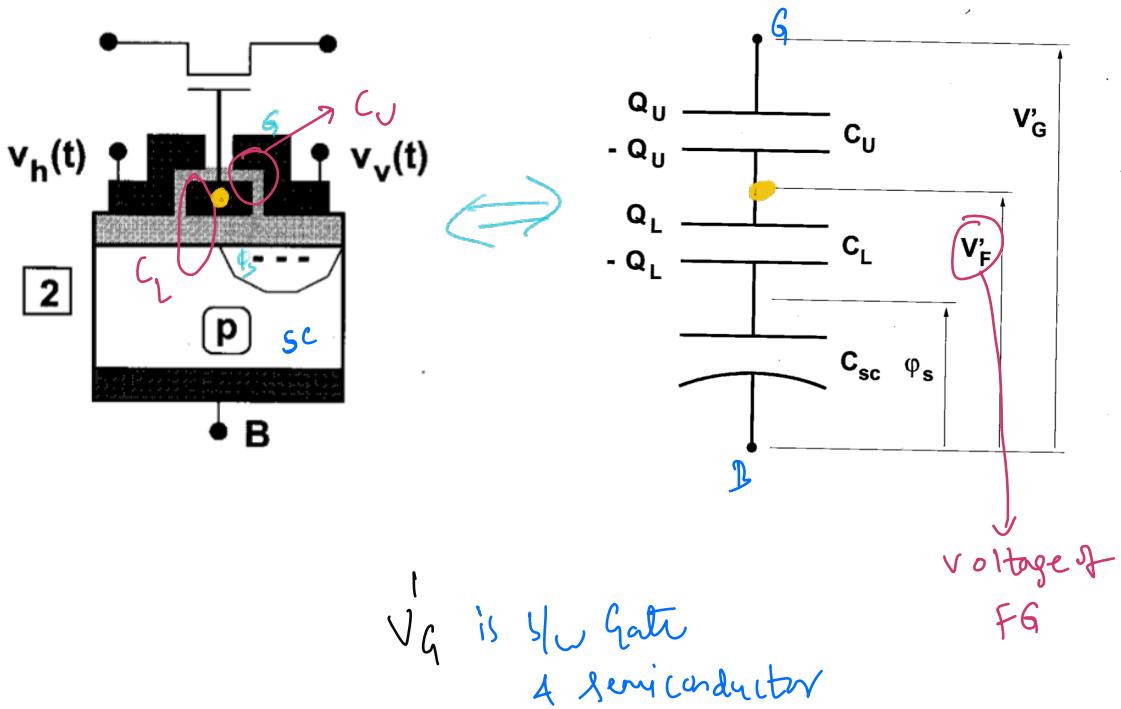
- Then keep Left High and Right Low and in this step the charge transfers completely to the left Interestingly this charge has passed under the channel under the Floating Gate this changes the Electric potential of the Floating Gate.

→ since EP of FG is also the EP of MOS Transistor on Top. When charge transfer takes from Right to Left the FG activates and switches on the channel in the MOS transistor and we can read a signal in the Transistor just because the charge in the Transistor just because the charge in the C1D made a transition from Right to Left or vice versa

- This type of reading is a Non Destructive Reading Of course it can be Repeated

This is incredibly efficient!

Q) What is the working operation of a Floating Gate?



- we want to know how the charge induction in the semiconductor affects V_F^1 because this is the voltage that is common with the MOS Transistor.
 - The two capacitors C_W & C_L are linear

Q_U charge per unit area present in the upper plate of C_U , $-Q_U$ is charge per unit area in the lower plate of C_U

Similarly Q_L , $-Q_L$ are for C_L

- On the other hand in the floating gate there is no charge. So the floating gate is globally neutral

$$\therefore Q_L = -Q_U$$

Floating Gate

For a *p*-type substrate, the inversion charge per unit area is given by

$$Q_i = -C_L (V_F - V_{FB} - \varphi_s - \gamma\sqrt{\varphi_s}), \quad \varphi_s \geq 0,$$

where V_F is the floating-gate voltage. As no net charge is present in the floating gate, it is $Q_U = Q_L$ whence

$$C_U (V_G - V_F) = \frac{C_U C_L}{C_U + C_L} (V_G - \varphi_s).$$

In the above, $C_{U(L)}$ is the upper(lower)-oxide capacitance per unit area, and Q_U, Q_L the corresponding charges per unit area. Solving for φ_s yields

$$\varphi_s = \frac{C_U + C_L}{C_L} V_F - \frac{C_U}{C_L} V_G \Rightarrow V_F - \varphi_s = \frac{C_U}{C_L} (V_G - V_F).$$

As the calculation holds only for $\varphi_s \geq 0$, from the above it follows $V_F \geq C_U V_G / (C_U + C_L)$. In conclusion, letting $r \doteq C_U / C_L$ the inversion charge as function of V_F reads

$$Q_i = -C_L [r (V_G - V_F) - V_{FB} - \gamma\sqrt{(1+r) V_F - r V_G}].$$

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→ Other applications of CCD

- 1) CCD as a Memory
- 2) CCD as a Delay Line