Computer organization and architecture

Lesson 21

Memory exercises

Exercise 21.1 – opposite to the Exercise 19.1

Come up with a sequence of addresses for which a fully associative cache with a size (capacity) of 16 words and block size of 4 words and with least recently used (LRU) replacement outperforms a direct mapped cache that has the same capacity and block size.

Exercise 21.2

You have a 2-word cache with block size of 1 word and access pattern: 0x0, 0x4, 0x8, ...

What is the miss rate for a direct-mapped cache and a 2-way set associative cache with the LRU policy?

Exercise 21.3 A cache has the following parameters:

b, block size given in numbers of words;

S, number of sets;

N, number of ways;

A, number of address bits.

a) In terms of the parameters described, what is the cache capacity, *C*?

b) In terms of the parameters described, what is the total number of bits required to store the tags?

c) What are *S* and *N* for a fully associative cache of capacity *C* words with block size *b*?

d) What is *S* for a direct mapped cache of size *C* words and block size *b*?

Exercise 21.4 Consider the following repeating sequence of LDR addresses:

0x40 0x44 0x48 0x4C 0x70 0x74 0x78 0x7C 0x80 0x84 0x88 0x8C 0x90 0x94 0x98 0x9C 0x0 0x4 0x8 0xC 0x10 0x14 0x18 0x1C 0x20

Assuming C = 16, and least recently used (LRU) replacement for associative caches, determine the effective miss rate if the sequence is input to the following caches, ignoring startup effects (i.e., compulsory misses).

a) direct mapped cache, b =1 word

b) fully associative cache, b =1 word

c) two-way set associative cache, b= 1 word

d) direct mapped cache, b =2 words

Exercise 21.5 You are building a computer with a hierarchical memory system that consists of separate instruction and data caches followed by main memory.

You are using the ARM multicycle processor from the lesson 15 running at 1 GHz.

a) Suppose the instruction cache is perfect (i.e., always hits) but the data cache has a 5% miss rate.

On a cache miss, the processor stalls for 60 ns to access main memory, then resumes normal operation.

Taking cache misses into account, what is the average memory access time?

b) How many clock cycles per instruction (CPI) on average are required for load and store word instructions considering the non-ideal memory system?

c) Consider the benchmark application that has 25% loads, 10% stores, 13% branches, and 52% data-processing instructions.

Taking the non-ideal memory system into account, what is the average CPI for this benchmark?

d) Now suppose that the instruction cache is also non-ideal and has a 7% miss rate.

What is the average CPI for the benchmark in part (c)?

Take into account both instruction and data cache misses.