Combinational logic blocks in Logisim and Verilog

Task 1

Design the complete 4-bit ALU circuit in Logisim having the following operations.

s_2	s_1	s_0	Operations
0	0	0	$B - 1$
0	0	1	A NOR B
0	1	0	$A - B$
0	1	1	A XNOR B
1	0	0	1
1	0	1	A NAND B
1	1	0	A plus B
1	1	1	A'

Task 2

Write a Verilog module for the complete 4-bit ALU circuit having the operations from the task 1.

Write a testbench that shows the work of your circuit.

Task 3

Larger multiplexers can be constructed from smaller multiplexers. Write a structural Verilog code that implements an 8-to-1 multiplexer constructed from seven 2-to-1 multiplexers.

Write a testbench that shows the work of your circuit.