

Task 1

Write a behavioral Verilog module for a 4-bit shifter from the lecture 3 "Combinational logic blocks". Write a testbench that shows the work of your circuit.

Task 2

Write a behavioral Verilog module for a 4-bit barrel shifter from the lecture 3 "Combinational logic blocks". Write a testbench that shows the work of your circuit.

Task 3

Design a 3-bit modulo 8 Gray code counter with no inputs and three outputs in Verilog. Write a testbench that presents the operation of your circuit.

Task 4

Construct the following circuit in Verilog. The circuit has five input signals and one output signal. The five input lines are labeled W, X, Y, Z, and E, and the output line is labeled F. E is used to enable (turn on) or disable (turn off) the circuit; thus, when $E = 0$, the circuit is disabled, and F is always 0. When $E = 1$, the circuit is enabled, and F is determined by the value of the four input signals, W, X, Y, and Z, where W is the most significant bit. If the value is odd, then $F = 1$, otherwise $F = 0$. Write a self-checking testbench for this module.