Switch level programming in Verilog

The switch primitives (transistor models) are: `nmos`, `pmos`, `cmos` (for the transmission gate)

Usage:

```
nmos (drain, source, gate);
pmos (drain, source, gate);
```

Transmission gate:

```
cmos (w, datain, ncontrol, pcontrol);
```

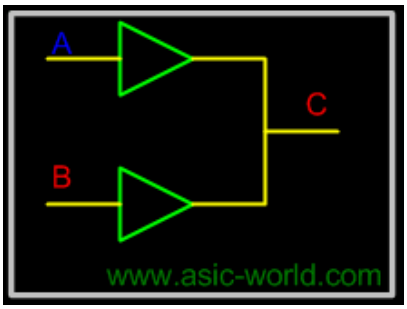
is equivalent to:

```
nmos (w, datain, ncontrol);
pmos (w, datain, pcontrol);
```

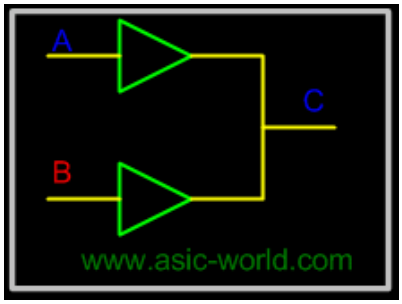
Verilog signal strength levels:

Strength Level	Specification Keyword
7 Supply Drive	`supply0  supply1`
6 Strong Pull	`strong0  strong1`
5 Pull Drive	`pull0  pull1`
4 Large Capacitance	`large`
3 Weak Drive	`weak0  weak1`
2 Medium Capacitance	`medium`
1 Small Capacitance	`small`
0 Hi Impedance	`highz0  highz1`

Examples:



Two buffers that have output
A : `pull1`
B : `supply0`
Since `supply0` is stronger then `pull1`,
Output C takes value of B.



Two buffers that has output
A : `supply1`
B : `large1`
Since `supply1` is stronger then `large1`,
Output C takes the value of A

CMOS not gate:

```
module not_switch (out, in);
   output  out;
   input   in;

   supply1 power;
   supply0 ground;

   pmos (out, power, in);
   nmos (out, ground, in);

endmodule
```

CMOS nand gate:

```
module nand_switch(out, a, b);
   input a, b;
   output out;

   supply0 vss;
   supply1 vdd;
   wire net1;

   pmos p1 (out, vdd, a);
   pmos p2 (out, vdd, b);
   nmos n1 (net1, vss, a);
   nmos n2 (out, net1, b);

endmodule
```