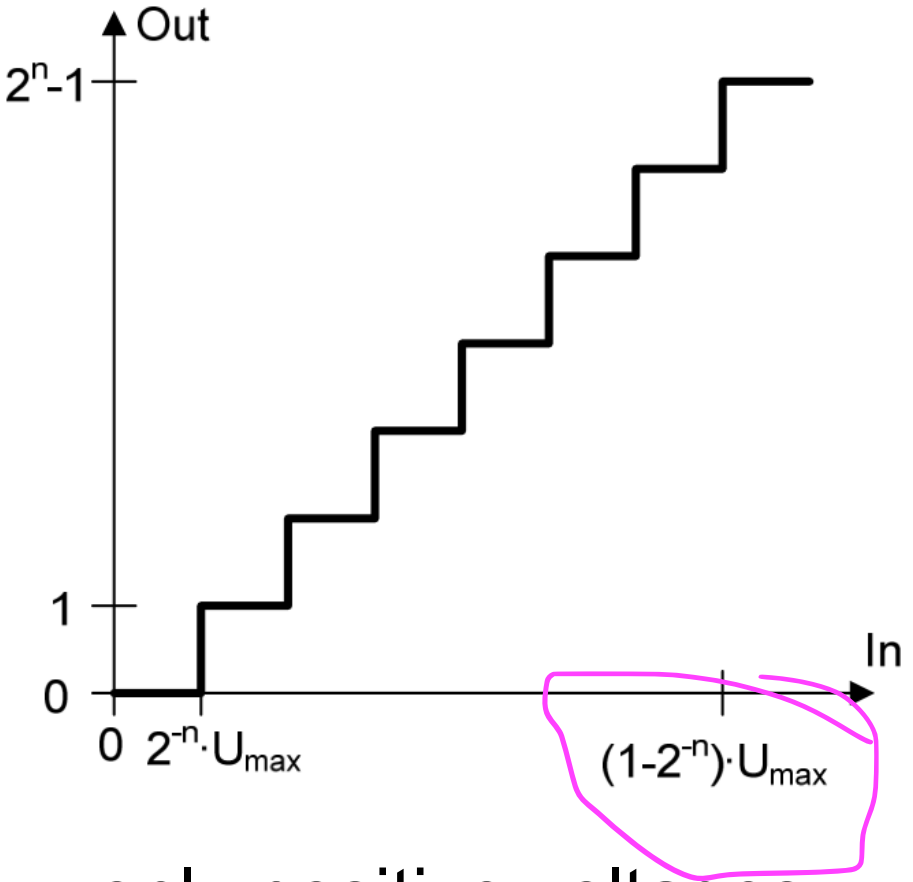
Digital Logic Design

Lecture 12

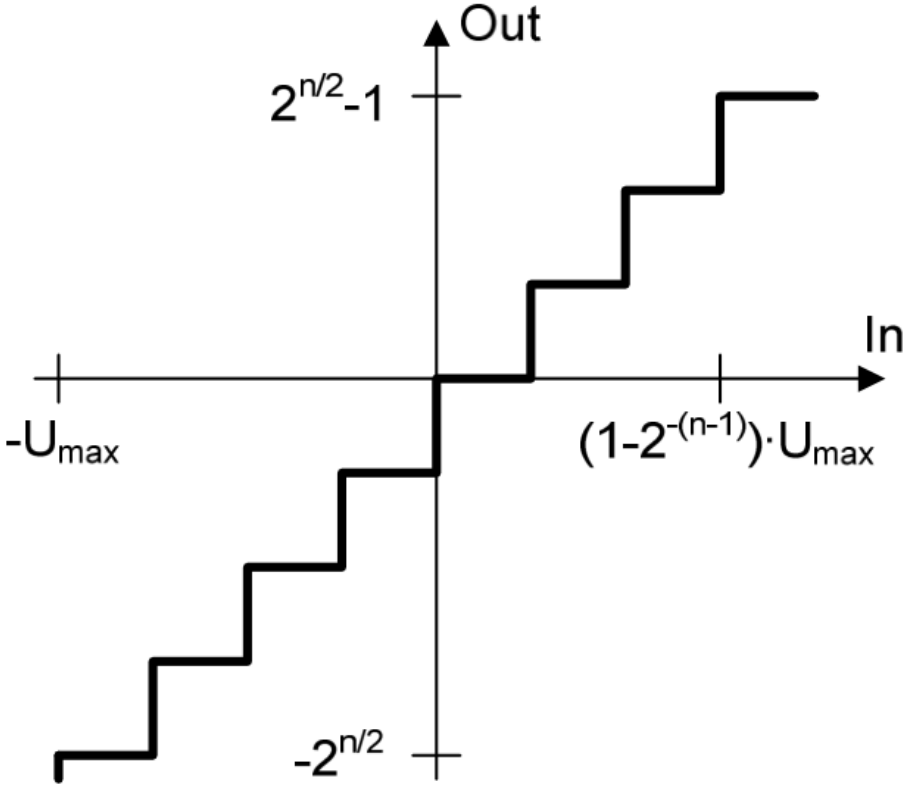
Digital to analog and analog to digital converters

Unipolar converter



only positive voltages

Bipolar converter



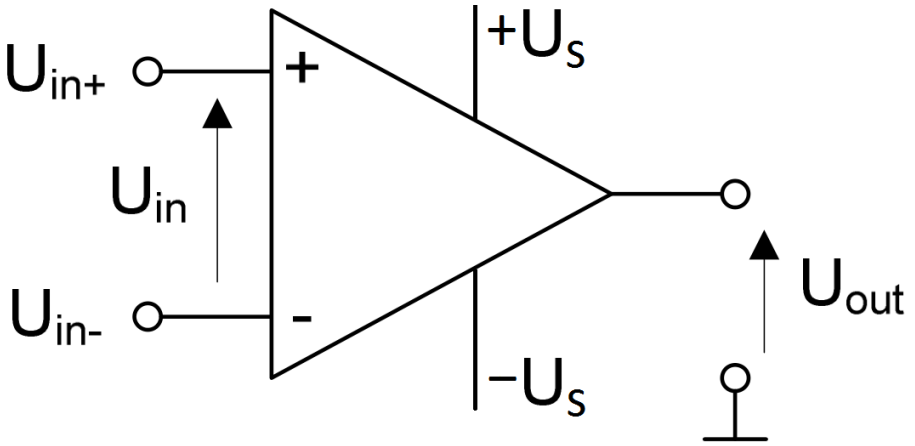
both positive and negative voltages

Unipolar converters are suitable when the property we want to convert from analog to digital always is positive.

Example: the measurement of the fluid level in a tank

Many ADCs contain a DAC as an internal building block

Many DACs are implemented using **operational amplifiers**



OpAmp is an integrated circuit that amplifies the differential signal supplied between the positive and the negative input terminal.

$$U_{out} = A\,U_{in} = A\left(U_{in+} - U_{in+}\right)$$

A is very large

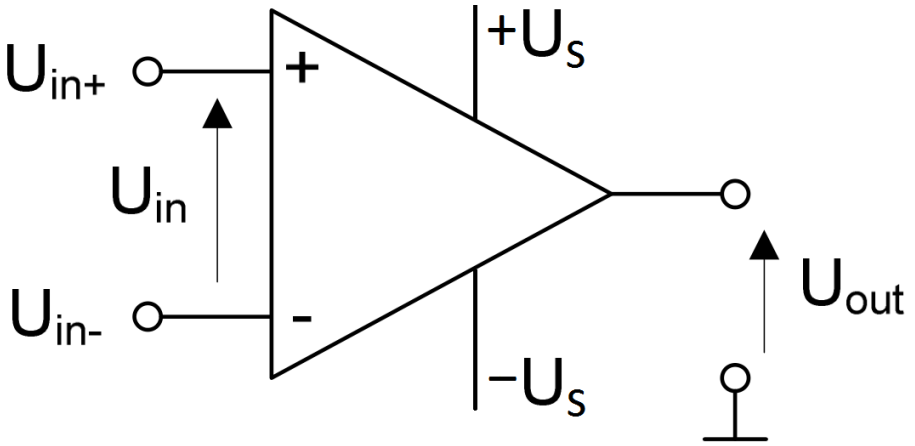
The input impedance of the OpAmp is very high (few MΩ)

This means that only a negligible current will flow in and out of the input terminals.

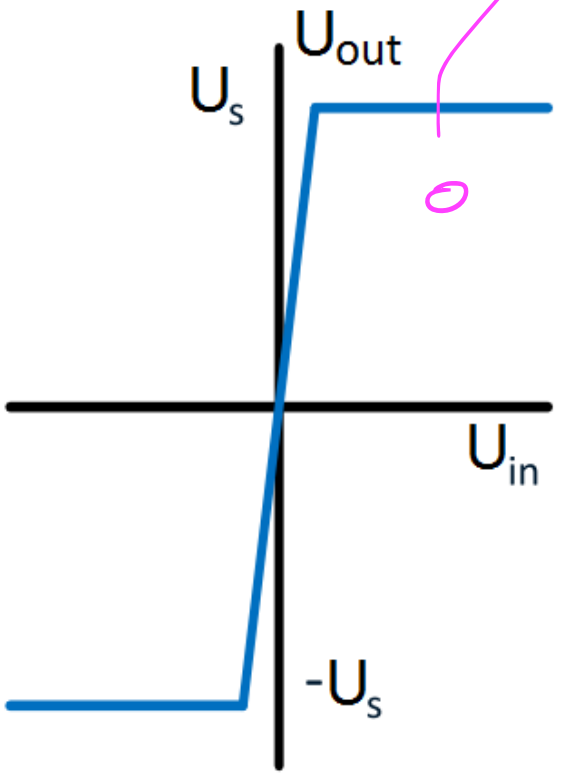
The output impedance is very low (few ohms).

This means that most of the output voltage will be supplied to the following circuit.

Comparator



$$U_{out} = \begin{cases} +U_s, & if \quad U_{in+} > U_{in+} \\ -U_s, & if \quad U_{in+} < U_{in+} \end{cases}$$



Since the amplification is very high the amplifier will saturate and the output voltage will not be the amplification *A* times the input signal but it will saturate at the positive supply voltage of the circuit.

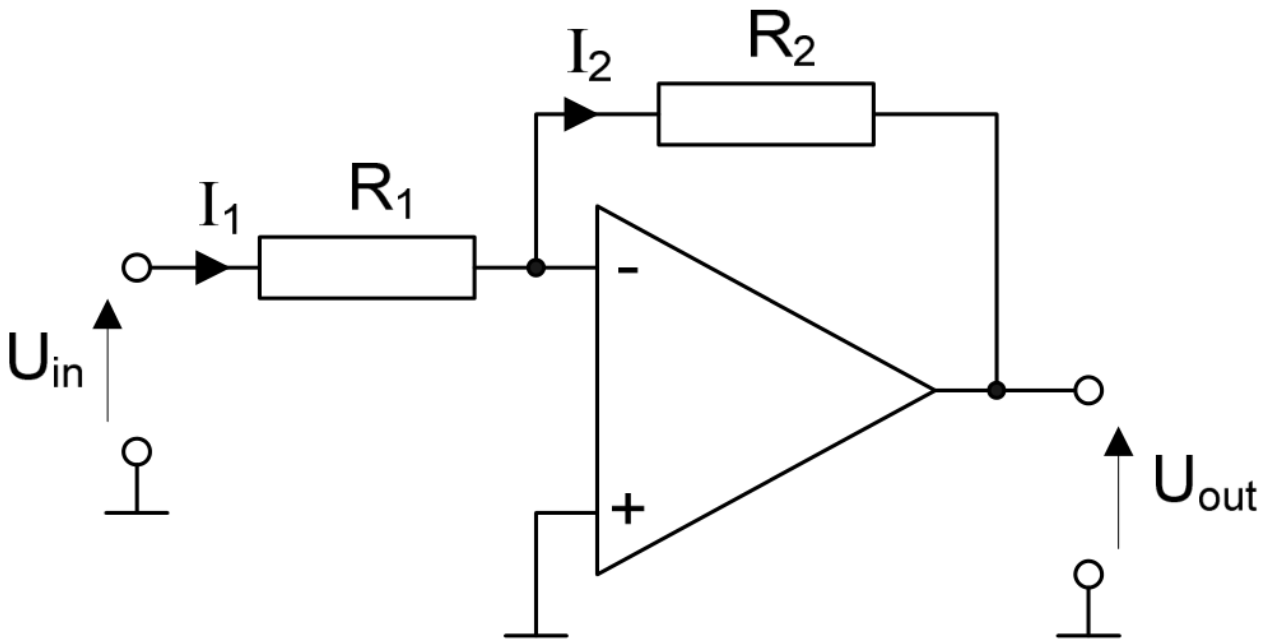
If the differential input signal is negative then the amplifier will saturate at the negative supply voltage.

Inverting amplifier

$$I_1 = I_2 \Rightarrow$$

$$\frac{U_{in} - 0}{R_1} = \frac{0 - U_{out}}{R_2} \Rightarrow$$

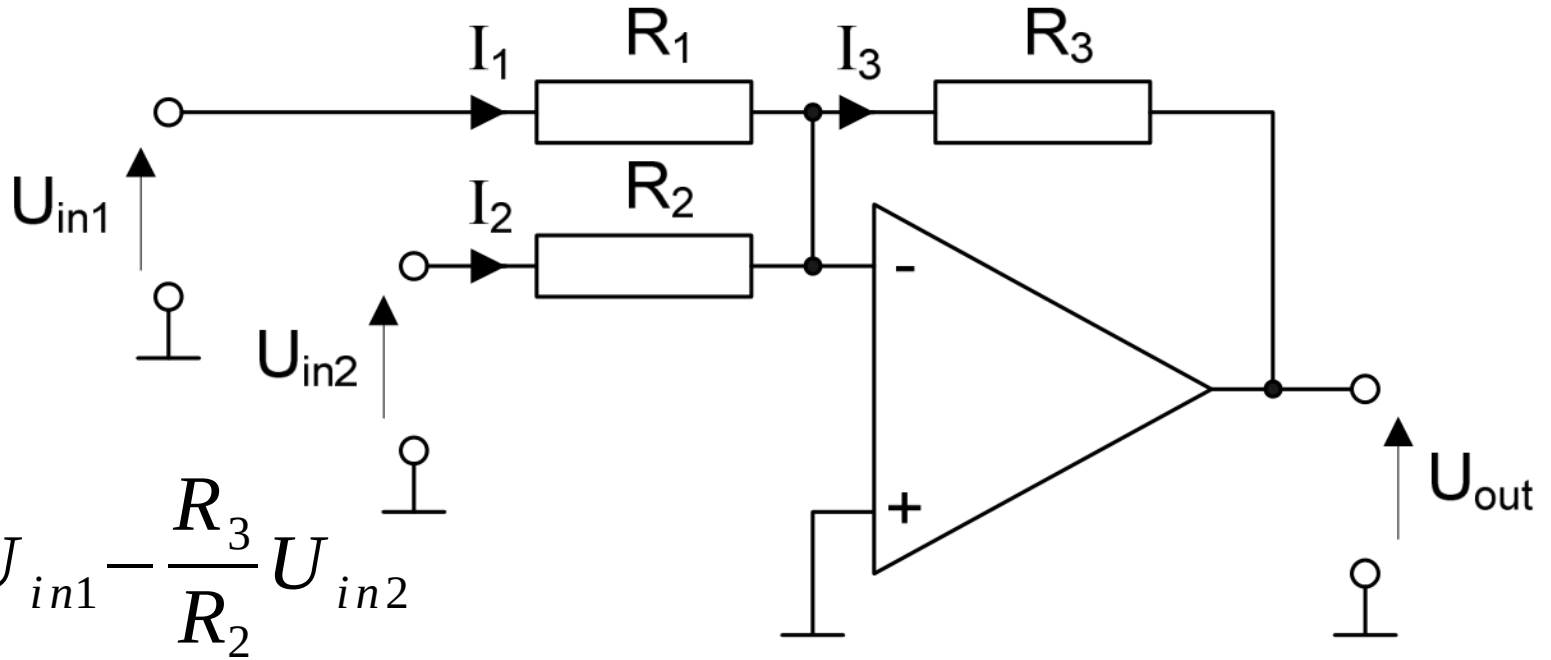
$$U_{out} = -\frac{R_2}{R_1} U_{in}$$



Summing amplifier

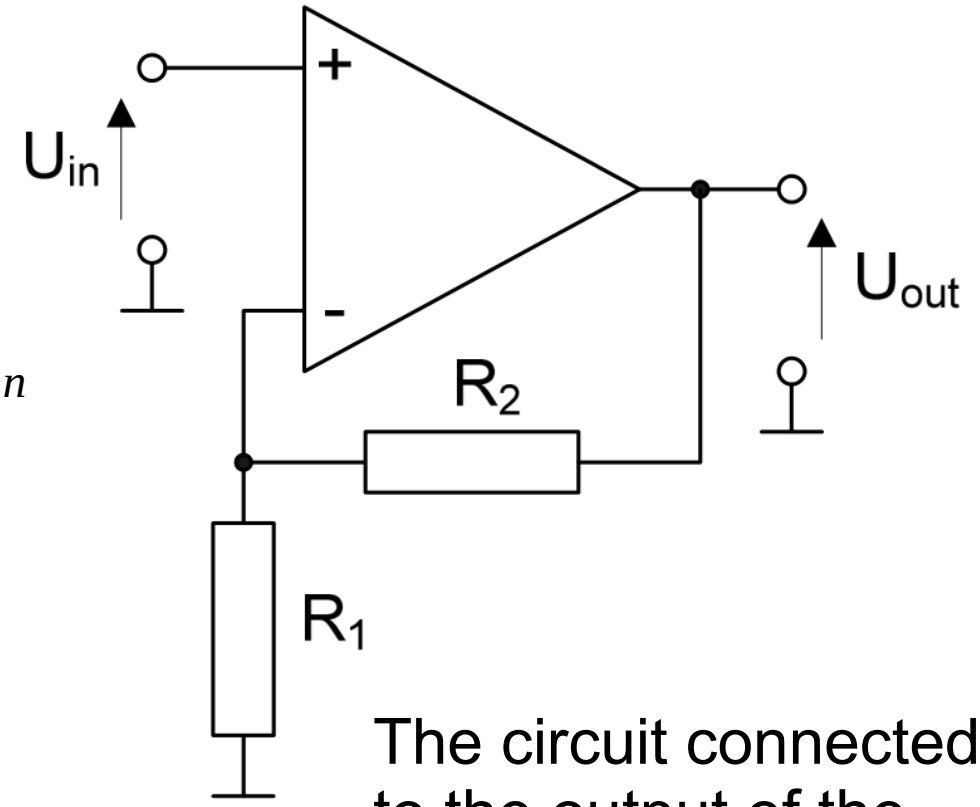
$$I_1 + I_2 = I_3 \Rightarrow$$

$$U_{out} = -\frac{R_3}{R_1} U_{in1} - \frac{R_3}{R_2} U_{in2}$$



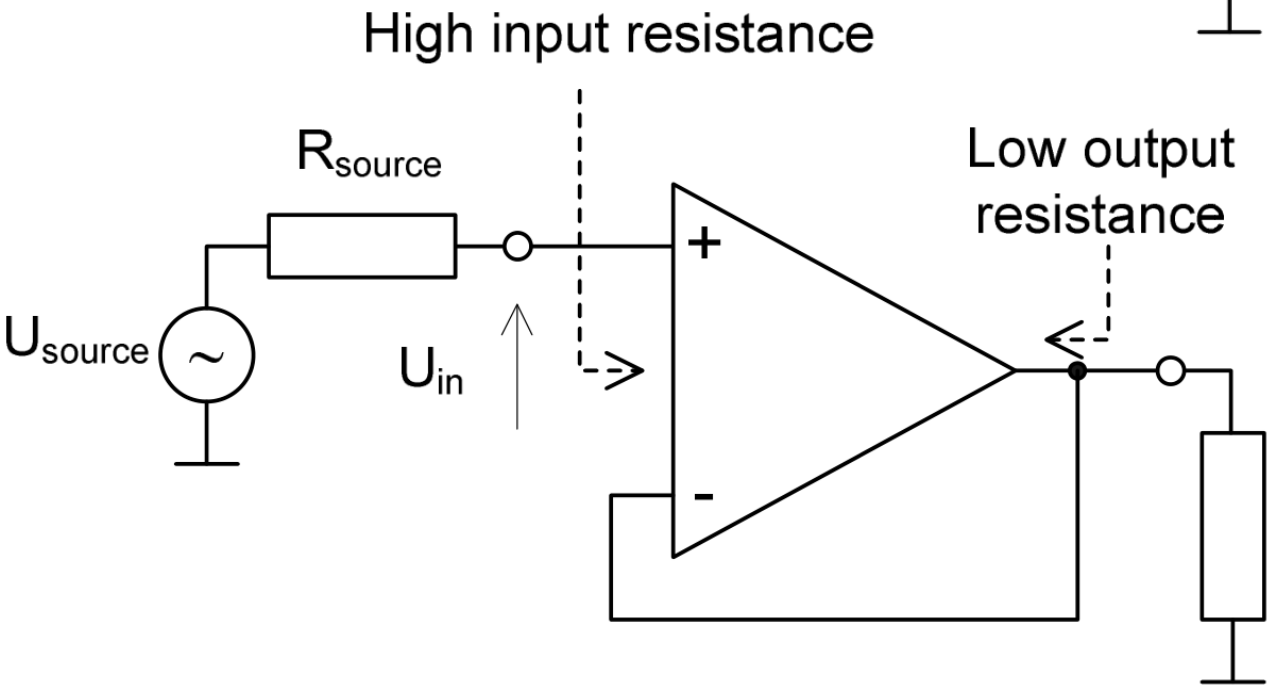
Non-inverting amplifier

$$U_{out} = \frac{R_2 + R_1}{R_1} U_{in} = \left(1 + \frac{R_2}{R_1}\right) U_{in}$$



Buffer

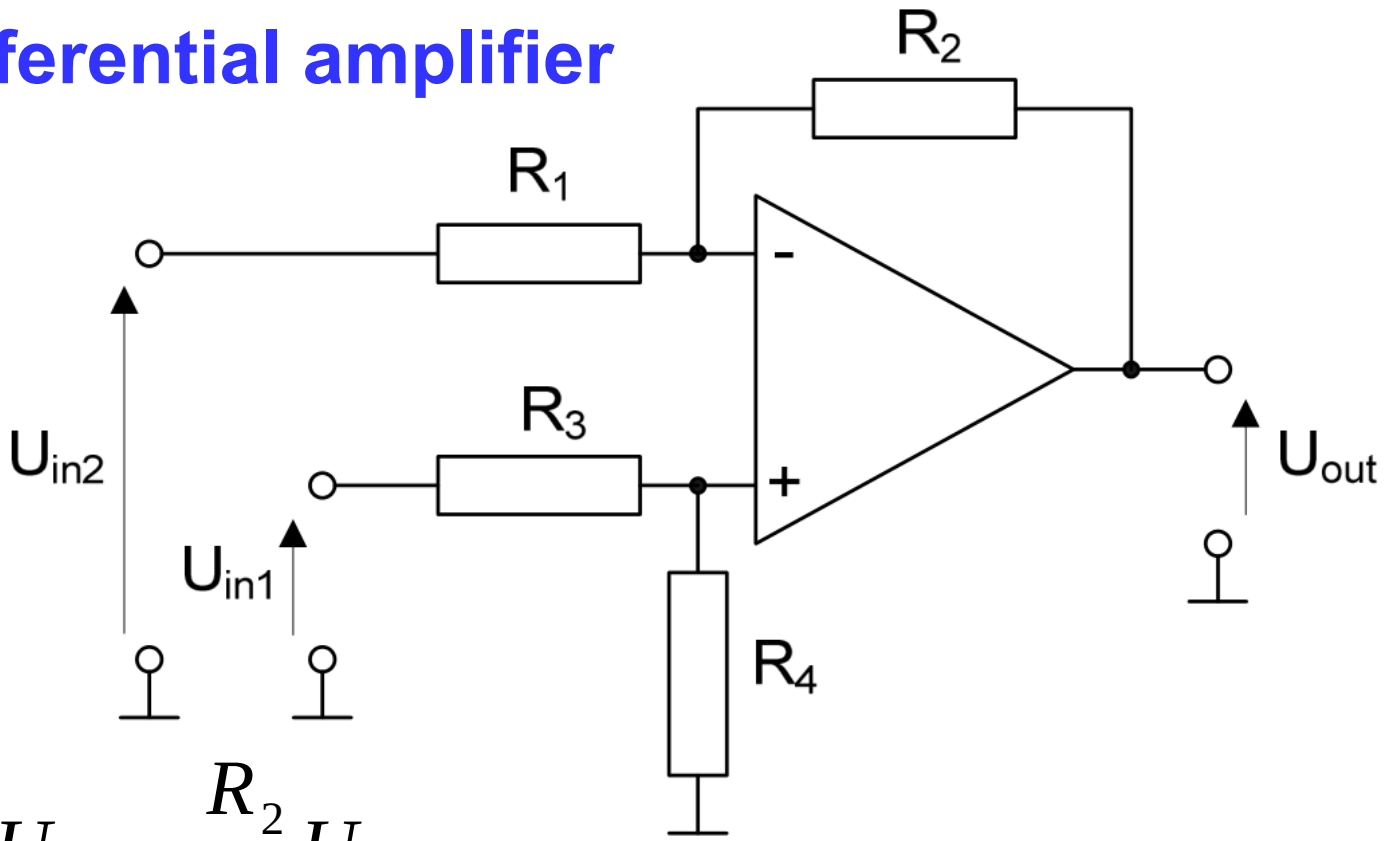
$$R_2 = 0, \quad R1 \rightarrow \infty, \quad U_{out} = U_{in}$$



The circuit connected to the output of the buffer will not draw any current from the circuit connected to the input of the buffer.

Also, there will be no voltage division at neither the input nor the output.

Subtracting, differential amplifier

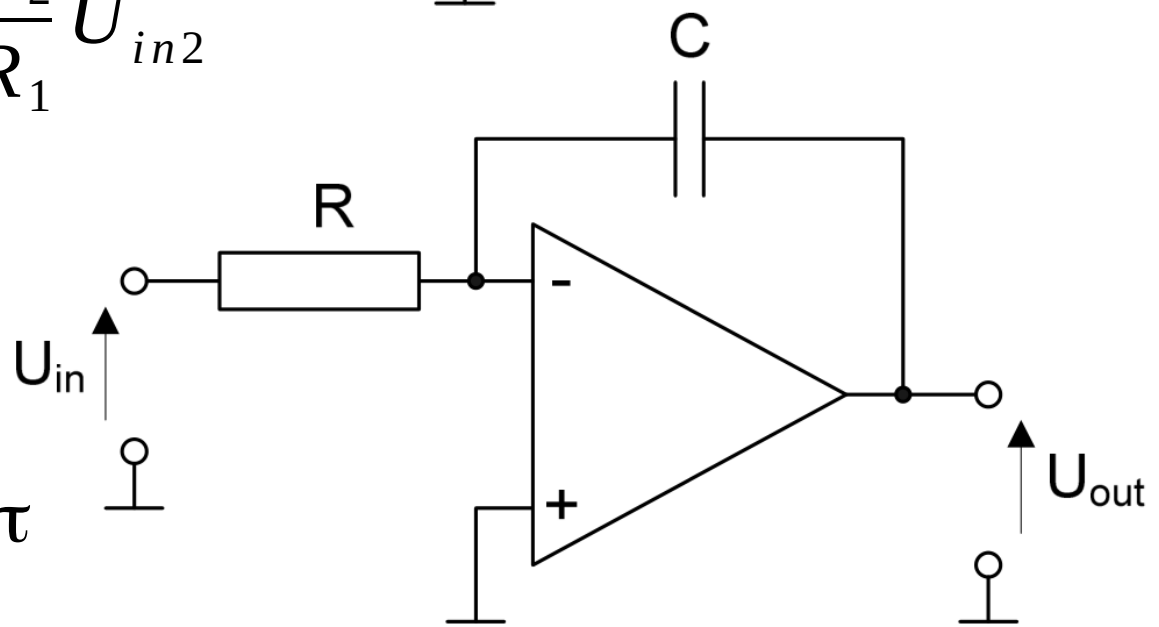


$$U_{out} = \frac{R_4}{R_1}\frac{R_1+R_2}{R_3+R_4}U_{in1} - \frac{R_2}{R_1}U_{in2}$$

Integrating amplifier

$$I = C\frac{dU_C}{dt} \Rightarrow$$

$$U_{out} = -\frac{1}{RC}\int_0^t U_{in}(\tau)\,d\tau$$



D/A-converters

Resistance ladder converter

Current summing D/A-converter

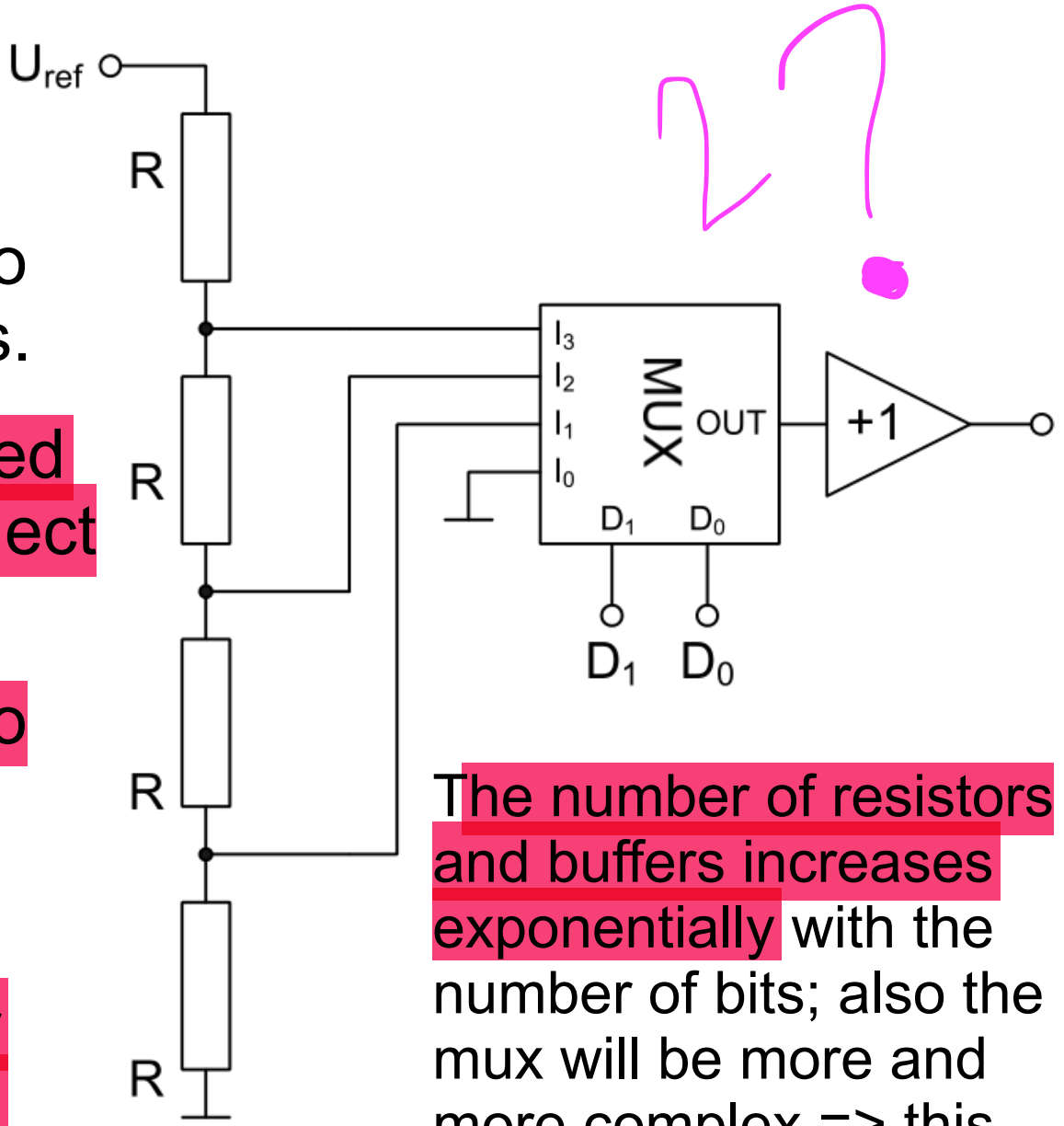
R-2R ladder D/A-converter

(2-bit) Resistance ladder converter

A set of resistors in a voltage divider configuration are used to create the voltage levels.

A set of digitally controlled switches are used to select the voltage.

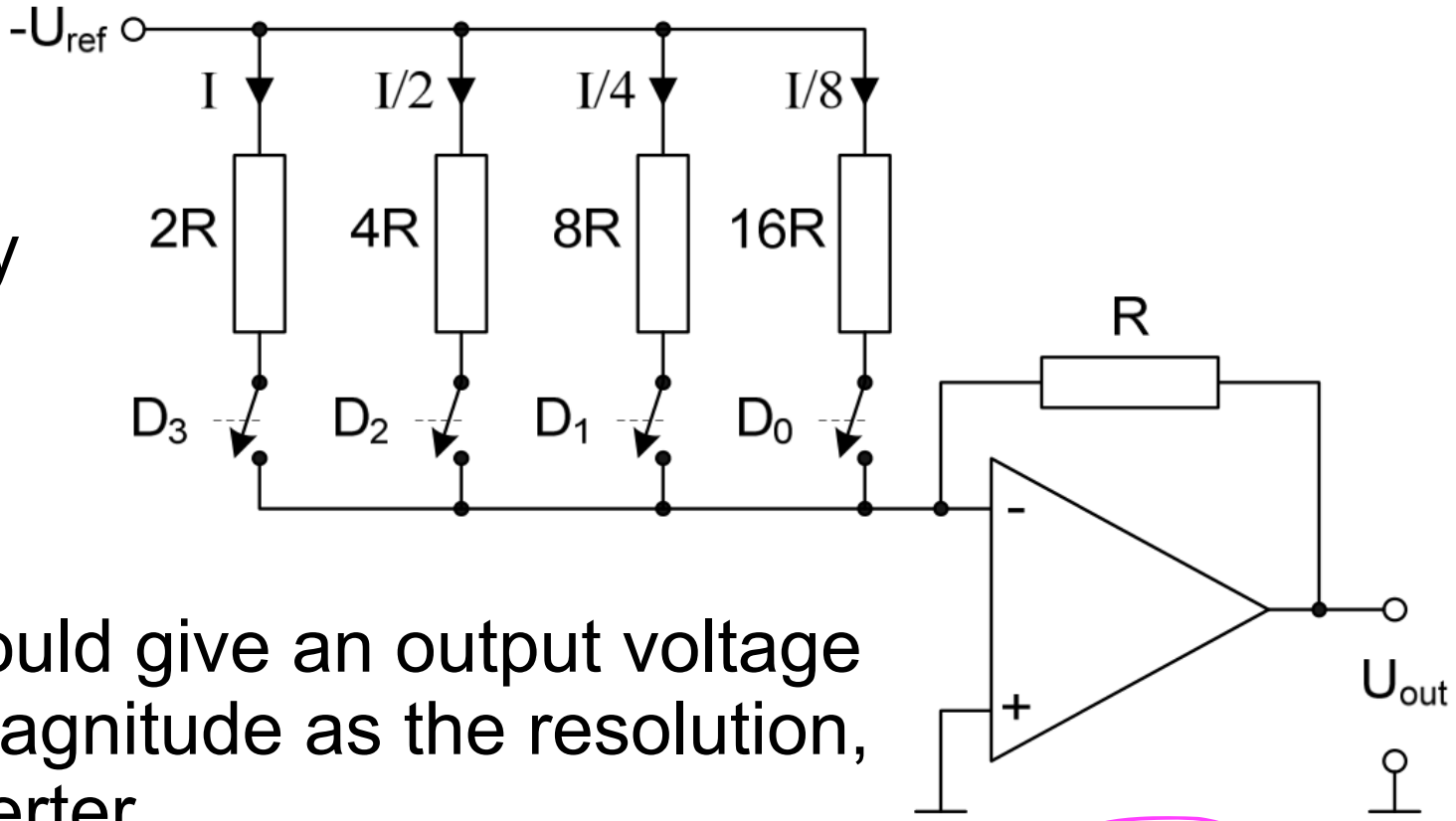
For the voltage divider to function properly the circuit connected to it should not draw any current from the resistor net so we need to insert a buffer at the output.



The number of resistors and buffers increases exponentially with the number of bits; also the mux will be more and more complex => this converter is rarely used

(4-bit) Current summing D/A-converter

D_0, D_1, D_2, D_3 – electronically controlled switches, e.g. transistors



A 1 in LSB should give an output voltage of the same magnitude as the resolution, Δ, of the converter.

4-bit converter => $\Delta = \frac{U_{ref}}{16}$

A 1 in the next bit should give twice that voltage: 2·Δ

The third bit should double this, a voltage of 4·Δ

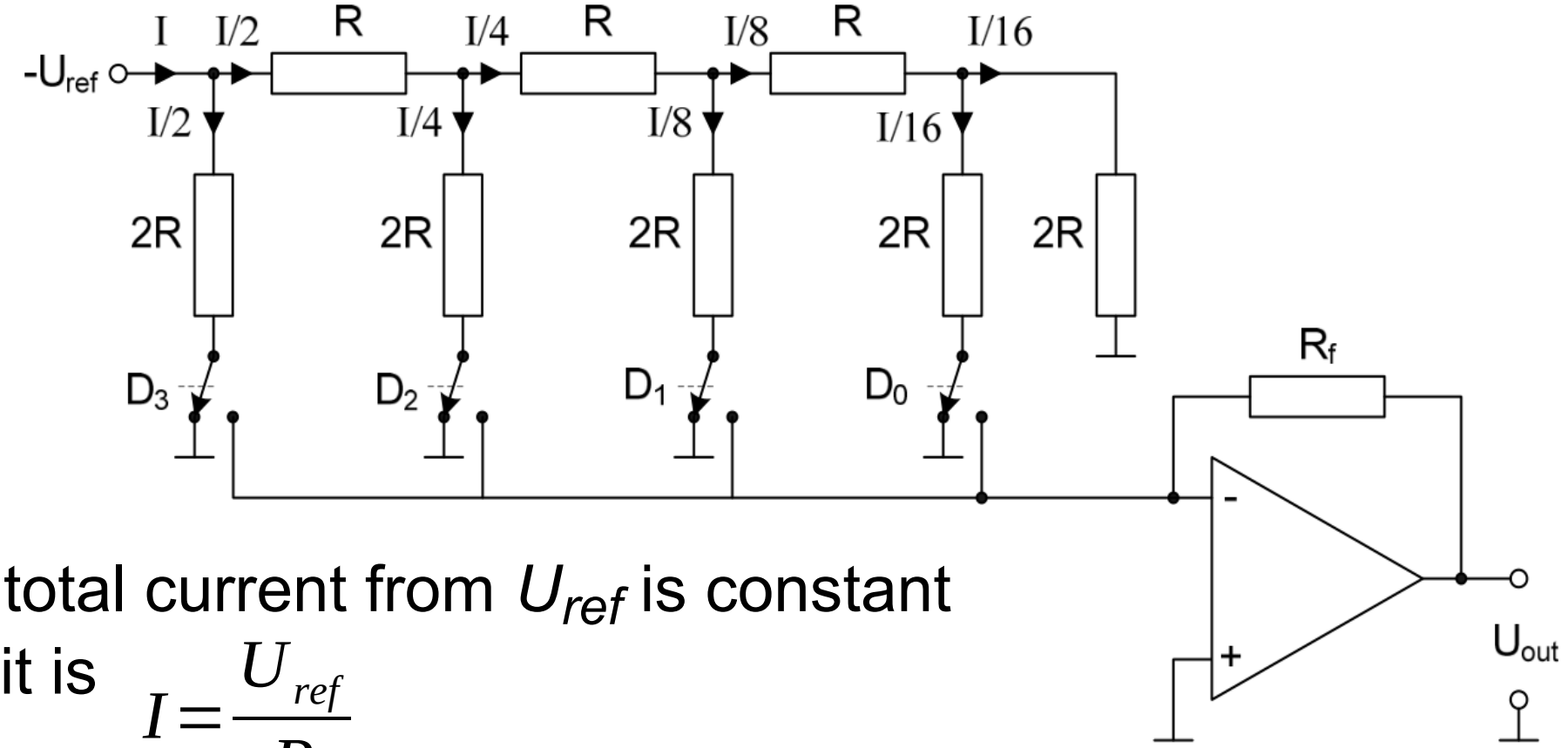
This schematic will not work that well if we increase the number of bits.

If we have 16 bits the largest resistor would have to have a resistance that is 32768 times the smallest resistor value.

It is hard to integrate resistors with so big differences in resistance values.

The way the values of the resistors change with temperature will not be the same for different values and this affects the linearity of the device.

R-2R ladder D/A-converter



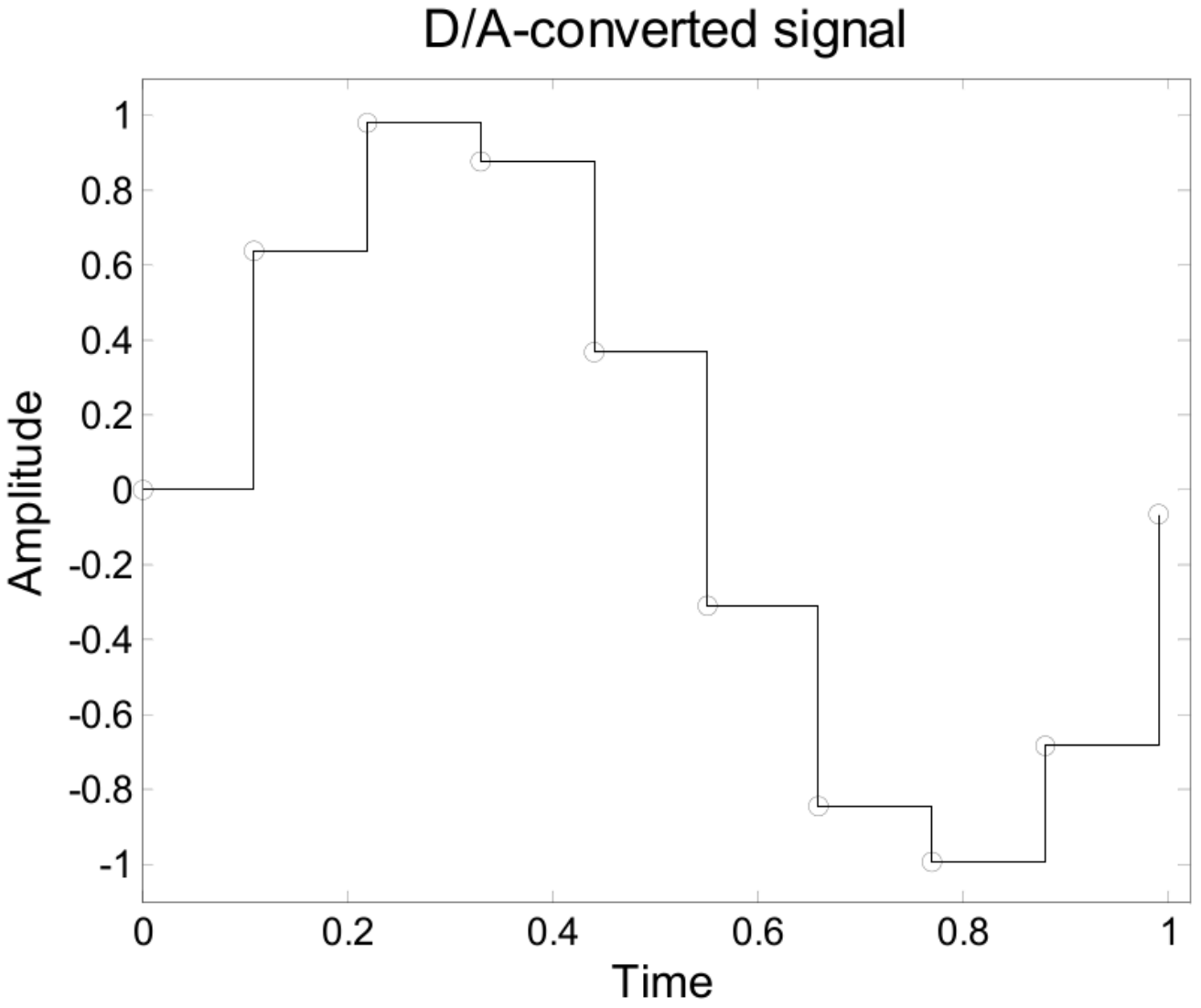
The total current from U_{ref} is constant and it is $I = \frac{U_{ref}}{R}$

A 1 in MSB will give an output voltage of $\frac{U_{ref}}{2}$ which is as expected

Only two different resistance values in the resistor net at the input even if we change the number of bits.

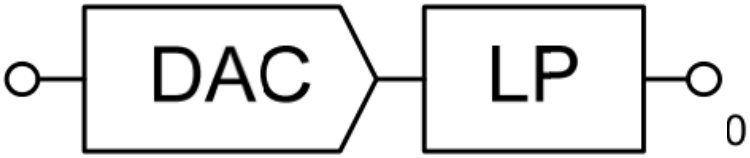
An analog voltage should be able to take on any value within its definition span.

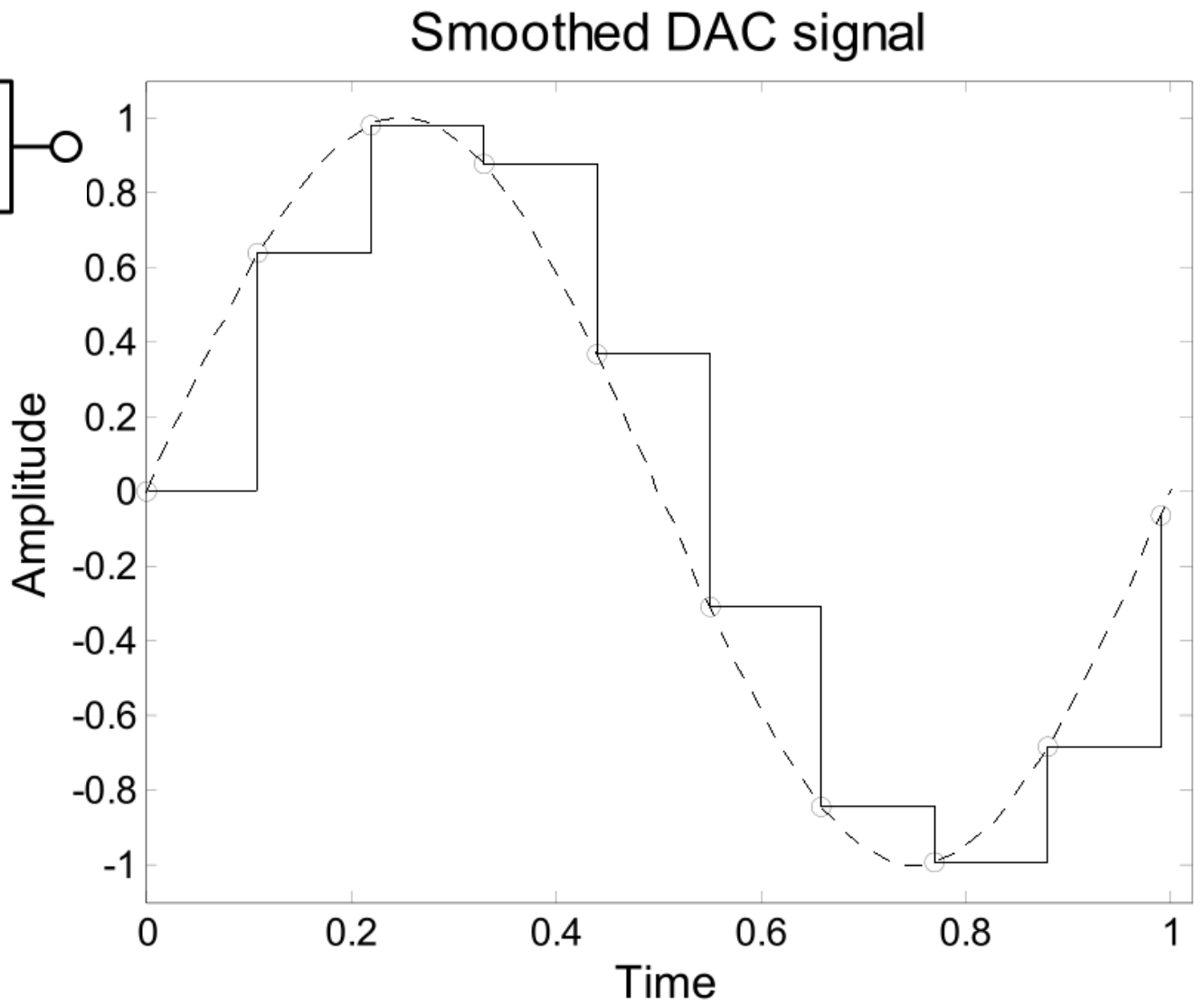
A DAC can only produce on a number of discrete values



To smooth this out we insert a low pass filter after the DAC

A **low pass filter** is a filter that stops the higher frequency contents in the signal from passing but lets the lower frequencies pass.





A/D-converters

Flash A/D converter

Counting A/D converter

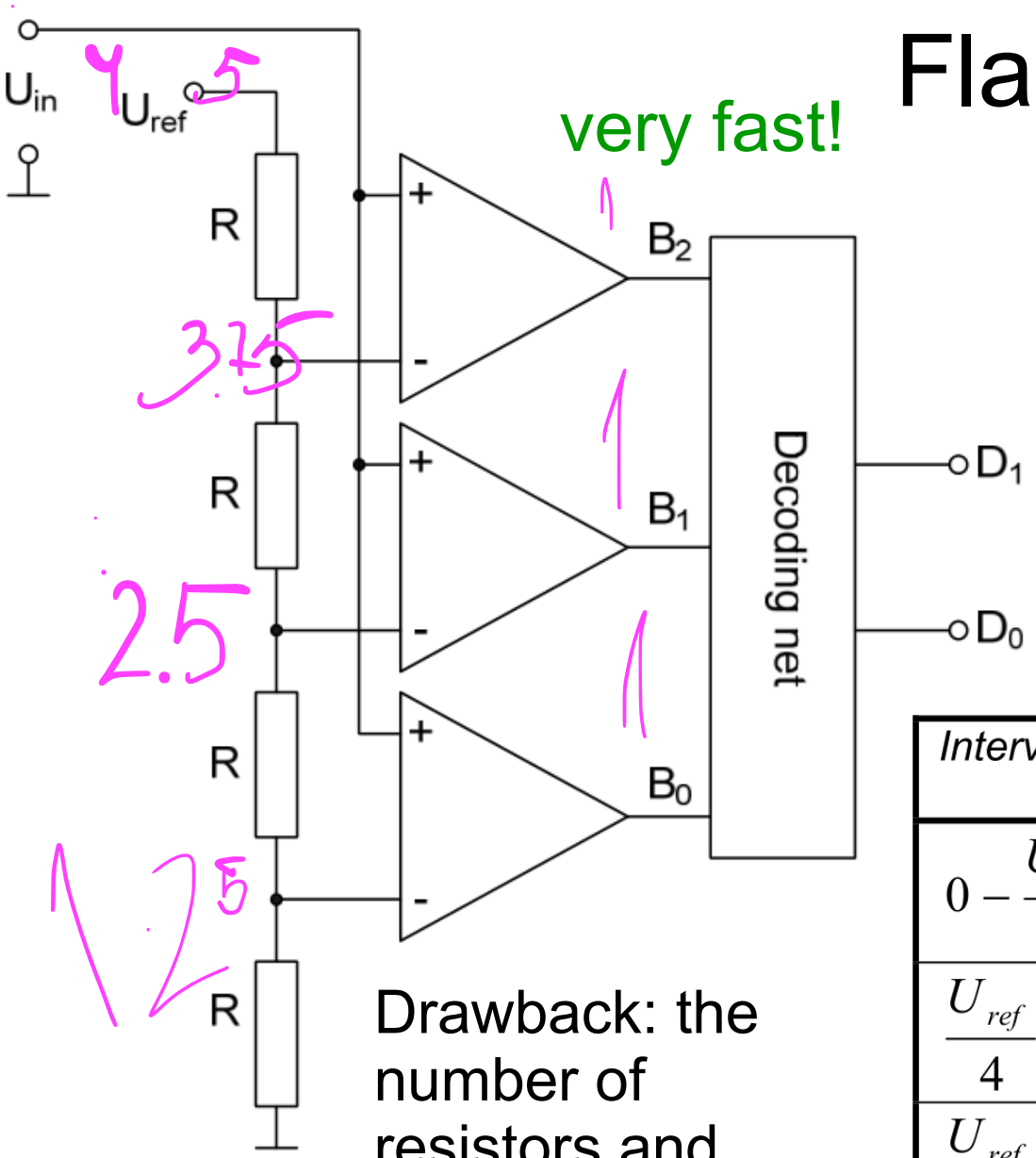
A/D converter using successive approximation

Integrating A/D converters

Single-slope integrating A/D converter

Dual-slope integrating A/D converter

Flash A/D converter



very fast!

The approach is to compare the analog input voltage with voltages corresponding to the discrete levels of the digital signal.

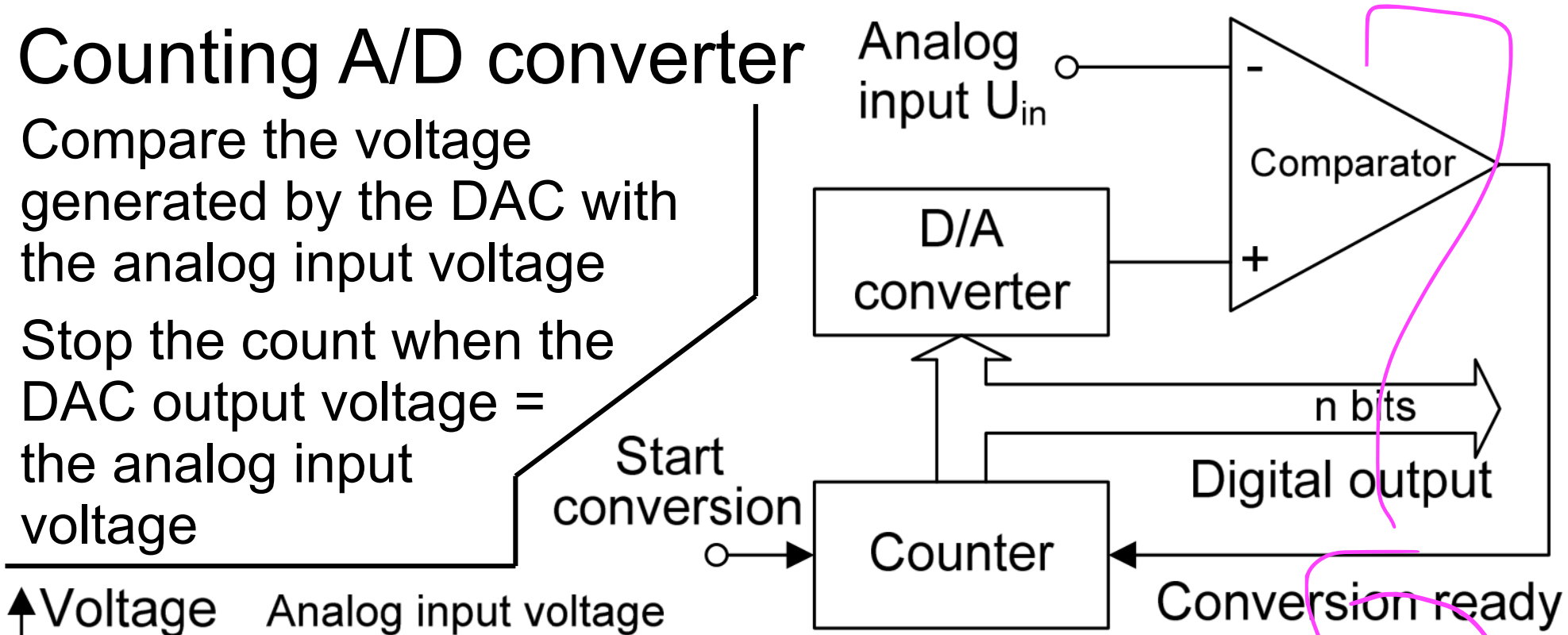
Interval	*Bits from comparators*	*Binary word*
$0 - \frac{U_{ref}}{4}$	*000*	*00*
$\frac{U_{ref}}{4} - \frac{U_{ref}}{2}$	*001*	*01*
$\frac{U_{ref}}{2} - \frac{3 \cdot U_{ref}}{4}$	*011*	*10*
$\frac{3 \cdot U_{ref}}{4} - U_{ref}$	*111*	*11*

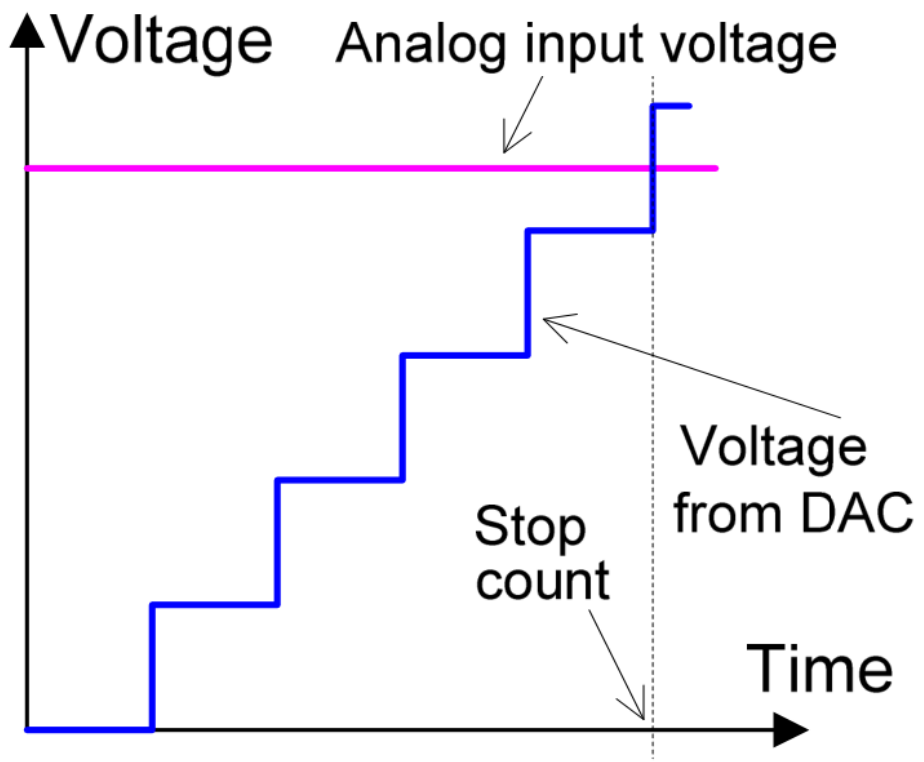
Drawback: the number of resistors and comparators is big if many bits in the digital word.

Counting A/D converter

Compare the voltage generated by the DAC with the analog input voltage

Stop the count when the DAC output voltage = the analog input voltage





The resolution is governed by the number of bits in the DAC.

This converter is called an **up-counting ADC**

The drawback of the **up-counting ADC** is that the time to find the digital output value is highly dependent on the input voltage.

If the input voltage is low then we need few clock pulses.

If the input voltage is high then we need many clock pulses.

This has two negative effects.

1) The conversion time will be long (many clock pulses) for a high input voltage.

2) We have no way of knowing how long time each conversion will take, so we need to design for the longest conversion time.

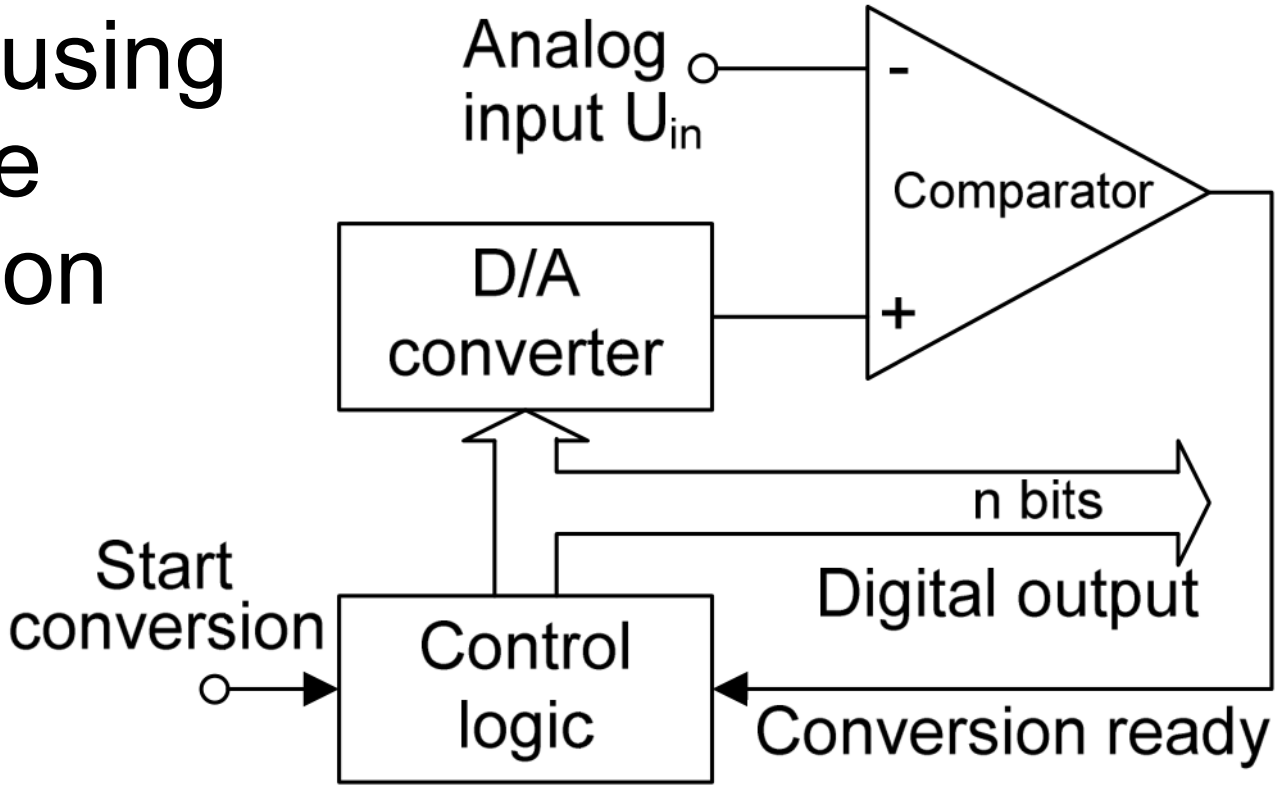
There are refinements of the counting A/D converter where we try to lower the conversion time by not starting our count from zero in every conversion cycle.

Instead, we start from the value that the last conversion gave and change the counter so that it can count both up and down.

In this case we use the assumption that the level of the signal does not change that much from one sample to the next.

We still have an unpredictable conversion time though.

A/D converter using successive approximation



Apply a digital word to the DAC with a 1 in MSB while the rest of the bits are 0

This tests if the analog input voltage lies in the upper or lower half of the DAC's voltage span.

If we are in the upper half we keep 1 in MSB, otherwise we reset MSB to 0.

Then continue the same test with the next bits till the LSB.

Such conversion will always consist of n comparisons, where n is the number of bits in the digital word.

The conversion time is constant and not dependent on the level of the analog input voltage.

Each conversion will only take n clock pulses.

Integrating A/D converters

In an integrating ADC we count the time it takes for a capacitor to charge to the same potential as the analog input voltage.

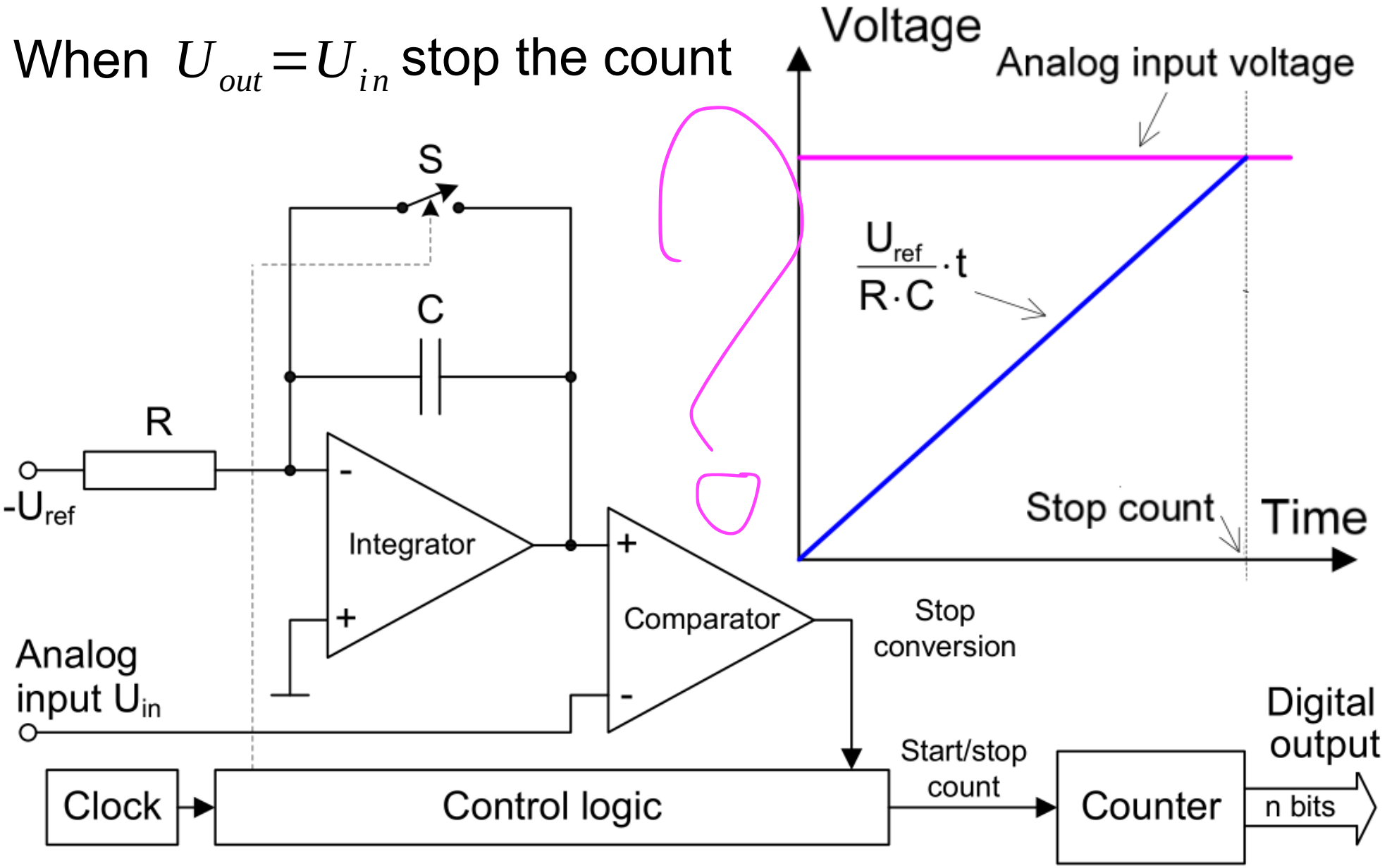
The higher the value, the longer the time.

We use the integrating OpAmp circuit for that.

Single-slope integrating A/D converter

$$U_{out} = \frac{U_{ref}}{RC} t$$

When $U_{out} = U_{in}$ stop the count

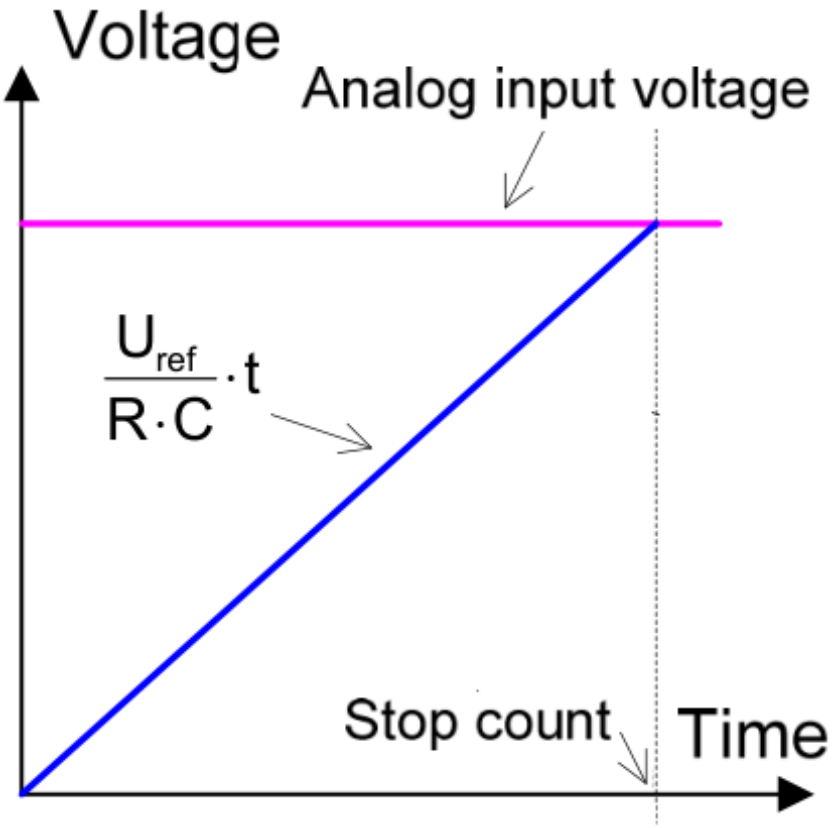


The switch across the capacitor is there to make sure that the capacitor is uncharged when the integration starts, that is it will open when the measurement period starts.

The higher the input voltage the longer it will take to reach the end level so the count is directly proportional to the value of the input voltage.

If we want accuracy in the measurement we need the count to be long so the converter will be slow.

We assume that the input voltage is constant under the integration time which means that we can only deal with slowly varying signals.



Advantage:

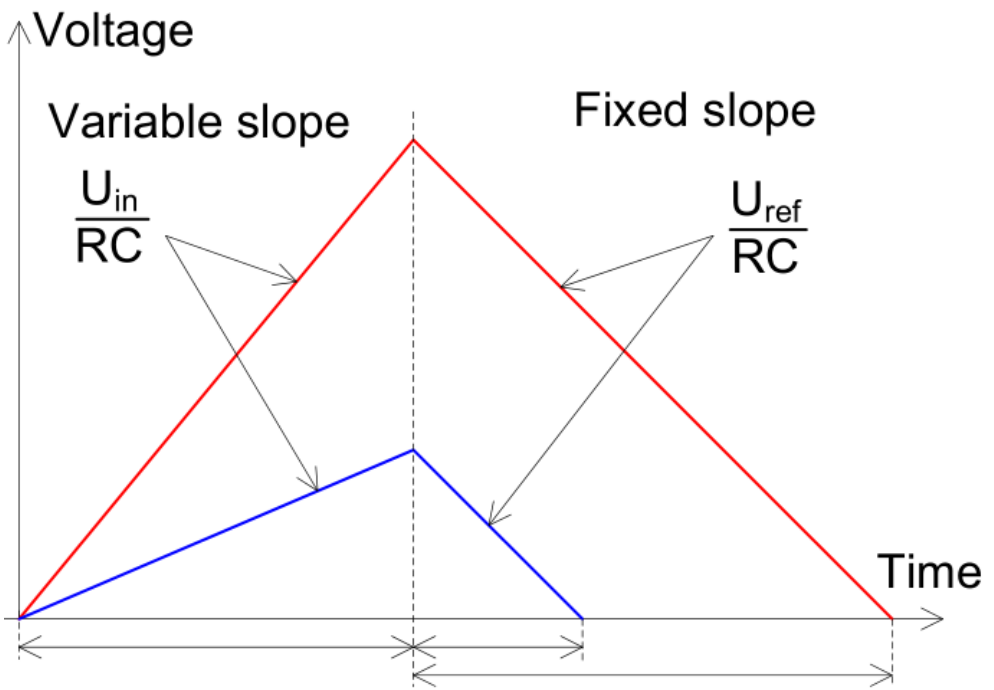
If we have noise in the input signal, that is small random fluctuations in the analog voltage over time, these variations could cancel out during the integration period.

Single-slope integrating A/D converter is sensitive to variations in the resistor and capacitor value and to fluctuations in the frequency of the clock used to control the counter so the circuit is seldom used.

Dual-slope integrating A/D converter

$$U_{Phase1} = \frac{U_{in}}{RC} t_{ref}$$

$$U_{Phase2} = U_{Phase1} - \frac{U_{ref}}{RC} t$$



In this circuit we start by letting the integrator integrate the input voltage U_{in} over a fixed time t_{ref}

The output voltage after this period is $U_{Phase1} = \frac{U_{in}}{RC} t_{ref}$

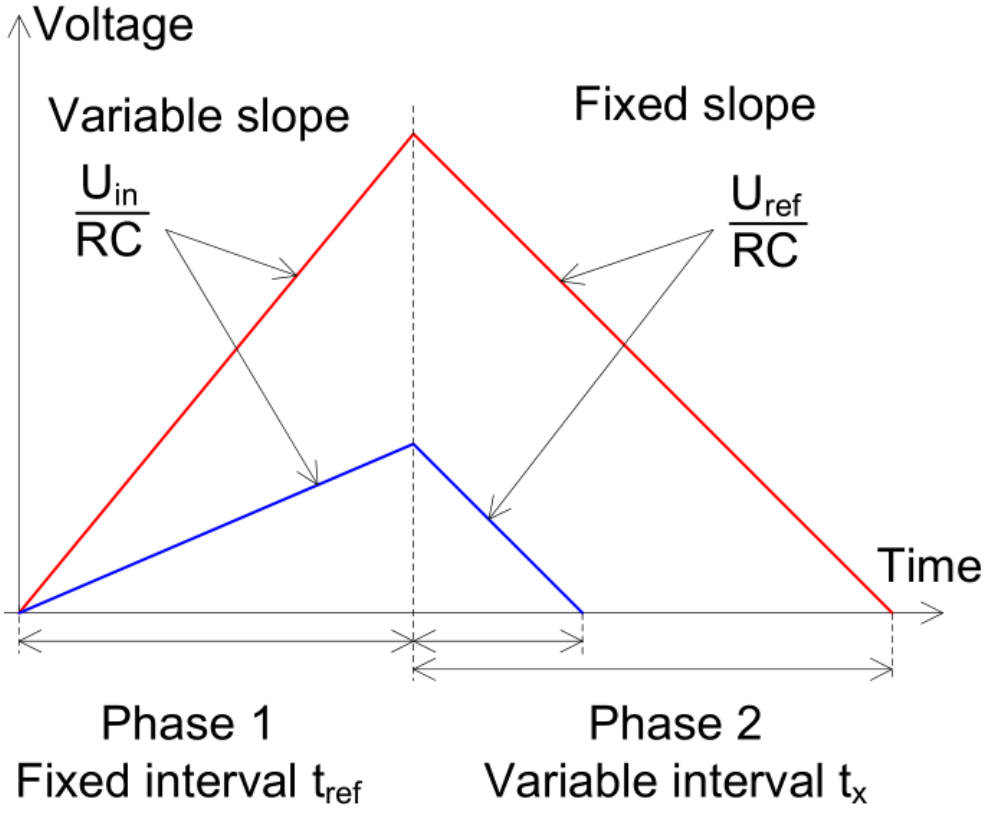
Then we replace the input voltage with a reference voltage

This voltage has an opposite sign to the input voltage.

The output voltage will now ramp down

$$U_{Phase2} = U_{Phase1} - \frac{U_{ref}}{RC} t$$

During this second time we let a counter count the time and we stop the count when the output voltage reaches 0 at the time t_x



The higher the input voltage U_{in}, the higher the output voltage after the 1st integration U_{Phase1} and the longer the 2nd integration time t_x and therefore the higher the count.

$$\frac{U_{in}}{U_{ref}} = \frac{t_x}{t_{ref}}$$

The resistor and capacitor values are no longer parts of the equation so the tolerances in their values will not affect the result.

This converter is more immune to fluctuations in the component values and the clock frequency than the single slope converter since we use the same components and the same clock in both integrations.

Since we have two integrations here dual-slope A/D converter is even slower than the single-slope converter.

This converter can cancel noise in the input signal the same way that the single-slope converter can.

The dual-slope A/D converter is common in multimeters where the measurement time can be long.

Voltage span

The **voltage span for the A/D-converter** is the analog input voltage that the converter can accept and convert to digital values.

The **voltage span for the D/A-converter** is the possible range of analog output voltages.

The span is unipolar or bipolar meaning that it either spans from 0 Volts to some maximal voltage U_{max} or have a symmetrical span $\pm U_{max}$

Accuracy

Every conversion generates some error due to the design of the converter.

The **accuracy** of the A/D- or D/A-converter is given in datasheets as a maximal error in number of resolution steps.

Typical values might be

$$\pm\frac{1}{4}LSB,\ \pm\frac{1}{2}LSB,\ \pm 1\,LSB$$

Conversion time

This only applies to A/D-converters

Conversion time is the necessary time to convert the analog input value to the digital output value.

In some cases the datasheet will give more than one conversion time with different levels of accuracy.

A shorter conversion time will give a lower accuracy.

The conversion time, t_c , limits the maximal sampling frequency

$$f_{s,max} = \frac{1}{t_c}$$

We have to be able to carry out the conversion before a new sample arrives.

Settling time

This is the equivalent to conversion time when we talk about D/A-converters.

Settling time is the time that it takes before the analog output signal generated by the digital word has settled to a stable value.

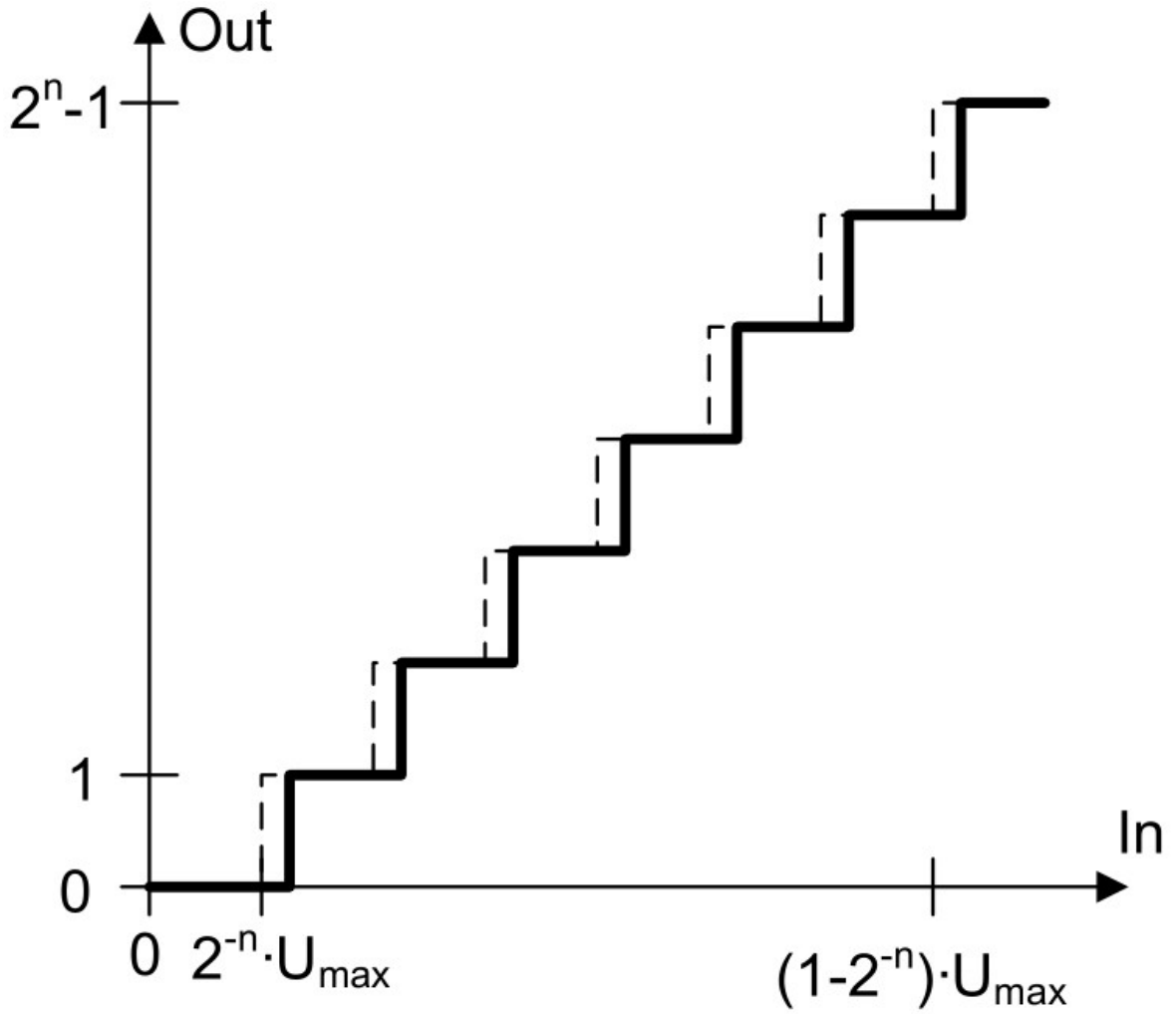
The output voltage stability is given as being within some error range, for example

$$\pm\frac{1}{2}\,LSB$$

Offset error

An **offset error** is a shifting of the signal upward or downward.

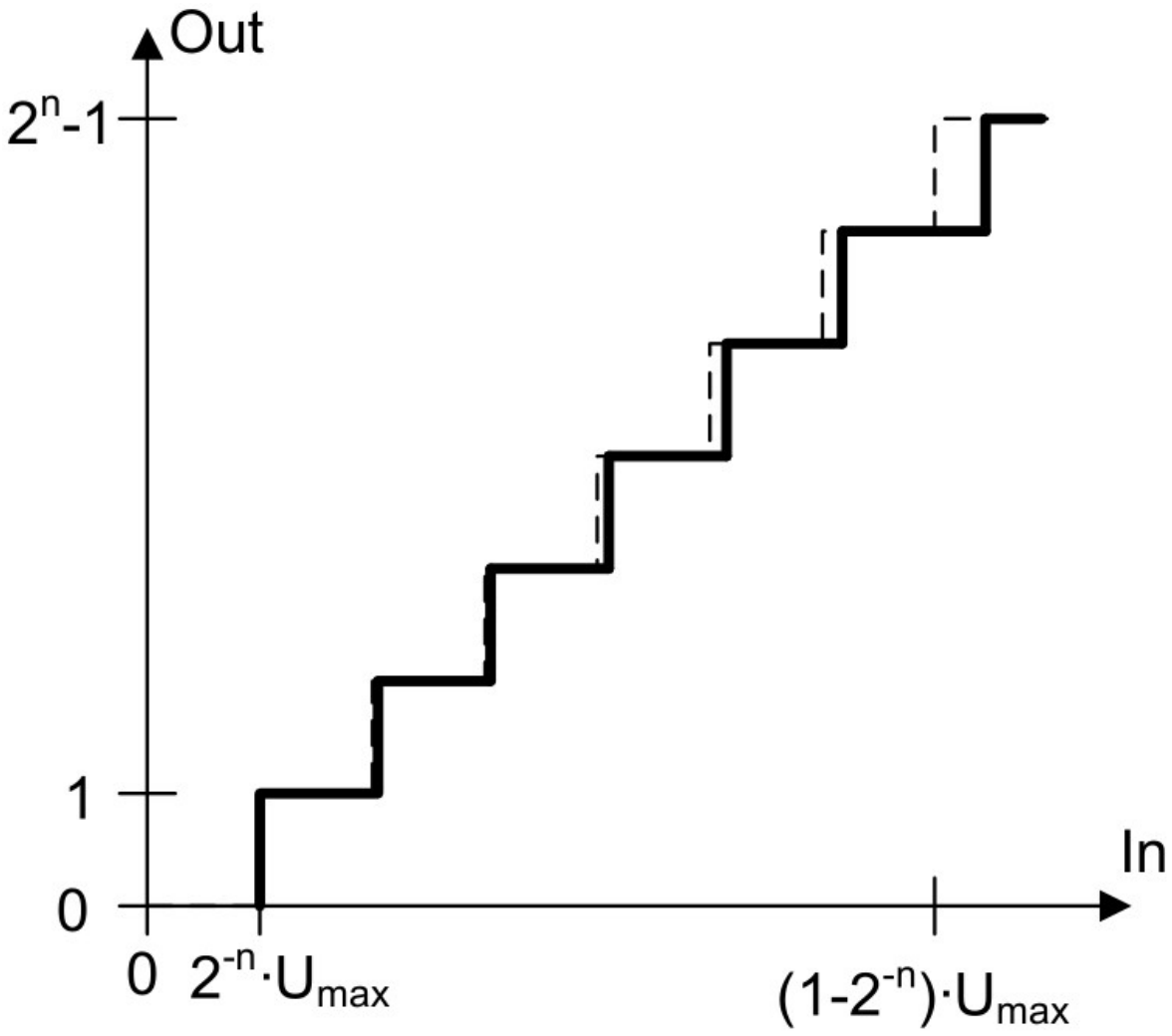
This means that the A/D or D/A conversion will always generate an error of the same magnitude no matter the signal level.



Amplification error

The **amplification error** is an error in the slope of the transfer curve.

In contrast to the offset error the amplification error will increase in size with the magnitude of the signal.



Another name for this error is **scale factor error**.

Linearity error

The **linearity error** is an error in the linearity of the transfer function

This means that the error at different levels in the transfer function differ but it will not necessarily increase with the magnitude of the signal.