MIDDLE EAST TECHNICAL UNIVERSITY

ELECTRICAL & ELECTRONICS ENGINEERING

EE464 - STATIC POWER CONVERSION II
HARDWARE PROJECT - FORWARD CONVERTER #1
POWERLOVERS
FINAL REPORT

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Contents

1 Introduction

Static Power Conversion II, a self-defined course, offers numerous isolated and non-isolated converters, inverters and their applications. In Spring'20, the theoretical background that have been acquired is to be turned into a hardware implementation of the combined knowledge all together. However, due to the pandemic, it is not possible to introduce a product but present a detailed design with software supports and PCB design. In this report, forward converter design of group Powerlovers will be introduced. Background information with objectives will take place. Then, all the steps of the projects, tests, design procedures and simulation results will be exhibited. We strongly believe, this project helped us understand the concepts we learnt in the lectures, and we had a chance to see beyond the horizons.

2 Problem Definition, Objectives and Bonus Points

In the project, we are to do a forward converter design with specific properties.

Table 1: Parameters of the project

Minimum Input Voltage (V)	**24**
Maximum Input Voltage (V)	**48**
Output Voltage (V)	**15**
Output Power (W)	**48**
Output Volt. Peak-to-Peak Ripple (%)	**2**
Line Regulation (%)	**2**
Load Regulation (%)	**2**

Some of the points and objectives can be itemized as:

- Closed loop is a must and we are not allowed to use digital controllers
- PCB design of the converter will be presented.
- Bill of material will be presented
- Closed loop compansator design with bode-plot is a **bonus**
- We are to do thermal design and efficiency analysis of the project

We have mentioned couple of specifications of the project. Our goal was to accomplish the main specifications and add as much as bonus we can.

In the next section we are introduce a forward converter.

3 Forward Converter

3.1 General Structure

Forward converter is basically derived from the buck converter. We are going to observe the relationship in the derivation phase. Forward converter is isolated as we know, and it uses transformer as its regular use. Transformer transfers the power to the secondary side and it does not store energy in between. In forward converter, it is important to take the magnetizing current into account.

In Figure 3.1.1, the forward converter topology can be observed. This is the most simple model.

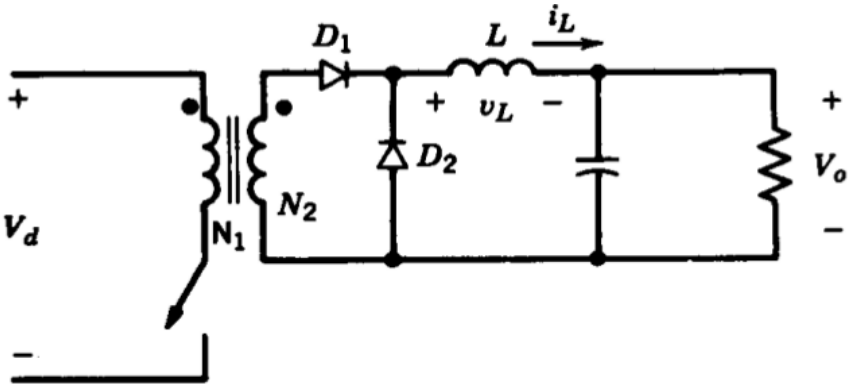


Figure 3.1.1: Forward Converter Topology

Assume the transformer is ideal for now to obtain the transfer function of the topology.
During the ON state of the switch, D_1 is conducting and D_2 is reverse biased. Therefore, the inductor voltage can be written down as

$$V_L = \frac{N_2}{N_1} V_d - V_o$$

Let us examine now the OFF state of the switch. D_1 is now reverse biased on D_2 forms a freewheeling path for the inductor. Load is fed by the stored energy in the inductor and the capacitor. Inductor voltage is easy to obtain and is as follows.

$$V_L = -V_o$$

Discussion so far end with applying the voltage-seconds rule for the inductor and this yields the transfer function of the forward converter topology as

$$\frac{V_o}{V_d} = \frac{N_2}{N_1} D \tag{1}$$

However, a question might arise rightfully at this point: how does this topology deal with the magnetizing current? During the OFF state, L_m has no path to discharge and it seems to be charged again and again during ON state. This situation ends up saturating the core and threatens the proper operation of the converter.
A variety of solutions for this problem are available. A snubber circuitry connected in parallel to the primary winding, a two switch topology are among them. A more practical and wide-spread application ,however, is adding a third reset winding. The resultant topology can be seen in Figure 3.1.2.

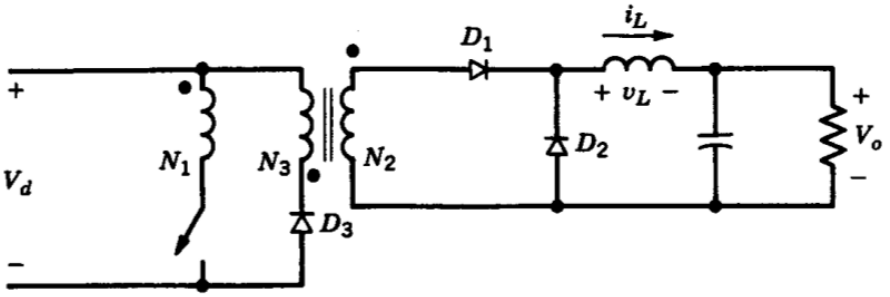


Figure 3.1.2: Practical Forward Converter Topology

In this topology, the third winding namely N_3 is in use in order to reset the winding so that the core does not saturate. As its nature opposes, the forward converter has limitations itself. One and the most important thing is that D_max namely maximum duty cycle is limited to the following equation

$$D_{max} = \frac{1}{1 + N_3/N_1} \tag{2}$$

In most of the cases, $N_1 = N_3$ is taken to simplify the structure and the organization. We followed the same approach in our solutions.

4 Design of the Forward Converter

4.1 System Level Design

The most important element in isolated power supplies is the transformer. Without knowing the transformer properties, it is not possible to move on with the simulations. Hence, the design process is now orderly. Output inductor and capacitor can also be chosen by theoretical knowledge.

Although it is possible to have a "pre-simulation" idea on the voltage stresses or current carrying capabilities for the semiconductor devices in the topology, it is safer to choose them in the guidance of the simulation results. Some of the non-idealities will also be involved in the simulations as well, allowing us to make more accurate assumptions about component selection.

In this part, we need to look at general specifications of the forward converter. Our customer, from Habelsan, asked us to satisfy these specifications:

- Input voltage rate: $24V - 48V$
- Output voltage: $15V$
- Output power: $48W$
- Output voltage ripple: 2%, maximum
- Line and Load regulations: 2%, maximum

Firstly, we need to look at input-output voltage relationship of the forward converter. Ratio between the two is derived in the previous parts as:

$$\frac{V_o}{V_d} = \frac{N_2}{N_1} D \tag{3}$$

Output current's average value is $\frac{48W}{15V} = 3.2A$. As mentioned before, demagnetization of the core in the forward converter is important. Among different techniques,it is decided to use a reset winding. Turn number of the reset winding is chosen to be equal to that of the primary winding, conventionally and we will stick to that convention as well. This situation puts a restriction on the duty cycle to ensure proper demagnetization of the core.Duty cycle for the operation should be $D < 0.5$.

Turns Ratio & Duty Cycle

In the project, required voltage transfer ratios are 48V to 15V, and 24V to 15V. It is important to take into account that the limit of duty cycle is $D_{max} = 0.5$, and it is very crucial to reset all the core.

Using the input output equation and duty cycle restrictions, we choose the turn ratio between first and secondary winding as:

$$\frac{N_2}{N_1} = 2$$

Using these ratio, it is now easy to find required duty ratios. For 48V input,

$$D = \frac{48}{15} = 2 \implies D_{min} = 0.156$$

and For 24V input,

$$D = \frac{24}{15} = 2 \implies D_{max} = 0.3125$$

As can be seen, the duty cycle ratios obey the restrictions and they also allow a margin to compensate for the non-idealities.

Frequency

As switching frequency of the MOSFET, it is important to note that higher frequencies increases the switching losses. Also, at high frequencies, skin depth of the cable decreases dramatically. Moreover, it is also needed to be pointed that at higher frequencies hysteresis losses increase in the core. Therefore, we decided to keep our frequency less than 30kHz, $f < 30kHz$

Secondly, as frequency decreases, the amount of ripple at the output increases due to longer switching periods. Furthermore, it is important to keep the frequency at inaudible range so that the converter is not noisy. We decided that frequency should be higher than 20kHz, $f > 20kHz$.

Combining these two

$$20kHz < f < 30kHz$$

In the simulations, we decided as the best frequency would be 25kHz. Therefore, for our forward converter the frequency is $f = 25kHz$

4.2 Transformer Design

In the forward converter topology, it is important to realize the fact that transformer is introduced in order to transfer the power from primary to secondary. For this reason, we do not need any air gap in our transformer design. Moreover, a transformer with high inductance will allow us to operate in low magnetizing current levels due to high impedance of the inductor. When we combine these, we can start our calculations.

The first approach is to calculate $WaAc$, it shows the power handling capacity of our transformer. Its formula is as follows:

$$W_a A_c = \frac{P_o D_{cma}}{K_t B_{max} f} \tag{4}$$

Here $P_o = 48W$, power out in watts, $D_{cma} = 500\ cir/mils.amp$, is current density, $K_t = 0.0005$, topology constant given for forward converter. $B_{max} = 2500G$, maximum flux density in gauss and $f = 25kHz$ is the frequency.

When we calculate the result

$$W_a A_c = 0.768\ cm^4$$

Now, using the magnetics' available cores offered for power handling capacities, we are going to choose a proper core. We chose an R material E shaped core, it is high in inductance and low in loss. It is very proper for this application.

The core link: Core

Now it is important to choose turn number for primary side. The secondary and third windings depend on the primary side. We are going to apply following approach:

$$N_p = \frac{V_p 10^8}{4BA_c f} \tag{5}$$

We choose following parameters for this application: $V_p = 48V$, $B = 0.25T$, $A_c = 0.87cm^2$ it given in the datasheet of the core and $f = 25kHz$. The result is:

$$N_p = 22\ turn$$

Naturally, we have $N_1 = 22, N_2 = 44, N_3 = 22$ due to our selection.

The turns number for windings are determined as

- Primary winding, $n_1 =$ **22 turns**
- Reset winding, $n_3 =$ **22 turns**
- Secondary winding, $n_2 =$ **44 turns**

Now, it is very important to take magnetizing inductance into account. In the datasheet we can easily see that the AL value is given as $AL = 2667nH/T^2$. As we decided our turn number is 22, we can easily calculate the magnetizing inductance as:

$$L_m = 22^2 * 2667 * 10^{-9} = 1.3mH$$

This is a great value becuase a low magnetizing inductance will increase the magnetizing current at the primary side, as a result we would need a higher current capability. However, 1.3mH is a legitimate value. If we calculate the magnetizing current at operating frequency:

$$I_m = \frac{V}{Z} = 0.235A$$

4.3 Cable Selection

In practical cases maximum fill factor achievable is stated at 50%. We need to take these two parameters into account.

Moreover, it is important to notice that, the input current at the maximum operation is $I_{in} = 2A$ and $I_m = 0.235A$, as overall we need minimum of $I_1 = 2.3A$ at the primary side. At the secondary side we are going to have a maximum of $I_o = 3.2A$, we have to take these into account.

Using a simple approach $1mm^2$ of cable can carry $4A$, and considering skin depth. We have chosen to use AWG22 cable. It's area is $0.327mm^2$ and it can carry a current up to $1.3A$. Also, it's maximum skin depth is applicable up to $42kHz$, that is to say since our operating frequency is $25kHz$, this cable is proper to use. Considering margins, we are going to choose needed parallel cable amount.

In the output we need 2 parallel cables, and at the output we need 3 parallel cables.

Now, it is important to have a look at the fill factor. It is very crucial to have a fill factor around 50% so that our transformer is realizable.

If we calculate the cable areas:

$$A_{cable} = 0.326 * 22 + 0.326 * 22 + 0.326 * 44 = 71.9mm^2$$

If we check our core's window area, we can see that it is:

$$A_{window} = 9.8 * 8 * 2 = 156.8mm^2$$

So the fill factor of our transformer is:

$$k = \frac{61.1}{156.8} = 46\%$$

This fill factor is applicable and not an overdesign. Therefore, the cable selections are proper. We have a legitimate fill factor, we have 100% skin depth, and we have margins so that there is no burnout. In the next step we are going to cover the capacitor and inductor.

4.4 Inductor and Capacitor Design

To design the inductor, we are focus on the maximum ripple current allowed. In the specifications, it is not determined, so we are going to have 20% maximum ripple current so that our output current would be out of harmonics and the filtering capacitor would be smaller.

At the ON period, the inductor is charging, and using the voltage among the terminals we can find the ripple current value.

$$\Delta I = \frac{1}{L}\int_0^{DT_s} V_L dt < \frac{3.2A}{5}$$

$$\Delta I = \frac{1}{L}\int_0^{DT_s} (V_s\frac{N_2}{N_1} - V_o)dt < 0.64A$$

$$0.62mH < L$$

Also, it is very important to take rated current into account. The minimum rated current that inductor can carry must be minimum of $3.2A + 0.65A \approx 3.8A$

Using digikey website, we chose a proper inductor. It is important to have a small inductor in order to decrease the size and the weight.

Inductor Link: Inductor

Capacitor design is depending on the inductor design. As we know, we have to limit the ripple value of the output voltage. Also, the current that is flowing through the output is equal to the inductor current. We need to follow the following approach.

$$\Delta V = \frac{\Delta Q}{C} \tag{6}$$

$$\Delta Q = \Delta I_L * \frac{T_s}{8} \tag{7}$$

Here, we are using buck converter capacitor design approach. They are same in the application:

$$\Delta V = 0.3V > \frac{DT_s^2(V_s\frac{N_2}{N_1} - V_o)}{8LC}$$

$$C > 28\mu F$$

Also, apparently the rated voltage of the capacitor should be higher than the rated voltage of the output, for that reason $C_{v,rated} > 15V$

Capacitor Link: Capacitor

ESR value of the capacitor is:

4.5 Switch and Diode Design

In these voltage levels and frequency levels it is proper to use MOSFET due to their fast recovery. It is also easy to implement a MOSFET into a converter. While designing the MOSFET, it is very important not to exceed its rated voltage and current values.

In the simulations with idealities, we came up with the values that:

- Switches' stress have their maximum values for input of 48V naturally. We can say that switches must be endurable minimum of 100V rated reverse voltage and 10A forward voltage.

- Switches must be proper to operate at 25kHz range, reverse recovery times should be appropriate.

The MOSFET Link: MOSFET

Silicon diodes are proper because they are cheap in cost and they have proper operation for this implementation range.

In the simulations with idealities, we came up with the values that:

- Diode' stress have their maximum values for input of 48V naturally. We can say that switches must be endurable minimum of 100V rated reverse voltage and 4A forward voltage.
- Diode must be proper to operate at 25kHz range, reverse recovery times should be appropriate.

Results of simulations will be introduced at next part.

4.6 Feedback Controller Circuitry

To keep the voltage constant at 15V and to satisfy the line/load regulations, an analog controller IC is to be used. A very popular PWM controller IC for power supplies, **TL494** by *Texas Instruments* is chosen. Additional features comes with it makes it a favorable choice and in this section, some of them that we implemented in our design are to be presented.

To power up the module, a DC-DC converter is used.

TL494 is able to drive two switches together, but only one of the outputs is to be used in our project. Soft starting and current limiting features are to be adapted to our application, though. Additional circuitry for them can be found in the application notes regarding TL494.

To ensure electrical isolation between input and output sections of the converter, an optocoupler is to be used to drive the switching element. Our choice for this element is **TLP250** by *Toshiba*. It is a familiar IC for us, since it is used previously on the hardware project of EE463.

5 Ideal Simulations

5.1 Simulation Results

Below in the Figure 5.1.1, the simulation model schematic can be seen.

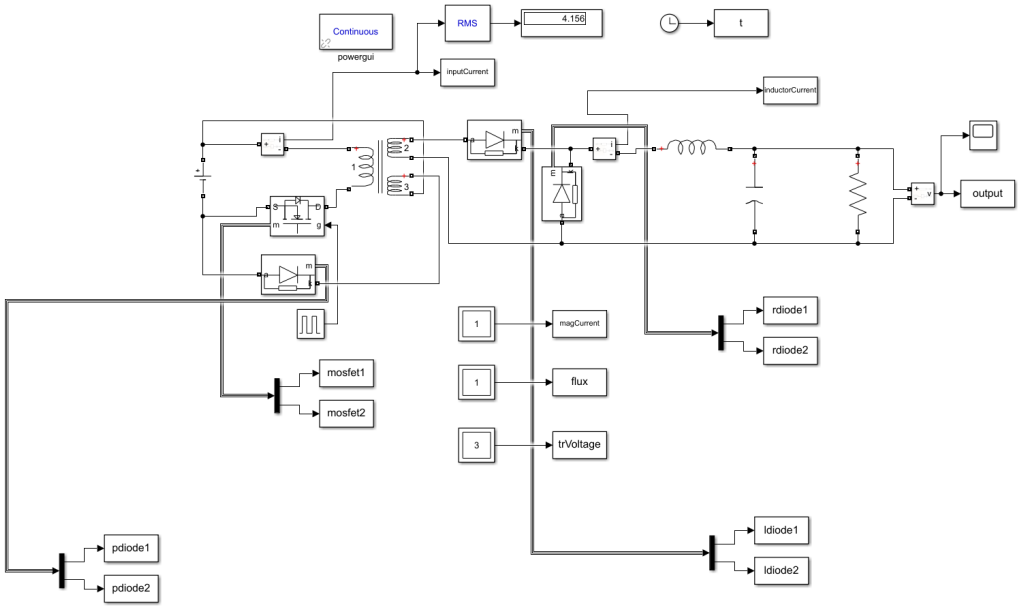


Figure 5.1.1: Simulation model

First, we simulated the ideal models in order to see the overall system operation. It is open-loop operation simulation and we would like to validate the duty cycles, operation principle and validity of our selections.

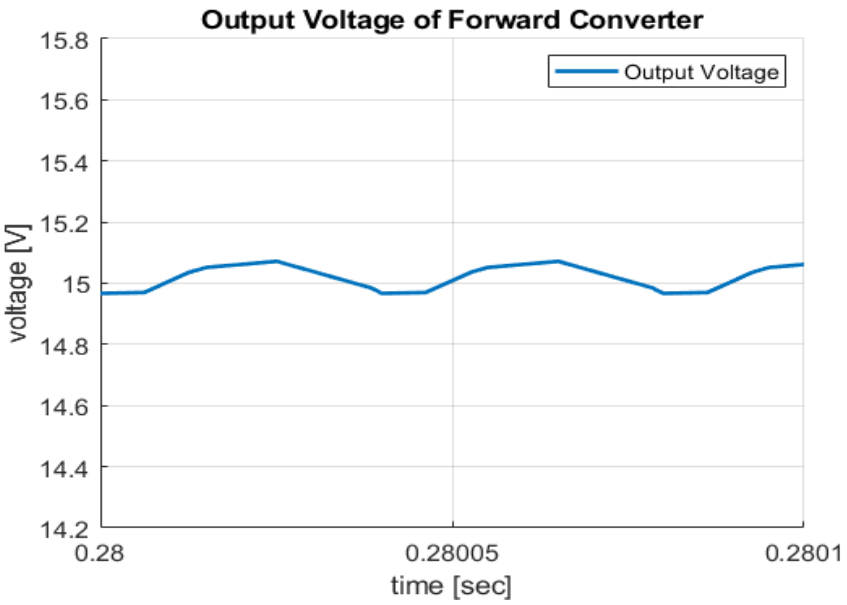
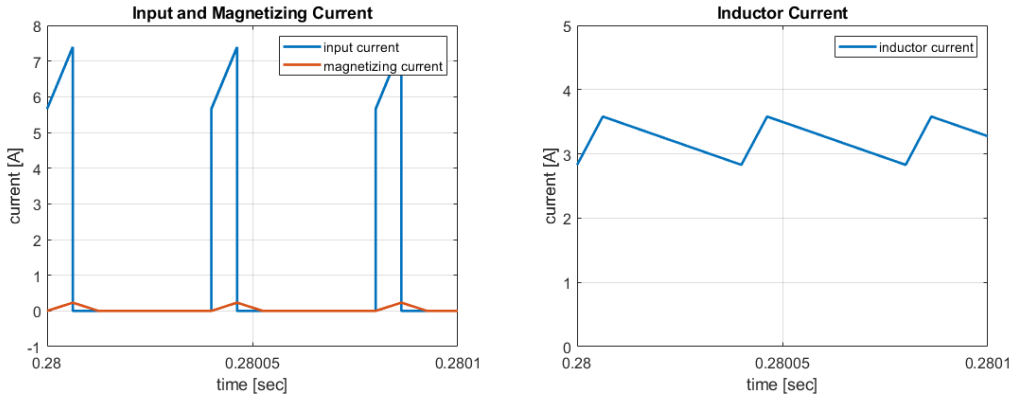


Figure 5.1.2: Output waveform of the forward converter under 48V operation



(a) Input and Magnetizing Current

(b) Inductor Current

Figure 5.1.3: Forward converter input and inductor current under 48V input operation

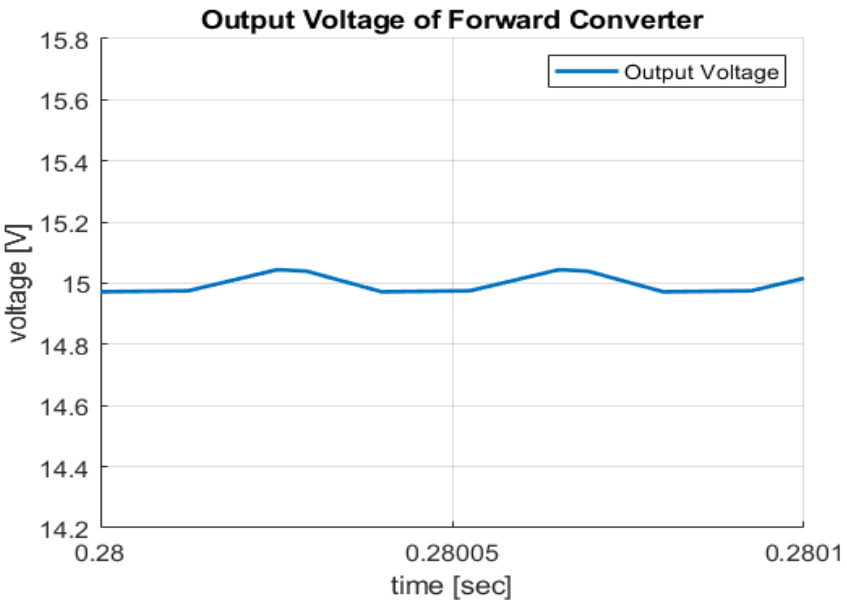
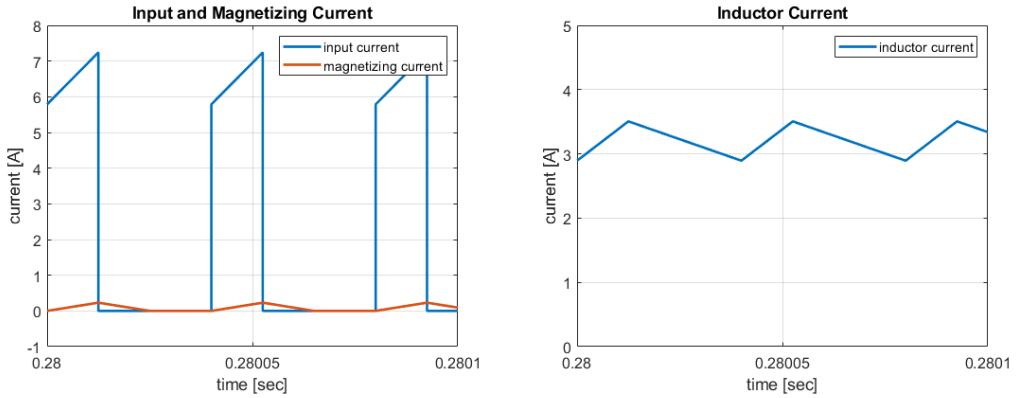


Figure 5.1.4: Output waveform of the forward converter under 24V operation



(a) Input and Magnetizing Current

(b) Inductor Current

Figure 5.1.5: Forward converter input and inductor current under 24V input operation

As we can see from the Fig. 5.1.4 and 5.1.2 the output ripple is below 2%. The operation is stable and the duty cycles are as expected. However, when non-idealities are presented the duty cycle values will be re-calculated in order to compansate the voltage drops of losses and diodes etc.

Also, from the Fig. 6.2.5 and 5.1.3, we can observe the magnetizing current is as expected around $0.3A$ and the inductor ripple is around $0.6A$ for both operations. These results show that our calculations are valid. Now we are going to add non-idealities of the circuit.

6 Non-idealities of Forward Converter

6.1 Adding the Non-idealities and Their Solutions

Firstly, we added the loss components of the MOSFET and the diodes. As we can see from the datasheet, MOSFET has $R_{ds,ON} = 12.4m\Omega$, this value is added to the MOSFET. Then, the forward voltage values of the diodes are added to the software $V_f = 0.7V$ in our operation topology. After adding these, $R_{d,ON} = 1m\Omega$ added for the diodes representing the losses on the selected diodes.

Series resistance of the inductor is given as maximum of $R_{max} = 0.113\Omega$ for convenience we took this value as 0.6Ω to obtain an average operation range. Also, using the datasheet of the capacitor, we found out that the ESR value of the capacitor is around $3m\Omega$. This is a low value, because the capacitor is a seramic capacitor and it has very low ESR operation.

Next step was to add the leakage inductances of the transformer, we have taken the leakage inductance as 1% of the magnetizing inductance and introduced the leakage inductance as $13\mu H$ to the primary side of the transformer.

Then it is very crucial to notice that the stored energy in the leakage inductance needs a way to decharge itself. For this very reason it is very important to design a snubber circuit around the MOSFET in order to block burnouts and have a smooth operation. We have decided to move on with a RC Snubber.

When designing the RC snubber we can use an Application Note, in the application note, there is a snubber designed. We changed the R and C variables in order to adjust the solution into our problem. We have twice of voltage at the input and the current is twice. So, we used four times of R and two times of C. The values and the layout is in Figure 6.1.1:

$R = 1250\Omega$, $C = 0.5\mu F$

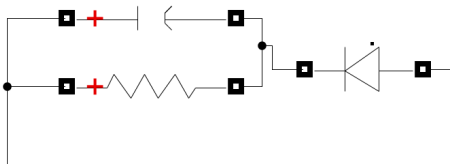


Figure 6.1.1: Snubber Layout

6.2 Simulation of Non-ideal Case

When we introduce all the non-idealities and run the simulation, the result is surprising. The output voltage waveform can be seen in Figure 6.2.1

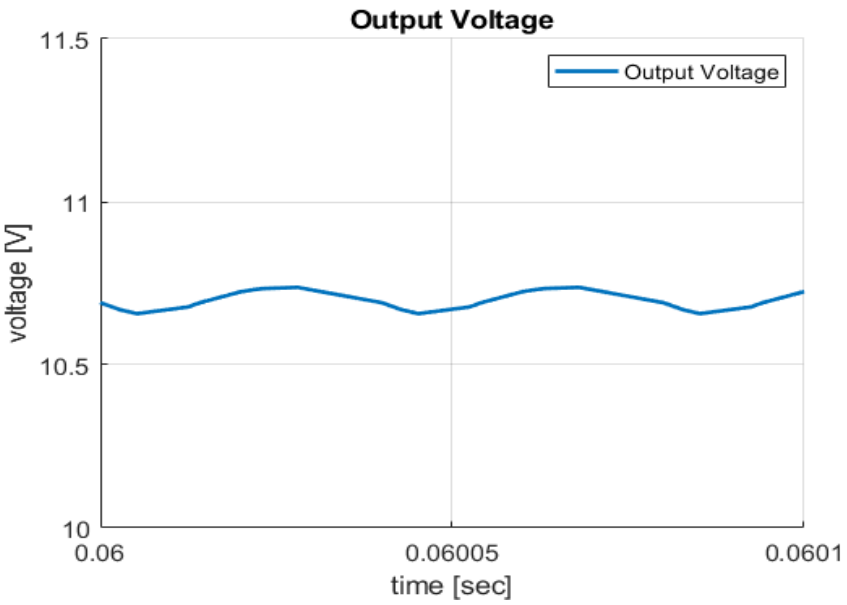


Figure 6.2.1: Output waveform of the forward converter 24V operation non-ideal

We can see that due to the drops on the diodes, and the series parasitic resistances, the output voltage almost dropped to the $10.7V$. In order to compansate this value, we need to boost the duty cycle. We boost duty cycle to the 43.5% for 24V operation.

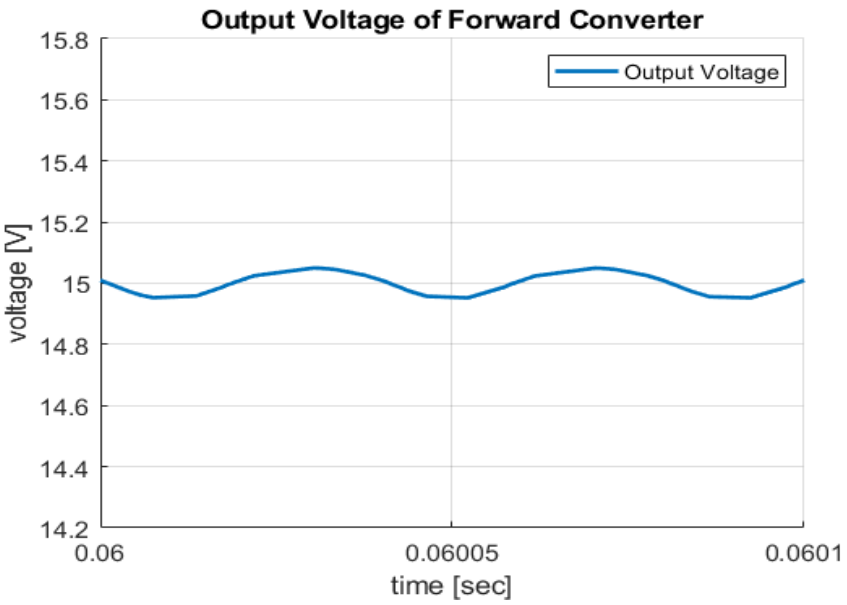
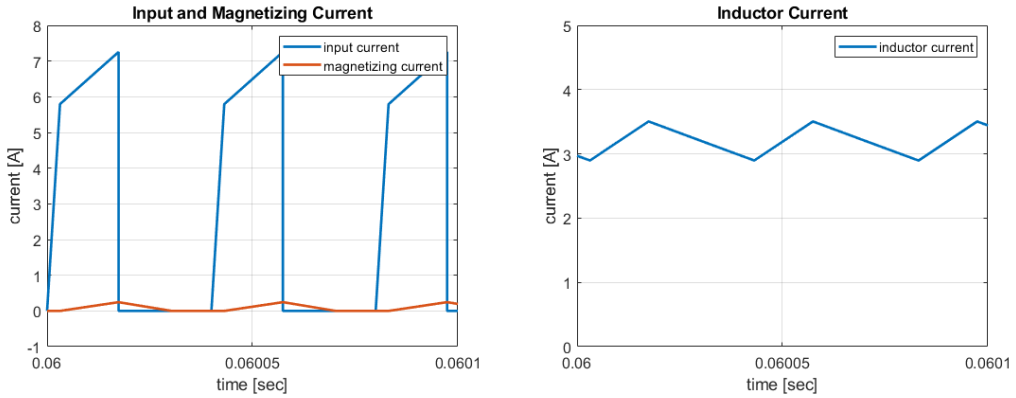


Figure 6.2.2: Output waveform of the forward converter 24V operation non-ideal



(a) Input and Magnetizing Current

(b) Inductor Current

Figure 6.2.3: Forward converter input and inductor current under 24 non-ideal operation

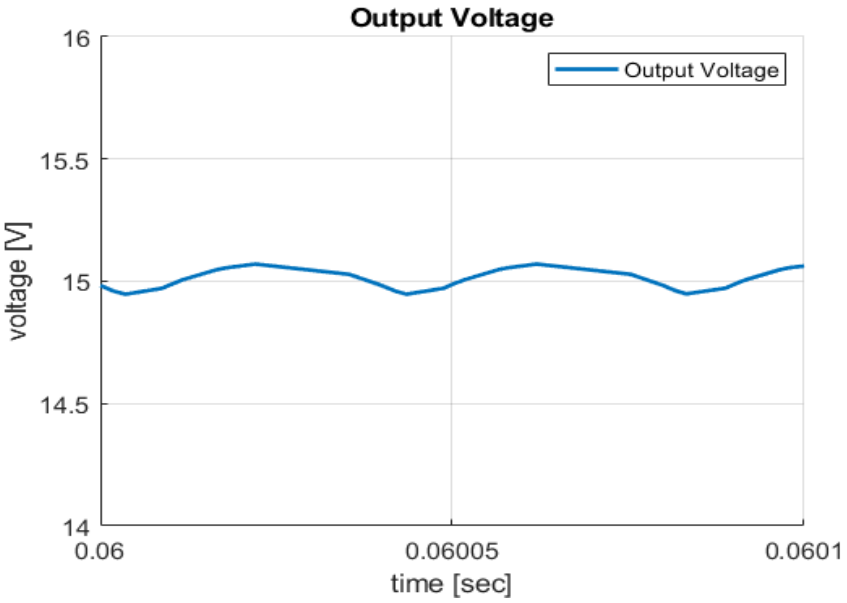
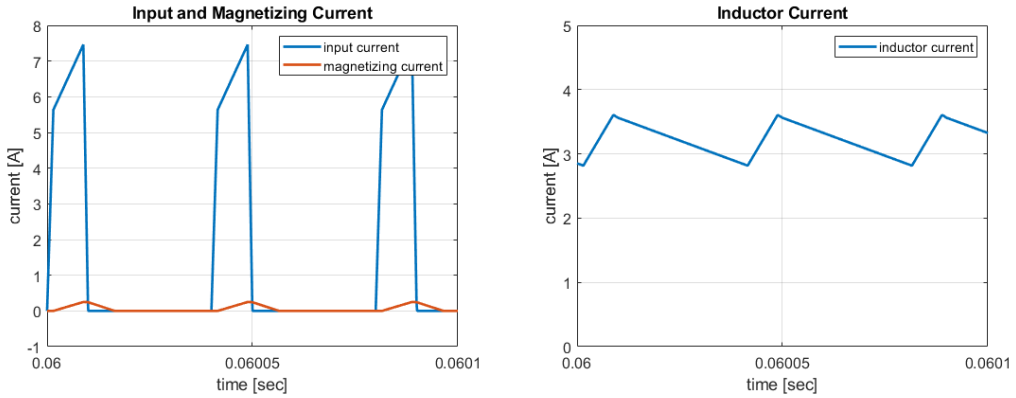


Figure 6.2.4: Output waveform of the forward converter 48V non-ideal operation



(a) Input and Magnetizing Current

(b) Inductor Current

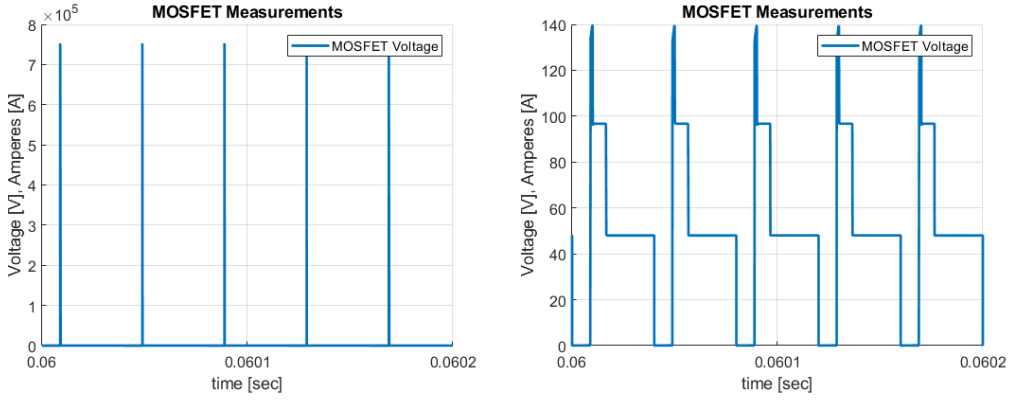
Figure 6.2.5: Forward converter input and inductor current under 48V non-ideal operation

The above simulations are for the non-ideal case with open-loop operation. Non-idealities drop the output voltage almost 2/3 of its value and decreases efficiency. Efficiency analysis will be done in the following parts.

In the ideal operations the duty cycles were calculated as: $D_{min} = 15.65\%$ and $D_{max} = 31.25\%$. However, in the non-ideal cases these values arised to higher values. So, it is very important to take non-idealities into account. This may result in inapplicable duty cycle values. Fortunately, our turn ratio decision $N = 2$ is enough for non-ideal operation. Our non-ideal case duty cycles are:

$D_{min} = 22.05\%$, and $D_{max} = 43.5\%$

One of the most important parts is the snubber around the switch. We know that the leakage inductance of the transformer create high voltages around the switch and causes burn outs. We designed a snubber circuit and introduced it. The results of non-ideal switching with snubber is below:



(a) MOSFET Voltage without Snubber (b) MOSFET Voltage with Snubber

Figure 6.2.6: Snubber effect on the MOSFET operation with leakage inductance

Since our MOSFET has a rated voltage of 150V, it is applicable. This snubber design is working.

7 Transfer Function and Compansator Design

7.1 Transfer Function Derivation

In the transfer function derivation, we are going to use averaging method.

In the forward converter below Figure 7.1.1 we can observe the forward converter. Here, we are starting with defining the $x_1 = i_L$ and $x_2 = v_c$. These two states will be taken into account from now on.

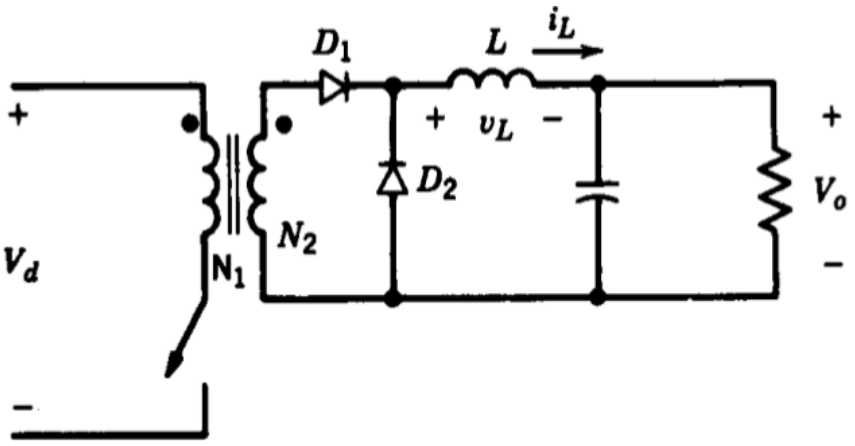
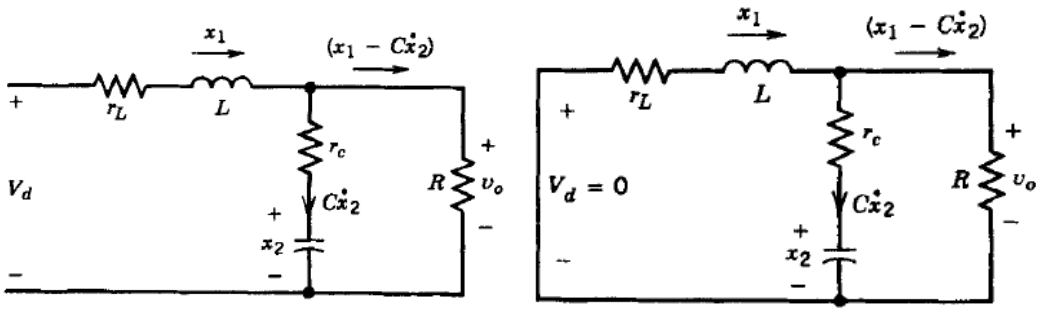


Figure 7.1.1: Forward Converter Topology

When we use the averaging method. It is important to use the switch ON and switch OFF models of the converter. Below, we can observe these models in Fig. 7.1.2.



(a) Switch ON

(b) Switch OFF

Figure 7.1.2: Forward converter averaging models switch on (a) and switch off (b)

In the first model, we can write that: assuming turn ratio is N.

$$-NV_d + r_L i_L + L\dot{i_L} + R(i_L - C\dot{v_C}) = 0 \tag{8}$$

and

$$-v_c + Cr_c\dot{v_C} + R(i_L - C\dot{v_c}) = 0 \tag{9}$$

Basically, when switch is on if we call this state space representation number 1, then it will have following structure:

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_C} \end{bmatrix} = \begin{bmatrix} -\dfrac{Rr_c + Rr_L + r_C r_L}{L(R + r_C)} & -\dfrac{R}{L(R + r_C)} \\ \dfrac{R}{C(R + r_C)} & -\dfrac{R}{L(R + r_C)} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} NV_d \tag{10}$$

Let us call this state space representation as

$$\dot{x} = A_1 x + B_1 u$$

When the switch is off, we can write following equations:

$$r_L i_L + L\dot{i_L} + R(i_L - C\dot{v_C}) = 0 \tag{11}$$

and

$$-v_c + Cr_c\dot{v_C} + R(i_L - C\dot{v_c}) = 0 \tag{12}$$

Switch is off, if we call this state space representation number 2, then it will have following structure:

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_C} \end{bmatrix} = \begin{bmatrix} -\dfrac{Rr_c + Rr_L + r_C r_L}{L(R + r_C)} & -\dfrac{R}{L(R + r_C)} \\ \dfrac{R}{C(R + r_C)} & -\dfrac{R}{C(R + r_C)} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} \tag{13}$$

Let us call this state space representation as

$$\dot{x} = A_2 x$$

As we can easily see $A_1 = A_2$ and more importantly $B_2 = 0$. Therefore averaging is much easier in this topology. Now, we can say that

$$A = A_1 D + A_2(1 - D) = A_1 \tag{14}$$

and

$$B = B_1 D \tag{15}$$

Let's derive the output. If we are to define the output as v_o then we can write that

$$v_o = R(i_L - C\dot{v_C}) \tag{16}$$

in state space form for both switch on and off cases

$$v_o = \begin{bmatrix} \frac{Rr_c}{R+r_C} i_L & \frac{R}{R+r_c} v_C \end{bmatrix} \tag{17}$$

To simplify these state space representations, we will follow a simple approach. In our circuitry, $r_c = 3m\Omega$, $r_L = 60m\Omega$ where $R = 4.7\Omega$. Starting from this point, apparently, we can assume that

$$R \gg (r_C + r_L) \tag{18}$$

so A is simplified as:

$$A = \begin{bmatrix} -\frac{r_c + r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix} \tag{19}$$

B is simplified as:

$$B = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} D \tag{20}$$

C is simplified as:

$$C = \begin{bmatrix} r_C & 1 \end{bmatrix} \tag{21}$$

Now, we need to introduce small signal perturbations to the system.

$$d = D + \tilde{d} \tag{22}$$

$$v_o = V_o + \tilde{v_o} \tag{23}$$

and

$$x = X + \tilde{x} \tag{24}$$

Now the equation becomes:

$$\tilde{\dot{x}} = A\tilde{x} + BNV_d\tilde{d} \tag{25}$$

and

$$\tilde{v_o} = C\tilde{x} \tag{26}$$

when we use the laplace transformation:

$$\tilde{x}(s) = [sI - A]^{-1}(B_1 V_d)\tilde{d(s)} \tag{27}$$

So, output to control transfer function can be written as:

$$\frac{\tilde{v_o}(s)}{\tilde{d}(s)} = C[sI - A]^{-1}BNV_d \tag{28}$$

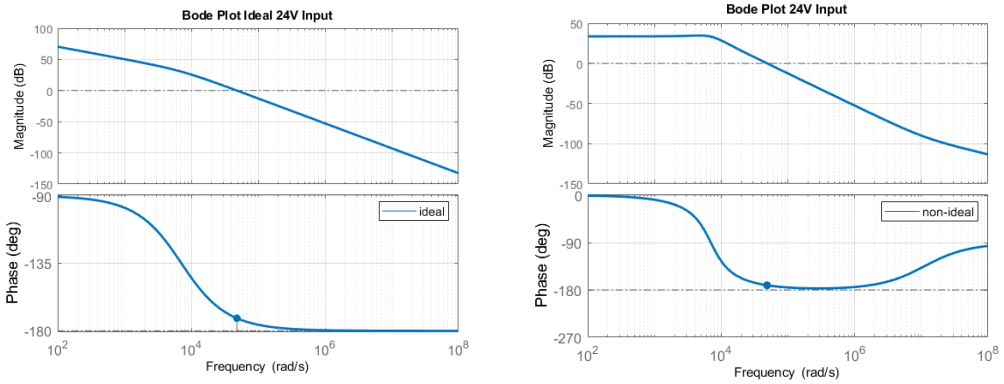
$$\frac{\tilde{v_o}(s)}{\tilde{d}(s)} = NV_d \frac{1 + sr_C C}{LC(s^2 + s(\frac{1}{RC} + \frac{(r_c + r_L)}{L}) + \frac{1}{LC})} \tag{29}$$

7.2 Bode Plot of the Forward Converter

Let's have a look at to the bode plot of the forward converter. In the ideal case where capacitor and inductor resistance does not exist, the transfer function can be simplified as:

$$\frac{\tilde{v_o}(s)}{\tilde{d}(s)} = NV_d \frac{1}{LC(s^2 + s\frac{1}{RC} + \frac{1}{LC})} \tag{30}$$

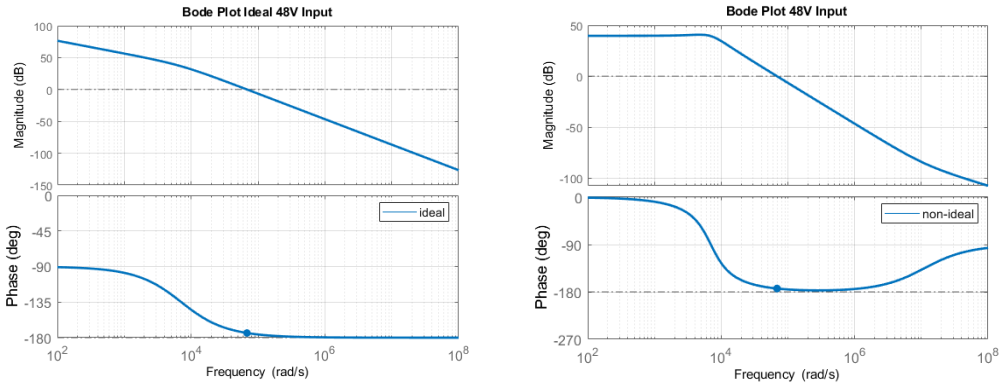
When we obtain its bode plot using Matlab, the resulting graph is below Fig **??**



(a) Ideal

(b) Non-ideal

Figure 7.2.1: Bode plot with input 24V ideal (a) and non-ideal (b)



(a) Ideal (b) Non-ideal

Figure 7.2.2: Bode plot with input 48V ideal (a) and non-ideal (b)

At the worst case, the input is 48V. Below, we can observe the phase margin of 48V input bode plot with all non-idealities. Figure 7.2.3

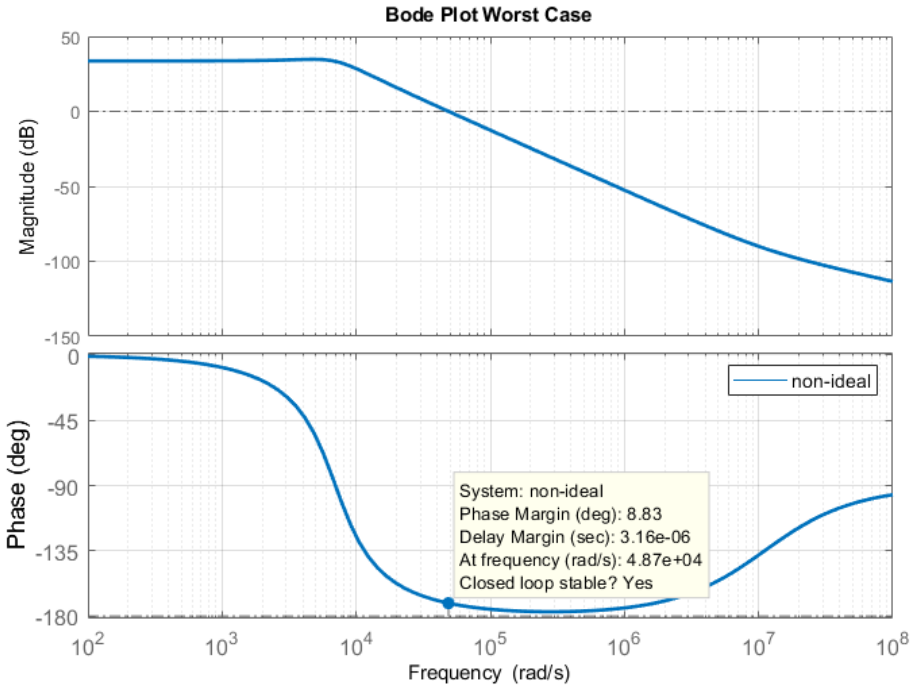


Figure 7.2.3: Bode plot of forward converter, worst case

As we can follow, forward converter is a stable converter with a very small phase margin. Nevertheless, we need to design a compansator that will boost the phase of the converter so that we can operate in stable region with considerable speed. Now, we are going to design a compansator to make this system more stable. Also, we want to operate in constant output voltage!

7.3 Compansator Design

8 Conclusion

In this project, our goal is to design a DC to DC converter. Our team has chosen forward converter configuration, #FOR1, for the project. In this report, we introduced possible topologies and the rationale behind our selection. Then, we theoretically calculated the needs of the project and the components. A detailed component by component calculation has been provided. Moreover, simulations for each component have been done and introduced. With the light of the simulations, our selections and theoretical calculations have been supported. It is now possible to say that the design introduced in this simulation report is doable, and properly functional. In conclusion, EE464 lectures have prepared us academically. We strongly believe that this project will enhance our understanding, and provide broader vision into power electronics area.