



MIDDLE EAST TECHNICAL UNIVERSITY

ELECTRICAL & ELECTRONICS ENGINEERING

EE464 - STATIC POWER CONVERSION II
HARDWARE PROJECT - FORWARD CONVERTER #1
POWERLOVERS
FINAL REPORT

Emre Deniz ŞENEL - 2167237
Burak YALÇIN - 2167534

24.06.2020

Contents

1	Introduction	3
2	Problem Definition, Objectives and Bonus Points	3
3	Forward Converter	4
3.1	General Structure	4
4	Design of the Forward Converter	5
4.1	System Level Design	5
4.2	Transformer Design	7
4.3	Cable Selection	8
4.4	Inductor and Capacitor Design	9
4.5	Switch and Diode Design	10
5	Ideal Simulations	12
5.1	Simulation Results	12
6	Non-idealities of Forward Converter	15
6.1	Adding the Non-idealities and Their Solutions	15
6.2	Simulation of Non-ideal Case	15
7	Transfer Function and Compensator Design	19
7.1	Transfer Function Derivation	19
7.2	Bode Plot of the Forward Converter	23
7.3	Compensator Design	25
8	Efficiency and Thermal Analysis	30
8.1	Efficiency Analysis	30
8.2	Thermal Analysis	33
9	PCB Design	34

9.1	Feedback Controller	34
9.2	Schematic	38
9.3	Footprints	41
9.4	PCB View	42
9.5	3-D View	44
9.6	Arrangement for 1000 Pieces from PCBWay	45
10	Conclusion	45
11	Appendix : Bill of Material Files	46

1 Introduction

Static Power Conversion II, a self-defined course, offers numerous isolated and non-isolated converters, inverters and their applications. In Spring'20, the theoretical background that have been acquired is to be turned into a hardware implementation of the combined knowledge all together. However, due to the pandemic, it is not possible to introduce a product but present a detailed design with software supports and PCB design. In this report, forward converter design of group Powerlovers will be introduced. Background information with objectives will take place. Then, all the steps of the projects, tests, design procedures and simulation results will be exhibited. We strongly believe, this project helped us understand the concepts we learnt in the lectures, and we had a chance to see beyond the horizons.

2 Problem Definition, Objectives and Bonus Points

In the project, we are to do a forward converter design with specific properties.

Table 1: Parameters of the project

Minimum Input Voltage (V)	24
Maximum Input Voltage (V)	48
Output Voltage (V)	15
Output Power (W)	48
Output Volt. Peak-to-Peak Ripple (%)	2
Line Regulation (%)	2
Load Regulation (%)	2

Some of the points and objectives can be itemized as:

- Closed loop is a must and we are not allowed to use digital controllers
- PCB design of the converter will be presented.
- Bill of material will be presented
- Closed loop compensator design with bode-plot is a **bonus**
- We are to do thermal design and efficiency analysis of the project

We have mentioned couple of specifications of the project. Our goal was to accomplish the main specifications and add as much as bonus we can.

In the next section we are introduce a forward converter.

3 Forward Converter

3.1 General Structure

Forward converter is basically derived from the buck converter. We are going to observe the relationship in the derivation phase. Forward converter is isolated as we know, and it uses transformer as its regular use. Transformer transfers the power to the secondary side and it does not store energy in between. In forward converter, it is important to take the magnetizing current into account.

In Figure 3.1.1, the forward converter topology can be observed. This is the most simple model.

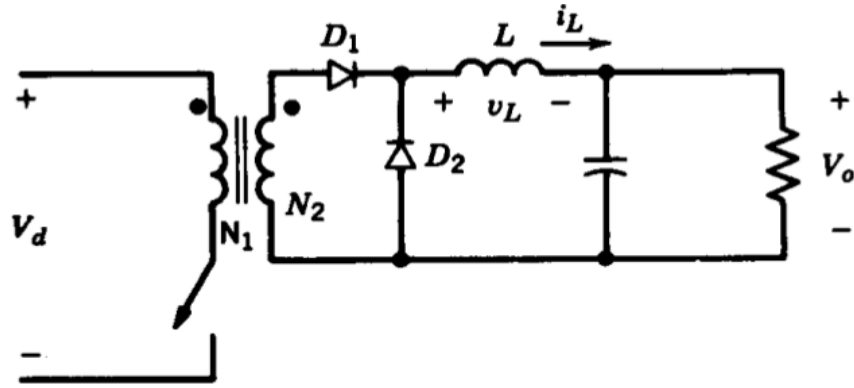


Figure 3.1.1: Forward Converter Topology

Assume the transformer is ideal for now to obtain the transfer function of the topology. During the ON state of the switch, D_1 is conducting and D_2 is reverse biased. Therefore, the inductor voltage can be written down as

$$V_L = \frac{N_2}{N_1} V_d - V_o$$

Let us examine now the OFF state of the switch. D_1 is now reverse biased on D_2 forms a free-wheeling path for the inductor. Load is fed by the stored energy in the inductor and the capacitor. Inductor voltage is easy to obtain and is as follows.

$$V_L = -V_o$$

Discussion so far end with applying the voltage-seconds rule for the inductor and this yields the transfer function of the forward converter topology as

$$\frac{V_o}{V_d} = \frac{N_2}{N_1} D \quad (1)$$

However, a question might arise rightfully at this point: how does this topology deal with the magnetizing current? During the OFF state, L_m has no path to discharge and it seems to be charged again and again during ON state. This situation ends up saturating the core and threatens the proper operation of the converter.

A variety of solutions for this problem are available. A snubber circuitry connected in parallel to the primary winding, a two switch topology are among them. A more practical and wide-spread application ,however, is adding a third reset winding. The resultant topology can be seen in Figure 3.1.2.

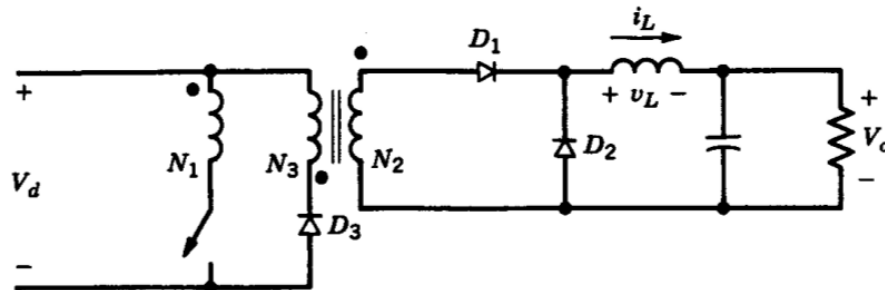


Figure 3.1.2: Practical Forward Converter Topology

In this topology, the third winding namely N_3 is in use in order to reset the winding so that the core does not saturate. As its nature opposes, the forward converter has limitations itself. One and the most important thing is that D_{max} namely maximum duty cycle is limited to the following equation

$$D_{max} = \frac{1}{1 + N_3/N_1} \quad (2)$$

In most of the cases, $N_1 = N_3$ is taken to simplify the structure and the organization. We followed the same approach in our solutions.

4 Design of the Forward Converter

4.1 System Level Design

The most important element in isolated power supplies is the transformer. Without knowing the transformer properties, it is not possible to move on with the simulations. Hence, the design process is now orderly. Output inductor and capacitor can also be chosen by theoretical knowledge.

Although it is possible to have a "pre-simulation" idea on the voltage stresses or current carrying capabilities for the semiconductor devices in the topology, it is safer to choose them in the guidance of the simulation results. Some of the non-idealities will also be involved in the simulations as well, allowing us to make more accurate assumptions about component selection.

In this part, we need to look at general specifications of the forward converter. Our customer, from Habelsan, asked us to satisfy these specifications:

- Input voltage range: $24V - 48V$
- Output voltage: $15V$
- Output power: $48W$
- Output voltage ripple: 2%, maximum
- Line and Load regulations: 2%, maximum

Firstly, we need to look at input-output voltage relationship of the forward converter. Ratio between the two is derived in the previous parts as:

$$\frac{V_o}{V_d} = \frac{N_2}{N_1} D \quad (3)$$

Output current's average value is $\frac{48W}{15V} = 3.2A$. As mentioned before, demagnetization of the core in the forward converter is important. Among different techniques, it is decided to use a reset winding. Turn number of the reset winding is chosen to be equal to that of the primary winding, conventionally and we will stick to that convention as well. This situation puts a restriction on the duty cycle to ensure proper demagnetization of the core. Duty cycle for the operation should be $D < 0.5$.

Turns Ratio & Duty Cycle

In the project, required voltage transfer ratios are 48V to 15V, and 24V to 15V. It is important to take into account that the limit of duty cycle is $D_{max} = 0.5$, and it is very crucial to reset all the core.

Using the input output equation and duty cycle restrictions, we choose the turn ratio between first and secondary winding as:

$$\frac{N_2}{N_1} = 2$$

Using these ratio, it is now easy to find required duty ratios. For 48V input,

$$D = \frac{48}{15} = 2 \implies D_{min} = 0.156$$

and For 24V input,

$$D = \frac{24}{15} = 2 \implies D_{max} = 0.3125$$

As can be seen, the duty cycle ratios obey the restrictions and they also allow a margin to compensate for the non-idealities.

Frequency

As switching frequency of the MOSFET, it is important to note that higher frequencies increases the switching losses. Also, at high frequencies, skin depth of the cable decreases dramatically. Moreover, it is also needed to be pointed that at higher frequencies hysteresis losses increase in the core. Therefore, we decided to keep our frequency less than 30kHz, $f < 30kHz$

Secondly, as frequency decreases, the amount of ripple at the output increases due to longer switching periods. Furthermore, it is important to keep the frequency at inaudible range so that the converter is not noisy. We decided that frequency should be higher than 20kHz, $f > 20kHz$.

Combining these two

$$20kHz < f < 30kHz$$

In the simulations, we decided as the best frequency would be 25kHz. Therefore, for our forward converter the frequency is $f = 25kHz$

4.2 Transformer Design

In the forward converter topology, it is important to realize the fact that transformer is introduced in order to transfer the power from primary to secondary. For this reason, we do not need any air gap in our transformer design. Moreover, a transformer with high inductance will allow us to operate in low magnetizing current levels due to high impedance of the inductor. When we combine these, we can start our calculations.

The first approach is to calculate $W_a A_c$, it shows the power handling capacity of our transformer. Its formula is as follows [1]:

$$W_a A_c = \frac{P_o D_{cma}}{K_t B_{max} f} \quad (4)$$

Here $P_o = 48W$, power out in watts, $D_{cma} = 500 \text{ cir}/\text{mils.amp}$, is current density, $K_t = 0.0005$, topology constant given for forward converter. $B_{max} = 2500G$, maximum flux density in gauss and $f = 25kHz$ is the frequency.

When we calculate the result

$$W_a A_c = 0.768 \text{ cm}^4$$

Now, using the magnetics' available cores offered for power handling capacities, we are going to choose a proper core. We chose an R material E shaped core, it is high in inductance and low in loss. It is very proper for this application.

The core link: [Core](#)

Now it is important to choose turn number for primary side. The secondary and third windings depend on the primary side. We are going to apply following approach:

$$N_p = \frac{V_p 10^8}{4BA_c f} \quad (5)$$

We choose following parameters for this application: $V_p = 48V$, $B = 0.25T$, $A_c = 0.87cm^2$ it given in the datasheet of the core and $f = 25kHz$. The result is:

$$N_p = 22 \text{ turn}$$

Naturally, we have $N_1 = 22, N_2 = 44, N_3 = 22$ due to our selection.

The turns number for windings are determined as

- Primary winding, $n_1 = \mathbf{22 \text{ turns}}$
- Reset winding, $n_3 = \mathbf{22 \text{ turns}}$
- Secondary winding, $n_2 = \mathbf{44 \text{ turns}}$

Now, it is very important to take magnetizing inductance into account. In the datasheet we can easily see that the AL value is given as $AL = 2667nH/T^2$. As we decided our turn number is 22, we can easily calculate the magnetizing inductance as:

$$L_m = 22^2 * 2667 * 10^{-9} = 1.3mH$$

This is a great value because a low magnetizing inductance will increase the magnetizing current at the primary side, as a result we would need a higher current capability. However, 1.3mH is a legitimate value. If we calculate the magnetizing current at operating frequency:

$$I_m = \frac{V}{Z} = 0.235A$$

4.3 Cable Selection

In practical cases maximum fill factor achievable is stated at 50%. We need to take these two parameters into account.

Moreover, it is important to notice that, the input current at the maximum operation is $I_{in} = 2A$ and $I_m = 0.235A$, as overall we need minimum of $I_1 = 2.3A$ at the primary side. At the secondary side we are going to have a maximum of $I_o = 3.2A$, we have to take these into account.

Using a simple approach $1mm^2$ of cable can carry $4A$, and considering skin depth. We have chosen to use AWG22 cable. It's area is $0.327mm^2$ and it can carry a current up to $1.3A$. Also, it's maximum skin depth is applicable up to $42kHz$, that is to say since our operating frequency is $25kHz$, this cable is proper to use. Considering margins, we are going to choose needed parallel cable amount.

In the output we need 2 parallel cables, and at the output we need 3 parallel cables.

Now, it is important to have a look at the fill factor. It is very crucial to have a fill factor around 50% so that our transformer is realizable.

If we calculate the cable areas:

$$A_{cable} = 0.326 * 22 + 0.326 * 22 + 0.326 * 44 = 71.9mm^2$$

If we check our core's window area, we can see that it is:

$$A_{window} = 9.8 * 8 * 2 = 156.8mm^2$$

So the fill factor of our transformer is:

$$k = \frac{61.1}{156.8} = 46\%$$

This fill factor is applicable and not an overdesign. Therefore, the cable selections are proper. We have a legitimate fill factor, we have 100% skin depth, and we have margins so that there is no burnout. In the next step we are going to cover the capacitor and inductor.

4.4 Inductor and Capacitor Design

To design the inductor, we are focus on the maximum ripple current allowed. In the specifications, it is not determined, so we are going to have 20% maximum ripple current so that our output current would be out of harmonics and the filtering capacitor would be smaller.

At the ON period, the inductor is charging, and using the voltage among the terminals we can find the ripple current value.

$$\Delta I = \frac{1}{L} \int_0^{DT_s} V_L dt < \frac{3.2A}{5}$$

$$\Delta I = \frac{1}{L} \int_0^{DT_s} (V_s \frac{N_2}{N_1} - V_o) dt < 0.64A$$

$$0.62mH < L$$

Also, it is very important to take rated current into account. The minimum rated current that inductor can carry must be minimum of $3.2A + 0.65A \approx 3.8A$

Using digikey website, we chose a proper inductor. It is important to have a small inductor in order to decrease the size and the weight.

Inductor Link: [Inductor](#)

Capacitor design is depending on the inductor design. As we know, we have to limit the ripple value of the output voltage. Also, the current that is flowing through the output is equal to the inductor current. We need to follow the following approach.

$$\Delta V = \frac{\Delta Q}{C} \quad (6)$$

$$\Delta Q = \Delta I_L * \frac{T_s}{8} \quad (7)$$

Here, we are using buck converter capacitor design approach. They are same in the application:

$$\Delta V = 0.3V > \frac{DT_s^2(V_s \frac{N_2}{N_1} - V_o)}{8LC}$$

$$C > 28\mu F$$

Also, apparently the rated voltage of the capacitor should be higher than the rated voltage of the output, for that reason $C_{v, rated} > 15V$

Capacitor Link: [Capacitor](#)

ESR value of the capacitor is: 3 mΩ

4.5 Switch and Diode Design

In these voltage levels and frequency levels it is proper to use MOSFET due to their fast recovery. It is also easy to implement a MOSFET into a converter. While designing the MOSFET, it is very important not to exceed its rated voltage and current values.

In the simulations with idealities, we came up with the values that:

- Switch stress has its maximum values for input of 48V naturally. We can say that our switch must be endurable minimum of 100V rated reverse voltage and 10A forward voltage.

- Switch must be proper to operate at 25kHz range, reverse recovery times should be appropriate.

We have chosen an N-Channel MOSFET with ratings 10 A, 150 V. The MOSFET Link: [MOSFET](#)

Silicon diodes are proper because they are cheap in cost and they have proper operation for this implementation range.

In the simulations with idealities, we came up with the values that:

- Diode' stress have their maximum values for input of 48V naturally. We can say that switches must be endurable minimum of 100V rated reverse voltage and 4A forward voltage.
- Diode must be proper to operate at 25kHz range, reverse recovery times should be appropriate.

A Schottky diode with ratings 5A and 100 V is chosen for our application.

The Diode Link: [Diode](#)

5 Ideal Simulations

5.1 Simulation Results

Below in the Figure 5.1.1, the simulation model schematic can be seen.

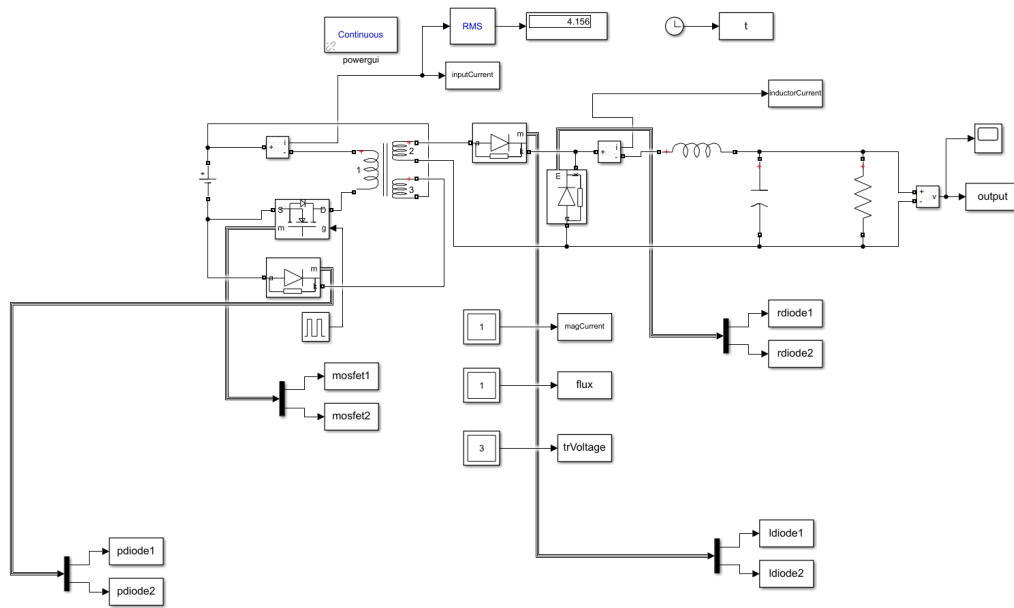


Figure 5.1.1: Simulation model

First, we simulated the ideal models in order to see the overall system operation. It is open-loop operation simulation and we would like to validate the duty cycles, operation principle and validity of our selections.

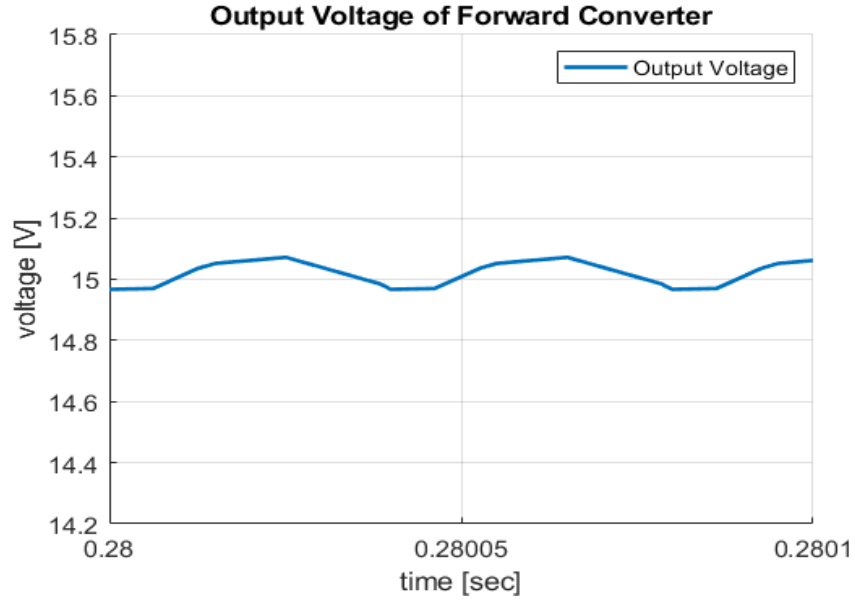


Figure 5.1.2: Output waveform of the forward converter under 48V operation

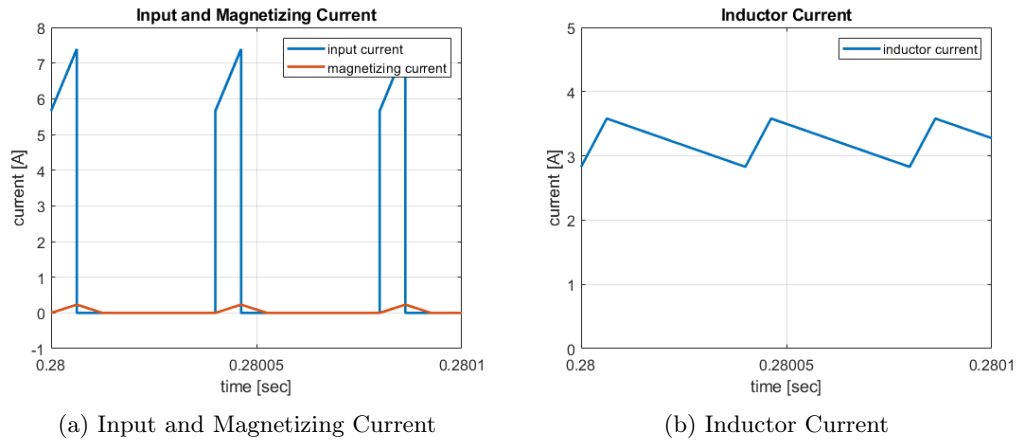


Figure 5.1.3: Forward converter input and inductor current under 48V input operation

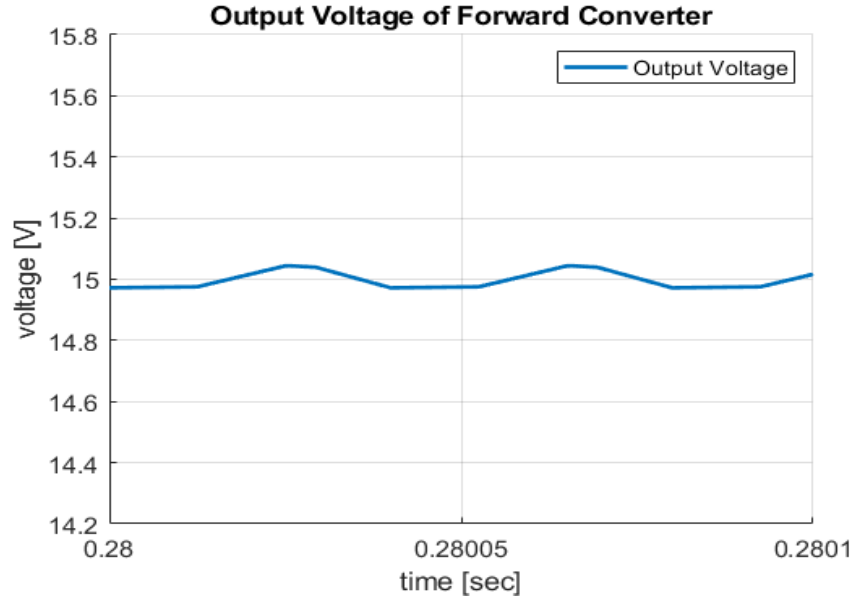


Figure 5.1.4: Output waveform of the forward converter under 24V operation

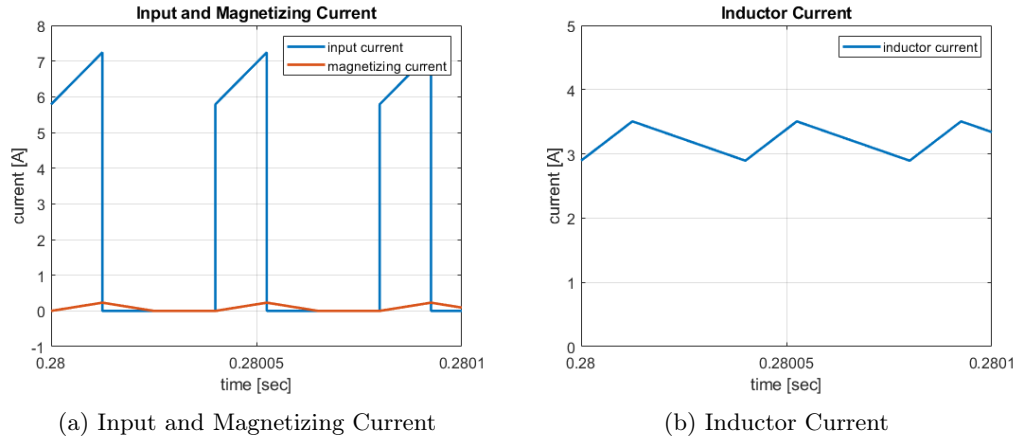


Figure 5.1.5: Forward converter input and inductor current under 24V input operation

As we can see from the Fig. 5.1.4 and 5.1.2 the output ripple is below 2%. The operation is stable and the duty cycles are as expected. However, when non-idealities are presented the duty cycle values will be re-calculated in order to compensate the voltage drops of losses and diodes etc.

Also, from the Fig. 7.3.2 and 5.1.3, we can observe the magnetizing current is as expected around 0.3A and the inductor ripple is around 0.6A for both operations. These results show that our calculations are valid. Now we are going to add non-idealities of the circuit.

6 Non-idealities of Forward Converter

6.1 Adding the Non-idealities and Their Solutions

Firstly, we added the loss components of the MOSFET and the diodes. As we can see from the datasheet, MOSFET has $R_{ds,ON} = 12.4m\Omega$, this value is added to the MOSFET. Then, the forward voltage values of the diodes are added to the software $V_f = 0.7V$ in our operation topology. After adding these, $R_{d,ON} = 1m\Omega$ added for the diodes representing the losses on the selected diodes.

Series resistance of the inductor is given as maximum of $R_{max} = 0.113\Omega$ for convenience we took this value as 0.6Ω to obtain an average operation range. Also, using the datasheet of the capacitor, we found out that the ESR value of the capacitor is around $3m\Omega$. This is a low value, because the capacitor is a seramic capacitor and it has very low ESR operation.

Next step was to add the leakage inductances of the transformer, we have taken the leakage inductance as 1% of the magnetizing inductance and introduced the leakage inductance as $13\mu H$ to the primary side of the transformer. Also, copper resistances added to the non-ideal system. At primary $R_1 = 0.33\Omega$ at secondary $R_2 = 0.44\Omega$

Then it is very crucial to notice that the stored energy in the leakage inductance needs a way to discharge itself. For this very reason it is very important to design a snubber circuit around the MOSFET in order to block burnouts and have a smooth operation. We have decided to move on with a RC Snubber.

When designing the RC snubber we can use an Application Note [2], in the application note, there is a snubber designed. We changed the R and C variables in order to adjust the solution into our problem. We have twice of voltage at the input and the current is twice. So, we used four times of R and two times of C. The values and the layout is in Figure 7.3.1:

$$R = 1250\Omega, C = 0.5\mu F$$

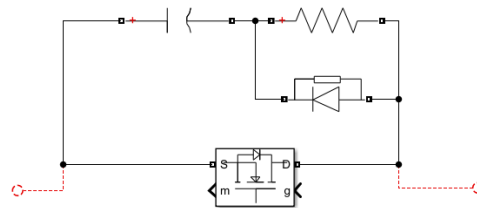


Figure 6.1.1: Snubber Layout

6.2 Simulation of Non-ideal Case

When we introduce all the non-idealities and run the simulation, the result is surprising. The output voltage waveform can be seen in Figure 6.2.1

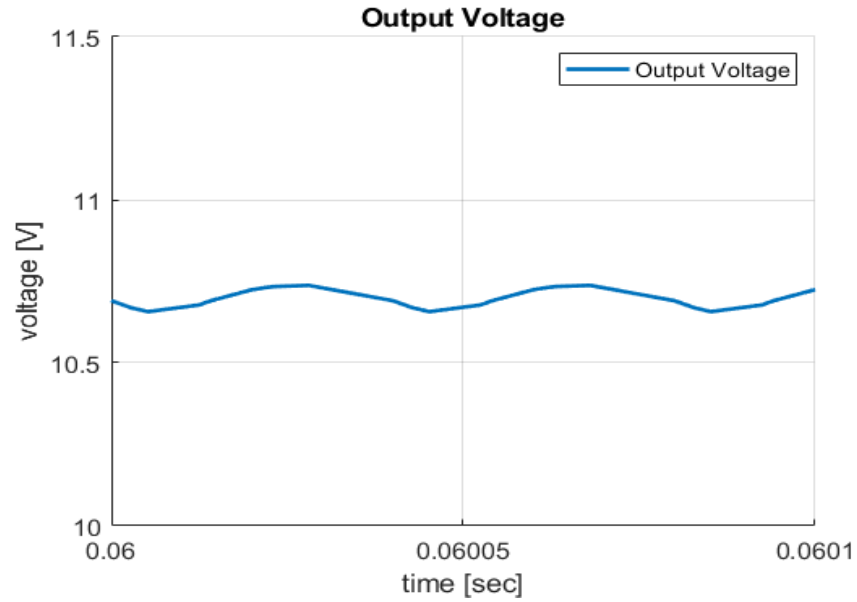


Figure 6.2.1: Output waveform of the forward converter 24V operation non-ideal

We can see that due to the drops on the diodes, and the series parasitic resistances, the output voltage almost dropped to the 10.7V. In order to compensate this value, we need to boost the duty cycle. We boost duty cycle to the 43.5% for 24V operation.

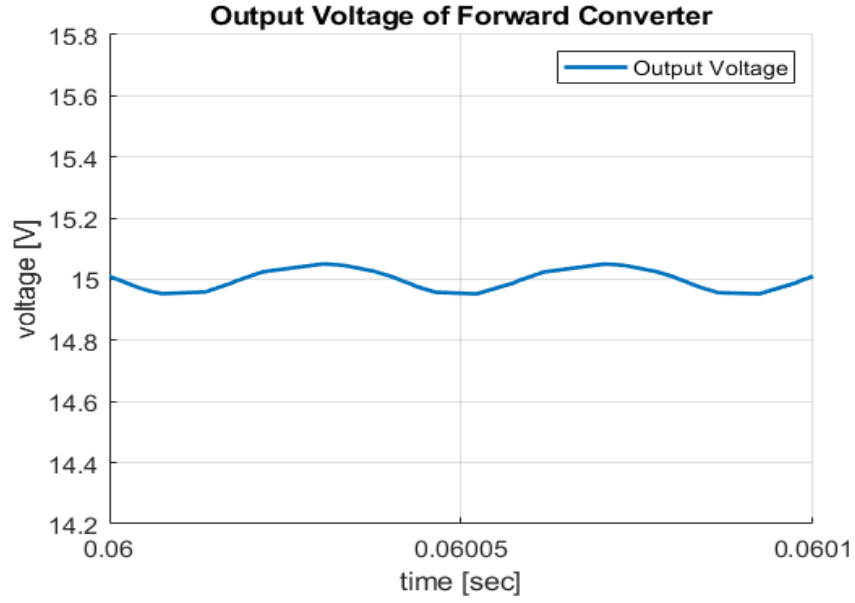


Figure 6.2.2: Output waveform of the forward converter 24V operation non-ideal

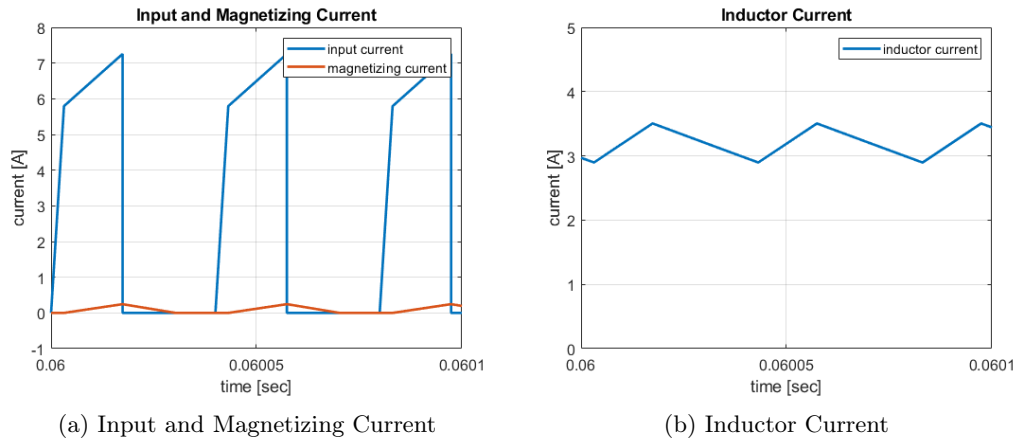


Figure 6.2.3: Forward converter input and inductor current under 24 non-ideal operation

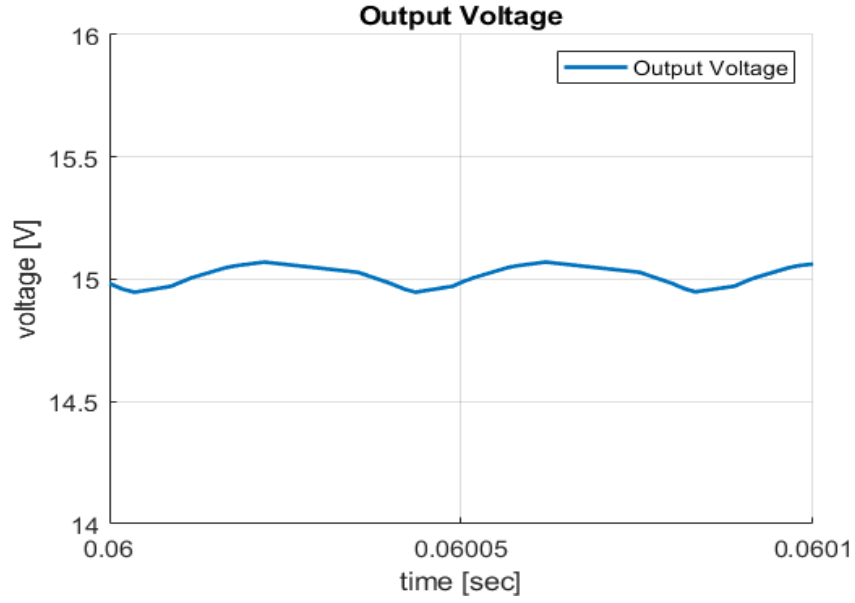


Figure 6.2.4: Output waveform of the forward converter 48V non-ideal operation

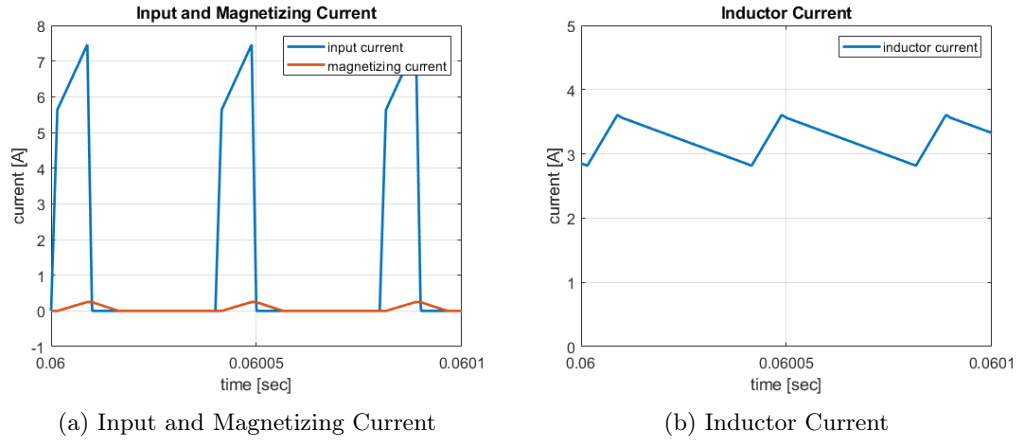


Figure 6.2.5: Forward converter input and inductor current under 48V non-ideal operation

The above simulations are for the non-ideal case with open-loop operation. Non-idealities drop the output voltage almost $\frac{2}{3}$ of its value and decreases efficiency. Efficiency analysis will be done in the following parts.

In the ideal operations the duty cycles were calculated as: $D_{min} = 15.65\%$ and $D_{max} = 31.25\%$. However, in the non-ideal cases these values arised to higher values. So, it is very important to take non-idealities into account. This may result in inapplicable duty cycle values. Fortunately, our turn ratio decision $N = 2$ is enough for non-ideal operation. Our non-ideal case duty cycles are:

$$D_{min} = 22.05\%, \text{ and } D_{max} = 43.5\%$$

One of the most important parts is the snubber around the switch. We know that the leakage inductance of the transformer create high voltages around the switch and causes burn outs. We designed a snubber circuit and introduced it. The results of non-ideal switching with snubber is below:

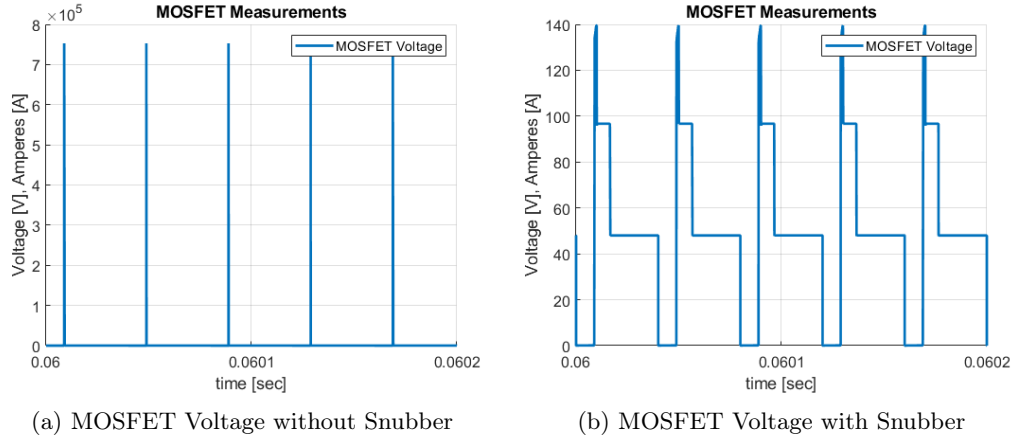


Figure 6.2.6: Snubber effect on the MOSFET operation with leakage inductance

Since our MOSFET has a rated voltage of 150V, it is applicable. This snubber design is working.

7 Transfer Function and Compensator Design

7.1 Transfer Function Derivation

In the transfer function derivation, we are going to use averaging method. [3]

In the forward converter below Figure 7.1.1 we can observe the forward converter. Here, we are starting with defining the $x_1 = i_L$ and $x_2 = v_c$. These two states will be taken into account from now on.

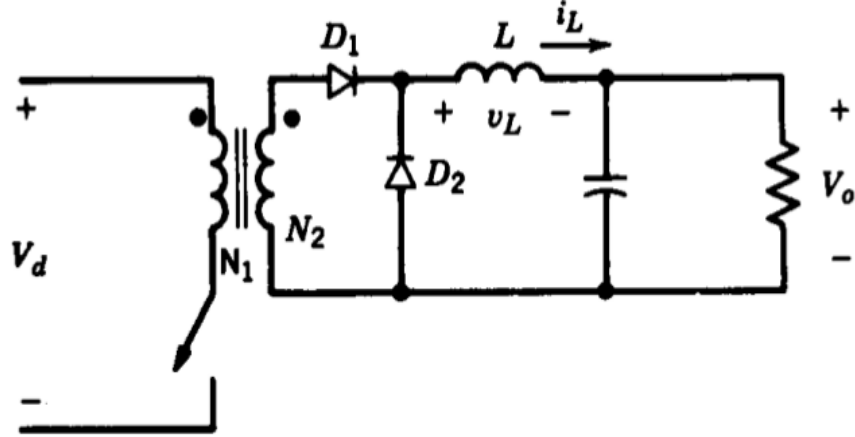


Figure 7.1.1: Forward Converter Topology

When we use the averaging method. It is important to use the switch ON and switch OFF models of the converter. Below, we can observe these models in Fig. 7.1.2.

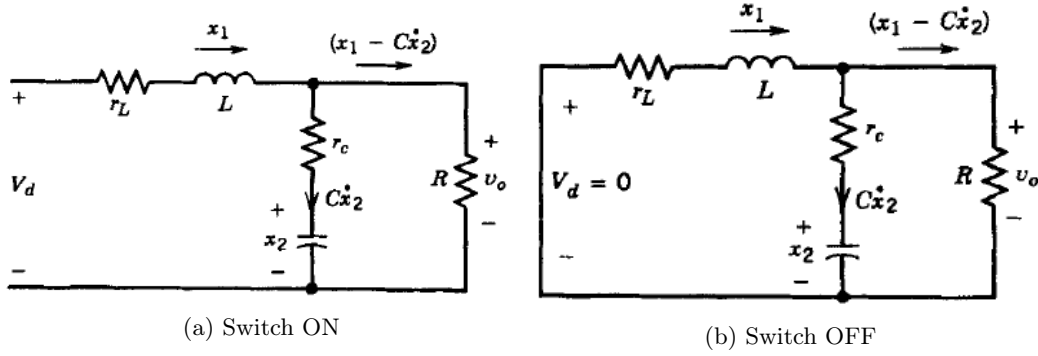


Figure 7.1.2: Forward converter averaging models switch on (a) and switch off (b)

In the first model, we can write that: assuming turn ratio is N .

$$-NV_d + r_L i_L + L \dot{i}_L + R(i_L - C \dot{v}_C) = 0 \quad (8)$$

and

$$-v_c + C r_c \dot{v}_C + R(i_L - C \dot{v}_c) = 0 \quad (9)$$

Basically, when switch is on if we call this state space representation number 1, then it will have following structure:

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{Rr_c + Rr_L + r_C r_L}{L(R + r_C)} & -\frac{R}{L(R + r_C)} \\ \frac{R}{C(R + r_C)} & -\frac{1}{C(R + r_C)} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} NV_d \quad (10)$$

Let us call this state space representation as

$$\dot{x} = A_1 x + B_1 u$$

When the switch is off, we can write following equations:

$$r_L \dot{i}_L + L \dot{i}_L + R(i_L - C \dot{v}_C) = 0 \quad (11)$$

and

$$-v_c + Cr_c \dot{v}_C + R(i_L - C \dot{v}_C) = 0 \quad (12)$$

Switch is off, if we call this state space representation number 2, then it will have following structure:

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{Rr_c + Rr_L + r_C r_L}{L(R + r_C)} & -\frac{R}{L(R + r_C)} \\ \frac{R}{C(R + r_C)} & -\frac{1}{C(R + r_C)} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} \quad (13)$$

Let us call this state space representation as

$$\dot{x} = A_2 x$$

As we can easily see $A_1 = A_2$ and more importantly $B_2 = 0$. Therefore averaging is much easier in this topology. Now, we can say that

$$A = A_1 D + A_2 (1 - D) = A_1 \quad (14)$$

and

$$B = B_1 D \quad (15)$$

Let's derive the output. If we are to define the output as v_o then we can write that

$$v_o = R(i_L - C \dot{v}_C) \quad (16)$$

in state space form for both switch on and off cases

$$v_o = \begin{bmatrix} \frac{Rr_c}{R+r_c}i_L & \frac{R}{R+r_c}v_C \end{bmatrix} \quad (17)$$

To simplify these state space representations, we will follow a simple approach. In our circuitry, $r_c = 3m\Omega$, $r_L = 60m\Omega$ where $R = 4.7\Omega$. Starting from this point, apparently, we can assume that

$$R \gg (r_c + r_L) \quad (18)$$

so A is simplified as:

$$A = \begin{bmatrix} -\frac{r_c + r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix} \quad (19)$$

B is simplified as:

$$B = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} D \quad (20)$$

C is simplified as:

$$C = [r_C \quad 1] \quad (21)$$

Now, we need to introduce small signal perturbations to the system.

$$d = D + \tilde{d} \quad (22)$$

$$v_o = V_o + \tilde{v}_o \quad (23)$$

and

$$x = X + \tilde{x} \quad (24)$$

Now the equation becomes:

$$\dot{\tilde{x}} = A\tilde{x} + BN V_d \tilde{d} \quad (25)$$

and

$$\tilde{v}_o = C\tilde{x} \quad (26)$$

when we use the laplace transformation:

$$\tilde{x}(s) = [sI - A]^{-1}(B_1 V_d) \tilde{d}(s) \quad (27)$$

So, output to control transfer function can be written as:

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = C[sI - A]^{-1} B N V_d \quad (28)$$

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = N V_d \frac{1 + s r_C C}{LC(s^2 + s(\frac{1}{RC} + \frac{(r_c + r_L)}{L}) + \frac{1}{LC})} \quad (29)$$

7.2 Bode Plot of the Forward Converter

Let's have a look at to the bode plot of the forward converter. In the ideal case where capacitor and inductor resistance does not exist, the transfer function can be simplified as:

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = N V_d \frac{1}{LC(s^2 + s\frac{1}{RC} + \frac{1}{LC})} \quad (30)$$

When we obtain its bode plot using Matlab, the resulting graph is below Fig 7.2.1a. Also, below we have non-ideal bode plots Figure 7.2.1b and 7.2.2b

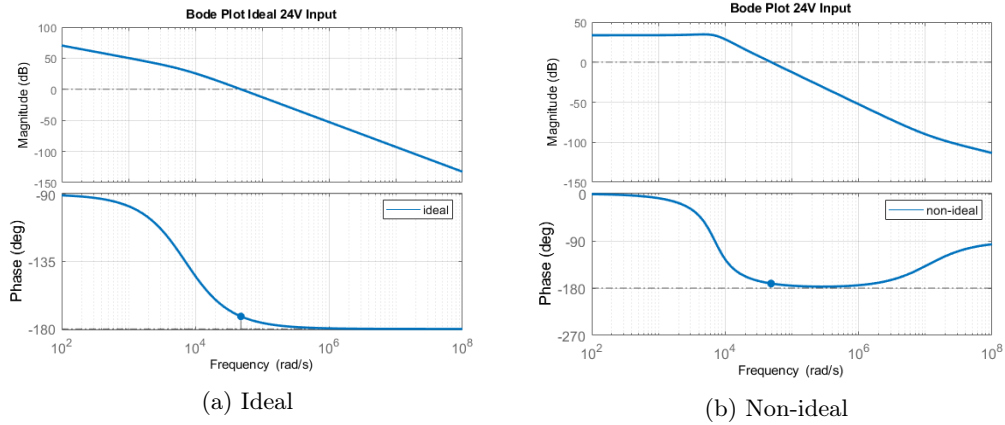


Figure 7.2.1: Bode plot with input 24V ideal (a) and non-ideal (b)

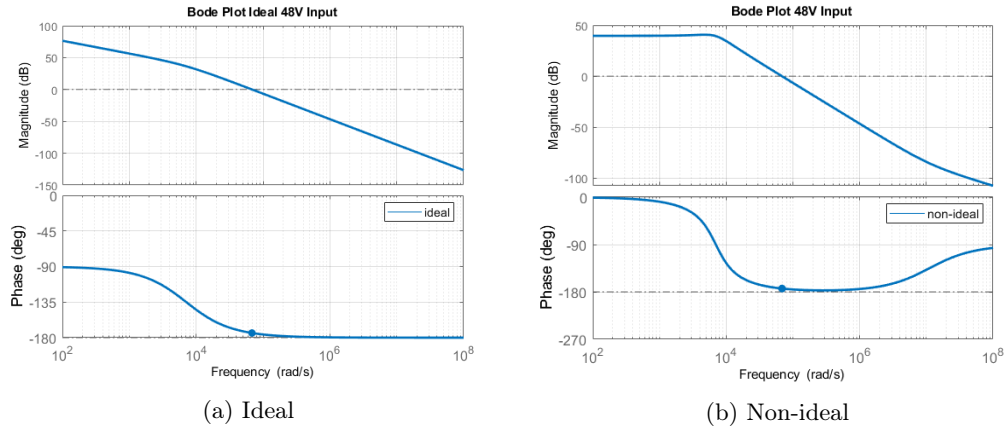


Figure 7.2.2: Bode plot with input 48V ideal (a) and non-ideal (b)

At the worst case, the input is 48V. Below, we can observe the phase margin of 48V input bode plot with all non-idealities. Figure 7.2.3

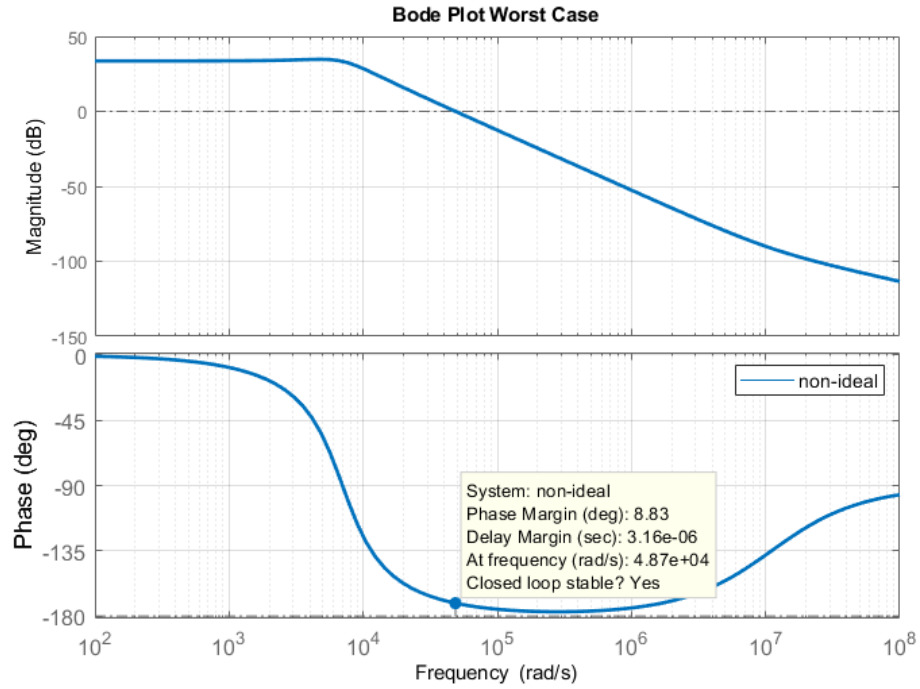


Figure 7.2.3: Bode plot of forward converter, worst case

As we can follow, forward converter is a stable converter with a very small phase margin. Nevertheless, we need to design a compensator that will boost the phase of the converter so that we can operate in stable region with considerable speed. Now, we are going to design a compensator to make this system more stable. Also, we want to operate in constant output voltage!

7.3 Compensator Design

Basically, a forward converter and a boost converter have similar transfer functions. Its difference is that the input voltage reflects with a turn ratio, nonetheless, the rest is almost same. Therefore, we can apply a buck compensator for the forward converter, and make it work! We are applying the procedure in the given note. [4]

Firstly, it is important to see that we need to boost our phase margin due to increase stability. An operation around $40-70^\circ$ will be enough for our operation. It is obvious that we need a type three compensator to boost our phase margin. Also, if we calculate the frequencies of the circuitry we can easily see that:

$$F_{esr} = \frac{1}{2\pi R_{ESR} C_o} = 1.77MHz \quad (31)$$

$$F_{LC} = \frac{1}{2\pi\sqrt{LC}} = 1.11kHz \quad (32)$$

$$F_0 = \frac{f_s}{10} = 2.5kHz \quad (33)$$

Basically, we can see that:

$$F_{LC} < F_0 < F_s/2 < F_{ESR} \quad (34)$$

We should use Type-III Compensator! Also, it is very convenient because we have used a ceramic capacitor at the output!

At this point, we need to introduce the schematic of compensator! This compensator consists of 3 poles and 2 zeros. One pole is an integrator, which makes the steady state error zero. So, at the low frequencies we have a -90° boost shift. However, at the proper locations we have a phase boost up to 90° theoretically. Here, an important factor is that, at the oscillator we are using $1.8V$ oscillator voltage with the frequency of $25kHz$. It is significant that, we should have a duty cycle limit of $D_{max} = 0.5$.

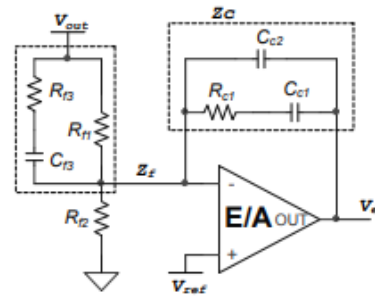


Figure 7.3.1: Snubber Layout

Nonetheless, we can apply further duty cycles, the third winding will be a problem. So, V_{ref} must be maximum of $0.9V$ for operation.

$$V_{ref} = 0.9V \quad (35)$$

Here is the transfer function:

$$H(s) = \frac{(1 + sR_{C1} + C_{C1})(1 + sC_{f3}(R_{f1} + R_{f3}))}{sR_{f1}(C_{C1} + C_{C2})(1 + sR_{C1}(\frac{CC1C_{C2}}{CC1 + C_{C2}}))(1 + sR_{f3}C_{f3}} \quad (36)$$

$$F_{Z1} = \frac{1}{2\pi R_{C1}C_{C1}} \quad (37)$$

$$F_{Z2} = \frac{1}{2\pi C_{f3}(R_{f1} + R_{f3})} \quad (38)$$

$$F_{p1} = 0 \quad (39)$$

$$F_{p2} = \frac{1}{2\pi R_{f3}C_{f3}} \quad (40)$$

$$F_{p3} = \frac{1}{2\pi R_{C2}C_{C2}} \quad (41)$$

Now, it is important to decide the pole and zero locations in order to have a proper compensator. We place the F_{p3} to the $F_s/2$ to have a low-pass structure, and to eliminate the ripples above the switching frequency.

$$F_{p3} = \frac{F_s}{2} = 12.5kHz$$

Now, we need to design the lead-compensator part. As we know, a type-3 compensator can boost up the phase margin maximum of 90° . However, in practical it is maximum 80° . A phase-lead compensator consists of one pole and one zero. This compensator must be located at the crossover frequency to boost up the phase margin. We should use following formulas:

$$F_{Z2} = F_0 \sqrt{\frac{1 - \sin \theta}{1 + \sin \theta}}$$

$$F_{p2} = F_0 \sqrt{\frac{1 + \sin \theta}{1 - \sin \theta}}$$

Since, my phase margin is negative right now, i should get the maximum of phase shift. We put the θ at limit, $\theta = 80^\circ$. Since, i selected the crossover frequency as $F_s/10$ the zero of the lead-compensator will result in increment of the gain. We were expecting an increase in gain in the lead-compensator part.

$$F_{Z2} = 418Hz$$

$$F_{p2} = 28.38kHz$$

We chose the second zero before the first one in order not to have decrements in the gain. It is significant to sustain gain level. We chose

$$F_{Z1} = \frac{F_{Z2}}{2} = 210Hz$$

After this point, we need to select a proper capacitor for C_{f3} , i choose this capacitor value as $2.2nF$.

$$R_{f3} \approx 2.55k\Omega$$

then

$$R_{f1} \approx 170k\Omega$$

using this the data given in the application note:

$$R_{C1} = \frac{2\pi F_0 L_o C_o V_{osc}}{V_{in} C_{f3}}$$

There, since it is a forward converter the capacitor and inductor values are what they are!

$$R_{C1} \approx 5.46k\Omega$$

using R_{C1}

$$C_{C1} = 140nF$$

$$C_{C2} = 2.33nF$$

$$R_{f2} = \frac{R_{f1} V_{ref}}{V_{out} - V_{ref}} = 10.9k\Omega$$

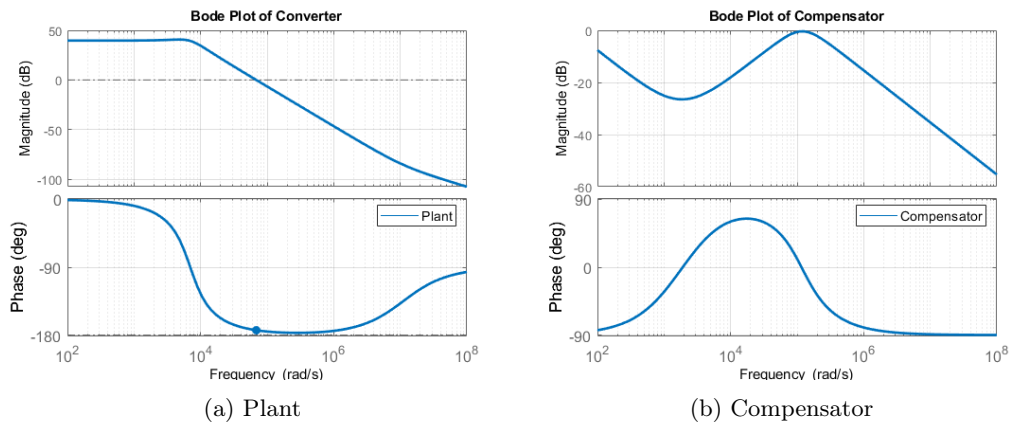


Figure 7.3.2: Forward converter plant (a) and compensator (b) bode plot

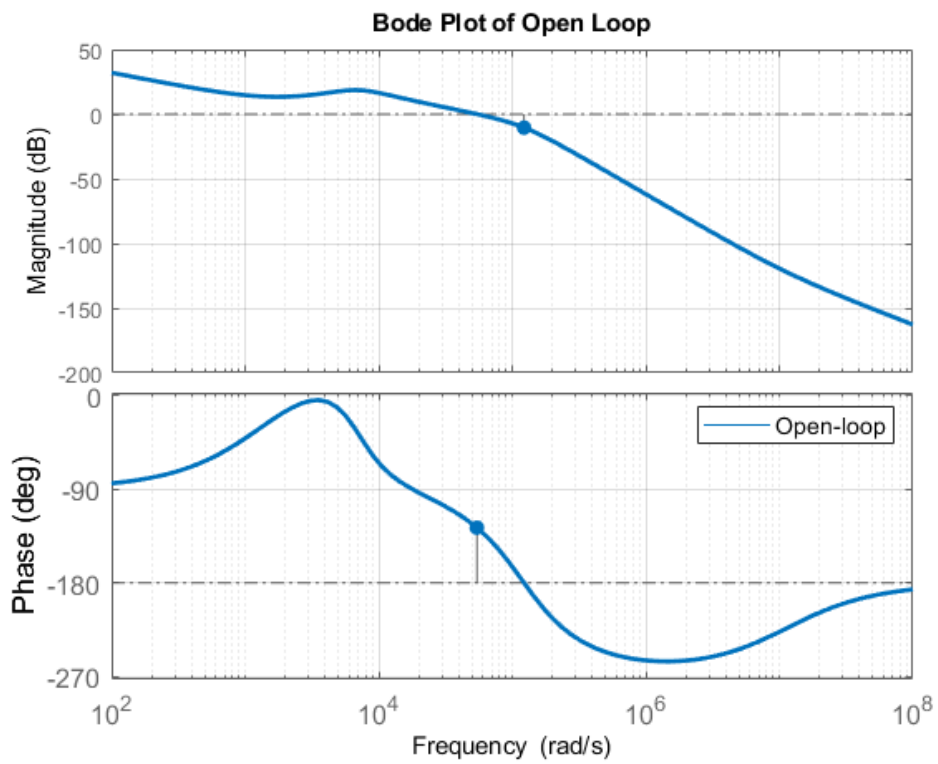


Figure 7.3.3: Open-loop bode plot

In the resultant bode plot, we can see that the phase margin is boosted up to 55° and the bandwidth is very convenient. Let's construct the LTSpice model of this compensator.

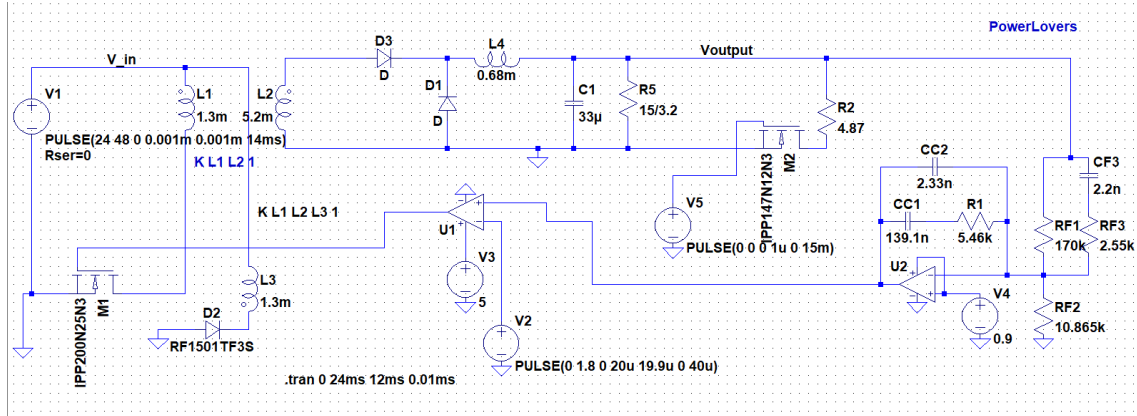


Figure 7.3.4: Forward converter with compensator

To simulate the line regulation and load regulation, first we increased the input from 24V to 48V, and observed the output. Below in the Fig 7.3.5 we can see the output waveform. We changed the output from 24V to 48V at 2ms.

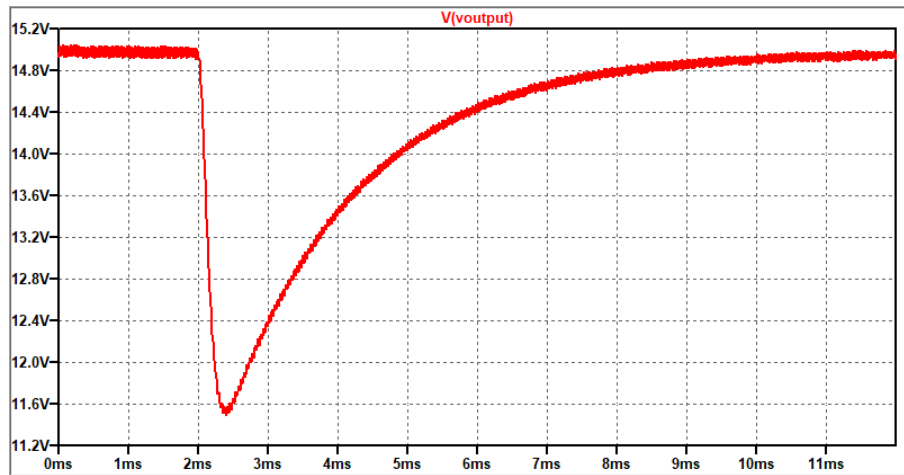


Figure 7.3.5: Input change line regulation

Fig 7.3.5 shows that the line regulation is below 2%, the output goes back to 15V after the line regulation, and it continues its operation. The transient is stable and we observe an overshoot around the regulation time. Therefore, our compensator design is valid. Let's now look at the load regulation.

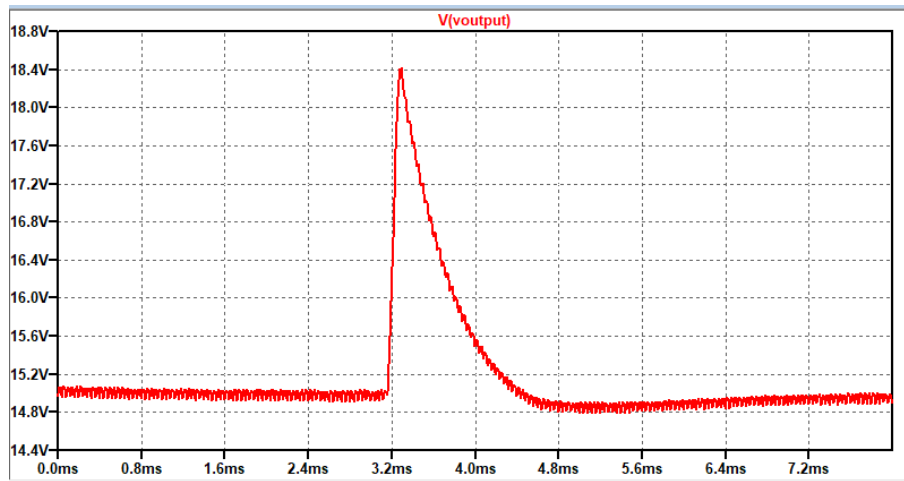


Figure 7.3.6: Load change, load regulation

Again, in the Fig 7.3.6, we can observe that the load regulation is less than 2%. In this case at 3ms, we increased the load from 0.32A, to 3.2A (full load) and we can see that after the transient our load regulation is as expected. We have some overshoot during the transient.

In this part, we designed our compensator and now we have a closed loop operation. The converter is stable and line, load regulations are below 2 %.

8 Efficiency and Thermal Analysis

8.1 Efficiency Analysis

In the project, the converter is non-ideal, and there are losses expected to be. Now, analytically, one by one, we are going to cover the losses on the circuit.

Capacitor ESR Losses

Over the capacitor, the current that will flow is the amount of inductor current ripple. So, the average current over the capacitor is

$$I_c = \frac{\Delta I_L T_s}{8} = 0.31A \quad (42)$$

Easily, the loss on the ESR of the capacitor is:

$$P_{esr,loss} = 0.31^2 * 0.003 = 0.3mW \quad (43)$$

It is a quite low value because we have chosen a ceramic capacitor.

Inductor ESR Losses

Over the inductor, the current flowing is 3.2A since output current is equal to inductor average current.

$$P_{L,loss} = 3.2^2 * 0.06 = 0.61W \quad (44)$$

Diode Losses

Over the diodes, inductor current is flowing. So, easily:

$$P_{D,loss} = 0.7 * 3.2 = 2.24W \quad (45)$$

MOSFET Loss

Over the MOSFET, the loss at 10A current is given in the datasheet as 2.4W. We are going to use this value:

$$P_{MOSFET} = 2.4W \quad (46)$$

Transformer Loss

At the primary side:

$$P_{pri} = 0.033 * 2^2 = 0.13W \quad (47)$$

At the secondary side:

$$P_{sec} = 3.2^2 * 0.045 = 0.46 \quad (48)$$

At the third winding

$$P_{third} = 0.22^2 * 0.33 = 0.016W \quad (49)$$

For the core loss, we should calculate the loss:

Using the Magnetics R Material loss calculator, we have $124mW/cm^3$ loss in the core. Our core has a volume of $5.6 * 2 = 11.2cm^3$

$$P_{core} = 0.124 * 11.2 = 1.4W \quad (50)$$

Total Loss

Total loss over the circuit is ignoring the leakage inductance:

$$P_{total} = 0.003W + 0.61W + 2.24W + 2.4W + 0.13W + 0.46W + 0.016W + 1.4W = 7.3W \quad (51)$$

Efficiency

Efficiency, ignoring the loss around the snubber:

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{48W}{48W + 7.3W} = \frac{48W}{55.3W} = 86.7\% \quad (52)$$

When, we simulate the circuit without using the snubber circuit the resultant efficiency is:

$$\eta_{sim} = \frac{P_{out}}{P_{in}} = \frac{48W}{52.12W} = 92\% \quad (53)$$

However, this value does not include the core loss. When we analytically add the core loss on it!

$$\eta_{total} = \frac{48W}{54.62W} = 87.8\% \quad (54)$$

Analytical calculations and simulation results are so similar!!

When we think of the snubber circuit, we can see that the average current around the snubber is:

$$I_{snubber} = \frac{0.1}{2} = 0.05A \quad (55)$$

$$P_{snubber} = 0.05^2 * 1250 = 3.1W \quad (56)$$

So, efficiency including the snubber is:

$$\eta_{sn,total} = \frac{48W}{59W} = 81\% \quad (57)$$

In the simulations, the efficiency simulated is 79%. We can say that we have an efficiency of 80% including the snubber circuit, leakage inductance, all ESR values and MOSFET, diode losses. This is a good efficiency for a forward converter.

8.2 Thermal Analysis

Losses on semiconductors are calculated in the previous subsection. By looking at their values and the thermal resistances of these components, we can have an idea if the temperature of these devices are within the operating range. Heatsinks can be used to cool them down. A heatsink suggestion will be made for the components in this section.

MOSFET

Loss on MOSFET is calculated as 2.4 W. Thermal resistance is obtained from the datasheet. Two values are given based on the mounting specification of the device. If a copper pad is built under it the thermal resistance decreases significantly but that was not the practice in our design.

Normally, thermal resistance of the MOSFET is given as $113^{\circ}C$. Considering that the device can work properly up to 150 , a heatsink is definitely required. Junction to case thermal resistance of the MOSFET is

$$R_{jc} = 1.1^{\circ}C/W$$

A heatsink as small as possible is chosen from DigiKey website. Datasheet can be found [here](#). It is cheap yet efficient. Thermal resistance value for the heatsink is

$$R_{sink} = 25.9^{\circ}C/W$$

Assuming that the ambient temperature is $25^{\circ}C$, operating temperature for the MOSFET junction can be found as follows.

$$T_{op} = T_{amb} + P_{loss} * (R_{jc} + R_{sink}) \implies T_{op} = 25 + 2.4 * 27 \approx 90^{\circ}C$$

This value is reasonable for our device and operation can continue safely with no problems.

Diodes

From the datasheet, loss is obtained as 2.24 W on diodes. This value is very close to that of MOSFETs. Thermal resistance of diode is obtained from the datasheet as

$$R_{jc} = 3^{\circ}C/W$$

Same heatsink can be used for the diodes as well. Similar calculation yields nearly the same result.

$$T_{op} = T_{amb} + P_{loss} * (R_{jc} + R_{sink}) \implies T_{op} = 25 + 2.24 * 28.9 \approx 90^{\circ}C$$

We can say that with the suggested heatsink, semiconductors can operate at temperatures around 90. Switching losses are not included in the calculations since switching frequency is relatively low, but the margin is high enough to compensate for them as well.

9 PCB Design

A PCB design is done for the converter, as requested by the recent changes in the hardware project. An open source PCB design tool, KiCad is used for the design. Lots of schematic symbols and footprints created by the users were available online. The transformer model is created by the team only.

9.1 Feedback Controller

To keep the voltage constant at 15V and to satisfy the line/load regulations, instead of the previously designed compensator, an analog IC controller is implemented on PCB. A very popular PWM controller IC for power supplies, **TL494** by *Texas Instruments* is chosen. Additional features comes with it makes it a favorable choice and in this section, some of them that are implemented in our design are to be presented.

Pin configuration of the module can be seen at Fig 9.1.1

**D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)**

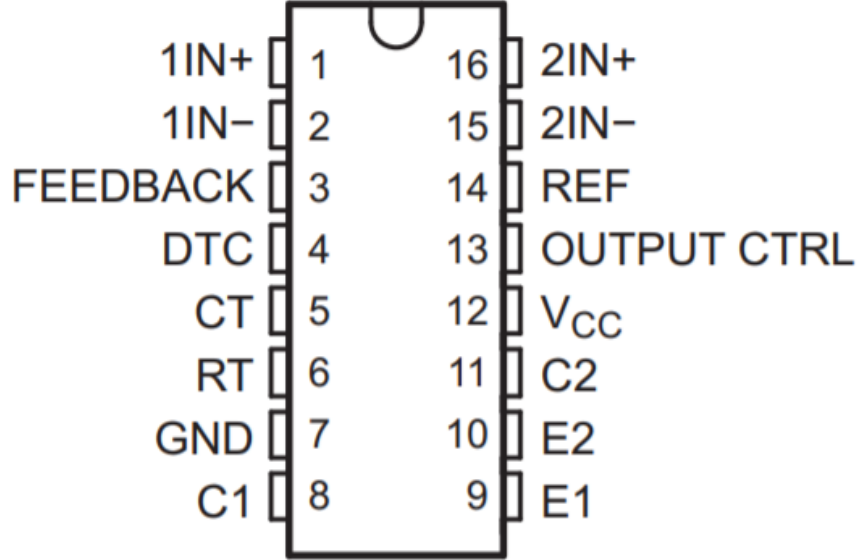


Figure 9.1.1: Pin Configuration for TL494

Powering Up TL494

To power up the module properly, a DC-DC converter is used. Input voltage to TL494 is set to 12 V. A DC-DC converter module by *Artesyn Inc.*, ATA00B36S-L is used. It can supply 3W of power at 12 V from an input between 18-75 V. Our input voltage to the system falls in its operation range, therefore this module can be used with no problems. Datasheet regarding this module can be found [here](#).

Basic Wiring For the wirings described as of this subsection, the application note by the TI is used. [5] TL494 is able to drive two switches together, but only one of the outputs is to be used in our project. First of all, the switching frequency of the module should be set. It is done by a simple RC circuit connected to pins 5 and 6. Internally it connects to the oscillator of the module and sets the frequency. Switch frequency is 25 kHz in our design.

$$f_{switch} = \frac{1}{R_T C_T}$$

Standard values are chosen for the components and $f_{switch} \approx 25.9kHz$ is achieved.

$$R_T = 8.2 k\Omega$$

$$C_T = 4.7 nF$$

One of the error amplifiers in the module is for regulating the output voltage. The working principle is simple. Inverting input is fed by a constant voltage value from the voltage reference of the module. 2.5 V is chosen for this. And the non-inverting input is fed from the output voltage of the converter. A schematic is given in Fig 9.1.2.

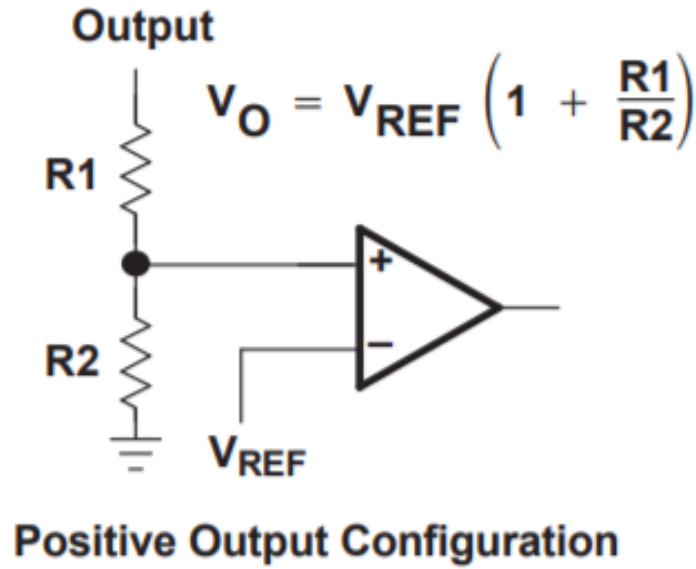


Figure 9.1.2: Output Voltage Regulation by TL494

Output voltage of the converter is 15V, therefore the voltage divider resistances are chosen as follows.

$$R_1 = 10 k\Omega$$

$$R_2 = 2 k\Omega$$

Amplifier gain is increased to 101 with a simple feedback loop formed between pins 2 and 3, inverting input and output of the amplifier respectively. Two resistors with ratings $51k\Omega$ and $510k\Omega$ are used to achieve this.

Current Limitation

A second error amplifier is reserved for output current limitation. When the output current goes beyond the adjusted value, the gate signal to the converter is cut therefore a short-circuit protection is implemented by the control circuitry.

Again, voltage reference output of the controller is fed to the inverting input of the current error amplifier. Voltage is set to 1V here. The current limit here is chosen as 5A in our application. Therefore, a really small resistor, referred to as R_{13} in Fig 9.1.3, is connected in series with the load. In our application it is chosen as 0.2Ω .

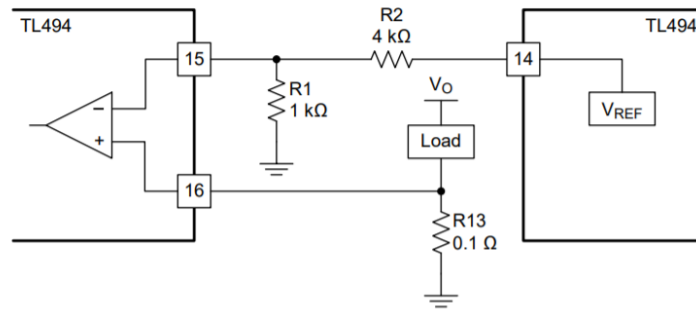


Figure 9.1.3: Short Circuit Protection by TL494

Soft Start Application

There is only one switching element in our design, therefore the dead time application is not needed. Nevertheless, a soft starting mechanism is added. The wiring can be seen at Fig 9.1.4.

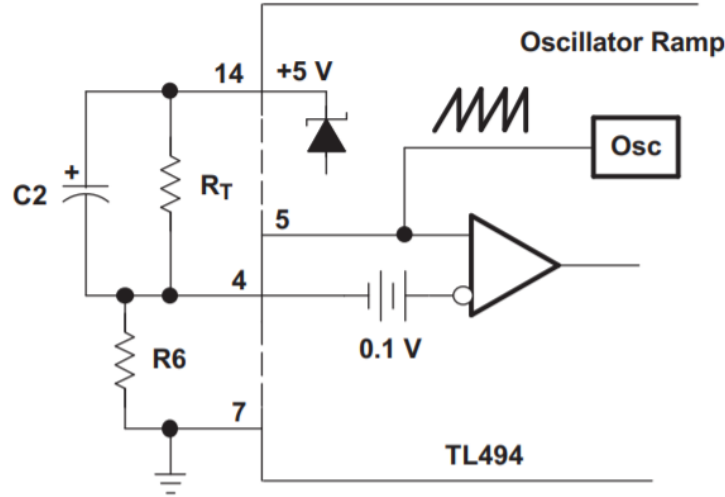


Figure 9.1.4: Soft Start with TL494

At the beginning of the regulation, C_2 capacitor charges through R_6 and by this way, the output pulse slowly increases till the control loop takes command. Considering R_6 is about one tenth of R_T resistor, which corresponds to a $1k\Omega$ resistance, the capacitor value can be calculated as follows. 50 cycles is chosen for the soft start time.

$$C_2 = \frac{\text{Soft - start duration}}{R_6} = \frac{40\mu s * 50}{1k\Omega} \approx 2.2\mu F$$

Gate Driver

To ensure electrical isolation between input and output sections of the converter, an optocoupler is to be used to drive the switching element. Our choice for this element is **TLP250** by *Toshiba*. It is a familiar IC for us, since it is used previously on the hardware project of EE463. A separate power supply is needed to drive the gate driver, therefore there are two power input pin pairs to the converter : one for the main supply and for the gate driver.

9.2 Schematic

A schematic is the first step to create a PCB. Kicad's "Eeschema" tool is used for this means. Generic symbols for diodes, inductors and such are used. Semiconductor symbols were available at the library. The symbol created for the three-winding transformer can be seen at Fig 9.2.1.

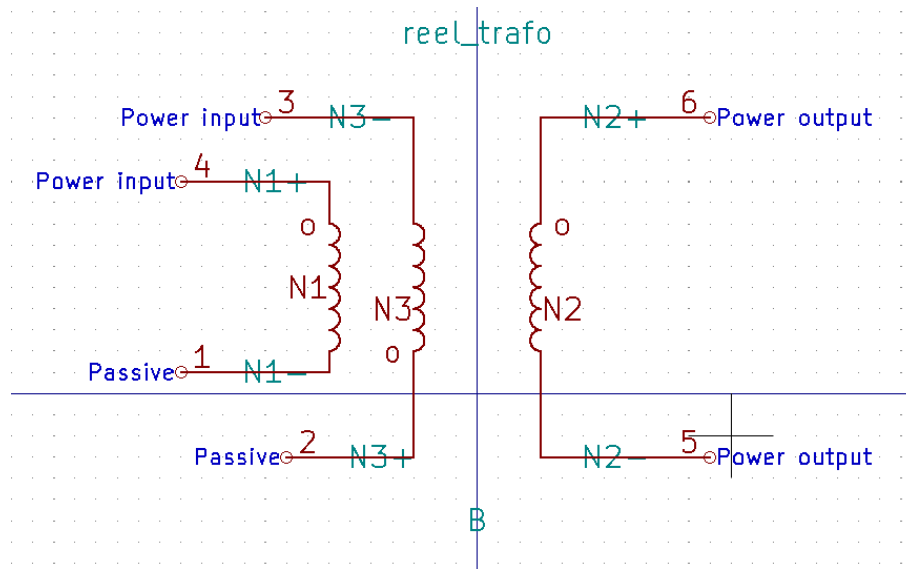


Figure 9.2.1: Schematic Symbol for Transformer in KiCad

Necessary wirings for TL494 are done as told in previous subsection. DC-DC Converter is added. Resulting schematic can be seen at Fig 9.2.2.

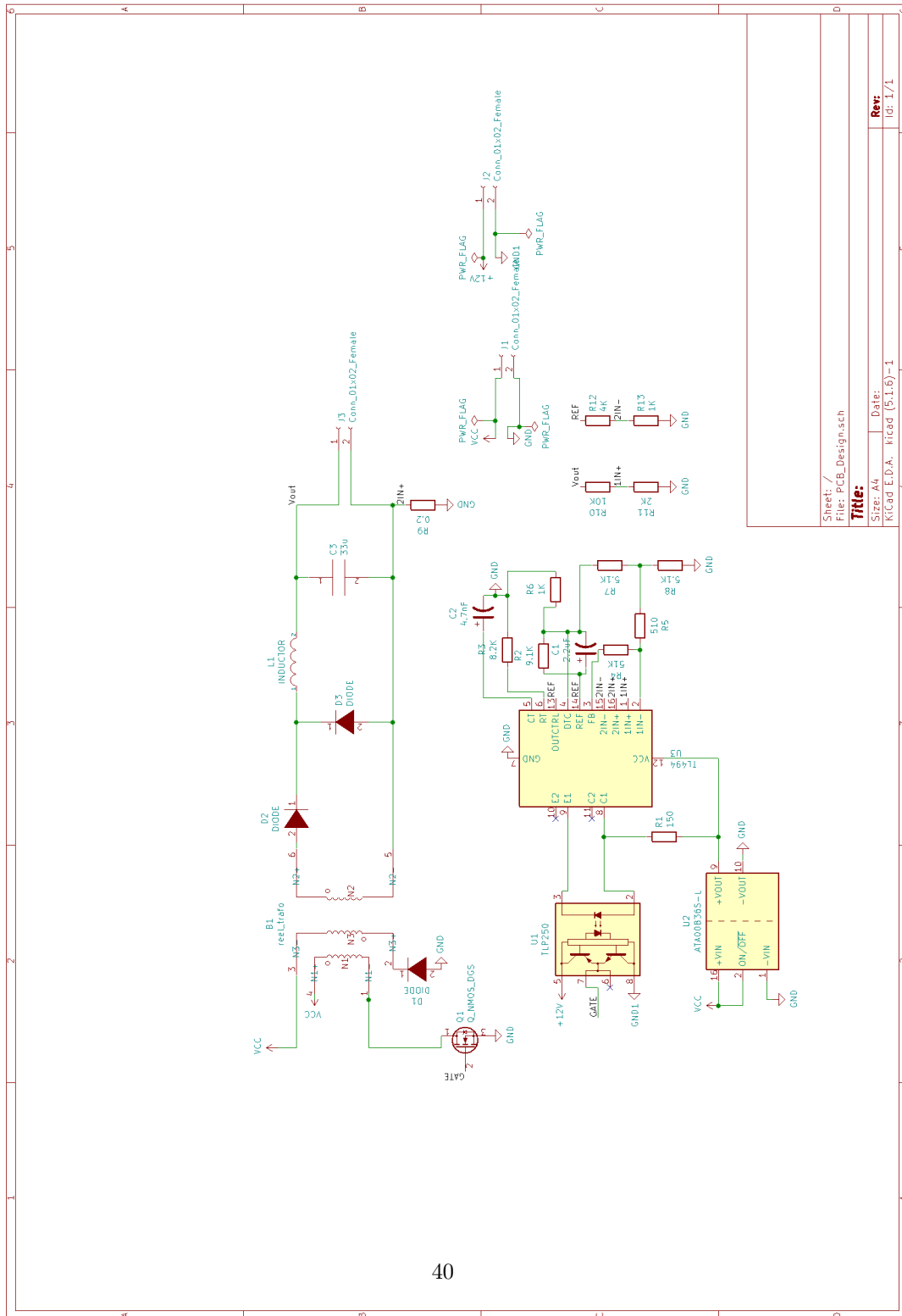


Figure 9.2.2: Converter Circuit Schematic in KiCad

9.3 Footprints

After the schematic is completed, components should be annotated and footprints should be assigned to each one of them. The packages are matched with each component chosen. The list for the components used in the PCB Design and the corresponding footprint selections can be seen in Fig 9.3.1.

Symbol : Footprint Assignments		
1	B1 -	reel_trafo : Transformer_THT:trafo
2	C1 -	2.2uF : Capacitor_SMD:C_1206_3216Metric_Pad1.42x1.75mm_HandSolder
3	C2 -	4.7nF : Capacitor_SMD:C_1206_3216Metric_Pad1.42x1.75mm_HandSolder
4	C3 -	33u : Capacitor_SMD:C_1206_3216Metric_Pad1.42x1.75mm_HandSolder
5	D1 -	DIODE : Package_TO_SOT_SMD:TO-277A
6	D2 -	DIODE : Package_TO_SOT_SMD:TO-277A
7	D3 -	DIODE : Package_TO_SOT_SMD:TO-277A
8	J1 - Conn_01x02_Female :	Connector:Banana_Jack_2Pin
9	J2 - Conn_01x02_Female :	Connector:Banana_Jack_2Pin
10	J3 - Conn_01x02_Female :	Connector:Banana_Jack_2Pin
11	L1 -	INDUCTOR : Inductor_THT:L_Toroid_Horizontal_D32.5mm_P28.90mm_Bourns_2300
12	Q1 -	Q_NMOS_DGS : Package_TO_SOT_SMD:PQFN_8x8
13	R1 -	150 : Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal
14	R2 -	9.1K : Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal
15	R3 -	8.2K : Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal
16	R4 -	51K : Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal
17	R5 -	510 : Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal
18	R6 -	1K : Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal
19	R7 -	5.1K : Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal
20	R8 -	5.1K : Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal
21	R9 -	0.2 : Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal
22	R10 -	10K : Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal
23	R11 -	2K : Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal
24	R12 -	4K : Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal
25	R13 -	1K : Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal
26	U1 -	TLP250 : Package_DIP:DIP-8_W7.62mm
27	U2 -	ATA00B36S-L : Converter_DCDC:Converter_DCDC_Artesyn_ATA_SMD
28	U3 -	TL494 : Package_DIP:DIP-16_W7.62mm

Figure 9.3.1: Footprint List in KiCad

A footprint for the transformer was not readily built, since the transformer is to be designed by the team. Only the transformer's footprint is custom made. The dimensions of the chosen core is taken into consideration. 6 pads are formed for each ends of three windings. The resulting footprint can be seen in Fig 9.3.2.

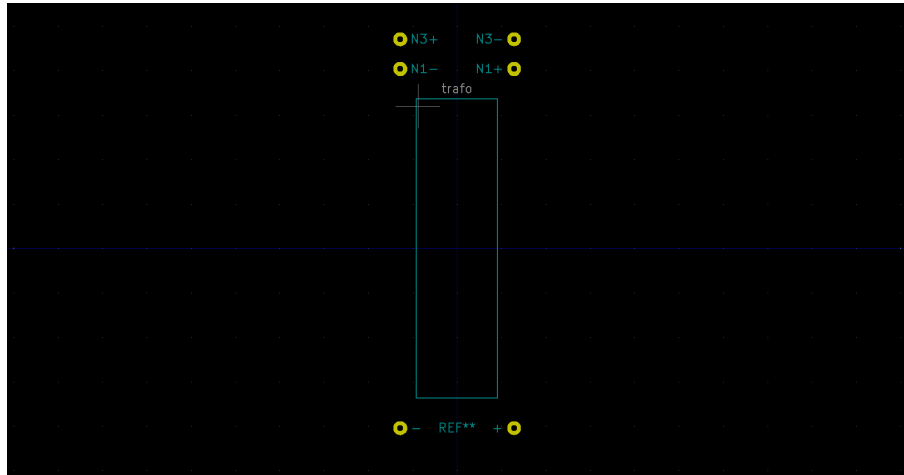


Figure 9.3.2: Footprint for Transformer

9.4 PCB View

After all these arrangements are made, the PCB design process can begin. There are some basic rules to that, although we are not so experienced in PCB design we tried to apply all we know.

First of all, traces should not make perpendicular turns. This can cause serious EMI problems and should be avoided all the times. Second thing that is considered with utmost attention is the trace widths. In the converter, currents can reach up to 3-4 A during operation. A simple PCB trace width calculator is used to make sure that our design can carry such currents. For control parts, default trace width is used but at the input and output stages, trace widths are 22 and 32 mils, respectively. It is assumed that $2oz/ft^2$ of copper will be used.

In order to make connections easier and to use less vias, through hole resistors are used. This can be changed and compactness could be improved but overall, the design looked neat enough to us. Some components are flipped when necessity occurred. 3-4 vias are used as well.

The PCB View of the design can be seen in Fig 9.4.1 at the next page. The copper filling for the back layer is also done but to make components and connections more visible, it is not given in the following representation.

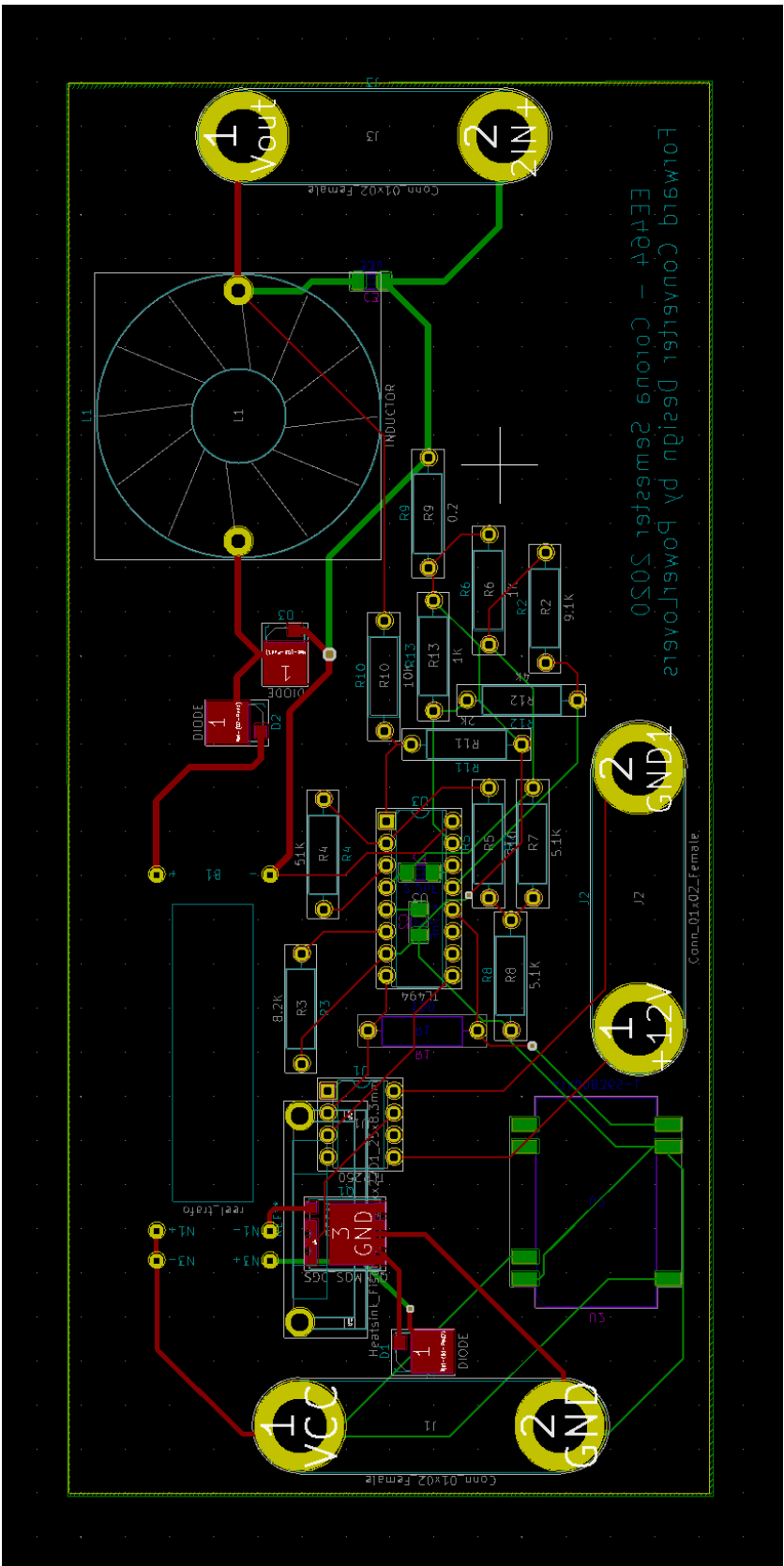


Figure 9.4.1: PCB Design in KiCad

9.5 3-D View

Transformer and connector models are absent but a 3-D View of the project is presented below.

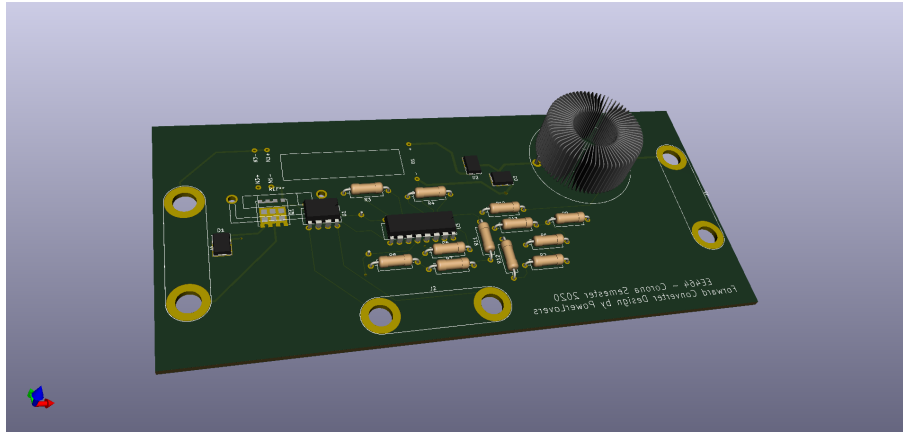


Figure 9.5.1: 3-D View of the PCB, Top Layer

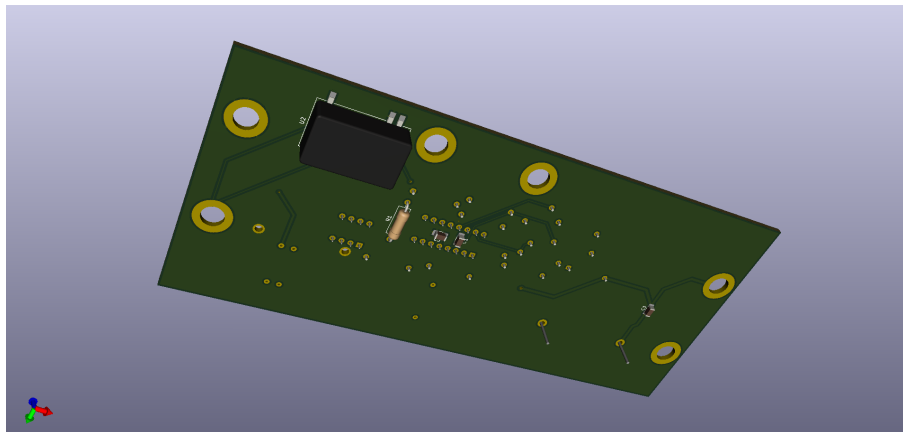


Figure 9.5.2: 3-D View of the PCB, Bottom Layer

9.6 Arrangement for 1000 Pieces from PCBWay

When the design is completed, Gerber files are obtained and the board is ready for production. As suggested in the GitHub page, PCBWay has been the choice for producing the board. Price for 5 pieces, which is the minimum number allowed is calculated as **\$ 63** and for 1000 pieces it is **\$ 1320**.

Component prices are given in detail in the Bill of Materials (BOM) presented in the following pages. Overall manufacturing costs are calculated from BOMs.

- One piece production cost : **\$52.43**
- 1000 piece production, cost per piece : **\$28.95**

It can be easily seen that mass production is more profitable. For each cases BOMs are presented in the Appendix. Original Excel files can be found at GitHub repository.

10 Conclusion

In this report, we have introduced PowerLovers forward converter closed loop design, PCB implementation, and analysis in means of efficiency, thermal durability, and affordability. We included non-ideal simulations with supported analysis and calculations. We strongly believe that this project allowed us to understand more about all the theoretical knowledge we have gained so far. Also, by doing research, we have met advanced information about converters, snubber design, cores, efficiency, switches, stability... It was a great opportunity to work on such a project all together. Apart from the project, it is also essence of power electronics to understand how to design from beginning to the end considering all the relations between the electronics and nature itself. We hold on that we are now more experienced designing converters!

11 Appendix : Bill of Material Files

Reference	Quantity	Value	Footprint	Price	
B1		1 trafo	Transformer_THT:trafo	\$	4.00
C1		1 2.2uF	Capacitor_SMD:C_1206_3216Metric_Pad1.42x1.75mm_HandSolder	\$	0.29
C2		1 4.7nF	Capacitor_SMD:C_1206_3216Metric_Pad1.42x1.75mm_HandSolder	\$	0.10
C3		1 33u	Capacitor_SMD:C_1206_3216Metric_Pad1.42x1.75mm_HandSolder	\$	1.20
D1 D2 D3		3 DIODE	Package_TO_SOT_SMD:TO-277A	\$	0.62
J1 J2 J3		3 Conn_01x02_Female	Connector:Banana_Jack_2Pin	\$	1.44
L1		1 INDUCTOR	Inductor_THT:L_Toroid_Horizontal_D32.5mm_P28.90mm_Bourns_2300	\$	2.83
Q1		1 Q_NMOS_DGS	Package_TO_SOT_SMD:PQFN_8x8	\$	1.82
R1		1 150	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	0.10
R10		1 10K	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	0.10
R11		1 2K	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	0.10
R12		1 4K	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	0.63
R2		1 9.1K	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	0.63
R3		1 8.2K	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	0.10
R4		1 51K	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	0.10
R5		1 510	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	0.10
R6 R13		2 1K	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	0.10
R7 R8		2 5.1K	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	0.10
R9		1 0.2	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	3.08
U1		1 TLP250	Package_DIP:DIP-8_W7.62mm	\$	1.15
U2		1 ATA00B36S-L	Converter_DCDC:Converter_DCDC_Artesyn_ATA_SMD	\$	16.39
U3		1 TL494	Package_DIP:DIP-16_W7.62mm	\$	0.53

Total Price :

PCB Price

Overall

<https://www.pcbway.com/QuickOrderOnline.aspx>

Core Eq

<https://www.digikey.com/product-detail/en/tdk-electronics-inc/B66381G0000X172/495-76794-ND/>

Around 2 dollars

Cable

AWG #22 - Around 2 dollars

Total Price	Datasheet
\$ 4.00	https://www.mag-inc.com/Media/Magnetics/Datasheets/0F43515EC.pdf
\$ 0.29	https://www.digikey.com/product-detail/en/murata-electronics/GRM155R60J225ME15D/490-4519-1-ND/1033278
\$ 0.10	https://www.digikey.com/product-detail/en/murata-electronics/GRM155R71H473KE14D/490-10702-1-ND/5251398
\$ 1.20	https://product.tdk.com/info/en/documents/chara_sheet/C3216JB1E336M160AC.pdf
\$ 1.86	https://www.digikey.com/product-detail/en/vishay-semiconductor-diodes-division/SS5P10-M3-86A/SS5P10-M3-86AG
\$ 4.32	https://www.digikey.com/product-detail/en/cinch-connectivity-solutions-johnson/108-0901-001/J150-ND/5928
\$ 2.83	https://www.digikey.com/product-detail/en/bourns-inc/2300LL-681-H-RC/2300LL-681-H-RC-ND/725890
\$ 1.82	https://www.digikey.com/product-detail/en/on-semiconductor/FDMS86255/FDMS86255TR-ND/4555505
\$ 0.10	https://www.digikey.com/product-detail/en/stackpole-electronics-inc/CF14JT150R/CF14JT150RCT-ND/1830603
\$ 0.10	https://www.digikey.com/product-detail/en/stackpole-electronics-inc/CF14JT10K0/CF14JT10K0CT-ND/1830374
\$ 0.10	https://www.digikey.com/product-detail/en/stackpole-electronics-inc/CF14JT2K00/CF14JT2K00CT-ND/1830357
\$ 0.63	https://www.digikey.com/product-detail/en/vishay-dale/CMF554K0000FEBF/CMF554K0000FEBF-ND/3634189
\$ 0.63	https://www.digikey.com/product-detail/en/yageo/MFP-25BRD52-9K1/9-1KADCT-ND/2059152
\$ 0.10	https://www.digikey.com/product-detail/en/stackpole-electronics-inc/CF14JT8K20/CF14JT8K20CT-ND/1830372
\$ 0.10	https://www.digikey.com/product-detail/en/stackpole-electronics-inc/CF14JT51K0/CF14JT51K0CT-ND/1830392
\$ 0.10	https://www.digikey.com/product-detail/en/stackpole-electronics-inc/CF14JT510R/CF14JT510RCT-ND/1830343
\$ 0.20	https://www.digikey.com/product-detail/en/stackpole-electronics-inc/CF14JT1K00/CF14JT1K00CT-ND/1830350
\$ 0.20	https://www.digikey.com/product-detail/en/stackpole-electronics-inc/CF14JT5K10/CF14JT5K10CT-ND/1830367
\$ 3.08	https://www.digikey.com/product-detail/en/ohmite/15FR200E/15FR200E-ND/822920
\$ 1.15	http://toshiba.semicon-storage.com/info/docget.jsp?did=16821&prodName=TLP250
\$ 16.39	https://www.artesyn.com/power/assets/ata_series_ds_01apr2015_79c25814fd.pdf
\$ 0.53	http://www.ti.com/lit/ds/symlink/tl494.pdf

\$ 39.83

\$ 12.60

\$ 52.43

[/3914869](#)

Reference	Quantity	Value	Footprint	Price	
B1		1 trafo	Transformer_THT:trafo	\$	2.00
C1		1 2.2uF	Capacitor_SMD:C_1206_3216Metric_Pad1.42x1.75mm_HandSolder	\$	0.06
C2		1 4.7nF	Capacitor_SMD:C_1206_3216Metric_Pad1.42x1.75mm_HandSolder	\$	0.01
C3		1 33u	Capacitor_SMD:C_1206_3216Metric_Pad1.42x1.75mm_HandSolder	\$	0.38
D1 D2 D3		3 DIODE	Package_TO_SOT_SMD:TO-277A	\$	0.24
J1 J2 J3		3 Conn_01x02_Female	Connector:Banana_Jack_2Pin	\$	0.39
L1		1 INDUCTOR	Inductor_THT:L_Toroid_Horizontal_D32.5mm_P28.90mm_Bourns_2300	\$	2.30
Q1		1 Q_NMOS_DGS	Package_TO_SOT_SMD:PQFN_8x8	\$	1.82
R1		1 150	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	0.01
R10		1 10K	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	0.01
R11		1 2K	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	0.01
R12		1 4K	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	0.20
R2		1 9.1K	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	0.15
R3		1 8.2K	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	0.01
R4		1 51K	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	0.01
R5		1 510	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	0.01
R6 R13		2 1K	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	0.01
R7 R8		2 5.1K	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	0.01
R9		1 0.2	Resistor_THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	\$	1.49
U1		1 TLP250	Package_DIP:DIP-8_W7.62mm	\$	0.68
U2		1 ATA00B36S-L	Converter_DCDC:Converter_DCDC_Artesyn_ATA_SMD	\$	16.39
U3		1 TL494	Package_DIP:DIP-16_W7.62mm	\$	0.19

<https://www.pcbway.com/QuickOrderOnline.aspx>

Total Price :
PCB Price
Overall
Per Piece

Core Eq

<https://www.digikey.com/product-detail/en/tdk-electronics-inc/B66381G0000X172/495-76794-ND/>
Around 1 dollars

Cable

AWG #22 - Around 1 dollars

Total Price	Datasheet
\$ 2,000.00	https://www.mag-inc.com/Media/Magnetics/Datasheets/0F43515EC.pdf
\$ 61.00	https://www.digikey.com/product-detail/en/murata-electronics/GRM155R60J225ME15D/490-4519-1-ND/1033278
\$ 9.00	https://www.digikey.com/product-detail/en/murata-electronics/GRM155R71H473KE14D/490-10702-1-ND/5251398
\$ 380.00	https://product.tdk.com/info/en/documents/chara_sheet/C3216JB1E336M160AC.pdf
\$ 720.00	https://www.digikey.com/product-detail/en/vishay-semiconductor-diodes-division/SS5P10-M3-86A/SS5P10-M3-86AGI
\$ 1,170.00	https://www.digikey.com/product-detail/en/cinch-connectivity-solutions-johnson/108-0901-001/J150-ND/5928
\$ 2,300.00	https://www.digikey.com/product-detail/en/bourns-inc/2300LL-681-H-RC/2300LL-681-H-RC-ND/725890
\$ 1,820.00	https://www.digikey.com/product-detail/en/on-semiconductor/FDMS86255/FDMS86255TR-ND/4555505
\$ 7.30	https://www.digikey.com/product-detail/en/stackpole-electronics-inc/CF14JT150R/CF14JT150RCT-ND/1830603
\$ 7.30	https://www.digikey.com/product-detail/en/stackpole-electronics-inc/CF14JT10K0/CF14JT10K0CT-ND/1830374
\$ 7.30	https://www.digikey.com/product-detail/en/stackpole-electronics-inc/CF14JT2K00/CF14JT2K00CT-ND/1830357
\$ 200.00	https://www.digikey.com/product-detail/en/vishay-dale/CMF554K0000FEBF/CMF554K0000FEBF-ND/3634189
\$ 150.00	https://www.digikey.com/product-detail/en/yageo/MFP-25BRD52-9K1/9-1KADCT-ND/2059152
\$ 7.30	https://www.digikey.com/product-detail/en/stackpole-electronics-inc/CF14JT8K20/CF14JT8K20CT-ND/1830372
\$ 7.30	https://www.digikey.com/product-detail/en/stackpole-electronics-inc/CF14JT51K0/CF14JT51K0CT-ND/1830392
\$ 7.30	https://www.digikey.com/product-detail/en/stackpole-electronics-inc/CF14JT510R/CF14JT510RCT-ND/1830343
\$ 14.60	https://www.digikey.com/product-detail/en/stackpole-electronics-inc/CF14JT1K00/CF14JT1K00CT-ND/1830350
\$ 14.60	https://www.digikey.com/product-detail/en/stackpole-electronics-inc/CF14JT5K10/CF14JT5K10CT-ND/1830367
\$ 1,490.00	https://www.digikey.com/product-detail/en/ohmite/15FR200E/15FR200E-ND/822920
\$ 680.00	http://toshiba.semicon-storage.com/info/docget.jsp?did=16821&prodName=TLP250
\$ 16,390.00	https://www.artesyn.com/power/assets/ata_series_ds_01apr2015_79c25814fd.pdf
\$ 186.00	http://www.ti.com/lit/ds/symlink/tl494.pdf

\$ 27,629.00
 \$ 1,320.00
 \$ 28,949.00
 \$ 28.95

[3914869](#)

References

- [1] Transformer Design with Magnetics Ferrite Cores. [Online]. Available: <https://www.mag-inc.com/Design/Design-Guides/Transformer-Design-with-Magnetics-Ferrite-Cores>.
- [2] "AN-776 20 Watt Simple Switcher Forward Converter", 2020. [Online]. Available: <https://www.ti.com/lit/an/snva027a/snva027a.pdf?ts=1592752724490>
- [3] N. Mohan, T. M. Undeland, and W. P. Robbins, Power Electronics: Converters, Applications, and Design. Hoboken, NJ: John Wiley & Sons, 2003.
- [4] "Compensator Design Procedure for Buck Converter with Voltage-Mode Error-Amplifier", Infineon.com, 2020. [Online]. Available: <https://www.infineon.com/dgdl/an-1162.pdf?fileId=5546d462533600a40153559a8e17111a>.
- [5] Designing Switching Voltage Regulators With the TL494", 2020. [Online]. Available: <https://www.ti.com/lit/an/slva001e/slva001e.pdf?ts=1592314978873>