Ultra-Low Inductance Phase Leg Design for GaN-Based Three-Phase Motor Drive Systems

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***Abstract*— This paper presents an improved phase leg power loop design for enhance mode lateral structure Gallium Nitride (GaN) transistors. Static characterization results of a 650V/30A GaN transistor are presented. The gate driver circuit is designed based on the characterization results. In order to reduce current commutation loop inductance within the GaN phase leg, an improved power loop design with vertical structure is proposed for lateral structure GaN transistors. The control of Common Mode (CM) noise current propagation is also considered during the gate driver design by optimizing the power distribution and grounding structure of the gate driver and digital control circuits. By differentiating the propagation path impedance of digital control circuits and their power supply circuits, conductive CM noise can propagate through power supply path to protect the digital control circuits. The design is verified through experiments on a phase leg prototype which prove the effectiveness of the proposed phase leg on the overvoltage reduction during current transition along with less cross-coupling between power loop and gate loop compared with conventional lateral power loop design. Finally, a three phase motor drive system is designed and tested based on the proposed phase leg.**

Keywords—GaN HMET, Characterization, Gate Driver, EMI; Three phase motor drive

I. INTRODUCTION

Wide band-gap gallium nitride power switches outperform silicon counterparts in terms of switching speed and on-resistance, and therefore provide the potentials to improve the power density of various converters by shrinking the size of passive components and improving the power conversion efficiency. [1~6] For 600V rated power devices, the cascode structure has been dominant, however, it has issues with lower reliability and high common source inductance [7]. Recently, the enhancement mode lateral structure GaN HEMTs become commercially available.[8,9] These devices have small package with low packaging inductance which provides the potential of ultra-high switching speed for medium power applications (several kW) [9]. In such structures, current flows at near surface in the devices which enable the usage of Si substrates instead of GaN free standing substrates to reduce the cost of GaN devices. Moreover these devices are formed from non-doped AlGaN and GaN. Then, the lateral HEMTs have a low parasitic capacitance which means that these devices have both lower conduction losses and low switching losses, providing the potentials for ultra-high switching frequency in power conversions. However, fast switching also generates high dv/dt and di/dt in the system that requires an advanced isolation for gate driver circuits and improve power loop layout design to achieve proper EMI noise control and small parasitic inductance for both power loop and gate loop.[10]. In order to extract the full benefits from these the enhanced-mode lateral GaN devices, this paper presents an improved phase leg power loop design with vertical power loop structure and CM noise current propagation control for a 650V/30A enhancement mode GaN switch (GS66508) from GaN systems. The static characterization results are presented to verify the better performance of GaN switches compared with Si MOSFETs. Based on the static characterization results, a gate drive circuit design is presented considering the CM noise current propagation control by controlling the propagation path impedance of digital control circuits and their power supply circuits to control more conductive CM noise propagate through power supply path to protect the digital control circuits. Moreover, a vertical power loop layout is proposed to minimize the current commutation loop inductance. The design is verified through experiments on a phase leg prototype which prove the effectiveness of the proposed phase leg on the overvoltage reduction during current transition along with less cross-coupling between power loop and gate loop compared with conventional lateral power loop design. Finally, a three phase motor drive system is designed and tested based on the proposed phase leg.

II. STATIC CHARACTERIZATION GAN TRANSISTORS

In order the better performance of GaN switches compared with Si MOSFETs, A static characterization test is conducted for the 650V/30A enhancement mode GaN switches (GS66508) from GaN systems with curve tracer. Figure 1(a) shows the static characterization results of device I-V characterization under different gate voltages, which indicates that the channels is fully enhanced at gate voltage above 7 V. since the maximum gate voltage rating is 10V from the device datasheet, device driving voltage is set to be 7V in the gate driver design. The test results also indicate that

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the switch can work at reverse conduction mode and the characteristics are almost the same with normal conduction mode, therefore there is no need for anti-parallel diodes. Since negative gate voltage will increase the on state voltage drop in the reverse conduction mode which will increase the conduction loss significantly, negative gate voltage is not implemented in the gate driver. Figure 1(b) shows the capacitance of the devices changes with drain-source voltage, where both the input and output capacitances of the devices are much lower than those of the silicon devices, which indicate that GaN switches have faster gate charge and lower capacitor charge loss during switching. However the fast switching generates high dv/dt and di/dt in the system that requires an advanced layout design to achieve proper EMI noise control and small parasitic inductances for both power loop and gate loops. Based on the static characterization results, a phase leg structure as shown in figure 2 is studied.

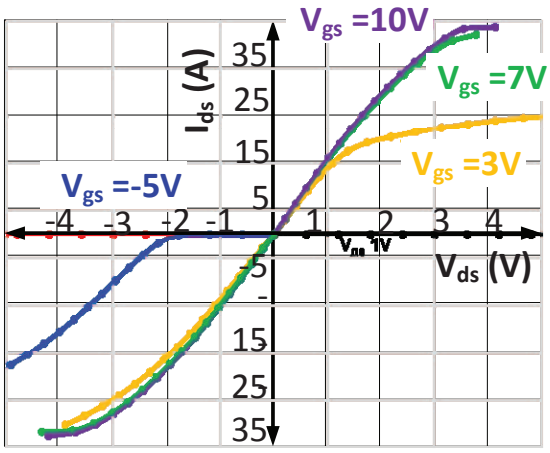

Figure 1(a): I-V characteristics

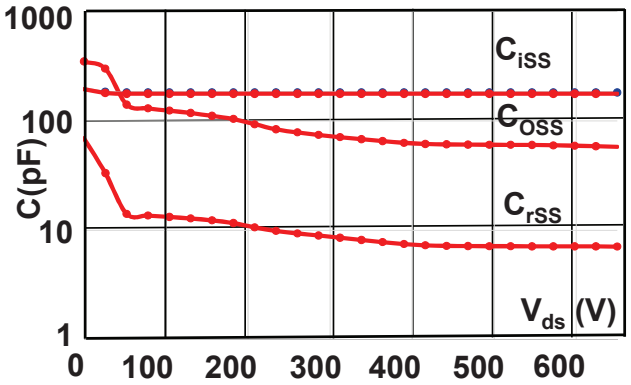

Figure 1 (b): Capacitance characteristics

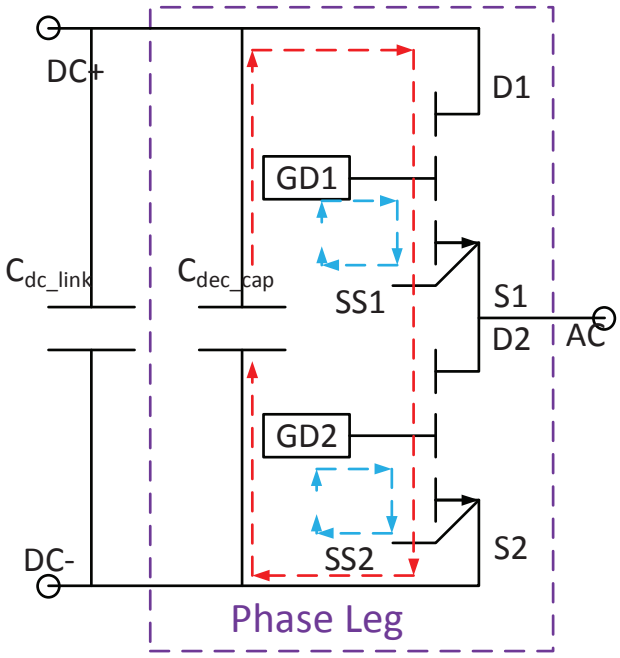

Figure 2: GaN Phase leg configuration

III. Gate Driver Circuit Design with CM Noise Propagation Control

Isolation is necessary to block the high frequency noise generated by the high dv/dt in the power stage. Especially for GaN devices with fast switching speed, where the voltage slew rate can be as high as hundreds of volts per nanosecond and the harmonic frequency related with the turning-on and turning-off of the devices may be up to several hundreds of mega-hertz, these high dv/dt can generate high frequency EMI noise that propagates through the parasitic capacitance to the whole system including the power stage and control circuits and bring electromagnetic compatibility (EMC) issues to the system, which needs to be well controlled to avoid its interference with the digital control circuits, especially the propagation of the common mode EMI noise current. With this consideration the gate driver circuit is designed with digital isolators SI8410 from Siliconlabs to provide high isolation between logic control circuits and power circuits, a commercial gate driver chip IXDN609 from IXYS is implemented as the gate driver and current booster. A 5.2kVdc rated isolated power supply MEJ2S1509SC from Murata is implemented to provide isolation between gate driver power supply and the power circuits. Two non-isolated linear regulators are used to provide the +7V for gate driver and +5V for digital isolator. The schematic of the gate driver design is shown in Figure 3.

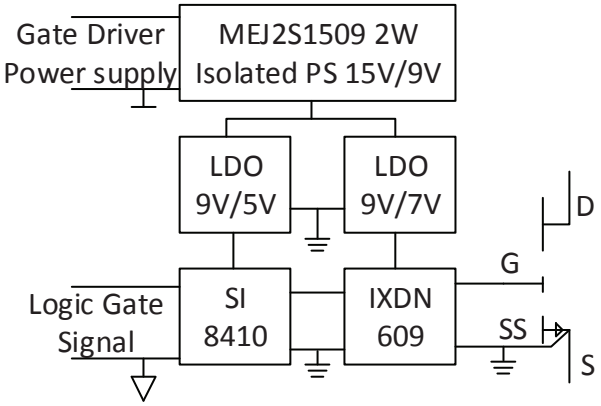

Figure 3 Schematic of gate driver circuit design

In order to improve the electromagnetic compatibility of the system, CM noise propagation is controlled by differentiating the propagation path impedance of digital control circuits and their power supply circuits. The block diagram is shown in Figure 4, where digital isolators with ultra-low isolation capacitance are selected for both top and bottom devices to provide good isolation for high frequency EMI noise. The power supply for the digital control circuit is selected with ultra-low isolation capacitance to create a high impedance path to reduce CM noise current through the digital control circuits. Meanwhile the gate driver power supply is selected with relatively higher isolation capacitance to create a lower impedance path to bypass and therefore reduce the CM noise current through the digital control circuits, since the gate drive power supply have higher susceptibility to the noise.

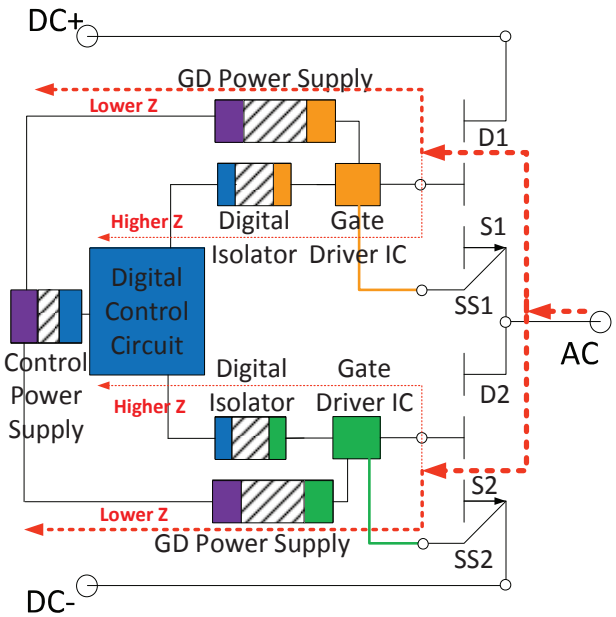

Figure 4: Gate driver circuit design with CM noise propagation control

IV. Vertical Power Loop Design for Loop Inductance Minimization

The fast switching of GaN devices also generates high di/dt in the power loop, if the parasitic loop inductance is too high, the overvoltage during switching will also be high and it will increase the voltage stress on the devices which degrade the maximum bus voltage and prevent further increase of the switching speed. Therefore it is very important to design the power stage layout with low loop inductance. [8] Figure 5 shows the reference layout recommended by the devices vendors [11] and Figure 5(b) shows the power loops and gate loops in the reference design. The current need to propagate through the two lateral located devices and create a relatively high current loop with higher parasitic loop inductance. Besides, the gate loop and current loop is parallel which will increase the near field coupling between the power loop and the gate loop. Moreover, the DC input and AC output are coupled together which increases the interaction between input and output.

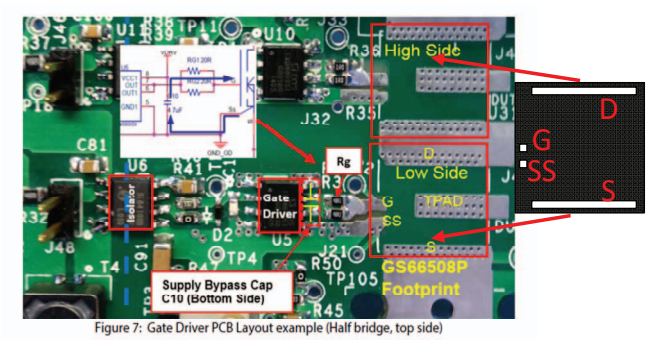

Figure 5(a) Reference layout

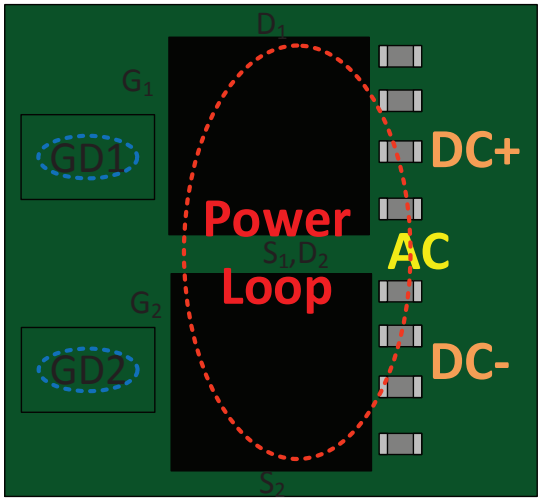

Figure 5(b) Reference design power loop

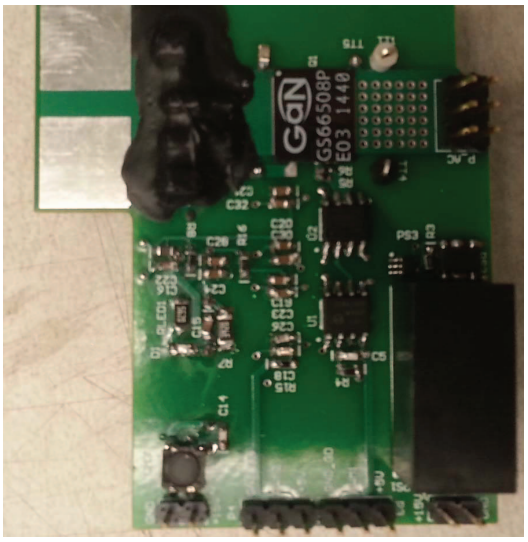

Figure 6(a): Proposed phase leg design

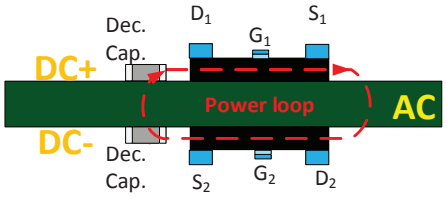

Figure 6(b): Proposed design power loop (side view)

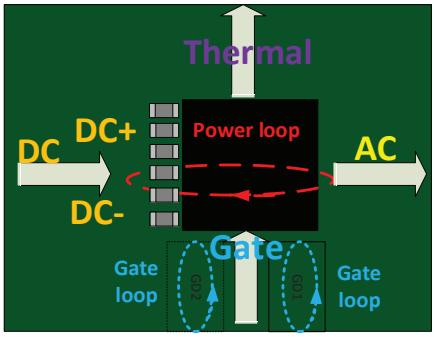

Figure 6(c): Proposed design power loop (top view)

Table I Parasitic inductance comparison

	Reference Lateral Layout	Proposed Vertical Layout
Power Loop	28.7 nH	3.1 nH
Gate Loop	0.4 nH	0.2 nH

To solve these issues, a vertical power loop design is proposed and shown in Figure 6 where GaN devices are mounted in both sides of the PCB board. Figure 6(b) (c) shows the current loop and gate loop in the proposed design, where the power loop is folded to increase the mutual coupling between the current through the two devices and the decoupling capacitor is mounted near the devices as close as possible, therefore the current commutation loop inductance can be reduced significantly compared with the reference design, For lateral GaN devices, the current conducts along the devices shown as in Fig. 6(b) therefore the proposed vertical layout is more suitable for lateral devices compared with vertical devices. Table I shows the parasitic loop inductance estimation through Q3D extraction which shows that the power loop inductance is reduced 10 times compared with the reference layout design. Figure 6(c) also indicates that the gate loop is perpendicular to the current loop which can also reduce the near field coupling due to the high di/dt in the current commutation loop. Moreover, the DC input and AC output terminals are separated in the proposed layout, which reduces the interaction between input and output noise. The thermal design is more challenging in the proposed layout since the devices are overlapping each other and the heat has to dissipate along the PCB board. The heat dissipation can be improved by implementing the power loop with direct bonded copper (DBC) or using the newly-released top-cooled devices.

V. Experimental Verification

Two phase legs are implemented with 650V/30A GaN HEMT (GS66508P from GaN systems) following the reference layout (Fig.5(a)) and the proposed design layout (Fig. 6(a)) respectively. A standard double pulse test is conducted for both phase legs with the same gate resistance to verify the proposed phase leg design. Figure 7 shows the test results of the bottom device at 400V dc link voltage and 32A inductor peak current with the proposed phase leg design. Table II shows the comparison of the peak device voltage during turning-off and peak gate voltage during turning-on. For reference design, the peak voltage is already near 600V which prevent further increase of the device switching speed however, the proposed phase leg layout can reduce voltage overshoot during turning-off by 100V, therefore the device can switch faster with no issues.

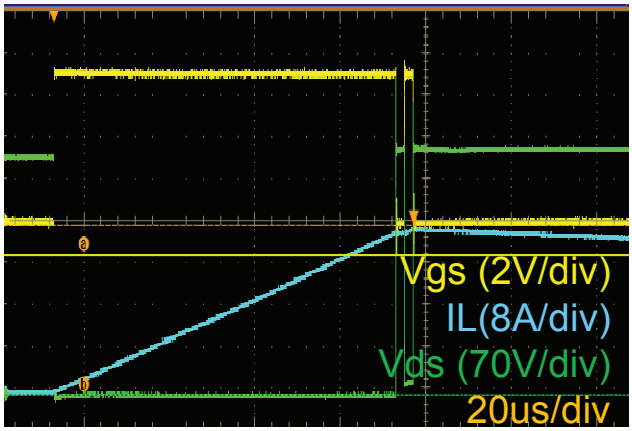

Figure 7(a): Double pulse test results

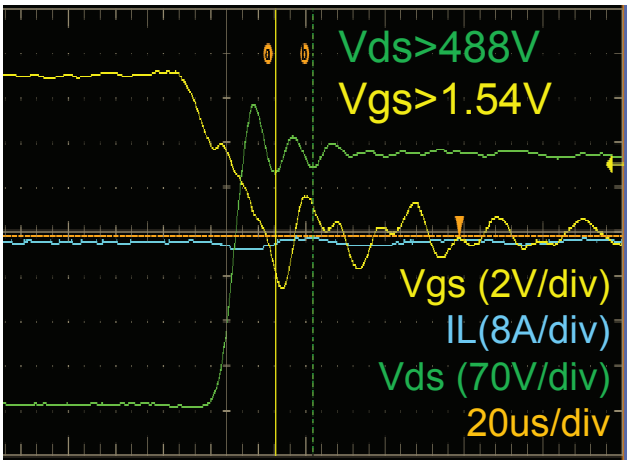

Figure 6(b): Turning-off

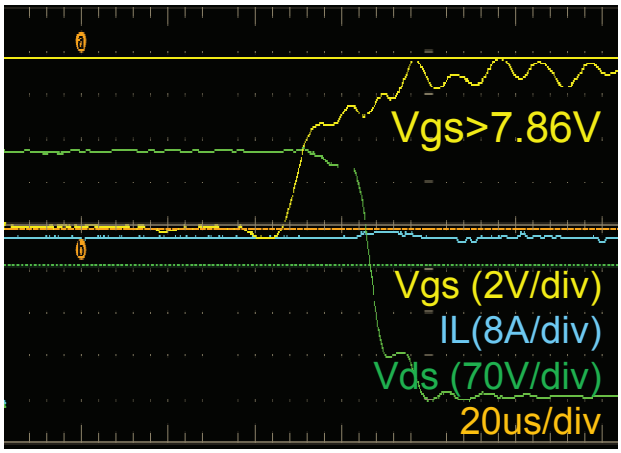

Figure 6(c): Turning-on

Table II Double pulse test comparison

	Vds_max	Vgs_max
Reference Design	588 V	8.59V
Proposed Design	488 V	7.88V

The phase legs are designed and implemented as a power electronics building block (PEBB), three phase legs are assembled to a custom designed dc link baseboard with dc bulk capacitors and distributed dc link capacitors to form a three phase motor drive system. Figure 7(a) shows the implemented GaN based three phase voltage source inverter (VSI) and figure 7(b) shows the structure of the test circuit. Where a RL load is used to simulate a motor load. The test conditions are: dc link voltage Vdc= 270 V; switching frequency fs = 100 kHz, fundamental frequency f1= 400 Hz; Load inductance L_L= 500 uH; Load resistor R_L= 16ohm; modulation index M=0.7, output power Pout= 1.3 kW; modulation method is center-aligned continuous space vector modulation. Figure 8 shows the test results of the system. The system continuously runs for over 20 minutes with no fault or protection triggered which verify the validity of the electromagnetic compatibility (EMC) design of the system.

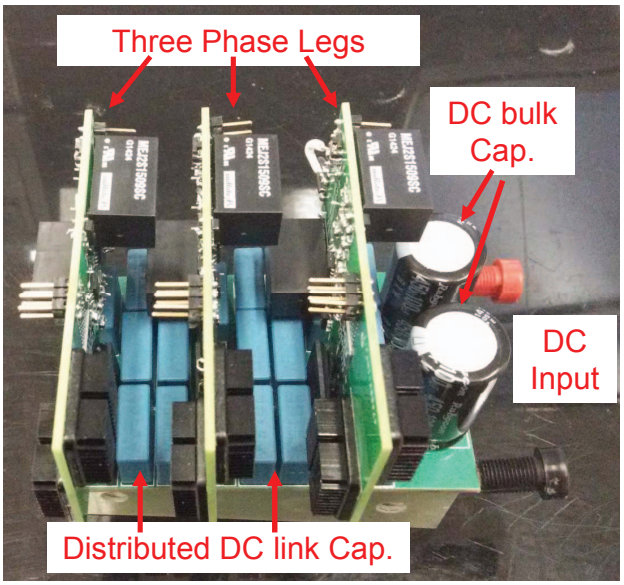

Figure 7(a) Implemented GaN based three phase VSI

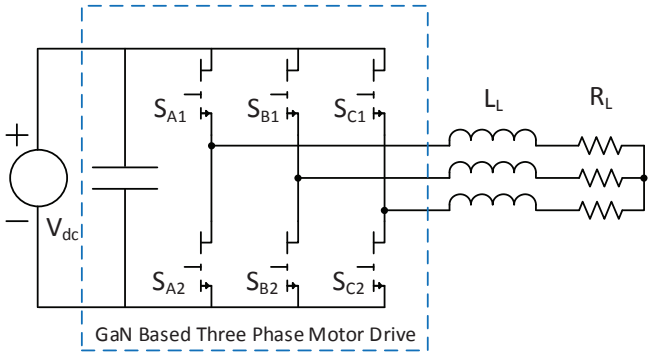

Figure 7 (b) Structure of test circuit

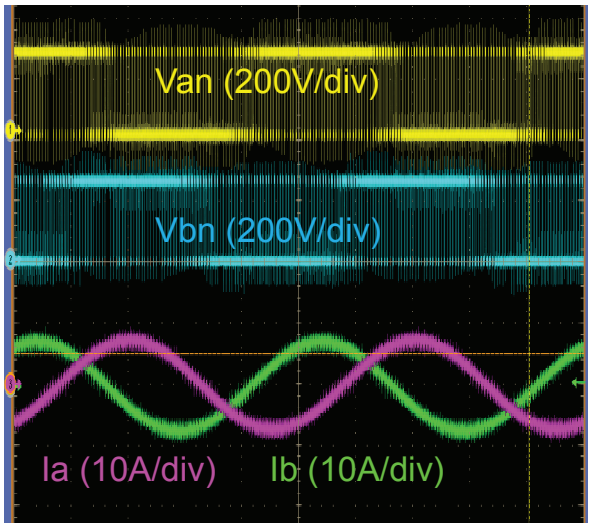

Figure 8 Test results
(Pout=1.3kW Vdc=270V, fs=100 kHz, f1= 400 Hz M=0.7)

VI. Conclusions

This paper presents an improved phase leg design for lateral enhance mode GaN switches with vertical power loop structure and CM noise current propagation control. The characterization results are presented to verify the better performance of GaN switches comparing with silicon MOSFET. However, the fast switching speed of GaN devices also bring EMI issues to gate driver circuit design. A gate driver circuit is designed based on the characterization results with the consideration of the CM noise current propagation control by controlling the propagation path impedance of digital control circuits and their power supply circuits. Moreover, a vertical power loop layout is proposed to minimize the current commutation loop inductance. The design is verified through experiments on a phase leg prototype which prove the effectiveness of the proposed phase leg on the overvoltage reduction during current transition along with less cross-coupling between power loop and gate loop compared with conventional lateral power loop design. Finally, a three phase motor drive system is designed and tested based on the proposed phase leg.

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