

Low Inductance PCB Layout for GaN Devices: Interleaving Scheme

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Abstract— Wide-Bandgap devices are pushing the boundaries of switching frequencies, power densities, and efficiencies of modern power converters. To utilize the full potential of these devices, the parasitic elements formed by the printed circuit board (PCB) layout requires special attention. This work introduces a novel approach, that helps to reduce the parasitic inductance of the commutation loop in a half-bridge topology with surface-mount power devices. The approach uses multiple PCB layers for enhanced current distribution and magnetic cancellation, which results in low inductance designs with less sensitivity to the geometric parameters of the PCB design. The approach is validated with simulation results via a Finite Element Analysis (FEA) as well as with experiments. The results show a promising reduction in inductance and geometric sensitivity compared to the conventional solution.

Index Terms—PCB-Design, Low Inductance Power Loop Design, Finite element analysis (FEA), Wide-Bandgap (WBG), Printed Circuit Board (PCB) Design

I. INTRODUCTION

Wide-bandgap (WBG) semiconductors have become popular in the field of power conversion in recent years since they offer higher power density and higher efficiency solutions for high-frequency operation compared to traditional silicon devices [1]. One of the limiting factors for WBG devices are the parasitic inductances, which are mainly formed by the printed-circuit-board (PCB) interconnections of the devices. They can lead to high-frequency oscillations [2], [3], during a transition of a power switch from on- to off-state and vice-versa. These oscillations are caused by the consequent commutation current flowing through the parasitic inductances. These oscillations contribute to undesired effects, such as increased noise generation [4], [5], increased switching losses [3], [5], [6] and increased voltage stress [3], [5], [7] within the power conversion application.

Several contributions addressed this issue, by minimizing the effective loop area for the commutation current in order to minimize the resulting inductance effectively [6], [8]–[11]. However, in high-voltage or high-power applications, a further reduction of the loop area may become challenging with the conventional approach. In high-voltage applications, the dielectric strength of the PCB material might prevent a further reduction of the loop area. Moreover, in high-power applications, the thermal stress might impose an increased distance between the switches for thermal relief, which forbids a further reduction of the loop area in the conventional way. Furthermore, recent research in planar-magnetics

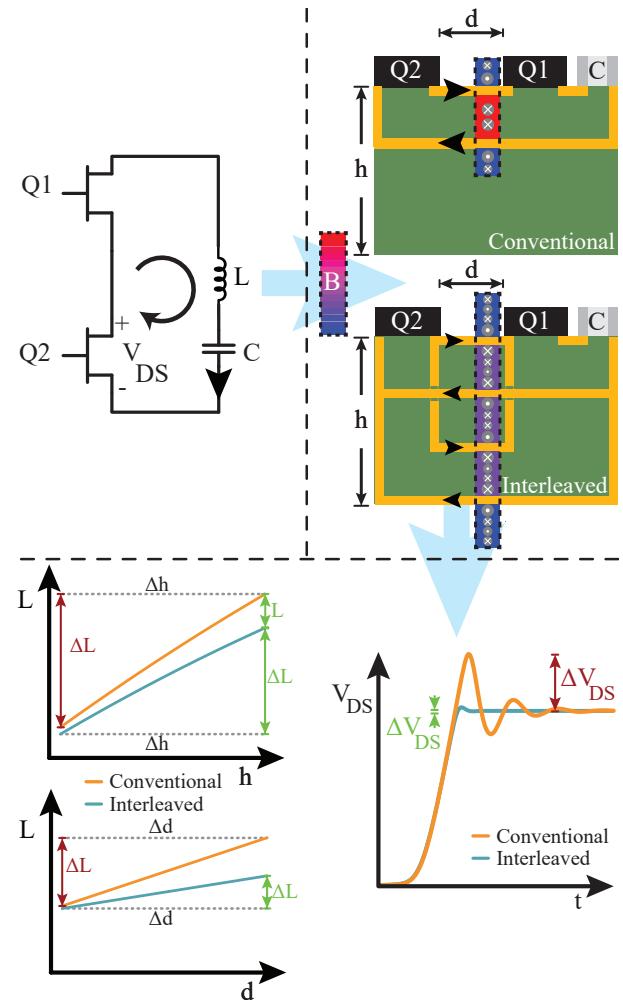


Fig. 1: The proposed approach for reducing the inductance of PCB commutation loops in a fundamental half-bridge topology, with a cross-section of the conventional and proposed scheme, highlighting current flows as well as B-field orientation and intensity; showing the influence of geometric constraints, such as the distance (d) between the switches (Q_1 , Q_2) and PCB-height (h) as well as the influence of the resulting loop inductance of each scheme on the switching transient.

suggests the use of multiple layers in an interleaved manner, to achieve enhanced current distribution and magnetic field cancellation, which results in a significant reduction of parasitic inductance in high-frequency applications [12]–[14].

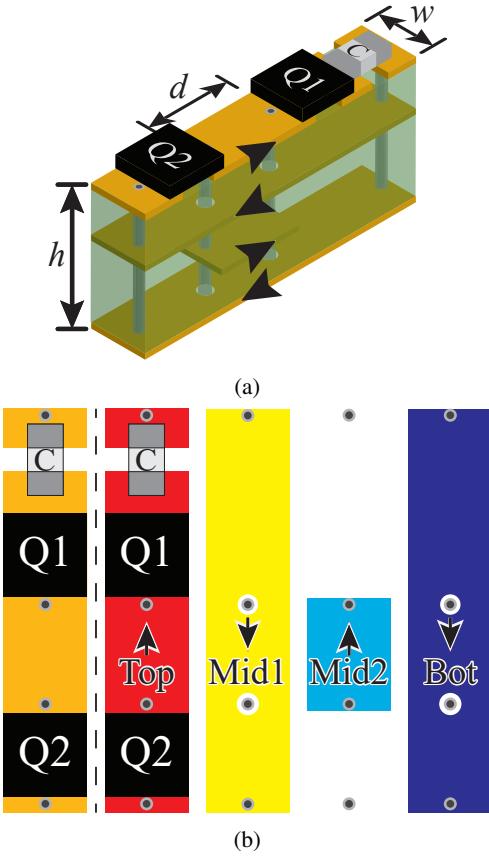


Fig. 2: The proposed scheme: (a) isometric view and (b) top-down view; Indicating current flows, PCB-layer description, and geometric parameter of the scheme, namely the distance (d) between the switches, the loop width (w), and the PCB-height (h).

This paper proposes an interleaved scheme for the commutation loop in a fundamental half-bridge topology with surface-mount power devices to achieve designs with less parasitic loop inductance. The proposed scheme achieves this through enhanced current distribution by utilizing four layers (two more than conventional). This approach takes advantage of four or more layer designs, which are commonly utilized in modern power converter applications. In addition, the current flow in the proposed scheme is designed in an alternating way, which enables magnetic cancellation where possible. Both effects translate into designs with less parasitic inductance. This reduction can accomplish an improvement in noise generation, switching loss, and voltage stress for a fundamental half-bridge topology, which utilize surface-mount power switches. A sensitivity analysis for the main geometric impact factors, such as the distance between the switches (d), and the PCB-height (h), is conducted to ensure a good performance of the proposed scheme for a wide range of the geometric parameters.

Figure 1 illustrates an outline of the approach, which displays a typical half-bridge topology including the decoupling capacitor and the PCB-Design realization for conventional and the interleaved scheme. The schemes contain a B-field overlay, indicating the B-field intensity, orientation, and

distribution for each scheme. It can be seen that the proposed scheme achieves a reduction of the B-field intensity. The resulting field intensity of each scheme translates into the parasitic commutation loop inductance (L) of a half-bridge topology. The sensitivity towards geometric constraints, namely the distance (d) between the switches and the PCB-height (h), is shown. It can be seen that the proposed scheme provides lower inductance compared to the conventional approach. In addition, it shows less sensitivity to changes in h and d compared to the conventional approach. The effect of the resulting loop inductances of the different schemes is illustrated in a typical voltage waveform of a switching transition. Due to the reduced inductance, the proposed scheme provides a reduction of voltage stress for the same geometric constraints compared to the conventional approach. In other words, the interleaved scheme outperforms the conventional approach with the same geometric constraints. Alternatively, for the same performance, the geometric constraints can be more relaxed in the interleaved scheme compared to the conventional scheme. This improvement on the trade-off between geometric dimensions and performance represents a significant contribution to the design of switch-mode power converters.

The proposed scheme is illustrated in an isometric and top-down view in Fig. 2 indicating the layer and via-connection arrangement as well as highlighting the major geometric parameters, namely the PCB-height (h), the distance between the switches (d), and the width of the loop (w). It is worthwhile mentioning, that the proposed layout can be implemented with standard manufacturing capabilities.

II. LOOP INDUCTANCE THEORETICAL ANALYSIS

PCB loop inductance can be approximated via a basic magnetic circuit with

$$L = \frac{\mu_0 \cdot \mu_r \cdot A}{l}, \quad (1)$$

where μ_0 is the permeability of free space, μ_r is the relative permeability of the material, A the area which contains the magnetic flux and l the magnetic average path length. This results in the conventional approximation for PCB loop inductances when l is defined as the width (w) of the loop (see fig.2) and A is defined by

$$A = d_v \cdot d_h \quad (2)$$

where d_v is the distance between the layers and d_h the horizontal length of the loop.

For the conventional scheme, d_v corresponds to

$$d_v = \frac{h - n \cdot c_t}{n - 1} \quad (3)$$

where h is the PCB-thickness, c_t is the copper-thickness and n the layer count (see. fig 2). Further, d_h for conventional layouts can be defined as

$$d_h = d + 2 \cdot Q_{le} + C_{le} \quad (4)$$

where d is the distance between the switches, Q_{le} the length of the switch and C_{le} the length of the decoupling capacitor (see fig. 2). Thus, a reduction of inductance in PCB

commutation loops in the conventional manner according to (1) is achieved by reducing A and increasing l . However, this approximation is no longer accurate when multiple current paths and resulting magnetic fields are considered. In this situation, an enhanced representation of the effective inductance can be expressed via the energy relationship between the inductance and electromagnetic fields with

$$E = \frac{1}{2} \cdot L \cdot I^2 = \frac{1}{2} \cdot \oint H \cdot B dV, \quad (5)$$

where E is Energy, L is inductance, I the commutation current, H the magnetic field intensity, B the magnetic flux density and V the volume that contains the magnetic field. Rearranging results in

$$L = \oint H \cdot B dV / I^2. \quad (6)$$

Based on (6), it is evident that reducing B decreases the magnetic energy, which translates into a lower L . Therefore, the interleaved scheme reduces its inductance by lowering B in different regions. While (6) provides an accurate expression for L , solving it analytically involves the complex computation of fields and integrals, which might not provide a practical solution. Thus, in this paper, a Finite Element Analysis (FEA) approach is utilized for the computation, which translates into high fidelity results as the method also incorporates skin and proximity effects.

III. FEA SIMULATION ANALYSIS

A. Field reduction

According to (6), the interleaved scheme achieves a lower L by reducing B and H . The reduction of B and H needs to be significant since the area and the volume containing the magnetic field is considerably larger in the proposed scheme compared to the conventional one (see Fig. 1). This reduction is realized through the enhanced current distribution and arrangement of the current flow in an interleaved manner for magnetic cancellation in the proposed approach (see Fig. 2). Other schemes with four layers, which also provide enhanced current distribution, may perform worse than the proposed interleaved scheme as magnetic cancellation potential is not fully utilized.

The flux density distribution of the different schemes are computed through FEA simulations with the same current excitation I of 2 A, which will distribute itself for the given geometries provided by the conventional and interleaved scheme. The constraints for the geometries of this particular simulation are 2 mm for the PCB-height, 10 mm for the length, 5 mm for the width, and 35 μ m for the copper thickness. Fig. 3 shows the results of this simulation, where it can be seen that the B -field is reduced by 63 % in the interleaved scheme compared to the conventional case.

B. Inductance reduction and sensitivity analysis

The significant field reduction through the enhanced current distribution and interleaved arrangement of the current flow leads to a reduced L according to (6). For verification of this reduction, L is computed for the conventional and

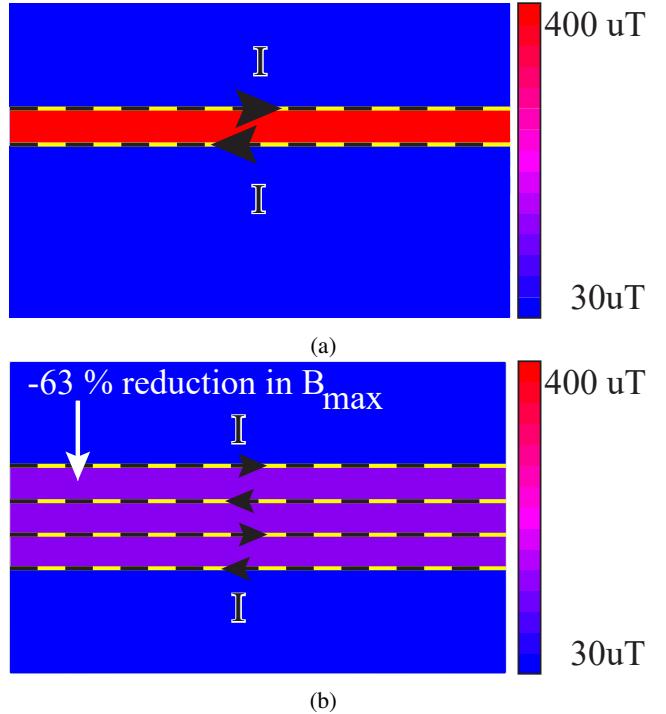


Fig. 3: Schemes with Finite Element Analysis (FEA) results of the B -field distribution for the same current excitation: Conventional (a) and interleaved (b)

interleaved scheme with (6) and an FEA-Software (Q3D) for different geometric configurations at 100 kHz.

For simplicity, the width (w) of the loop is kept constant at the width of the surface-mount switch and the copper thickness at 35 μ m. This allows for enhanced current distribution and consequent magnetic cancellation in respect to the switch geometries. Additionally, the geometries of the discrete components ($Q1, Q2, C$) are also kept constant. The switch geometries are defined as 4 mm width and 8.5 mm length. The capacitor size is defined with the dimensions of a common 1206 package. Therefore, the remaining degrees of freedom for the loop consists of the distance between the switches (d) and the PCB-height (h) as indicated in Fig. 2. The investigated range for h is chosen to be 0.4 mm to 2 mm and for d to be 1 mm to 25 mm. Whereas the values for h are aligned with common manufacturing limits. The values for d are selected to reflect potential assembly and thermal management constraints for the low-end and high-end respectively.

Fig. 4 illustrates the results of the loop inductance estimation through FEA analysis for the conventional and interleaved schemes. It can be seen that the interleaved scheme provides a significantly lower inductance than the conventional approach over the whole range of the parameters. The significance of the inductance reduction is highlighted in the extreme scenarios indicated as points A, B, and C in the figure. Depending on the scenario, the inductance reduction ranges from 12 % up to 35 %. In addition, the sensitivity of the inductance of the different schemes are shown, with respect to the degrees of freedom. It can be obtained that

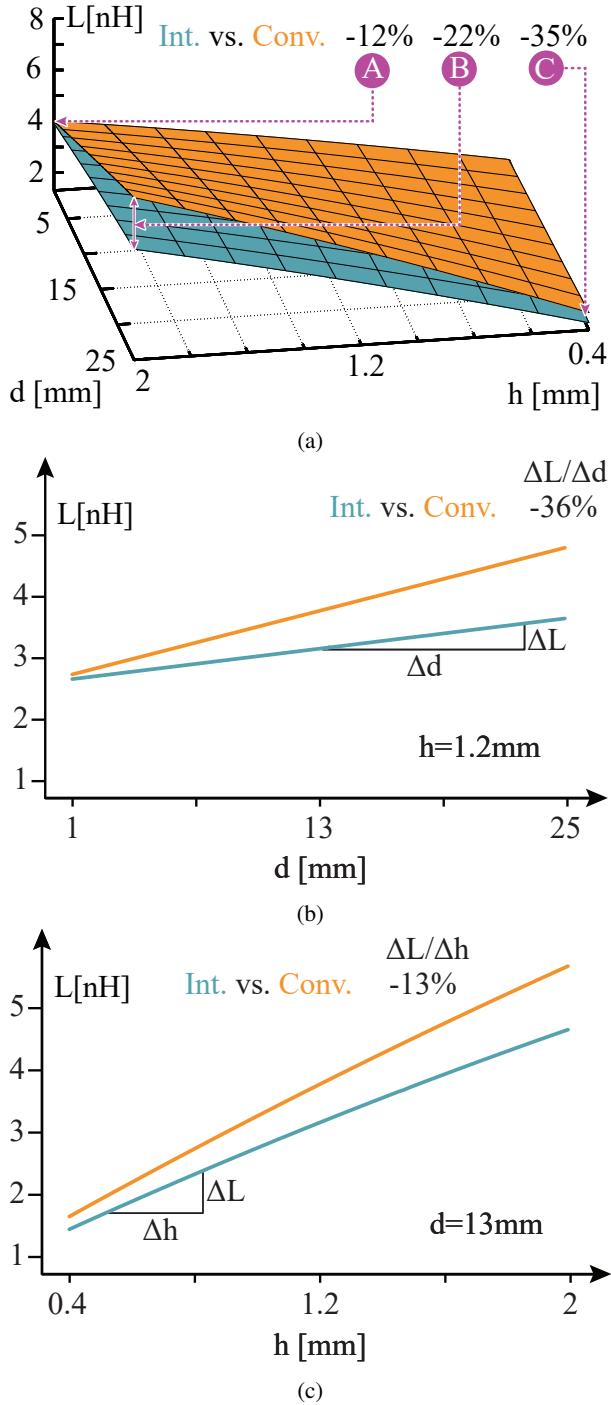


Fig. 4: Surfaces (a) and Sensitivity (b) of the inductance of the conventional and interleaved scheme in respect of the loop geometry; Parameters are the distance between the switches (d) and the PCB-height (h)

the interleaved approach provides a significant reduction of sensitivity to the loop geometry compared to the conventional case. The interleaved scheme provides 13 % and 36 % reduction in PCB-height and distance sensitivity respectively compared to the conventional design. It is noteworthy that the difference between the schemes converges for small h and d while it diverges for large h and d .

IV. EXPERIMENT

The developed schemes have been realized in PCB designs that incorporate 650 V GaN switches (GS66508B) with isolated drivers (1EDI20N12AF). The clearance and creepage of the designs are chosen to comply with functional isolation requirements based on the rated voltage of the switch. Moreover, the embodied vias are standard vias with a hole size of 0.3 mm. For these designs, d is chosen to be 15 mm and h is selected to be 1.6 mm.

The experimental verification has been performed through a motherboard and daughterboard concept for comparability. Thus, the different design schemes have been realized as daughter boards that can be seamlessly incorporated in the topology. The different schemes have been analyzed in a buck-topology, which is a half-bridge derived topology with the corresponding parameters found in table I.

The experimental setup is shown in fig. 5a including the auxiliary power supply, the motherboard and, the daughter-cards (DUTs) as well as the control board, the buck-inductor and the probes. It is worthwhile mentioning that the voltage across the bottom switch ($V_{DS-Bottom}$) is measured with a high bandwidth and high voltage passive probe, whereas the DC-Bus is measured with a differential probe and the gate voltage is measured with an isolated probe.

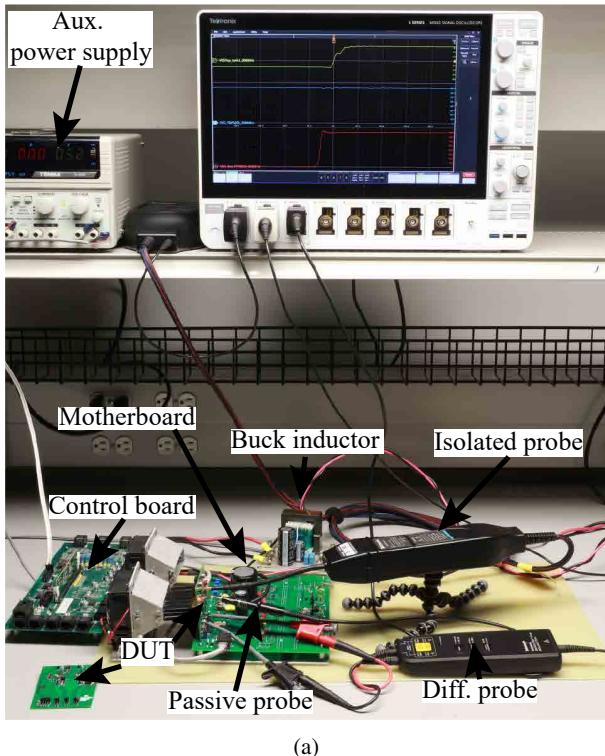
The turn-off waveform of $V_{DS-Bottom}$ for the same operating conditions but different schemes can be seen in 5b, including a zoom-in of the overshoot region. It can be seen that the interleaved layout achieves 1.1 % improvement in overshoot compared to the conventional approach which results in an effective improvement of 34 % when compared directly. Further, it can be seen that the rise time of the interleaved layout is longer than the conventional layout. Consequently, the slew-rate of the interleaved layout is lower than the conventional layout.

V. CONCLUSION

This work proposed a novel approach to reduce the inductance of PCB commutation loops and their sensitivity to the loop geometry in a fundamental half-bridge topology with surface-mount wide-bandgap power devices. The approach utilizes multiple PCB layers, which are utilized in a way that allows the commutation current to flow in an alternating pattern. This enhances the current distribution and magnetic field cancellation. This reduces the inductance, which has

TABLE I: Experimental parameter for Buck-topology

Parameter	Value
V_{in}	400 V
V_{out}	200 V
f_{sw}	100 kHz
I_{out}	1 A
L_{Buck}	380 μH
C_{out}	172 μF
$R_{on/off}$	0 Ω



(a)

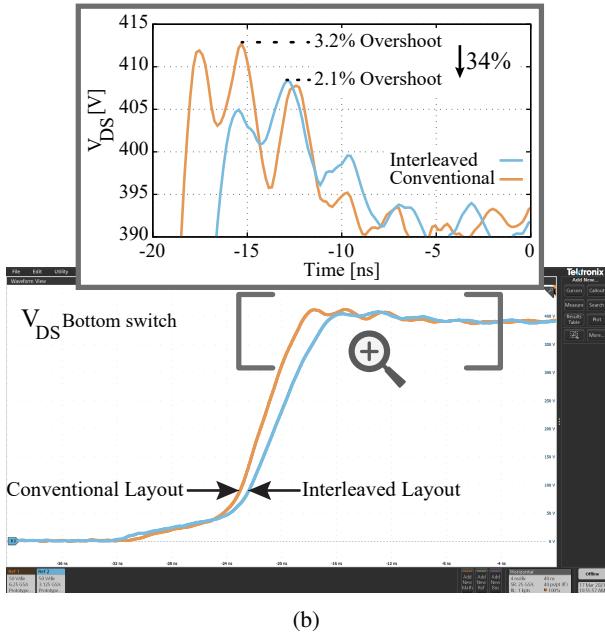


Fig. 5: Experimental captures: (a) setup with the motherboard, the daughter boards (DUTs) and the control board; (b) Turn-off waveforms V_{DS} of the bottom switch for different schemes

been verified by FEA simulations. A sensitivity analysis of the influence of the geometry on the inductance has been carried out. The proposed approach demonstrates a lower baseline inductance and less sensitivity to the loop geometry compared to the conventional approach. The theoretical analysis and the simulations have been verified experimentally. The experiments demonstrate a reduction of overshoot, which is commonly linked to a reduction of loop inductance.

The proposed scheme provides a significant improvement in the design of power electronics systems, as designers are able to mitigate geometric constraints within low inductance designs via the proposed approach, which greatly reduces voltage stress in fundamental half-bridge topologies. The advantage of the proposed approach over the conventional approach is two-fold. The interleaved scheme provides a lower baseline inductance, which translates into better performance for the same geometric parameter compared to the conventional approach. Alternatively, the geometric constraints can be more relaxed while maintaining the same performance with the interleaved scheme compared to the conventional scheme. In other words, the lower baseline inductance and the flatter response to geometry changes of the interleaved approach may provide an attractive solution for PCB designers when faced with design challenges in respect of thermal management, voltage clearance and creepage as well as cost constraints.

The findings introduced in this work can be extrapolated to PCB designs with a higher number of layers, in which the benefits obtained would be larger as the current distribution and flux density cancellation will improve. Furthermore, these findings are not limited to wide-bandgap devices and can be applied to other surface-mount power switches, such as silicon and silicon-carbide based devices, underlying the significance of this work. Some interesting effects have become apparent from the experimental results, which will be addressed in future research.

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