Accurately modelling of parasitics in power electronics circuits using an easy RLC-extraction method

Pieter Jacqmaer*, Jeroen Zwysen†, Ratmir Gelagaev‡ and Johan Driesen§

Research Group ELECTA, Department of Electrical Engineering, Katholieke Universiteit Leuven
*Email:pieter.jacqmaer@esat.kuleuven.be
†Email: jeroen.zwysen@esat.kuleuven.be
‡Email: ratmir.gelagaev@esat.kuleuven.be
§Email: johan.driesen@esat.kuleuven.be

***Abstract*—A method for accurately modelling parasitics in power electronic circuits, is presented in this paper. The freeware software programs FastCap and FastHenry are used to create a model of the printed circuit board tracks, consisting of resistances, self and mutual inductances, and self and mutual capacitances. This model can be easily loaded into a standard circuit simulator such as Spice, together with models for other components, such as the diodes, transistors, coils and capacitances. Thus, the power electronic circuit can easily be simulated in the time domain, returning electrical currents and voltages typically being subject to ringing effects and overshoot.**

I. Introduction

Recently, the power electronics community is becoming more and more interested in using wide-bandgap semiconductors as building material for power switches. These materials exhibit advantageous features such as a diminished thickness for the same blocking voltage with respect to silicon components. Hence, devices, made from wide-bandgap materials, are faster than silicon devices and can operate at increased switching frequencies. However, when frequencies increase, the layout of the circuit, typically implemented as a printed circuit board (PCB), starts to play an important role in the behaviour of voltages and currents, because unwanted parasitics due to the geometry of the copper tracks of the PCB are always present. Voltages and currents will show oscillations and sometimes huge overshoots due to these parasitics, and will subject the active switching components to much more electrical stress, which diminishes their life expectancy. Also, sometimes the parasitic effects are so important that the correct working of the circuit deteriorates or even ceases. Therefore, it is highly advisable to have a method for modelling the parasitics, so that one can quickly see what their effect is on the circuit In this paper, a method is presented to extract an RLC-equivalent network, representing the PCB tracks. This is done using the freeware software tools FastHenry and FastCap, extracting respectively the resistance and inductance matrix, and the capacitance matrix from a circuit consisting of conductors and (for FastCap) one or more dielectric volumes. FastHenry and FastCap are developed at the Computational Prototyping Group of Massachusetts Institute of Technology (M.I.T.) by Jacob White, Mattan Kamon et al. They calculate the R-, L- and C-matrices under the quasi-static assumption and use the multipole expansion technique for speeding up the calculation process. This step in the method, outlined in this paper, produces an electrical model for the PCB tracks, which can be inserted in Spice, together with the other elements of the power electronic converter, such as coil, diodes, mosfets, igbts.... Also other circuit simulators can be used, but in this work, we will choose Spice. The method is explained with an example, first cited in [1], where a sort of resistance-divider circuit, subjected to a step voltage, is modelled. The circuit is built and measurements are compared with the simulation results. In a next section, the method is applied to a step-down power electronics circuit, which is called a reversed buck circuit, because the switch has its source connected to the ground, making it possible to use a non-isolated gate-driver. Again, measurements and simulation results are compared and show a good agreement, indicating that the method of this paper produces accurate results. In the last section of this paper, a freeware software program is presented, implementing the method of this paper. It can be freely downloaded from the Internet, and extracts a Spice-subcircuit modelling the parasitics of the PCB tracks of power converters. The possible PCB geometries the program can process, must have PCB tracks with a rectangular cross section, on a single layer dielectric board, where the tracks are parallel or orthogonal to each other. Also, because the program makes use of FastHenry and FastCap, the parasitics are calculated under the quasi-static assumption.

II. Method for parasitics extraction

A. Resistance-divider network

The method of modelling the parasitics of a PCB circuit, is explained with an example: a resistance-divider network which is presented in Fig. 1. All dimensions are in millimeters. The tracks are 1.2 mm wide and 35 μm high. The point where resistor R_s is attached to, has coordinates (0,0). The copper

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tracks are printed on a substrate with relative permittivity $\epsilon_r = 4.5$ and with corners (-10, -71), (50.2,-71), (-10, 10), and (50.2, 10) mm, therefore having a width of 60.2 mm and a height of 81 mm.

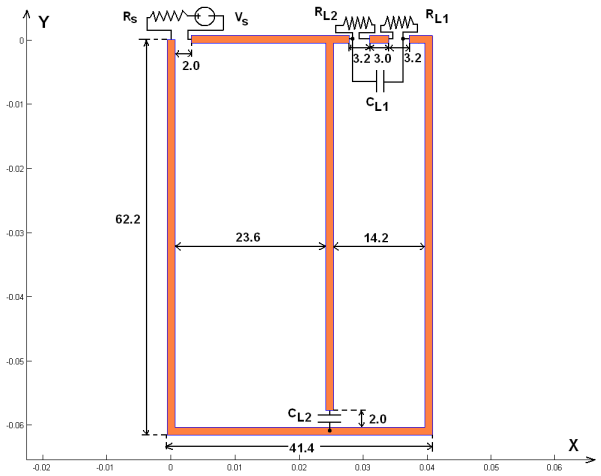

Fig. 1: Resistance-divider circuit.

A voltage source with an output resistance of $R_s = 50\ \Omega$ produces a step voltage V_s. This voltage is applied to the series connection of the resistors $R_{L1} = 51\Omega$ and $R_{L2} = 300\Omega$. Also, there are some capacitors $C_{L1} = 10\ pF$ and $C_{L2} = 27\ pF$ present in the circuit.

B. Using FastHenry for extracting the resistances and the inductance matrices

FastHenry calculates the self- and mutual resistances and inductances of conductors and conductor-pairs. A quasi-static assumption is made in order to make the calculation process more easy. The structure of conductors needs to be partitioned in smaller segments where the current stays constant. Each segment needs to be much smaller than the smallest occurring wavelength. If Δl is the length of a segment, and λ_{min} is the smallest wavelength, the rule of thumb which is used to determine the length of a segment is:

$$\Delta l < \frac{\lambda_{min}}{5} \tag{1}$$

Also, if the size of the structure under consideration becomes large, or if the highest occurring frequency has a high value, time delay effects due to the propagation of the electromagnetic waves at finite speed become important. For segments in the structure that are far apart, the mutual inductances (and mutual capacitances), calculated with the quasi-static assumption, may couple with the wrong phase. The phase error is still tolerable if the size of the structure, Δr, is such that:

$$\Delta r << \lambda_{min} \tag{2}$$

say $\Delta r < \lambda_{min}/5$. Because in the example circuit $\Delta r = \sqrt{62.2^2 + 41.4^2} = 74.7$ mm, and $\lambda_{min} = 373.5$ mm, the highest allowable frequency is $c/\lambda_{min} \approx 800$ MHz, where $c = 299792458$ m/s is the speed of light. Therefore, the length of the segments must be, according to (1) smaller than $373.5/5 = 74.7$ mm. In Fig. 2, the input for FastHenry is presented. There are nine segments, numbered with the red numbers with the large font size, between 11 nodes, numbered with the black numbers with the smaller font size. Also, it can be seen that the segment between nodes 8 and 10 are split in two segments: 6 and 7, because the node 9 must exist in order to connect a capacitor to it. FastHenry calculates the impedance matrix $[R] + j\omega[L]$ for a frequency of 1 MHz, but the quasi-static assumption of the program implies that all resistances and inductances are frequency-independent.

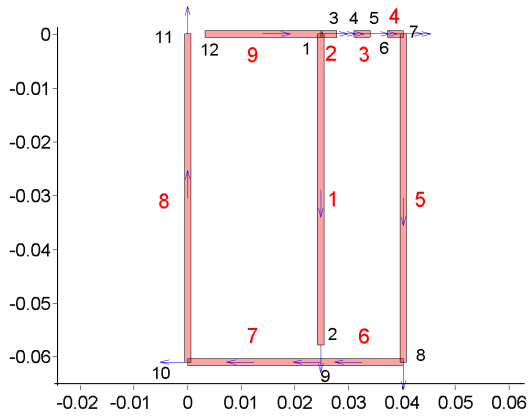

Fig. 2: Partitioning the resistance-divider circuit for FastHenry.

The input file for FastHenry becomes:

```
*
.Units M
.Default z=0 sigma=5.8108e7
N1 x=0.0248 y=0 z=0
N2 x=0.0248 y=-0.0578 z=0
N3 x=0.0278 y=0 z=0
N4 x=0.031 y=0 z=0
N5 x=0.034 y=0 z=0
N6 x=0.0372 y=0 z=0
N7 x=0.0402 y=0 z=0
N8 x=0.0402 y=-0.061 z=0
N9 x=0.0248 y=-0.061 z=0
N10 x=0 y=-0.061 z=0
N11 x=0 y=0 z=0
N12 x=0.0032 y=0 z=0
E1 N1 N2 w=0.0012 h=3.5e-005
E2 N1 N3 w=0.0012 h=3.5e-005
E3 N4 N5 w=0.0012 h=3.5e-005
E4 N6 N7 w=0.0012 h=3.5e-005
E5 N7 N8 w=0.0012 h=3.5e-005
E6 N8 N9 w=0.0012 h=3.5e-005
E7 N9 N10 w=0.0012 h=3.5e-005
E8 N10 N11 w=0.0012 h=3.5e-005
E9 N12 N1 w=0.0012 h=3.5e-005
.external N1 N2
.external N1 N3
.external N4 N5
.external N6 N7
.external N7 N8
```

```
.external N8 N9
.external N9 N10
.external N10 N11
.external N12 N1
.freq fmin=1e6 fmax=1e6 ndec=1
.end
```

Moreover, in order to take the skin effect into account, the segments can be partitioned further in their width-direction and in their height-direction in smaller filaments. The thickness of the thinnest filament must be smaller than the skin depth δ of the current in the conductor:

$$\delta = \sqrt{\frac{1}{\pi f \sigma \mu}} \tag{3}$$

$$\delta > \begin{cases} \frac{W}{2\sum_{i=0}^{nwinc/2-1}(rw)^i} & \text{if } rwinc = \text{even;} \\ \frac{W}{(rw)^{\frac{nwinc-1}{2}} + 2\sum_{i=0}^{(nwinc-1)/2-1}(rw)^i} & \text{if } rwinc = \text{odd.} \end{cases} \tag{4}$$

where σ is the conductivity of the material, μ is the permeability and f is the highest occurring frequency of the current. For 800 MHz, the skin depth is equal to 2.3 μm. W is the total width of the conductor, H is the height, rh is the ratio of the heights of two adjacent filaments, rw is the ratio of the widths of two adjacent filaments, $nhinc$ is the total number of filaments in the heigth-direction, and $nwinc$ is the total number of filaments in the width-direction. Because the current in a plane conductor is distributed exponentially, a good approximation for rw or rh is $2 \ldots 3$ ($e \approx 2.718$). Then, $nwinc$ can be determined, and added to the input file for FastHenry. A similar expression as (4), can be stated for the filaments in the height-direction. For a track width of 1.2 mm, a height of 35 μm and the skin depth at 800 MHz, if $rw = rh = 2.7$, then $nwinc = 14$ and $nhinc = 6$

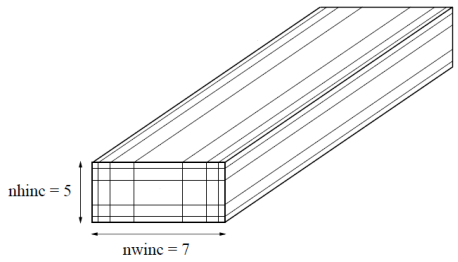

Fig. 3: Meaning of $nwinc$ and $nhinc$ in FastHenry [source: [2]].

FastHenry produces following results for the self and mutual partial inductances (see table I). A comparison with the calculated values of [1] is given. Differences might be due to a slightly different geometry. Therefore, also, inductances of segments 2, 3 and 4 are not stated in the table. The reference work [1] did not give a value for $Lp69$, because it is very small.

TABLE I: Inductances computed by FastHenry and in [1]

ind	FastHenry [nH]	[1] [nH]	ind	FastHenry [nH]	[1] [nH]
Lp11	56.7	57.2	Lp15	15.2	14.7
Lp55	60.5	62.1	Lp18	11.2	10.6
Lp66	11.1	11.6	Lp58	8.1	7.7
Lp77	20.2	21	Lp67	2.6	2.4
Lp88	60.5	59	Lp69	0.52	NA
Lp99	17.0	20	Lp79	0.86	1

C. Using FastCap for extracting the capacitance matrix

The resistance-divider circuit is partitioned in 12 conductors, each of which is located 'around' each of the 12 nodes. As can be seen in Fig. 4, conductors 2, 3, 4, 5, 6, 9, 11 and 12 are straight, conductor 1 has a T-shape, conductor 7 has a Γ-shape, conductor 10 has an L-shape and conductor 8 the shape of an L which is mirrored around a vertical axis. In the figure, different colours are given to different conductors. The surface of the conductors is segmented in smaller panels, having a size of 1.2 mm, which corresponds to the width of the PCB tracks. The top plane of the dielectric substrate is triangularly meshed around each of the conductors (Fig. 5) and this mesh is a .qui-input file for the FastCap-listfile, having an outer relative permittivity of 1 and an inner relative permittivity of 4.5. As can be seen, there is actually a 'hole' in the substrate top plane with which the bottom side of the copper PCB tracks make contact. A separate .qui-input file exists for the bottom side of each copper PCB track, making contact with the substrate, because the outer relative permittivity is then 4.5. The other panels of each copper conductor are part of a different .qui-file, having an outer relative permittivity of 1. Plus signs are used in the listfile to state that the bottom layer of a copper track and the other layers are actually part of the same conductor. The input listfile is thus:

```
* list file for capacitive partitions
C cond2.qui 1 0 0 0 +
C cond2_bottom.qui 4.5 0 0 0
C cond3.qui 1 0 0 0 +
C cond3_bottom.qui 4.5 0 0 0
C cond4.qui 1 0 0 0 +
C cond4_bottom.qui 4.5 0 0 0
C cond5.qui 1 0 0 0 +
C cond5_bottom.qui 4.5 0 0 0
C cond6.qui 1 0 0 0 +
C cond6_bottom.qui 4.5 0 0 0
C cond9.qui 1 0 0 0 +
C cond9_bottom.qui 4.5 0 0 0
C cond11.qui 1 0 0 0 +
C cond11_bottom.qui 4.5 0 0 0
C cond12.qui 1 0 0 0 +
C cond12_bottom.qui 4.5 0 0 0
C cond1.qui 1 0 0 0 +
C cond1_bottom.qui 4.5 0 0 0
C cond7.qui 1 0 0 0 +
C cond7_bottom.qui 4.5 0 0 0
C cond8.qui 1 0 0 0 +
C cond8_bottom.qui 4.5 0 0 0
C cond10.qui 1 0 0 0 +
C cond10_bottom.qui 4.5 0 0 0
D substrate.qui 1 4.5 0 0 0 0 0 0 +
```

```
D substrate_top.qui 1 4.5 0 0 0 0 0 0
```

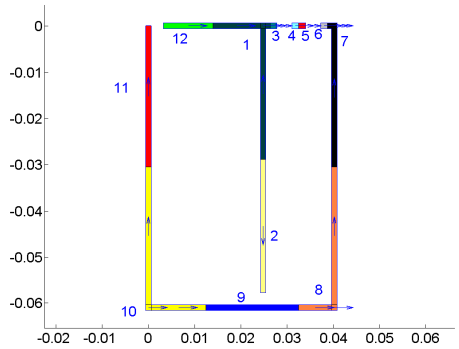

Fig. 4: Partitioning the resistance-divider circuit for FastCap.

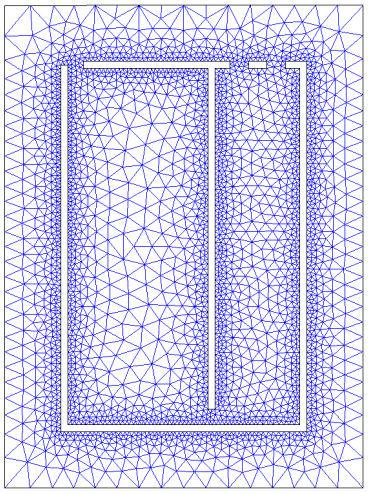

Fig. 5: Triangular mesh of the top plane of the dielectric substrate.

In fact, FastCap produces not normal capacitance matrix C, but in fact produces a short-circuit capacitance matrix C_s ([3],p22). The following transformations exist between the two matrices:

$$\begin{array}{rcll} C_{ii} & = & \sum_{j=1}^{M} C_{sij} & \text{for } i = 1, 2, \ldots, M \\ C_{ij} & = & -C_{sij} & \text{for } i \neq j \end{array} \quad (5)$$

FastCap produces following results for the self and mutual partial capacitances (see table II). A comparison with the values of [1] cannot be made because in this work the dielectric substrate was not taken into account. Also a comparison with the reported values in other works cannot be made, because either a different segmentation is used, or the substrate is not taken into account. Only the capacitances greater than 14 fF are reported in this table.

D. Using Spice to simulate the voltage and current waveforms

The self and mutual partial inductances, the self resistances (mutual resistances are not used in this work), and the self and mutual partial capacitances are inserted in a Spice subcircuit

TABLE II: Inductances computed by FastCap

cap	[fF]	cap	[fF]	cap	[fF]	cap	[fF]
Cp11	574	Cp(1,6)	196.3	Cp(9,12)	80.6	Cp(10,11)	228.1
Cp22	40.6	Cp(1,7)	57.6	Cp(3,10)	21.3	Cp(7,8)	138.1
Cp33	49.7	Cp(1,8)	14. 1	Cp(4,9)	24.9	Cp(7,9)	135.0
Cp44	51.0	Cp(1,9)	210.7	Cp(4,10)	29.3	Cp(7,10)	49.9
Cp55	48.5	Cp(1,10)	79.5	Cp(5,9)	15.6	Cp(7,11)	41.9
Cp66	459.2	Cp(1,11)	208.1	Cp(5,10)	112.9	Cp(7,12)	245.0
Cp77	784.7	Cp(1,12)	137.7	Cp(6,7)	22.8	Cp(8,9)	190.9
Cp88	297.6	Cp(2,3)	13.86	Cp(6,9)	26.0	Cp(8,10)	24.3
Cp99	845.2	Cp(2,9)	122.6	Cp(6,10)	23.2	Cp(8,12)	22.2
Cp1010	819.5	Cp(3,4)	72.8	Cp(6,11)	220.1	Cp(9,10)	215.4
Cp1111	957.9	Cp(3,9)	32.6	Cp(6,12)	222.3	Cp(9,11)	86.9
Cp(10,12)	48.3	Cp(11,12)	84.5				

(.SUBCKT) modelling the PCB tracks, with respectively the Spice elements L, K, R, C and C. The element K, the coupling coefficient between two inductances, is defined as:

$$K_{ij} = \frac{L_{ij}}{\sqrt{L_{ii} L_{jj}}} \quad (6)$$

If there are N self inductances, there are $N(N-1)/2$ mutual inductances. In order to reduce this number, and speed up the Spice calculation process, the 20% smallest mutual inductances can be ignored. Also, the 20% smallest mutual capacitances can be neglected.

PSpice from Cadence [4] is used as Spice simulation tool. The subcircuit modelling the PCB tracks, is imported and the external resistors R_{L1} and R_{L2} capacitors C_{L1} and C_{L2} are connected, together with the voltage source and its 50Ω-input resistor (Fig. 6). Because the simulation results are compared with measurements, not an ideal step voltage is applied, but the `VPWL_FILE` element is used. With this element, a piecewise linear voltage can be specified in a file. The voltage across the 51 Ω-resistor is then calculated and measured.

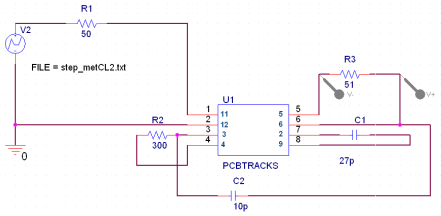

Fig. 6: Importing the model for the PCB tracks into Spice.

E. Results

The Spice simulation results are compared with measurements, with the results of a commercial partial element equivalent circuit (PEEC) simulator (CST PCB Studio [5]) and with the results of a Method of Moments based circuit simulator, not taking the dielectric substrate into account, developed by J. Zwysen et al. at the Katholieke Universiteit Leuven [6]. Two cases are considered: the circuit with the capacitor C_{L2} and the circuit without this capacitor. For every case, the input step voltage is slightly different. The results are shown in Fig. 7.

As can be seen, the measurement data agree very well with the behaviour predicted by the method of this work, and also with the results produced by CST PCB Studio, and the Moment Method technique of [6]. In fact, these last two results are almost identical. The method of this paper, making use of FastHenry, FastCap and Spice, produces results that predict very well the rise times, overshoots, oscillation behaviours and steady state values of the voltages across the 51 Ω-resistor.

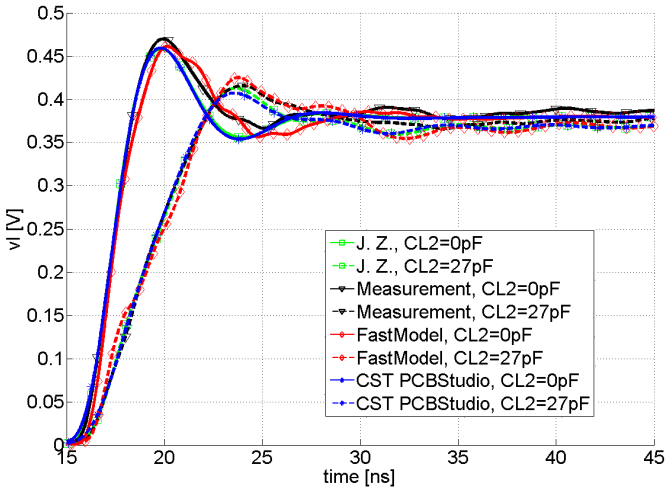

Fig. 7: Importing the model for the PCB tracks into Spice.

III. Determining the behaviour of a fast switched-mode power supply

A. Geometry

The method of this work can also be used to determine the currents and voltages of a switched-mode power supply (SMPS). As an example, a so-called reversed buck converter is used. It has almost the same operating principle as an ordinary buck, or step-down, converter, but in the reversed buck topology, the source of the switching transistor is connected with the ground line, thus facilitating the gate-driver, which does not have to be isolated as explained in [7]. The topology is depicted in Fig. 8 with the dimensions expressed in millimeters (except for the X and Y axes, being measured in meters). All tracks have a width of 2 mm and a thickness of 35 μm. Point (0,0) is the point in the middle of the lower left corner of the switching cell. The switching cell is the region between the input capacitor C_{s2}, the diode D_1 and the switch M_1. As can be seen, the switching cell has a size of more or less 10x10 cm. A substrate with a relative permittivity of 4 is present and has as corner nodes (-56.99,108.77), (235.5,108.77), (-56.99,-59.48) and (235.5,-59.48) mm, therefore having a width of 292.49 mm and a height of 168.25 mm. Following table (III) outlines the components used for the converter. The switch is operated at 1 MHz, with a duty cycle of 50 %. Therefore, the output voltage is 20 V and the output current is 1.333 A.

All measurements are done with a 500 MHz, 5 GSa/s Tektronix TDS5054 oscilloscope, with 500 MHz Tektronix P5050 voltage probes and the current is measured with the

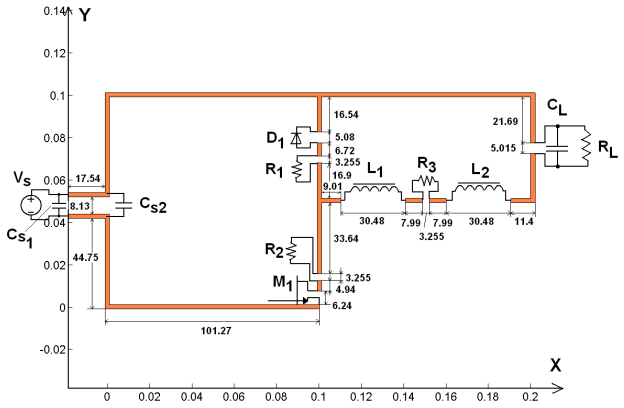

Fig. 8: Geometry, components and dimensions of the reversed buck.

TABLE III: Components used in the reversed buck converter

Component	Type/Value
V_s	40 V, Delta Elektronika SM120-13 adjustable power supply
C_{s1}	2200 μF, 63V, Panasonic ECOS1JP222BA
C_{s2}	220 nF, 63 V, Vishay Roederstein MKT1820422065
D_1	600 V, 4 A, SiC diode, Infineon SDT04S60
M_1	200 V, 12 A, GaN HFET, EPC-Corp EPC1010
$R_1 = R_2 = R_3$	0.125 Ω
C_L	100 μF, 100 V, Vishay BC Components MAL213669101E3
R_L	15 Ω, Welwyn WH5010RJI (10 Ω) + Vishay Dale RH0505R000FE02 (5 Ω)
L_1	40 μH, 2 A, Epcos B82111EC23
L_2	40 μH, 2 A, Epcos B82111EC23

500 MHz differential probe P6250 from Tektronix, measuring the voltage across the shunts R_1, R_2 and R_3. The P5050-probe capacitance of about 13.15 pF is taken into account in the simulations, and so is the skin effect. The Spice models of the switch and diode, as supplied by the manufacturer are used. The simulations and measurements of the voltage across the switch M_1 and the current through the diode D_1 are depicted in Figs. 9 and 10 respectively.

The measurement and simulation of the voltage show a great resemblance, having almost equal rise and fall times and overshoot. However, the ringing falls down more quickly in the real situation than in the simulations. Furthermore, there is a mismatch in the frequency content of the ringing phenomenon, although it is not so great. The measurements show a frequency of 13.3 MHz, whereas the simulations predict a frequency of 13 MHz. Furthermore, in the off-state, the simulations show no ringing, contradicting the measurements.

The measurement and simulation of the current also show a great resemblance, especially during the off-time of the switch. However, there is a mismatch in the frequency content of the ringing phenomenon, although it is not so great during the off-time. The measurements show a frequency of 13.6 MHz during off-time of the switch and 40 MHz during on-time, whereas

the simulations predict a frequency of 12.8 MHz during off-time (agreeing with the measurements) and 50.5 MHz during on-time. The behaviour of the current during on-time is clearly less well simulated than during off-time. A possible reason for this lies in the Spice model of the diode, which can not so well correspond with reality.

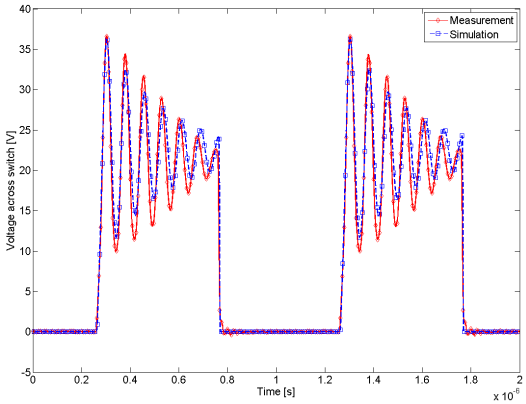

Fig. 9: Measured and simulated voltage across the switch of the reversed buck converter.

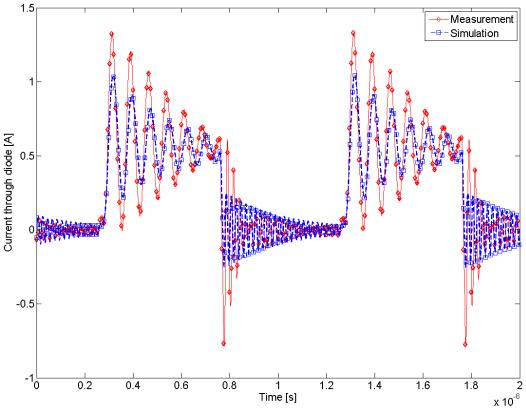

Fig. 10: Measured and simulated current through the diode of the reversed buck converter.

IV. PCBParC

A software tool, PCBParC (Fig. 11) -for PCB Parasitics Calculator- was developed implementing the method of this work. It runs on Windows PCs, is developed in Matlab, and uses Visual Basic Script together with the Windows Automation API to call FastHenry and FastCap, which can, for Windows, be freely downloaded from [8]. Only copper rectangular PCB tracks, which are parallel or perpendicular to each other, are allowed. Furthermore, they must be located in a plane, parallel to the XY-plane. A dielectric substrate immediately underneath the tracks or at a certain distance under them, can be included. Also, it is possible not to have a substrate present in the structure. In order to run the program, the Matlab Compiler Runtime (MCR) must be installed. PCBParC produces a file containing the Spice subcircuit of the inputted PCB tracks. The program can be freely downloaded from [9]. More information about its use and the underlying principles can be found in its manual.

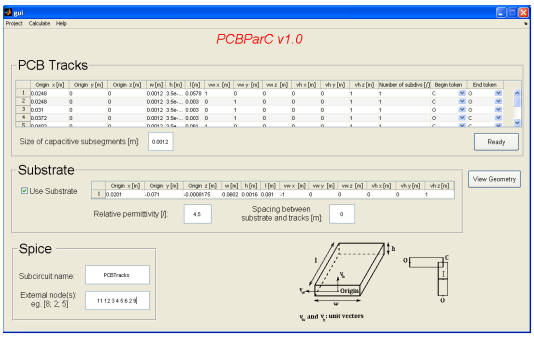

Fig. 11: PCBParC.

V. Conclusion

In this work, a method is outlined for accurately simulating the parasitic effects in power converters. First, a converter containing only linear elements, a resistance-divider circuit, is analyzed, and next, a switched-mode power supply is taken as an example. A quasi-static partial element equivalent circuit method is used for determining the step response and the voltage and current waveforms in the converters in the presence of parasitics, making use of the freeware programs FastHenry and FastCap. These software programs are combined in a tool which can be freely downloaded from the Internet, PCBParC, which extracts an RLC-equivalent circuit from the PCB tracks of a converter, that can be imported into Spice.

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