Wide Bandgap Technologies and Their Implications on Miniaturizing Power Electronic Systems

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***Abstract*— The current state of wide bandgap device technology is reviewed and its impact on power electronic system miniaturization for a wide variety of voltage levels is described. A synopsis of recent complementary technological developments in passives, integrated driver, and protection circuitry and electronic packaging are described, followed by an outline of the applications that stand to be impacted. A glimpse into the future based on the current technological trends is offered.**

***Index Terms*— Gallium nitride (GaN), power electronics, power integrated circuits, power semiconductor devices, silicon carbide (SiC), wide bandgap semiconductors.**

I. Introduction

WIDE bandgap device technology is a key enabler for the miniaturization of power electronic systems, a fact that has been described and demonstrated in the literature for some time and continues to gain momentum, as evidenced by this special issue [1]–[12]. While wide bandgap devices are only just beginning to be used in certain applications, continued growth of this technology will have far-reaching impacts on the way in which systems are designed and fabricated, leading to paradigm shifts within the power electronics industry as a whole.

One often asked question is: why is miniaturization of power electronics important? The most obvious answer is that some applications have space and/or weight restrictions that drive miniaturization. A second motivation is that new system architectures can be conceived as a result of higher power density (i.e., miniaturized) solutions. An applicable analogy is the impact of the miniaturization of integrated circuit features. Higher density integrated circuitry has enabled a mobile computing and communications revolution in such a pervasive manner over the past two decades that would not be possible without these advances. With power supply, management, conversion, and conditioning often being a large fraction of an electronic system footprint, particularly when the associated thermal management is considered, it becomes the limiting factor in many applications. In other applications, such as motor drives and sensing, miniaturization of necessary power electronics again enables breakthrough architectures to be achieved while simultaneously addressing reliability and performance.

A third consideration of miniaturization is that thermal issues become more important as power densities increase. Wide bandgap technologies are more capable of surviving high temperature environments due to lower intrinsic carrier concentrations and higher thermal conductivity. Thus, as the power electronics become smaller, these devices will survive and allow heat management techniques to efficiently remove the heat.

Silicon carbide (SiC) and gallium nitride (GaN) are currently the two most common wide bandgap technologies being pursued in power electronics and thus are the focus of this paper. However, the assertions made could apply to other material systems. While the device characteristics of SiC and GaN transistors enable higher speed switching and higher voltage operation than silicon-based electronics, other aspects of the systems play a subsequent, but important role in miniaturization. Among these are the passive components that are often large in the first place. Another important item is the driver and protection circuitry. The trend is to integrate more of this capability into single chips. The challenges include having this added integration in the presence of high voltages, di/dt, dv/dt, and electronically noisy environments. Last, a crucial aspect to the miniaturization of power electronics is electronic packaging. All of these are surveyed in this paper beginning with a brief overview of the power semiconductor devices that are driving this transformation in Section II. The packaging, passives, and integrated circuits are described in Section III followed by a description of some of the applications that benefit from miniaturization in Section IV.

II. Overview of Wide Bandgap Power Semiconductor Devices

There is an increasing variety of device types available in both SiC and GaN. It is expected that this variety of devices will continue to grow as the market grows, and eventually recede to a stable device set as best-in-class solutions become clear and wide bandgap devices approach commodity status. This section provides a brief snapshot of the currently available wide bandgap devices that are being evaluated for use by the power electronics community for use in a huge range of applications.

The common availability of 100-mm SiC substrates has facilitated the design of medium and high voltage vertical power devices, and the promise of 150-mm substrates will further reduce device cost [13], [14]. The family of available SiC devices is similar to Si, including bipolar junction transistors (BJTs), MOSFETs, diodes, and thyristors with the SiC insulated-gate bipolar transistor (IGBT) currently emerging.

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GaN substrate availability is limited, and most of the devices are grown on Si, SiC, or sapphire substrates. This limits most of the GaN devices to lateral geometries and low-voltage devices (in power terms). In contrast with SiC, GaN heterojunction devices are available, which provides enhanced mobility and carrier velocity.

A. SiC Devices

SiC can exist in any one of a large number of crystal structures called polytypes. Each polytype has different semiconducting properties, and is named for the number of layers in the stacking pattern and the crystal structure (4H indicates four layers before repeating and H represents a hexagonal structure, 3C indicates three layers in a cubic structure, etc). The first commonly used polytype was 3C, which was supplanted by 6H as fabrication techniques improved [15]. By the mid 1990s, the growth of 4H was sufficiently developed to begin building devices [16]. At this time, 4H-SiC is the predominate polytype in power devices. Unless otherwise stated, all references to SiC in this paper refer to the 4H-SiC polytype.

SiC devices will be roughly divided into two groups: those rated at less than 2 kV and those rated at more than 2 kV. Below 2 kV, switching devices such as MOSFETs, BJTs, super junction transistors, and junction FETs (JFETs) are commercially available. Above 2 kV, transistors such as MOSFETs, IGBTs, gate turn-OFF thyristors (GTOs), and other thyristor structures are obtainable, but more limited in availability.

The first commercially available SiC power devices were Schottky diodes. These devices have already achieved broad usage in new designs including hybrid solutions where the switching transistor is Si and the anti-parallel or rectifying diode is a SiC Schottky [17]–[19]. The combination of high breakdown electric field for SiC and fast recovery-time of the Schottky structure allows reduced diode losses in systems with voltages higher than Si Schottky devices can withstand. SiC Schottky diodes are currently available between 600 V and 1.7 kV with current ratings of 50-A per device [20].

Vertical SiC power MOSFETs are more recent additions to the market, but also widely available. These devices are available with ratings of 1.2 kV (with 1.7 kV coming) and current ratings up to 50 A. These devices show a significant decrease in $Q_g \cdot R_{\mathrm{ds,ON}}$ compared with the Si devices. The material resistivity of SiC devices is larger than their Si counterparts, but the order-of-magnitude improvement in the critical electric field of SiC allows for higher blocking voltages for a given thickness. When comparing SiC and Si devices of equivalent blocking voltages, the smaller thickness of the SiC device results in reduced $R_{\mathrm{ds,ON}}$, smaller gate area, and ultimately, reduced gate charge. The effect of reduced gate charge is faster switching capability. Several groups have demonstrated converters using SiC FETs at 400 kHz and above. Examples include a three-phase inverter and a hard switched, isolated full-bridge dc–dc converter. DC input voltages of 350–530 V and power outputs of 4–6 kW were achieved [21], [22]. A comparable high-performance phase-shifted full-bridge dc–dc converter using Si MOSFETS that provides 2 kW at 56 V output operates at 100 kHz [23].

Several companies offer SiC power BJTs and JFETs [Fig. 1(a)] with ratings between 1.2 and 1.7 kV and up to 50-A per device. With the closure of SemiSouth in 2012, all JFETs currently available are depletion-mode (or normally-on) devices. BJTs and JFETs suffer from the requirement to provide constant bias current (for normally-off devices) while conducting, or an additional low-voltage MOSFET in series (i.e., cascode arrangement) for normally-on operation. The lack of a gate oxide in JFETs and BJTs promises an improved reliability during high temperature operation. JFET devices have been demonstrated to operate at temperatures up to 500 °C [24]–[26]. Higher operating temperatures allow reduced system cooling and ultimately reduced system volume and mass, as will be described in Section III.

Above 2 kV, the commonly available devices are GTOs and MOSFETs [Fig. 1(b)]. GeneSiC offers devices rated at 6.5 kV and up to 80-A per device [27]. Cree has demonstrated a 12-kV GTO at 100 A and offers engineering samples of 10 kV and 10-A MOSFETs [28]. Electrically activated SiC GTOs have turn-ON times less than 1 μs, and turn-OFF times of 1–5 μs. Optically triggered GTOs have demonstrated turn-ON times less than 100 ns [29].

Although still in development, SiC IGBTs [Fig. 1(c)] offer the best features of SiC MOSFETs and Si IGBTs [30], [31]. The reduced gate charge and carrier lifetimes of SiC allow IGBTs with ratings of 12 kV and 10 A to switch at 10 kHz and above, where state-of-the-art Si devices (6.5 kV, 25 A) are limited to switching frequencies of 1–2 kHz [30]. As current ratings for SiC IGBTs increase, the conduction losses are expected to decrease in relation to MOSFETs with equivalent voltage ratings.

B. GaN Devices

While vertical GaN devices are a topic of investigation, currently available GaN power devices are lateral heterojunction structures [Fig. 1(d)] that exhibit attractive properties for high speed switching, but are limited in voltage breakdown capability. A heterojunction device uses junctions of dissimilar materials (GaN and AlGaN most often), instead of junctions of the same material with different dopings, leading to the well-documented 2-D electron gas (2-DEG) effect in the conducting layer. Most material properties of GaN are superior to those of SiC for power devices. However, until a suitable vertical structure is created for GaN, superior performance will be confined to lower voltage levels (<1 kV). For both bulk and heterojunction devices, the critical electric field is even higher than SiC; and for heterojunction devices the mobility and saturation velocity are improved with respect to SiC [34]. The only noteworthy property in which SiC is superior to GaN is thermal conductivity. Despite this, GaN is the predominant wide bandgap material only in devices with ratings of 600 V and below, due to the limited availability of high-quality GaN substrates and the fact that heterojunction devices are lateral instead of vertical. The use of non-GaN substrates eliminates the possibility of vertical devices. For higher blocking voltages, the drift region dominates the ON-resistance, and lateral devices can no longer

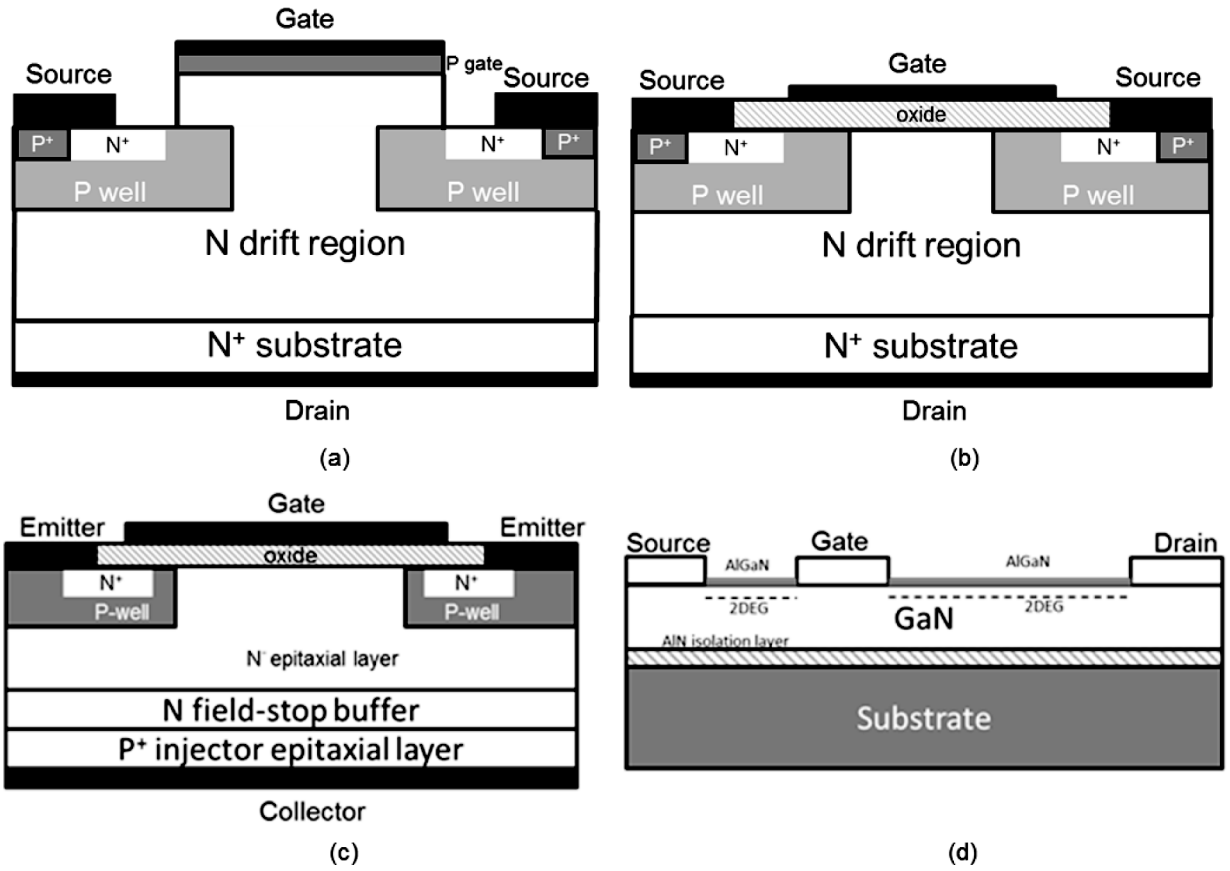

Fig. 1. Simplified device cross sections. (a) SiC JFET [32], (b) SiC MOSFET [32], (c) SiC IGBT [31], and (d) GaN HEMT [33]. In the case of SiC devices, the cross sections are very similar to those found in silicon power devices, with advantages (and disadvantages) being realized through material property differences.

compete with the larger cross-sectional area of vertical devices. In Fig. 1(a) and (b), the drift region is explicitly labeled. In Fig. 1(c), the drift region is the N^- epitaxial layer, and in Fig. 1(d), the drift region is the 2-DEG formed between the gate and drain terminals. The current crossover point between GaN and SiC appears to be blocking voltages of around 1 kV [35].

The majority of existing GaN power devices are high electron mobility transistors (HEMTs) and HEMT-derivatives. The HEMT is a heterojunction device made up of a layer of AlGaN formed on top of a GaN substrate. The AlGaN layer observed in Fig. 1(d) acts as a donor, providing carriers to the low-doped GaN layer. Since the GaN layer has few impurities, its effective mobility can be over twice the mobility of doped GaN [35]. The exact order and doping of layers can be adjusted within this basic framework, and HEMTs have been built both as normally-on and off transistors, and with both Schottky and insulated gates [36]. HEMT-type power FETs are available from Efficient Power Conversion (EPC) corporation with ratings from 40 V and 33 A to 200 V and 12 A, Transphorm with ratings up to 600 V and 17 A, and are expected from International Rectifier in 2014. The EPC parts are enhancement-mode (normally-off). The Transphorm and International Rectifier HEMTs are depletion-mode (normally-on) but use an in-package cascode low-V Si FET to provide normally-off functionality to the designer. Cree, Nitronex, RFMD, HRL, and others also produce GaN HEMTs, but these devices are designed for the high frequency (i.e., GHz) RF market for applications such as high power radar and, as such, are outside the scope of this overview.

Vertical GaN devices may soon become available as research intensifies in this area. Kyma Technologies sells 30-mm n-type bulk GaN wafers [37], and Avogy has demonstrated devices grown on 2″ wafers [38]. Vertical GaN devices that do not use heterojunctions have bulk mobilities of around 800 $cm^2/V\cdot s$ and relative permeability of 9.0, both lower than bulk SiC. Despite this, vertical (bulk) GaN devices have a higher Baliga's figure of merit (FOM), since GaN has a critical field of 3.3 MV/cm, 50% higher than SiC [35].[1]

III. Enabling Technologies for Miniaturization

The use of SiC and GaN improves the volumetric efficiency of power electronic systems for several reasons. The most significant reasons are: 1) they are able to switch faster than silicon devices; 2) they have greater thermal conductivity; and 3) the wider bandgap allows for higher temperature operation. Higher speed switching leads to lower valued capacitors and inductors for filtering, which are smaller in physical size. Greater thermal conductivity promotes more effective

[1]Baliga's FOM for power devices: $\varepsilon_r \mu_n E_{\text{crit}}^3$.

heat removal from the devices, which is important given that, with all other things being equal, the higher switching frequency will lead to more self-heating. Finally, just the basic fact that SiC and GaN are wider in bandgap than silicon means that, with their intrinsic carrier concentrations being lower (by several orders of magnitude in this case) at room temperature, they have more thermal headroom before the device is overwhelmed with thermally-generated carriers. Yet, it is prudent to point out that these devices remain viable at temperatures down to −55 °C, making them suitable over most of the common applications.

To fully realize the volumetric improvements promised by the use of wide bandgap device technology, constraints are placed on other parts of the system. If the system will operate at higher temperatures either because of the environment or because of increased power density, then other materials and components in the system have to be able to withstand those temperatures. One reason that designers may desire to operate the system at higher temperatures is because: 1) the wide bandgap devices can easily take it and 2) substantial size reduction is achieved by less aggressive thermal management. Therefore, if the materials, packaging and components can withstand the higher temperatures, then the volume of the system can be made smaller. The following sections describe the necessary contributing factors for devices, passives, and electronic packaging to achieve this miniaturization.

A. Devices

The first effect of wide bandgap material on miniaturization is device size itself. The increase in critical electric field for wide bandgap materials reduces the minimum size for a given blocking voltage, which, in turn, reduces ON-state resistance. This effect is fully realized in vertical devices, but less-so in lateral devices [35].

The optimal method for comparing dissimilar devices is to use the specific ON-resistance, and specific input-capacitance, and the Baliga high-frequency FOM (BHFFOM)[2] [39]. Other FOM (including the Baliga FOM), are material properties, not device measurements. Unfortunately, few manufacturers provide these parameters, and they are difficult to estimate for packaged devices.

Fortunately, data do exist for some devices to make a comparison of the specific ON-resistance of a Si and SiC power MOSFET. The Infineon CoolMOS C7 device is a class-leading vertical Si super junction MOSFET, rated for 650 V, with a specific R_{ON} of 10 m$\Omega\cdot$cm^2, approximately six times lower than the physical limit of a simple vertical Si MOSFET of similar voltage rating [40]. The Cree CPM2-1200-0025B is a second generation bare-die vertical power device rated for 1200 V and with a rated R_{ON} of 25 mΩ [41]. With a die size of 4.04 mm × 6.44 mm, this device has an approximate specific R_{ON} of 6.5 m$\Omega\cdot$cm^2. This represents a 35% decrease in specific resistance while simultaneously achieving an 85% increase in blocking voltage.

Comparing older, 1200 V class bare-die Si devices, the difference in specific R_{ON} is even more significant. The IXYS IXFD32N120P-99 device is a 1200 V bare-die device with an R_{ON} of 310 mΩ and a footprint of 1.581 cm × 1.431 cm [42]. The specific R_{ON} of this device is approximately 700 m$\Omega\cdot$cm^2. The IXTX20N150 is a newer, 1500 V device from IXYS, but is not available as bare die, and therefore is more difficult to compare.

Beyond the R_{ON} of the devices, higher switching speeds also contribute to miniaturization. Returning to the comparison of the C7 CoolMOS Si device and Cree CPM2 SiC device, the estimated BHFFOM for the C7 device is 5.12 GHz, while it is 13.5 GHz for the CPM2 device [41], [43]. As mentioned before, using higher switching speeds allows capacitors and inductors with smaller values and volumes.

Table I shows a comparison of device parameters for best-in-class devices for high-voltage Si, super junction Si, SiC, and GaN+Si (cascode) devices [41]–[45]. The natural comparison is between the 1200 and 1500 V IXYS Si devices, and 1200 V Cree SiC device in one group, and between the transphorm GaN + Si and 650 V Infineon super junction Si devices in the other. The 1200 V SiC device is the clear winner in its category, with $R_{\mathrm{DS,ON}}$, C_{iss}, and I_D much better than the 1200 and 1500 V Si devices. In the comparison of GaN + Si and Si, the best device is less obvious, since the 650 V Si device offers lower $R_{\mathrm{DS,ON}}$ and higher rated I_D, whereas the GaN + Si device has a superior C_{iss}. The higher resistance of GaN + Si device is still impressive when it is noted that the device is both lateral and includes a series low-voltage Si MOSFET.

An interesting device development that promises to induce further miniaturization is that of optically triggered devices [29]. With a suitable optically triggered power device, size issues associated with magnetic isolation can be mitigated while also simplifying gate drive circuitry.

B. Passives

Beyond the possibility of smaller passive components, wide bandgap power devices will actually require closer coupling of the passive components, thus further driving miniaturization. The cost of higher switching frequencies is that more elements of the system begin to function as antennas. Bogonez-Franco and Sendra [46] and Mostaghimi [47] show that replacing a Si switch or freewheeling diode with a SiC device on power converter printed circuit boards directly impacts the radiated emissions. The first and simplest method of reducing radiated emissions is to minimize path lengths by placing components as close as possible to the switching devices [48]. Ultimately, this will require driving passive components directly inside the package that contains the switch(es). Significant advances have been made in this area by developers of power supply on chip technology [49], although it is predominantly focused on low voltages suitable for modern microprocessors.

As power systems are miniaturized, low-voltage passive components used in the gate driver and other system subcircuits are placed ever closer to the power devices, where they are exposed to the same environmental conditions as the power devices. Since many power devices, particularly wide bandgap devices, operate at elevated temperatures, the availability of passive components that are stable and reliable

[2]Baliga's high frequency FOM $= 1/(R_{\mathrm{ON,sp}} \cdot C_{\mathrm{in,sp}}) = f_B$.

TABLE I
COMPARISON OF PARAMETERS FOR Si, SiC, AND GaN FETS

Device	Manufacturer	Material/Device	Blocking Voltage (V)	$R_{DS,on}$ (mΩ)	C_{iss} (pF)	Rated I_D (A)
IXFD32N120P-99	IXYS	Si/ MOSFET	1200	310	[Data Not Available]	
IXTK20N150	IXYS	Si/ MOSFET	1500	1000	7800	20
IPB65R045C7	Infineon	Si/ Super Junction MOSFET	650	96[1]	4340	29[2]
CPM2-1200-0025B	Cree	SiC/ MOSFET	1200	120	2980	50[3]
TPH3006PS	Transphorm	GaN+Si/HEMT+MOSFET	600	150	740	12[2]

(1) at 150° C (2) at 100° C (3) at 120° C

TABLE II
SURVEY OF HIGH TEMPERATURE CAPACITORS BASED ON DATA FROM WANG *et al.*

Materials		Vendor	Capacitance	Temperature	Max. Rated Voltage
Ceramic	NP0	Kemet Novacap Johanson Dielectrics Eurofarad	1.0 pF ~ 0.12 µF	-55 °C ~ 200 °C	7.5 kV
	X7R		100 pF ~ 3.3 µF	-55 °C ~ 200 °C	30 kV
Teflon		Eurofarad	470 pF ~ 2.2 µF	-55 °C ~ 200 °C	400 V
Tantalum		Kemet	0.15 µF ~ 150 µF	-55 °C ~ 175 °C	125 V
Mica		CDE	1.0 pF ~ 1500 pF	200 °C	1.5 kV

across wide temperature ranges becomes a limiting factor in integration and miniaturization. High temperature capacitors and magnetics and most of the resistors are rated to a maximum operating temperature of 200 °C, although wire-wound resistors rated as high as 275 °C are available [50]. Some work has been done to develop magnetic materials at 300 °C [51].

Generally, high temperature capacitors are one of three types. These types are ceramic, tantalum, and mica [50]; a survey of available high temperature capacitors is shown in Table II. For these capacitors, the low-voltage regime is covered by the tantalum capacitors and high-voltages are covered by the mica type. The ceramic capacitors have a broad range of operating voltages, but tend to be limited to lower capacitance values. When high-temperature-stable capacitors are not sufficient for the design of the system, several techniques can be used. As mentioned in [50], ceramic capacitors tend to have a higher CTE than the ceramic layer, which tends to mechanically force the capacitor apart when it is heated; other stresses come about for all types as a result of the solder joint used to attach the component.

One method to address these issues is to simply physically partition the system so that sensitive passive components are not subjected to high temperatures [52]. To address temperature effects on the value of the component, another approach is to use circuit topologies that can cancel out the temperature dependence of the passives [50] or reduce the need for passives such as some inductor-less topologies.

Commercially available inductors rated for high temperature applications are readily available; the operating temperature for some of these devices extends from −55 °C to 155 °C [53].

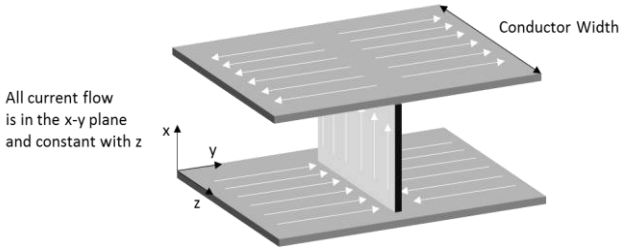

Fig. 2. Parasitic inductance is minimized using wide conductors and designing for the current flow to remain in the xy plane.

Examples of inductors that are rated up to 200 °C include [54] and [55]. Core materials that are rated up to 200 °C include [56] and [57]. Having Curie temperatures as high as 500 °C, it has been reported that some of these materials can withstand temperatures as high as 450 °C [26].

As wide bandgap devices enable higher switching frequencies, the corresponding reduction in the size of the magnetics allows for an overall reduction in the size of the system. At frequencies below 100 MHz, magnetic-core inductors yield an advantage with respect to inductance density and efficiency, while air-core become more competitive at higher frequencies [49]. Thus, magnetic-core inductors would be more suitable for low-voltage applications in wide bandgap-based systems where a reasonable switching speed might be 500 kHz. A number of microinductor structures were reviewed in [49], where it was pointed out that each particular structure had advantages and disadvantages that the designer had to take into consideration. Recently, researchers working to reduce the size of conventional inductors in point-of-load (POL) converters have leveraged low temperature co-fired ceramic (LTCC) technology to create low-profile LTCC inductors and potentially improve power density [58]. Ultimately, any improvement in inductor technology that allows for reduced losses, improved performance, and reduction in size is key to the potential miniaturization of power systems.

C. Packaging

As switching frequencies increase, and passive components become smaller and are driven inside the package, the parasitic inductances and capacitances of the system must also be reduced. Bayerer and Domes [59] demonstrate the design of a three-phase inverter using 1200 V, 600 A per-phase Si IGBT modules to illustrate the effect of minimizing parasitic inductance through good layout practices. In particular, the authors focus on using wide strip-line (bus-bar) conductors to minimize inductance, and designing the layout to keep current flow uniform in the directions shown in Fig. 2. If all of the strip-line conductors in a system are arranged so that their width is on the same axis (defined as the z-axis here), current will only flow in the xy plane. The current is then allowed to spread equally across the z-axis, and current crowding is minimized. This arrangement is shown in Fig. 2.

An excellent example of these strategies is shown in [60], where the authors report a 600 V, 60-A SiC JFET half bridge module. The authors report simulated and measured values of module inductance between 4.5 and 9.5 nH, depending on method. This module is designed to operate at junction temperatures of 200 °C and above, and includes internal gate-source capacitors to avoid parasitic turn-ON. This design points to the need for high-temperature passives described previously, as well as a need for high-temperature packaging.

As operating temperatures increase beyond the point at which traditional packaging materials can be used, it becomes necessary to seek out new materials. Among the critical packaging components to be considered are the coefficient of thermal expansion (CTE) of the package materials, the die attachment method, underfills and passivations, and the encapsulant [61]. The CTE of the materials used in a power module are critical, since the broad operating temperature range means that a significant CTE mismatch can lead to any number of failure mechanisms such as cracking at interfaces or in the die itself. This point emphasizes the importance of simulation tools, since concerns such as CTE mismatch and thermal performance must be taken into consideration very early in the module design process.

There are a number of high temperature die attachment materials that allow for operation at higher temperatures than is possible with traditional solders. Some Pb-based solders are viable for operation above 250 °C; however, the eutectic tin-lead solders fail near 200 °C and those with higher lead content fail near 300 °C [62]. In addition, the world-wide push to eliminate Pb from electronic assemblies tends to limit their use to research-based prototypes only.

Au-based alloys, and the Au80Sn20 eutectic (280 °C) in particular, are a Pb-free option that have been commonly used for high temperature solder attachment for some time. Ag-based sintering is a Pb-free approach that exhibits excellent electrical and thermal conductivity that can be processed at 300 °C while the melting point is at or near that of Ag (962 °C) [62].

Solid–liquid interface diffusion (SLID) bonding is a type of transient liquid phase (TLP) bonding in which the interlayer is a pure metal and also acts as the melting point depressant [63]. Au-Sn SLID has been shown to yield stable bonds at temperatures above 350 °C [64]. A number of researchers have recently demonstrated TLP bonding as a die attach method using Au-InSn, Ni-Sn, and Cu-Sn [65]–[67]. Besides being Pb-free, the TLP processes have the advantage that processing is performed at a lower temperature (usually at or below 300 °C), while the resulting bond reflows at a much higher temperature. This fact allows the same process to be used to attach components in multiple stages for the same assembly.

Alongside die attachment, the proper selection and application of solder for other components is, of course, also critical. To reduce the stresses for passive devices introduced by thermal cycling, the use of a reduced solder bond line may be necessary [50].

Many available encapsulant materials were originally targeted for use at temperatures below 175 °C [68], and therefore tend to degrade at higher temperatures. The availability of suitable products is particularly scarce at temperatures above

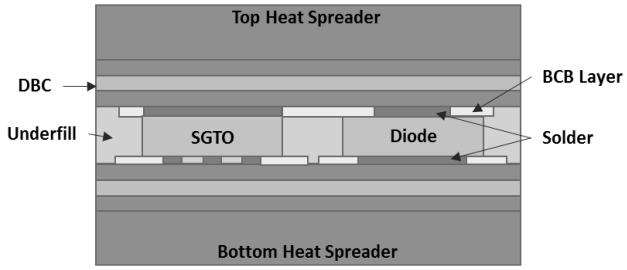

Fig. 3. Example of wire bond-less interconnect based on [72].

200 °C. It is important to note that the suitability of a material is not gauged solely on whether it survives the temperature excursion; while some materials do not breakdown physically at higher temperatures, they still exhibit a change in properties such as dielectric strength as they age at higher temperature [68].

Another material issue involves underfills and passivations used to provide stress relief, mechanical support, or high voltage blocking capability in the presence of high fields that exist around wide bandgap devices. Companies such as Kyocera and Curamik have developed high quality substrate materials involving direct bond copper (DBC) or direct bond aluminum (DBA). DBA has been found to exhibit better long-term reliability than DBC during temperature cycling [69], [70]. Aluminum nitride (AlN) DBC is a favorable choice, since AlN has approximately 10 times greater thermal conductivity than that of alumina and a CTE close to that of SiC.

The connection from the die to the substrate has classically been via wire bond technology. The high di/dt and dv/dt switching that is possible with wide bandgap devices, in conjunction with parasitic inductance in the power module, leads to ringing that can cause instability or even module damage. Wire bond-less technologies reduce inductive parasitics and reduce volume requirements, so they are one way to combat this issue [71], [72]. In addition, they can facilitate double-sided cooling of die, as shown in the topology in Fig. 3. In the topology shown in the figure, connections to the die are accomplished using a flip chip approach. This reduces parasitic inductance in the connections and also requires a smaller footprint as compared with using wire bonds to accomplish the same interconnect.

D. Integrated Circuits

As described previously, wide bandgap materials have long been investigated for integrated circuits. Benefits such as higher operating temperatures and radiation-hardness-by-process are desirable in applications well-beyond power electronics. Within power electronics systems, continued parasitic reduction requires that the low-power control and sensing circuits must be driven ever closer to the switching devices. This is particularly true for gate drivers used with wide bandgap power devices, as shown in Fig. 4. The combination of gate resistance and parasitic inductance limits the rise and fall time of the device. More concerning is the relatively small value of the gate-source capacitance in wide bandgap devices when current is injected through the gate-drain capacitance during high speed switching that produces large dv/dt excursions. If the impedance of the gate resistance and parasitic inductance is not sufficiently low, the injected current can cause spurious turn-ON, possibly leading to destructive shoot-through [73].

Several novel methods have been investigated to move a portion of the gate driver circuitry closer to the power devices [74], [75]. The most broadly applicable methods, however, will move the gate driver directly inside the package with the power device, as shown in Fig. 4. A gate driver collocated with the power device must be designed to withstand the same environment as the power device. For this reason, development of gate driver, protection, and even simple controller circuits for SiC power devices has focused on SiC and high-temperature silicon-on-insulator technologies [76]–[80]. Collocation of the gate driver with the power device also reduces the parasitic inductance in the interconnects between the driver and power device. Ultimately, wire bondless interconnect methods may be used if the gate driver and protection circuitry are attached directly to the DBC or DBA substrate. These approaches can lead to parasitic inductances less than 10 nH and in some cases substantially less. This results in much cleaner switching waveforms, less electromagnetic interference, and greater power efficiency. With the future of power electronics packaging pushing toward 3-D stacking of die, a low-voltage control and gate-drive layer could be added to the stack shown in Fig. 3. These 3-D package stacks will most likely integrate cooling in a very-high-density (VHD) package to remove the heat from the stack. In such cases, the CTE matching of the driver die to the power device die may be more critical. SiC (or GaN) integrated gate drivers mated with SiC (GaN) power devices would provide the most attractive solution for high reliability in a VHD package or module.

The level of integration within power electronic modules being described here is presented with a cautionary stance based on lessons learned in the aggressive drive toward mixed-signal circuit integration in the 90s. The lesson learned was essentially that trying to integrate analog, digital, and RF circuitry all on one chip was a nice theoretical exercise, but practically not the right approach in many cases. Too many performance compromises have to be made in one domain or the other because a single process was unsuitable for each domain. For instance, a process optimized for high performance RF will have thick interconnect metal, while a high-speed digital process will emphasize minimum device dimensions and several levels of metal interconnect. Therefore, the system-on-chip approach was tempered with a system-in-package approach that allowed analog, digital, and RF circuitry to each be designed in the most suitable process for that domain given the system requirements. The resulting independent die were then tightly packaged using advanced 3-D packaging techniques to achieve the highest performance and density. This progression is shown in Fig. 5. In this same vein, recent attempts to place gate driver circuitry onto the same die as the power device may or may not pan out to be the superior solution due to process limitations of the vertical power device technology [81]. However, 3-D power packaging

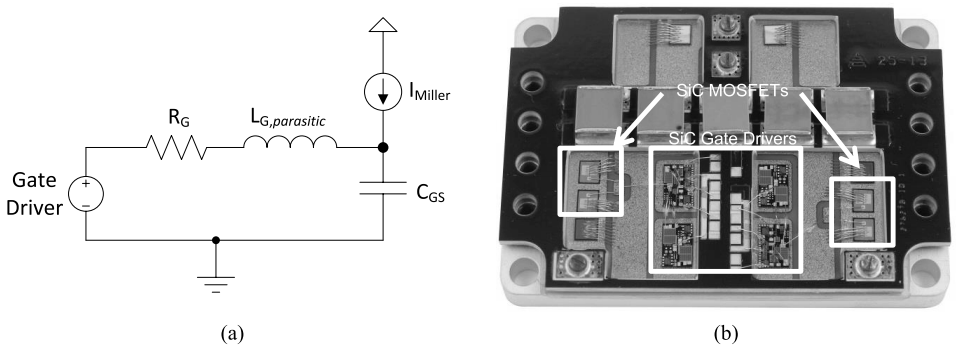

Fig. 4. (a) Equivalent circuit for a gate driver driving an insulated-gate power device in the presence of injected switching (Miller) currents. (b) SiC half-bridge switching module with integrated SiC gate drivers. The integrated gate drivers require no series gate resistance due to the low parasitic inductance. (Photo Courtesy of Arkansas Power Electronics International, Inc.)

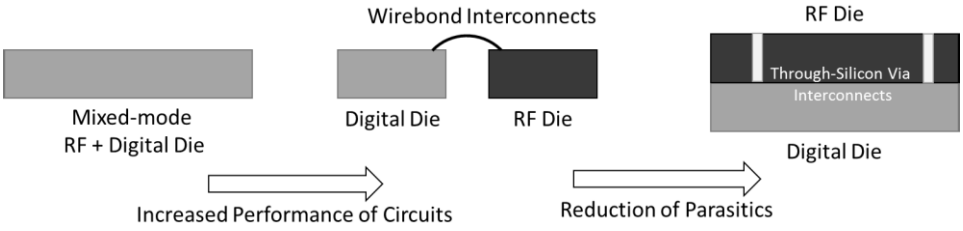

Fig. 5. Progression of mixed-signal integration through time. Using distinct processes allowed optimization of the chip performance, and 3-D packaging allowed reduced parasitics and high density integration.

may yet provide improvements in performance, reliability, and density.

E. Modeling and Optimization

Unequivocally, model-based engineering is required to achieve the miniaturized power electronics of the future. The days when simply building a breadboard and debugging designs until they perform as desired have ended in many fields and power electronics is no exception [82]. The technologies described in Section III all require models in one form or another for the design analyses to occur in advance of circuit and module fabrication. Gate drivers in single-chip integrated form already adhere to a design flow that is based on semiconductor device models for the low-voltage FETs [83]. Power electronic circuit design uses various levels of models depending on the step in the design flow, but physics-based models are needed to account for switching details, thermal issues, and final design sign-off [84]–[89].

The design of advanced power modules requires a simultaneous thermal, electrical, and mechanical analysis to perform the variety of tradeoffs required to achieve a manufacturable and functional design. These analyses are based on models in each domain. Recently, efforts have been pursued to bring these domains together to achieve a degree of design automation for power substrate layouts [90]–[92] some of which involve abstracted models in an optimization framework. As the industry pushes for greater levels of integration additional CAD tools, models, and algorithms will be needed to define a rigorous design flow through which the appropriate analyses are performed to ensure performance, manufacturability, and reliability.

IV. Applications

A. Transportation

The potential impact of wide bandgap induced miniaturization of power systems as applied to the transportation sector is significant. In addition to the reduction of power losses in the motor drive of electric vehicles [93], there are the ever present advantages of reduced weight, smaller footprint, reduction of cooling system complexity, and improved reliability that are all desirable traits for automotive components. The battery charger for plug-in electric vehicles is one example of how wide bandgap materials can reduce size and weight outside of the drivetrain; researchers have recently demonstrated a $>$5 kW, 95% efficient SiC bi-directional battery charger with a volume of 1.2 L and mass of 1.6 kg, reductions of over 75% compared with the commercial Si-based charger it is designed to replace [94]. Generally speaking, miniaturization stands to impact all modes of transportation, whether the power system is on an airplane, a ship, or on a train. All aspects of commercial, private, and military transportation stand to benefit from the traits afforded by power system miniaturization and, thus, the use of wide bandgap materials in those systems.

B. Energy Exploration

While not a large volume electronics industry when compared with others such as the automotive sector, the area of

energy exploration still stands to benefit from the application of wide bandgap devices. In these applications, drilling heads experience temperature rises of at least 10–30 °C for every kilometer of depth and there is a trend toward deeper wells [95]. The sensors, data acquisition, and motor drive electronics in the drilling head must be robust and able to handle high temperatures, high pressures, and high levels of vibration and shock. Miniaturization here allows the packing of more electronics in the available space.

C. Space

Space exploration is fundamentally limited by both mass and volume. Future deep space missions will likely use some type of ion thrust engine due to the improvement in thrust/fuel efficiency versus chemical rocket engines [96]. NASA's Jet Propulsion Laboratory is currently investigating the implications of an all-SiC power processing unit for Hall thrusters consisting of the solar arrays, cabling, power processing, and thrusters. Their studies indicate a potential mass reduction of 30% over a Si solution, primarily in cabling and heat exchangers. These savings are made possible by reduced current and increased device junction temperatures, respectively [97]. Additional design work has been done on the implementation of a SiC converter that drives the Hall thruster and provides thrust modulation [98], [99].

D. POL Conversion

POL conversion has the potential to reduce the power electronic system footprint. By integrating converters into sources and loads, a large central converter may be shrunk or rendered unnecessary. Wide bandgap devices have three specific benefits for POL conversion: reduced size, increased efficiency, and increased temperature range. A GaN nonisolated buck converter with 12 V input, 1.2 V, 20 A output has been built that achieves 86%–91% efficiency and a power density of 1.2 kW/in^3 [100]. A 7.5-kW SiC three-phase power factor correction buck rectifier designed for data center use converted a three-phase 480 V line-to-line input to 400 V dc for distribution inside the data center. This converter achieved losses of less than 100 W compared with nearly 250 W for a converter based on Si IGBTs and diodes, and demonstrated an efficiency of over 98% [101].

The benefit of increased temperature range may either be improved reliability (if actual operating temperature is kept the same), or reduced cooling requirements. In a wind generation system, Si IGBTs are replaced with SiC MOSFETs, but, due to the lower current and voltage ratings of the devices, the number of SiC devices is much higher than Si devices. At a switching frequency of 3 kHz and a junction temperature of 150°, a Si converter is operating at its maximum allowable temperature and achieves an efficiency of 90%. At a junction temperature of 200 °C, a SiC converter's efficiency is still greater than 96%. There is not a significant improvement in the volume of the power switching devices, but due to the increased efficiency and operating temperature of the SiC power devices, the heatsink can be approximately half the volume and air-cooled instead of liquid cooled [102].

E. Grid-Connected Applications

Grid-connected power electronics are not typically considered the application space benefitting from miniaturization. However, in many distribution applications like those involving smart grid devices such as residential power routers, fault current limiters, and solid-state breakers, a smaller footprint is welcomed by the consumer. As the application voltage increases the packaging becomes more important in achieving small volumes.

V. Future

It is easy to envision that wide bandgap device characteristics will continue to improve along with material quality. This path of accelerated growth has been forged in the past with very large scale integration as wafer sizes grew, and so we can gain some insight into the possible gains and performance improvements that might be on the horizon for power electronics. However, there is still much to overcome. The often quoted issue with material quality is elimination of defects in the substrate. It is also important to master the interface states and other long-term reliability factors in the devices so that characteristics do not shift over time under bias. In the case of GaN, there are many issues yet to overcome including sensitive gate drive voltages and vertical device structures for higher voltage operation.

A golden era for power electronics is emerging, just as it did for silicon electronics. The defragmentation of wide bandgap manufacturers will be a part of this process. As winning technologies emerge, mergers and acquisitions may come about, but the resulting new enterprises will result in new markets and new classes of power electronics, producing new devices and enabling applications that are not currently foreseen. For comparison, the global power semiconductor market is currently valued at $135 billion, with SiC accounting for approximately $100 million [103]. The market value of SiC is anticipated to grow to $1 billion by 2019 [103].

The miniaturization of power electronic systems enabled by wide bandgap materials will also open new frontiers in terms of system architectures. The integration of low-voltage devices with power MOSFETs, coupled with advancements made in the area of wide bandgap sensors, sets the stage for all-inclusive power cores that receive control signals wirelessly and require only a power source and a load to operate.

While it is impossible to know the speed at which innovations will occur, it is certain that miniaturization through the use of wide bandgap materials is happening now and will continue to accelerate as it is driven by applications. For anyone involved in the design of power electronic systems, the prospects enabled by wide bandgap material advancement should prove to make the next couple of decades both exciting and memorable.

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