An Optimized PCB High Frequency Parasitic Parameter Elimination Method for GaN Based Driving Circuit

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***Abstract*—In this paper, the switching oscillations of GaN power devices can be predicted accurately by Ansys Q3D high frequency parameter simulation. A ringing optimization method for GaN-Based Driving Circuit is proved to be feasible on the half-bridge standard boards with high switching frequency and low input voltage. And will be used for high frequency hard switching scenarios.**

Keywords—switching oscillation, GaN-based driver circuit, parasitic parameter optimization, buck converter

I. INTRODUCTION

In order to meet the increasing demand of high frequency, high voltage, and high density in power converter designs, wide bandgap (WBG) power devices are gradually considered more promising [1]-[2]. Due to the lower on-state resistance and lower gate charge, GaN HEMTs have smaller on-state and switching losses and also have faster switching speed than silicon devices.[3] However, the switching oscillations which are induced by high-frequency switching can bring about serious negative effects, such as electromagnetic interference (EMI) which may interfere with system operation, voltage overshoots which may destroy the devices, and additional power losses which will decrease converter efficiency and increase operating temperature [4]-[5]. And at the same time, the switching oscillations also bring new challenges to the reliability of power converters, because of the stricter gate drive voltage range of GaN devices.

Using turn-on and turn-off gate resistors is a commonly used method of reducing switching oscillations. However, it is sometimes difficult to achieve the desired effect by simply using driver resistors, for the gate resistances will limit the switching frequency and can do little help to the switch oscillation from drain to source of devices [5]. It needs some other methods as supplementary simultaneously, include RC snubber circuit [6], active gate driver [7], and optimizing PCB layout for instance.[8]-[9]

In this paper, a method of predicting oscillations based on parasitic parameters extracted by Ansys Q3D is proposed. A method of reducing switching oscillations is proposed.

II. MAIN CAUSES FOR SWITCHING OSCILLATIONS

A. The scenario to be applied

This optimization is going to use in a hard-switched GaN-based buck converter as shown in Fig. 1. Its switching frequency is 1MHz, and its input voltage range is 0-30V.

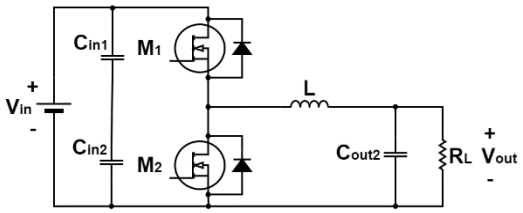

Fig. 1. Circuit schematic of buck converter.

B. Main causes for switching oscillation

For the buck converter, the main parasitic parameters are shown in the Fig. 2. The high dv/dt on C_{gd} and the high di/dt on L_s may lead to a high V_{gs}. The output capacitor of switch C_{oss} may resonate with the power loop parasitic inductor L_{line} to give a parasitic ringing. Both the different structures and packages of devices and the different PCB layout can bring different parasitic parameters which can influence the value of dv/dt and di/dt to affect the switching oscillations.[10]

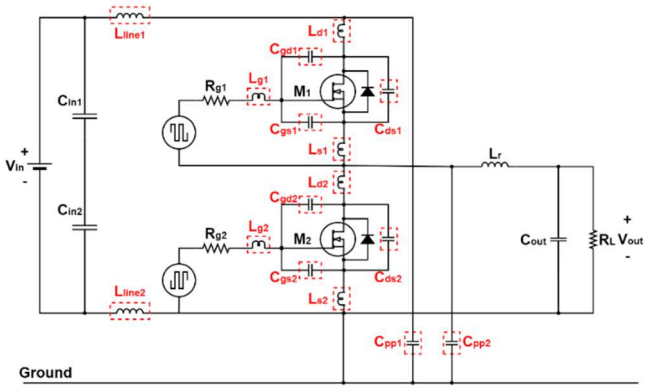

Fig. 2. Main parasitic parameters of LLC converter.

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III. Switching Oscillations Prediction Based on PCB High Frequency Parasitic Parameters

In order to predict and optimize the switching oscillations more conveniently, a half-bridge GaN based driving circuit standard board with high switching frequency and low input voltage has been made. The standard board will work at 1MHz, and the input voltage will be 5V.

Fig. 3 shows the PCB layout of the 1.0Version standard board. Its parasitic parameters at 1MHz which are shown in TABLE I. can be extracted by Ansys Q3D.

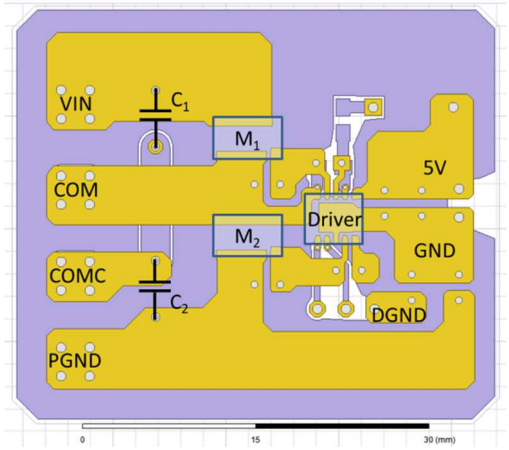


Fig. 3. PCB layout of the 1.0Version standard board.

TABLE I. Parasitic Parameters of 1.0Version Standard Board at 1MHz

Name	Value	Name	Value
C_{pp1}	5.78 pF	L_g	1.76 nH
C_{pp2}	3.94 pF	L_d	0.83 nH
C_{gs}	589 pF	L_s	0.78 nH
C_{gd}	11 pF	L_{line1}	3.77 nH
C_{ds}	300 pF	L_{line2}	6.14 nH

After extracting its parasitic parameters at 1MHz by Ansys Q3D, the time domain waveform of V_{ds1} (green line), V_{ds2} (blue line) and $V_{(COM,COMC)}$ (red line) can be simulated by LTspice as Fig. 4(a). The frequency domain waveform is shown in Fig. 4(b) and the unit of ordinate is μV. The corresponding experimental verification will be shown in Section V.

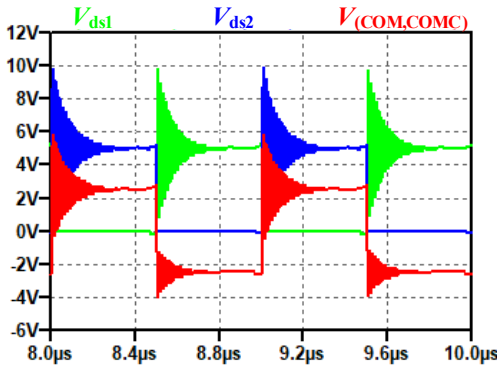
IV. Method of Ringing Optimization for Standard Board PCB Design

A. PCB dielectric layer thickness

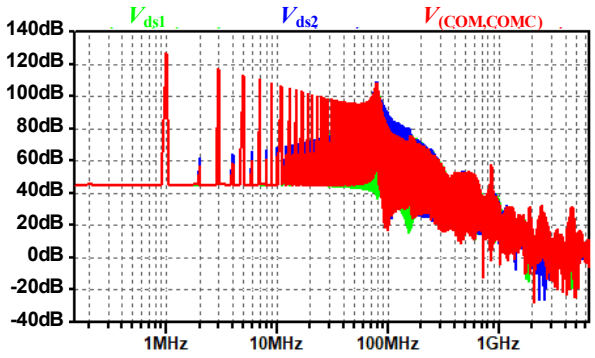
For 1.0Version standard board, three different thicknesses of PCB dielectric layer from 1.0mm to 2.0mm were simulated, to find the relationship between PCB dielectric layer thickness and switching oscillation. TABLE II. shows the variation of parasitic parameters with PCB dielectric layer thickness.

As the PCB dielectric layer thickens, the parasitic inductance of VIAs and PADs increase, but the parasitic capacitance between the copper foil and the ground decreases accordingly.

Fig. 5 shows the time domain waveform and frequency domain waveform of 1.0mm dielectric layer, Fig. 6 shows the waveforms of 2.0mm dielectric layer, and the 1.6mm one has been shown in Fig. 4. And just like before, green line means V_{ds1}, blue line means V_{ds2} and red line means $V_{(COM,COMC)}$.



(a) Time domain.



(b) Frequency domain.

Fig. 4. Simulation results of 1.0Version standard board with 1.6mm dielectric layer.

TABLE II. Parasitic Parameters of 1.0Version Standard Board of Various Thickness at 1MHz

Name	1.0mm	1.6mm	2.0mm
C_{pp1}	7.84 pF	5.78 pF	4.96 pF
C_{pp2}	5.11 pF	3.94 pF	3.44 pF
L_g	1.40 nH	1.76 nH	1.56 nH
L_d	0.68 nH	0.83 nH	0.74 nH
L_s	0.72 nH	0.78 nH	0.82 nH
L_{line1}	3.33 nH	3.77 nH	3.57 nH
L_{line2}	5.35 nH	5.42 nH	5.48 nH

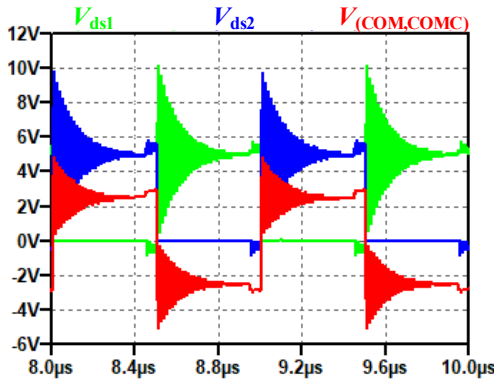
When the VIAs and PADs in the loop are small and the number of them is large, the thinner dielectric layer should be selected on the premise of meeting the insulation requirements. Due to the small number of VIAs and PADs in the 1.0Version standard board, the frequency of the switching oscillation is higher and the total duration of oscillation is shorter when the dielectric layer is thicker. However, the amplitude of switching oscillation doesn't change much when the thickness of the dielectric layer changes.

B. Device package and loop area

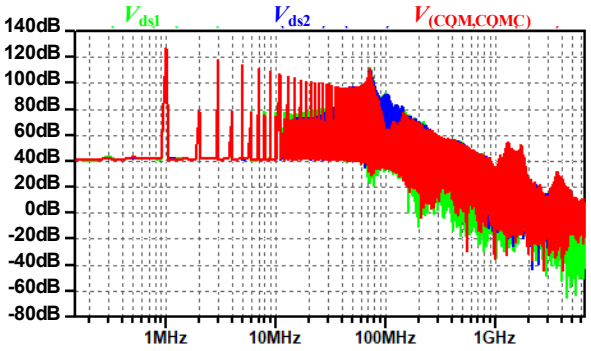
Through parameter scanning simulations of the loop, it can be found that the oscillation frequency can be increased and amplitude of switching oscillation can be reduced, when the loop parasitic parameters are reduced.

Resistors and capacitors in smaller packages generally have better high frequency characteristics and can also reduce the loop area and the loop parasitic parameters. To optimize the parasitic parameters of standard board, here comes the 2.0Version which changes all packages of resistances and

capacitances from 0805 to 0402. In 2.0Version standard board, shown in Fig. 7, the driver loop area is greatly reduced, the power loop area is also optimized, and the RC snubber circuit is reserved for further optimization.

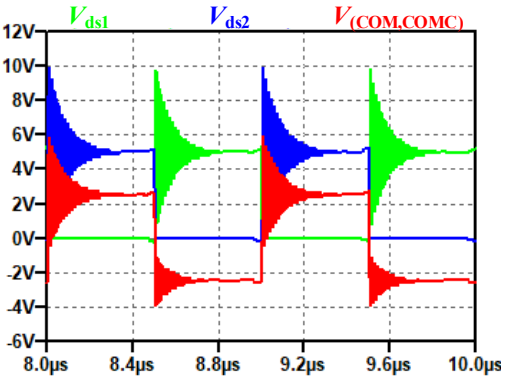


(a) Time domain.

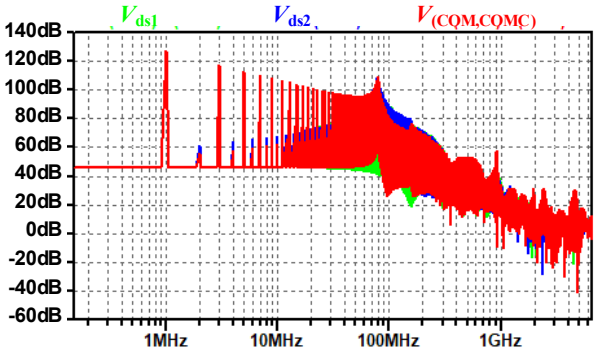


(b) Frequency domain.

Fig. 5. Simulation results of 1.0Version standard board with 1.0mm dielectric layer.



(a) Time domain.



(b) Frequency domain.

Fig. 6. Simulation results of 1.0Version standard board with 2.0mm dielectric layer.

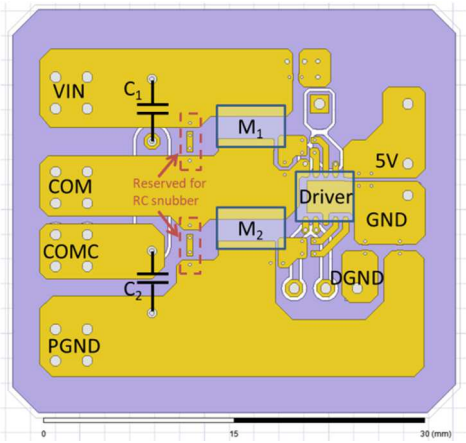


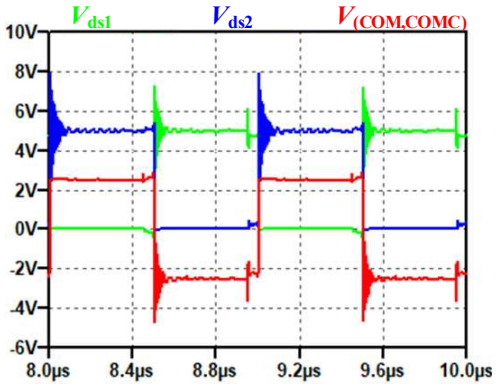
Fig. 7. PCB layout of the 2.0Version standard board.

The parasitic parameters of 2.0Version standard board at 1MHz which were extracted by Ansys Q3D are shown in TABLE III. .

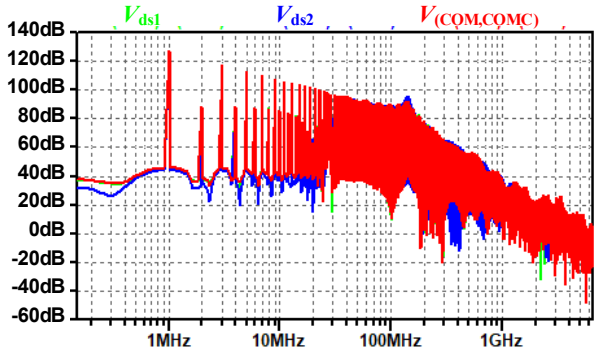
TABLE III. PARASITIC PARAMETERS OF 2.0VERSION STANDARD BOARD AT 1MHZ

Name	Value	Name	Value
C_{pp1}	5.64 pF	L_g	1.23 nH
C_{pp2}	3.49 pF	L_d	0.58 nH
C_{gs}	589 pF	L_s	0.61 nH
C_{gd}	11 pF	L_{line1}	2.77 nH
C_{ds}	300 pF	L_{line2}	5.72 nH

In order to distinguish whether there are RC snubber circuits on the standard board, 2.2Version is used for those with RC snubber circuits and 2.1Version for those without. The simulation results of 2.1Version are shown in Fig. 8.



(a) Time domain.



(b) Frequency domain.

Fig. 8. Simulation results of 2.1Version standard board (without RC snubber).

C. RC snubber circuit

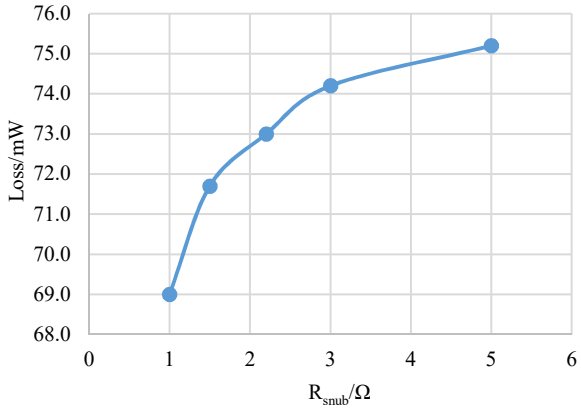
Another method to optimize loop parameters to eliminate switching oscillation is using the RC snubber circuit.

The function of resistor R_{snub} is to generate damping and absorb the resonant energy of the switching oscillation. The function of capacitor C_{snub} is to provide energy channel for R_{snub} to absorb, and the capacitance of C_{snub} determines the degree of absorption, which is related to the amplitude of the switching oscillation.

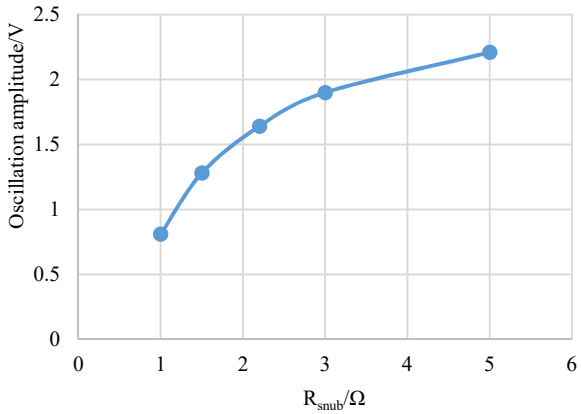
In order to select appropriate R_{snub} and C_{snub} values to make the RC snubber circuit have good suppression effect and low loss at the same time, Fig. 9 and Fig. 10 respectively compare the loss and suppression effect of RC snubber circuit under several groups of different parameters.

By comparison, it can be found that when the snubber capacitance C_{snub} is greater than 3nF, the elimination of oscillation amplitude is not so effective by increasing the capacitance further. Therefore, 3nF is chosen as the value of C_{snub}. If the value of R_{snub} is smaller, the oscillation duration will be longer, and if the value of R_{snub} is larger, the loss will increase. Therefore, choose 2.2Ω as the value of R_{snub}.

Select the RC snubber capacitance as 3nF, resistance as 2.2Ω. [6] The simulation results of 2.2Version are shown in Fig. 11.

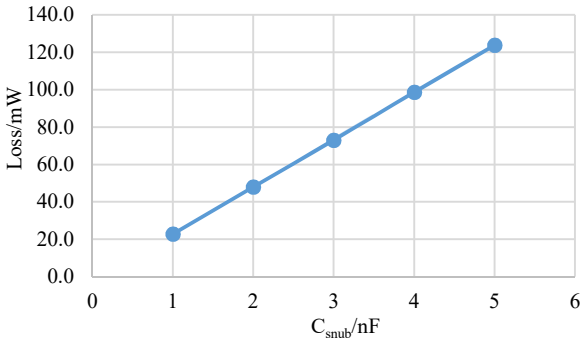


(a) The loss of RC snubber circuit.

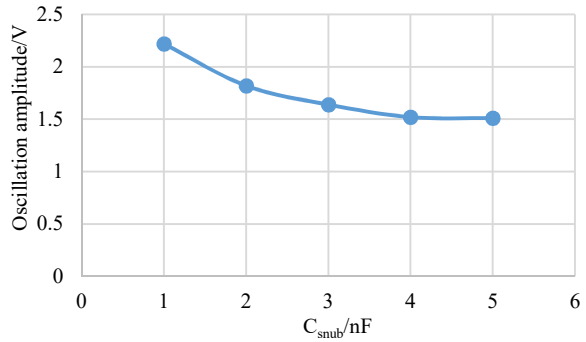


(b) The amplitude of switching oscillation.

Fig. 9. Snubber resistance R_{snub} is 1, 1.5, 2.2, 3 and 5 Ω, when C_{snub} is 3 nF.

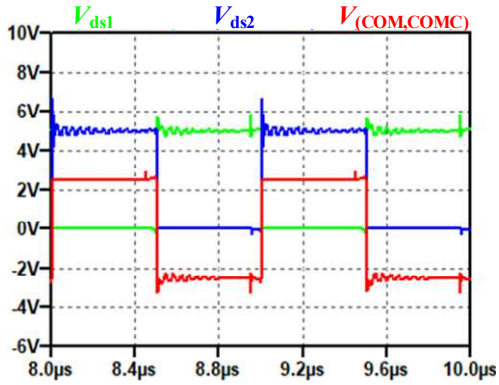


(a) The loss of RC snubber circuit.

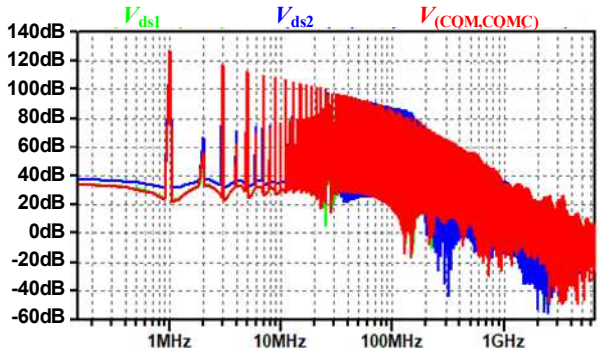


(b) The amplitude of switching oscillation.

Fig. 10. Snubber capacitance C_{snub} is 1, 2, 3, 4 and 5 nF, when R_{snub} is 2.2Ω.



(a) Time domain.



(b) Frequency domain.

Fig. 11. Simulation results of 2.2Version standard board (with RC snubber).

V. Experimental Verification

A. Experimental results of standard board

The photo of standard board prototype is shown as Fig. 12. The experimental results of standard boards are shown in Fig.

13. Due to the similar oscillation characteristics of V_{ds1}, V_{ds2} and $V_{(COM,COMC)}$, only the waveforms of V_{ds2} are shown.

It can be observed from the experimental waveform in Fig. 13 that the oscillation amplitude, oscillation frequency and oscillation time of the actual measured V_{ds1} are almost the same with which were predicted by simulation. The validity of the simulation prediction is verified, which provides a method for forward design of switching oscillation optimization.

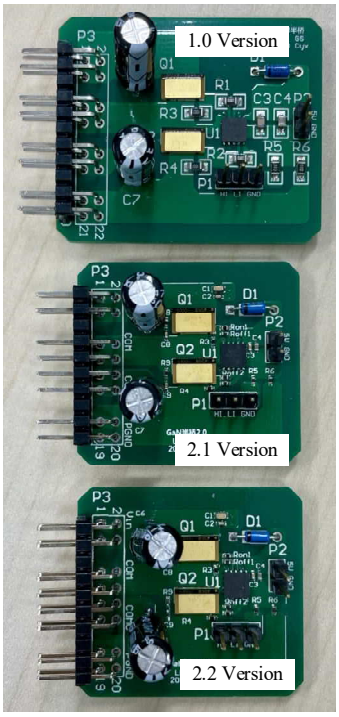
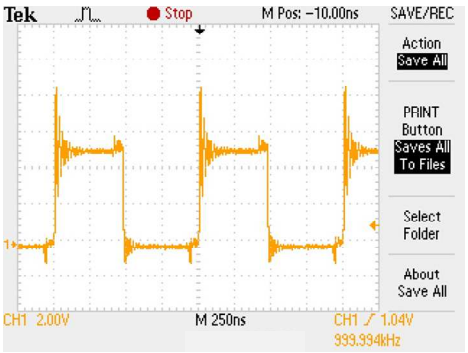
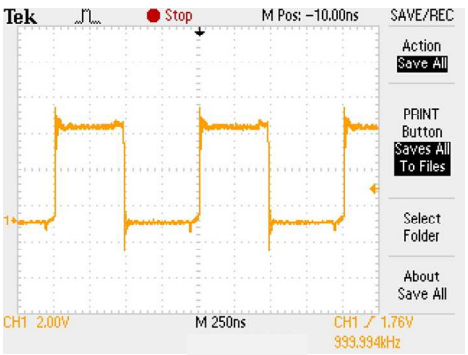


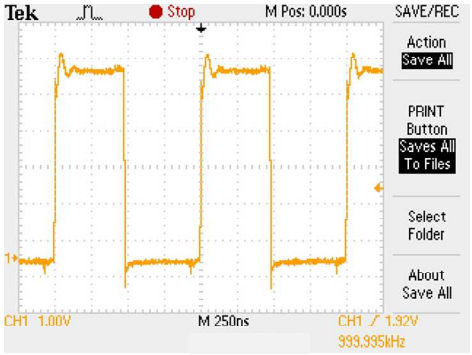
Fig. 12. Standard board prototype. From top to bottom: 1.0Version, 2.1Version, 2.2Version.



(a) 1.0Version



(b) 2.1Version



(c) 2.2Version

Fig. 13. Experimental V_{ds2} of standard boards.

And at the same time, the experimental results also prove the feasibility of several elimination method for GaN based driving circuit in the Section IV.

B. GaN-based buck prototype

The photo of buck prototype is shown as Fig. 14.

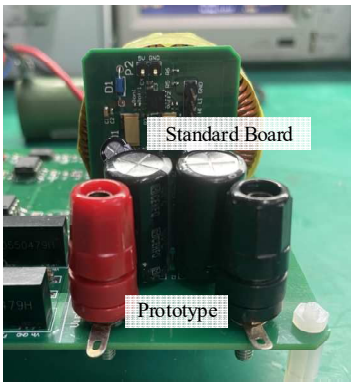
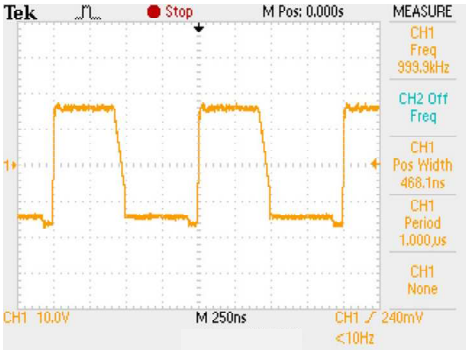


Fig. 14. Photo of buck prototype.

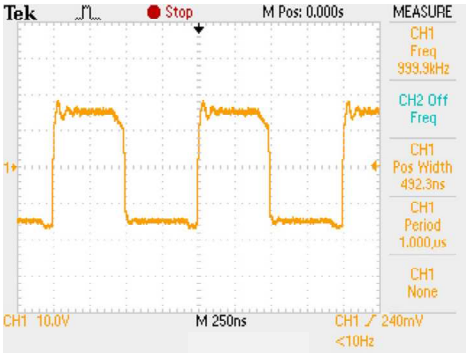
Using the half-bridge standard boards of different version on the prototype shown in the Fig. 14, the drain to source voltage of GaN HEMT can be measured, and its waveform is shown in Fig. 15. By FFT analysis of the time domain waveform obtained from the experiment, the frequency domain waveform of V_{ds2} can be obtained as shown in Fig. 16.

It can be observed from the time domain and frequency domain waveforms that the optimization methods proposed in this paper are feasible on the elimination of the parasitic parameter and switching oscillation of the high-frequency hard-switching converter.

(a) 1.0Version



(b) 2.1Version



(c) 2.2Version

Fig. 15. Experimental V_{ds2} of buck prototype.

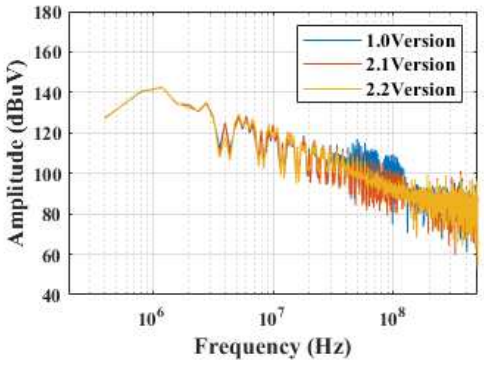


Fig. 16. Frequency domain waveform of Experimental V_{ds2} of buck prototype.

VI. Conclusion

The predicted switching oscillations of GaN power devices by Ansys Q3D high frequency parameter simulation are consistent with the experimental results. To optimize the thickness of PCB dielectric layer, the number of VIAs and PADs in PCB should be considered. Using smaller packages of resistances and capacitances can effectively optimize the high frequency characteristics of the PCB, and optimizing the PCB loop area can effectively reduce switching oscillations of GaN based driving circuit. Adding an appropriate RC snubber circuit can eliminate the switching oscillations without adding too much loss.

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