

PowerSynth: A Power Module Layout Generation Tool

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Abstract—PowerSynth is a multiobjective optimization tool for rapid design and verification of power semiconductor modules. By using reduced order models for the calculation of electrical parasitics of the layout and thermal coupling between devices, optimal trace layout and die placement can be simultaneously achieved orders of magnitude faster than conventional finite element analysis (FEA) techniques. An overview of the tool, its modeling methods, model validation, and module layout optimization are presented. The electrical and thermal models are validated against FEA simulations and physical measurements of built modules generated from the tool. The FEA comparisons are performed with FastHenry and ANSYS Icepak to evaluate electrical parasitics and thermal behavior, respectively. A sample hardware prototype based on a half-bridge circuit topology is chosen for testing. Excellent agreement between the FEA simulations, experimental measurements, and PowerSynth predictions are demonstrated. Additionally, when compared with conventional simulation runtime and workflow, PowerSynth takes considerably less computation and user time to produce several candidate layout solutions from which a designer may easily balance selected tradeoffs.

Index Terms—Design automation, layout, optimization methods, power electronics, semiconductor device packaging.

I. INTRODUCTION

THE field of power electronics is an ever growing one that has experienced several advancements in recent years. Among these are the advent and commercial availability of next generation, wide bandgap (WBG) power semiconductors [1]–[3], and their potential for increasing power density and efficiency while reducing environmental impact [4]–[8]. Some of the benefits afforded by these devices include higher switching

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frequency, faster-switching speed, and higher operating temperature. As a result, the design of WBG power electronics is requiring a fresh look at the capabilities of existing design automation tools and the creation of additional ones to account for the higher frequency effects of these applications. When considering high power density applications of these WBG devices, their high slew rates minimize switching losses and can reduce the size of system-level passive components. Similarly, higher operating temperatures lead to reduced thermal management requirements for the system, potentially reducing size and weight [9]. However, some of the very benefits that WBG devices promote are often hindered by the materials and methods used in packaging them [5], [10]. Some of the major problems that arise in the packaging of WBG devices include electrical parasitics—resistance, inductance, and capacitance—of traces and interconnects, as well as thermal management of the devices.

It is well known that, when the layout parasitics of multichip power modules (MCPM) are coupled with the high di/dt and dv/dt WBG devices are capable of, issues related to voltage and current overshoot and oscillation occur during switching transients [11], [12]. Additionally, when paralleling multiple transistors, a mismatch in device characteristics and branch inductances also leads to current spikes during switching events [13]–[15]. This problem is even more prevalent in high-current modules where voltage overshoot due to layout parasitic inductance can significantly decrease breakdown-voltage safety margins [16]. Current and voltage overshoot are also directly related to electromagnetic compatibility where electromagnetic interference (EMI) is generated due to module parasitics and high slew rates [17], [18]. In general, balanced and symmetrical layouts have been shown to reduce these effects. More recent power module designs incorporating flip-chipped devices and multilayer structures reduce parasitics and EMI by partial cancellation of magnetic fields and mutual inductance between routing layers [11], [19]–[22]. Heterogeneous integration of passive elements within the MCPM in both drive- and power-loops is also among emerging solutions to dampen oscillations and reduce transient overshoot [21], [23]. MCPMs must provide more than just good electrical performance. MCPM packaging must also reliably protect devices and provide sufficient heat removal since ambient conditions and local power dissipation of devices eventually lead to thermal fatigue and failure [24], [25].

During the power module design phase, parameters often ascribed to the reduction of electrical parasitics and

mutual-heating effects of devices in close proximity are often diametrically opposed [26]. For example, increasing the relative spacing among semiconductors will reduce thermal coupling effects at the cost of longer conductors increasing inductance in their drive or commutation loops. Additionally, given the wide range of fields incorporated in the design and fabrication of power modules—from materials science to mechanical and electrical engineering—multidisciplinary expertise is needed in the production of reliable, high-performance modules. This increases the time and cost necessary at all stages of development. Further exacerbating product time-to-market is the extensive use of finite element analysis (FEA) in the early product design stages. While FEA is widely accepted as an important method in providing accurate and reliable simulations of electrical and thermal phenomena in power electronics, it remains computationally expensive and time consuming [26]–[30].

In an effort to approach the multidisciplinary aspect of MCPM design, there have been some efforts by various groups in recent years to develop models, methods and electronic design automation (EDA) tools for this field. Early attempts in this area include using scripting tools and custom interfaces to string together commercial and open source applications for electrical and thermal cosimulation and optimization. For example, the researchers in [30] determine design variables for the geometry of a specific MCPM layout and automated the process of simulating electrical parasitics, device temperature, and module mass using commercial FEA software. The results of these simulations are used as a cost function in a multiobjective optimization process with the layout geometry parameters as design variables. The automation of data exchange between modeling programs enables high accuracy in finding optimal designs. This particular approach is only viable for optimizing an existing design and is very time consuming due to its heavy use of FEA. Yet, it shows significant improvement over performing the evaluations manually in terms of computational time and performance.

Similarly, previous members from the authors' group used the fmincon package in MATLAB to optimize simple layouts in a framework called PowerCAD [26]. In this approach, trace geometry is also used as a design variable to optimize simple MCPM layouts. Electrical parasitics are automatically extracted based on this geometry in FastHenry. A thermal resistance model is also constructed based on the geometry and material properties of the module and is evaluated using a circuit simulator. Like the previous example, these simulated results are used in cost function evaluation during optimization. However, this early prototype—while promising—is also limited in scope, time consuming when extracting electrical parasitics, and the thermal resistor model does not consider thermal coupling of neighboring devices. PowerCAD has since evolved into a more accurate and capable EDA tool known as PowerSynth [31], [32] and is the topic of this paper.

More recently, work described in [33]–[35] approached the optimization of module electrical design through methods found in design automation of very large-scale integration (VLSI) circuits, such as component placement and trace routing techniques. They use a genetic algorithm to optimize for minimal parasitics, paralleled-device parasitic imbalance, and footprint

area. An electrical netlist is combined with physical routing limits that are used by the optimization routine to find a solution with the best fitness. Parasitic resistance is calculated using the method of moments and parasitic inductance is computed using the boundary element method. Progress has been made over the years to extend the capabilities from traditional, wire-bonded module designs to include planar designs as well. They have also simplified their parasitic inductance calculation and are currently working on ways to incorporate device temperature prediction into the cost function using finite difference techniques. Optimized layouts from their work have shown good agreement with electrical parasitics extraction using ANSYS Q3D with the promise of fabricating them and performing measurements in the future.

Other topics in MCPM optimization include one that considers not layout, but rather module layer materials and thicknesses along with environmental and operational conditions to maximize thermomechanical reliability [36]. The authors use thermal and power cycling lifetime models as their cost function. Parameters for these include temperature estimation using a thermal resistor model that includes spreading resistances. They also formulate response surface models (RSMs) using FEA to capture the effects of nonlinear material properties associated with the lifetime models. Their group uses a genetic algorithm to construct a Pareto front of results and find that power cycling and thermal cycling lifetime estimations are in opposition to each other. The limited use of FEA helps to calculate module lifetime under various conditions faster.

The most recent efforts to develop an EDA tool that combines fast, accurate electrical parasitic, and thermal modeling for MCPMs within a multiobjective optimization framework are reported in this paper. The overarching goal is to create a tool that facilitates the design of reliable, high power density WBG power modules. In order to accomplish the goal of maximizing power density while maintaining reliability, it is necessary to account for electrical, thermal, and mechanical effects. The objective of the work reported here is to focus on the time and resources required for the electrical and thermal aspects. Several components of PowerSynth differentiate it from other methods presented in the literature and represent the key contributions of this paper. They are as follows.

- 1) The development and implementation of reduced order electrical and thermal models that have been validated against both FEA simulation and experimental measurements.
- 2) A unique symbolic layout representation of MCPMs that allows users to quickly define a design and populate layouts for optimization—i.e., rapid starting point definition.
- 3) The implementation of a user-extensible technology library and manufacturer design kit (MDK)—ensuring only manufacturable designs are produced.
- 4) Back annotation of layout-extracted parasitics to the original circuit schematic that enables designers to predict layout impacts on circuit performance prior to committing to manufacturing.
- 5) Export of three-dimensional (3-D) layouts to several commercial FEA tools for further analysis as desired.

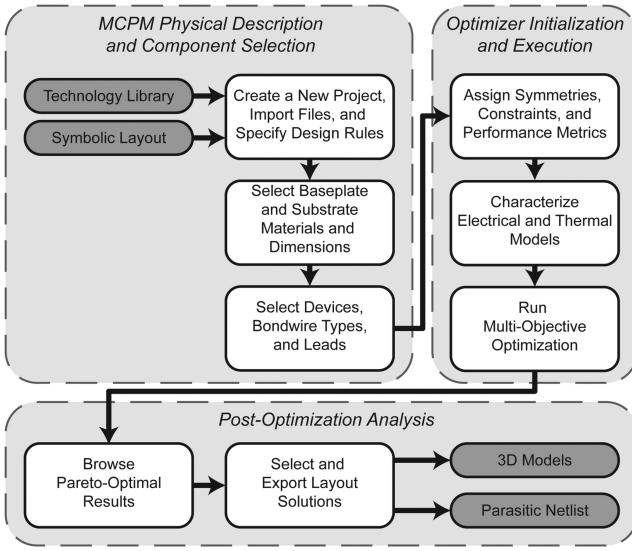


Fig. 1. PowerSynth workflow overview from a user's perspective.

This rich feature set, combined with the hardware-validated models in this paper, form a novel optimization framework that represents a paradigm shift in the design of module-based power electronics.

In Section II, an overview of the software and how it uses a symbolic layout to represent MCPMs for optimization is presented. In Section III, the electrical modeling methods PowerSynth uses to quickly estimate layout parasitics are described. This section also demonstrates how PowerSynth's electrical model compares to both simulated and experimentally measured results. Section IV presents the method used for rapidly and accurately predicting device junction temperature. This thermal model is then compared with simulated and measured results as well. Section V provides a description on how PowerSynth performs layout optimization and presents a case study using said optimization framework. Finally, conclusions and planned future work are presented in Section VI.

II. POWERSYNTH OVERVIEW

A. Software Overview

In its present implementation, PowerSynth functions as a tool to help bridge the gap between systems and packaging engineers by guiding the designer through the process of building-up an MCPM stack, assigning component types, and optimizing the module layout through the use of a graphical user interface. An overview of a typical workflow within the program is shown in Fig. 1 and is explained below.

1) MCPM Physical Description and Component Selection: Upon starting a new project in PowerSynth, the user is tasked with specifying a technology library defining components, their material properties, and dimensions. This can be done either by importing an existing library file or by using the built-in technology library wizard to capture the required information. Currently, this library supports entries for power devices, substrates, device and substrate attachments, heat spreaders, wire bonds, and leads.

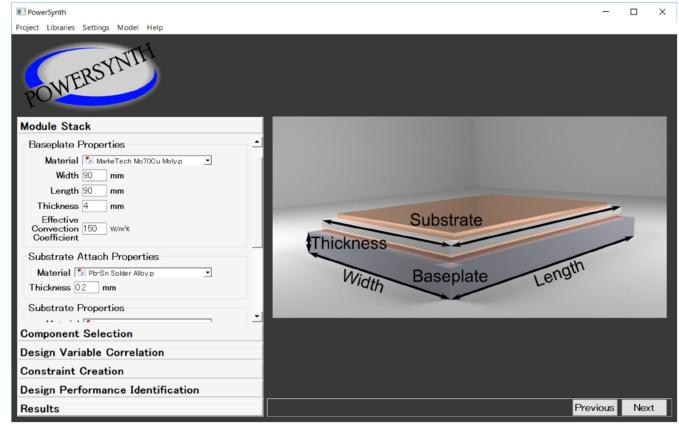


Fig. 2. PowerSynth main window showing the module stack initialization page.

Power devices can either be vertical transistors or diodes. Entries supported for devices include dimensions, thermal properties, and bondwire landing positions for both power and signal wires—as applicable. Substrates are assumed to be the same structure as direct bond copper (DBC), with an insulating ceramic layer between two metallization layers. Within the library, substrate metallization and isolation layer thicknesses along with thermal and electrical properties can be defined. Additionally, thermal properties for substrate and die attach and baseplate can be specified.

The electrical and thermal properties of a chosen bondwire technology may also be input into the technology library. Furthermore, the dimensions of the bondwire, as well as its profile, may also be specified. Finally, leads are treated as either cylindrical lugs or L-shaped terminals in this library. The user may specify whether they are to be used as either power or signal leads and can define their dimensions and electrical properties.

Upon import of the technology library, the user is then presented with the module stack description screen shown in Fig. 2. Here, the designer may stipulate the overall package dimensions along with the substrate, substrate attach, and baseplate components from the technology library. System-level properties such as device switching frequency, ambient temperature, and an effective heat transfer coefficient for the backside of the baseplate must also be input at this point.

Following the module stack description, the user must then import a “symbolic layout” file as described in Section II-C. This symbolic layout essentially defines an initial relative positioning of traces, devices, wires, and leads. After loading this file, the user selects areas on the symbolic layout that define individual devices, bondwire groups, and leads as discussed in Section II-C. Here, the designer may also specify the attachment technology to be used with each device along with their respective, steady-state power dissipation loading.

Finally, the user must incorporate the design rules to be applied as constraints during optimization and layout generation. These rules are defined in a spreadsheet and referred to as the MDK [37]. The MDK contains manufacturer-specific fabrication tolerances and features so that the tool can be customized for processes available by any manufacturing company (e.g.,

Wolfspeed, Danfoss, Semikron, Rohm, Powerex, etc.). Examples of fabrication tolerances include denoting the minimum trace width and spacing, die-to-die and die-to-trace spacing along with bondwire-to-trace and component spacing. By accounting for these constraints, only manufacturable designs are produced by PowerSynth.

2) Optimizer Initialization and Execution: After the above-mentioned parameters are defined, the designer may then specify several items as they pertain to the optimization routine outlined in Section V-A. Correlations may be defined between individual traces so that they may have the same widths, establishing symmetries that can speed up optimization. Constraints may also be applied to traces specifying a minimum, maximum, or fixed width.

The user must also define electrical or thermal performance metrics for which to establish a cost function for the optimization routine. Presently, electrical performance metrics include minimizing parasitic resistance or inductance between two selected nodes within the symbolic layout. Similarly, thermal performance can be specified as a maximum, average, or standard deviation of temperature among selected devices. The final input required by the user before the optimization routine can be executed is simply the number of generations for the genetic algorithm to perform. It is worth noting that the software architecture of PowerSynth is sufficiently open to allow other optimization algorithms to be utilized. An in-depth description of the architecture and alternate optimization algorithms is beyond the scope of this paper, but collaborators from other universities have successfully implemented algorithms into PowerSynth.

Upon running the optimizer, the software will determine if characterization data exists for the electrical and thermal models. If no data exists, a RSM for electrical parasitics will be generated based on the design-space as detailed in Section III. Similarly, if no thermal characterization data exists for the module stack, a thermal-resistor network model of the MCPM stack will be automatically computed as in Section IV. Conversely, if these data sets exist, PowerSynth will skip these characterization steps and proceed to run the optimization until completion.

The multiobjective optimization is now executed. As indicated earlier, many such algorithms could be used to perform this step since the architecture is sufficiently open to enable this. A genetic algorithm was utilized for this activity known as the NSGA-II [43]. This algorithm is chosen since the electrical and thermal performance metrics can be calculated fast enough to evaluate hundreds of layouts in a relatively short time. Additionally, previous work [33]–[35] has shown that a genetic algorithm is feasible and produces good results for this type of optimization. The output from the optimizer is a Pareto frontier of solutions. More details are provided on the optimization activity in Section V.

3) Postoptimization Analysis: Once the optimization routine is complete, a solution browser is presented to the user as in Fig. 3. From this window, a user may select pairs or triplets of performance metrics to see 2-D or 3-D plots of the resulting Pareto frontier, respectively. The user can then interactively examine design tradeoffs along the frontier by selecting a point and being presented with the resulting layout solution. This solution may then be saved for further analysis in external tools.

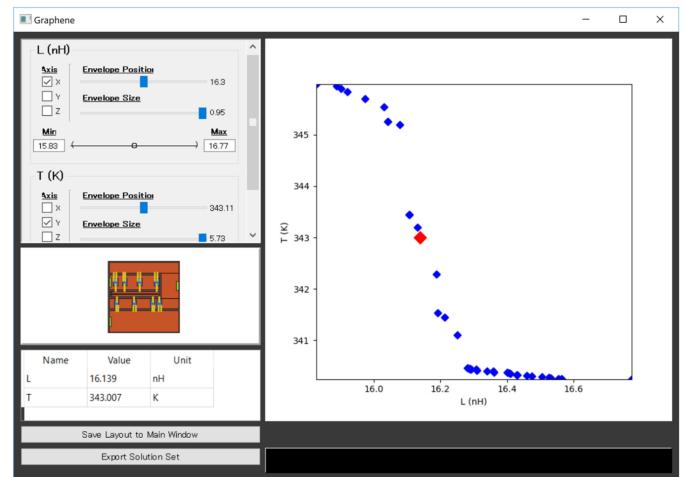


Fig. 3. Solution browser window showing Pareto-optimal results for two chosen performance metrics from which a candidate layout is selected.

Currently, the designer has a few options for exporting a layout solution when using PowerSynth. Solutions may be exported as scripts that will generate 3-D models in tools such as SolidWorks or ANSYS Electronics Desktop for creating mechanical drawings and performing thermal simulations or for further electrical analysis. Additionally, this tool has support for back annotating the parasitics from the layout onto a netlist representation of the module for subsequent analysis in a circuit simulator. This is an important feature enabling the designer to assess the impact of the parasitics on the layout on circuit performance before committing to manufacturing.

B. Assumptions and Limitations

Currently, PowerSynth relies on several assumptions that simplify the problem-space but impose restrictions on the types and varieties of designs that can be optimized using this tool. The following, while not exhaustive, is a description of the main limitations that are to be addressed as research and development continue.

At the moment, PowerSynth assumes that an MCPM is comprised of wire bonded, vertical power devices that are attached to a substrate with a single routing layer. This substrate is, in turn, attached to a heat spreader and must consist of an isolation layer between two metallization layers. In addition to having only one routable layer, traces and wires must follow Manhattan design rules—meaning all interconnects must be orthogonal and there can be no curving traces or non-90° angles among traces and bondwires.

C. Symbolic Layout Representation of Power Modules

In PowerSynth, a symbolic layout is a representation of an MCPM layout without regard to either specific component positions or types, or geometric dimensions and scale. It is similar to stick diagrams found in integrated circuit design. The symbolic layout produces a parameterized layout defined by the design parameters. These design parameters are what will be passed to the optimizer—which is described in Section V. This section

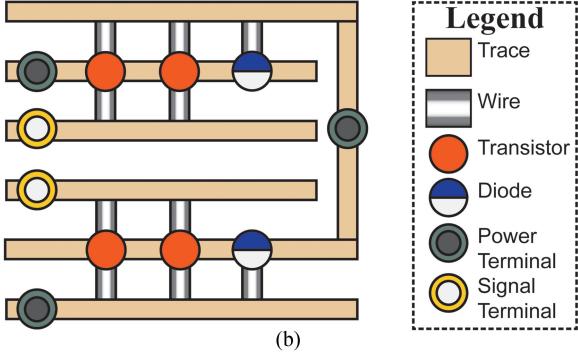


Fig. 4. (a) Plan-view illustration of a simple, half-bridge substrate layout. (b) Symbolic layout representation of the substrate in (a).

provides an overview of how PowerSynth handles traces and components within this framework.

The symbolic layout currently contains only points and lines. Points represent either a device or terminals while lines represent traces or bond wires. In all cases, the user is able to specify what each line or point represents through a graphical interface. Each of these, in turn, can be defined by using the built-in technology library and its associated editor. Fig. 4(a) shows an example of the physical layout of a simple, half-bridge layout with two transistors in parallel with an antiparallel diode in each switch position along with bondwires and power and signal terminals. The corresponding symbolic layout representing this particular design is shown in Fig. 4(b).

The symbolic layout is represented either as a scalable vector graphics (SVG) file or by a set of coordinates representing all of the lines and points and both are generated by the user. Once PowerSynth has read either of these inputs, the constituent line and point coordinates are normalized and only unique coordinate values are stored in lists corresponding to x - and y -components. After normalizing, these lists are combined to produce a 2-D matrix where each entry corresponds to a coordinate. Each entry in this matrix also contains a list of references—or pointers—to the layout objects at those coordinates as shown in Fig. 5.

III. ELECTRICAL MODELING

A. Electrical Model Formulation

Electrical modeling within PowerSynth is handled by converting the symbolic layout representation into a graph-based one. An RSM is generated prior to optimization based on the

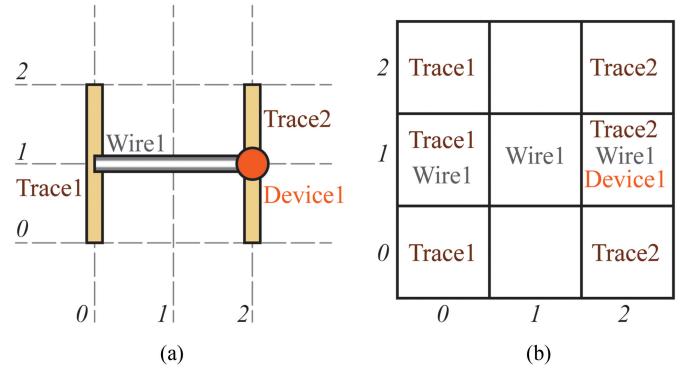


Fig. 5. (a) Example of a normalized symbolic layout and (b) its matrix representation.

substrate geometry with FastHenry to allow for fast calculation of parasitics between each node.

1) *Graph-Based Representation*: Leveraging the symbolic layout mentioned above, a graph-based modeling approach is applied to represent the different module components. Here a layout is described by a set of rectangular traces that are used to construct the graph where nodes represent either trace intersections, or device or lead connections. Edges then contain parasitic inductance and resistance for the trace or bondwire group as well as a parasitic capacitance to the substrate backside metallization. Multiple attributes for each edge are assigned using a key-value pair using the Python package NetworkX [38]. Here, the key is the name of a given attribute (e.g., resistance, inductance, etc.). The value portion of this pair need not be constrained to just floating-point values. In fact, they often include programming objects pertaining to device or lead parameters. A full description of the methodology can be found in [39]. Therefore, only a summary of the main points is presented in this section.

Measurement of the effective resistance and inductance parasitics between any two nodes in this graph can be accomplished. Calculation of the parasitics contained in each edge is done using RSM techniques outlined in Section III-A-2). To make this measurement, two nodes are chosen and the graph is converted to a Laplacian matrix. This is similar to the admittance matrix found in SPICE simulators [40], [41]. In forming this representation, each node from the graph is assigned a unique integer that corresponds to both column and row indices of the Laplacian matrix as shown in Fig. 6.

The effective resistance is measured between the two selected nodes by applying a unitary current flow between them. If this is not a valid path, the software automatically detects this and throws an error, indicating that the user should respecify the points. Since the current flow is 1.0 A, we are left with a case where Ohm's law states that the voltage between these two nodes is equal to the resistance. When using the Laplacian matrix, this value can be defined as follows:

$$R_{\text{eff}}^{s,t} = \mathbf{x}_{s,t}^T \mathbf{L}(G)^{\dagger} \mathbf{x}_{s,t} \quad (1)$$

where $\mathbf{x}_{s,t}$ is the net flow between source s and sink t in vector form. $\mathbf{L}(G)^{\dagger}$ is the Moore–Penrose pseudoinverse of the Laplacian matrix of graph G . Here, $\mathbf{x}_{s,t}$ corresponds to the

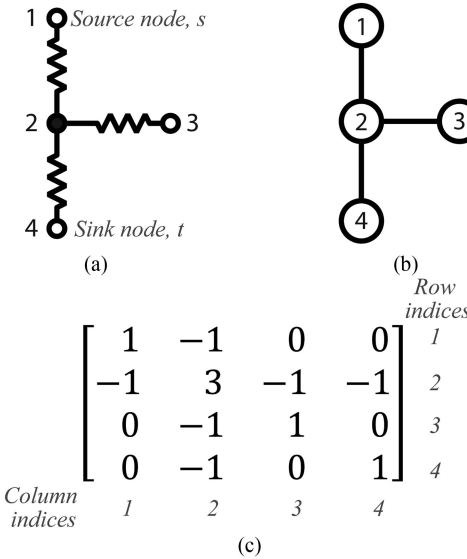


Fig. 6. (a) Parasitic network. (b) Graph representation. (c) Corresponding Laplacian matrix.

node indices in G mentioned above. Also, as shown in Fig. 6, a value of -1 in the Laplacian represents a sink and a value of $+1$ represents a source. All other entries in the vector $\mathbf{x}_{s,t}$ are zero, indicating no other net flows in the system and conserving net current.

Effective inductance is measured in the same way as effective resistance. However, we should stress that using a unitary current, in this case, is not analogous to a real current. Yet, this representation provides a convenient, mathematical aid in computing effective inductance. This was chosen simply because both inductance and resistance share the same rules for parallel and series configurations.

2) Response Surface Modeling for Parasitic Resistance and Inductance Calculation: To the best of the authors' knowledge, analytical formulae for parasitic extraction are not currently available for MCPMs—especially the resistance and inductance of rectangular traces. While similar methods for structures resembling those of MCPMs, such as the microstrip model, are available and can be used as a unit cell of the abovementioned graph theory approach, this was shown to have some prediction inaccuracies in [42]. To overcome these issues, parasitic models built using response surface techniques are chosen as the best candidate for use in PowerSynth.

Response surface modeling is a mathematical model used to create an interpolation between selected design parameters x_1, x_2, \dots, x_k to a chosen response y . This method provides fast and accurate cost functions in an optimization framework that have been chosen to replace computationally expensive numerical simulations. There are three main steps in formulating a RSM. First, a design of experiments methodology is used to define selected design parameters. Then, different design configurations are applied to automate the numerical simulation process in FastHenry. Finally, the RSM can be used to map the design parameter space to the collected simulation responses. Among available RSMs, the Kriging model [43] has

TABLE I
TRACE WIDTH AND LENGTH PARAMETER RANGES

Parameter	Range (mm)
Width (W)	$\left[\text{Design Rule Minimum}, \max\left(\frac{A}{2}, B\right) \right]$
Length (L)	$\left[\max\left(\frac{A}{4}, B\right), \max(A, B) \right]$

been chosen. This model has shown to be the best candidate for parasitic modeling, since it provides interpolated functions that are accurate and smooth.

To correctly model the parasitics of rectangular traces in power module structures, several design parameters are required. This includes the widths (W) and lengths (L) of traces along with their thickness (t) and vertical separation with the substrate backside metal (h). However, it is challenging for response surface algorithms to capture both function accuracy and smoothness for this many variables. In PowerSynth, the graph-based representation above splits the layout into multiple trace cells. Therefore, only two variables (W, L) are used in the optimization loop to calculate the parasitics of each trace. The RSM can be formed using these two parameters, where the rest can be treated as constants.

The reason for this is that h and t do not change for a given substrate technology. Hence, only one RSM needs to be generated for a given design. The range for W and L selection is shown in Table I based on the selected substrate width and length (A and B).

To capture frequency dependent effects, a frequency range for the model can also be defined. For each different geometrical configuration, selected frequency points are assigned to FastHenry simulations. A list of response surfaces can be formed using geometrical design parameters for each frequency value in the range. The skin-depth effect for the rectangular trace structures can be captured by appropriate meshing in FastHenry. The skin depth value given in (2) is computed based on the highest desired frequency value to ensure accurate frequency-dependent prediction over the desired range. This value is then assigned to the smallest trace filament to correctly form the mesh [see Fig. 7(a)]. The following equation is used to estimate the skin-depth value, where δ is the skin depth in m, σ is the conductivity of the material ($S \cdot m^{-1}$), ω is angular frequency, and μ is permeability of the isolation material ($4 \times \pi \times 10^{-7} H \cdot m^{-1}$):

$$\delta = \sqrt{\left(\frac{2}{\omega \mu \sigma}\right)}. \quad (2)$$

Wire bonding remains a standard practice to create interconnects between WBG devices and power or signal traces in MCPMs. Bondwire parasitic inductance can have a profound impact on overall loop inductance and must be carefully considered. During the optimization process, the length of each bondwire group is varied with device position. This causes the electrical parasitics of the bondwire group to change, impacting the total parasitics for a given loop. To correctly capture the

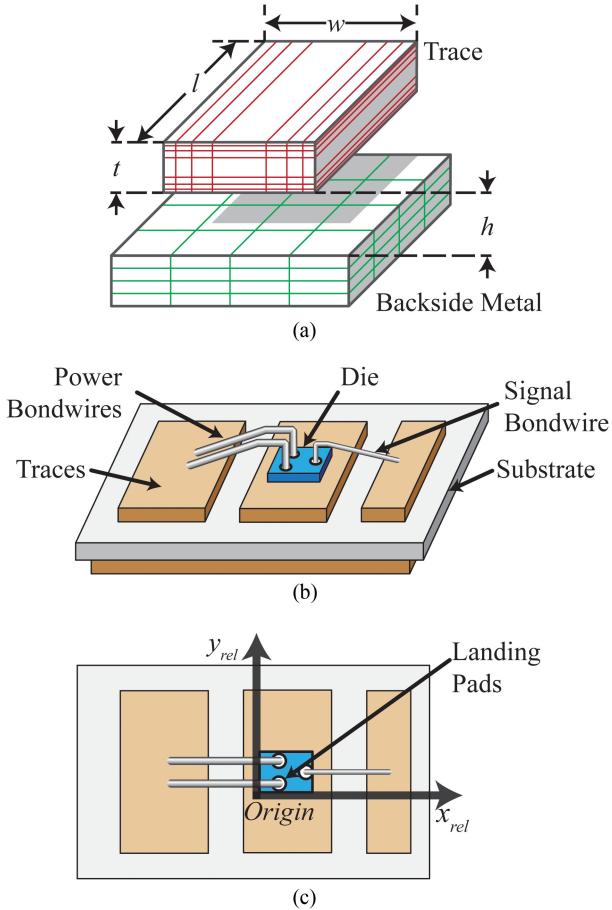


Fig. 7. (a) Example meshing structure for response surface modeling using FastHenry. (b) Perspective view of the bond wire profiles. (c) Plan view of the relative positioning of their landing pads.

parasitic values of each bondwire group, and ensure fast evaluation, FastHenry simulations are run prior to the optimization process. These simulations take into account the user-defined relative bondwire landing locations [see Fig. 7(c)] on a selected device, the number of wires, and the operating frequency.

For both traces and bondwires, PowerSynth automates the process of defining the design-specific parameters necessary to run simulations in FastHenry. The results from these simulations are then used to formulate the RSM. This RSM is then stored in a model library and can be used during the layout optimization routine.

B. Electrical Model Validation

To verify the accuracy of the parasitic modeling method, simulations and experimental measurements are performed on a test vehicle and compared to the electrical model (i.e., RSM) used in PowerSynth.

1) *Electrical Test Vehicle Design:* This sample is built on DBC with a half-bridge layout pattern etched into the top-side copper layer. The dimensions of this substrate are 40×50 mm with the copper and aluminum nitride layers having thicknesses of 200 and $635 \mu\text{m}$, respectively.

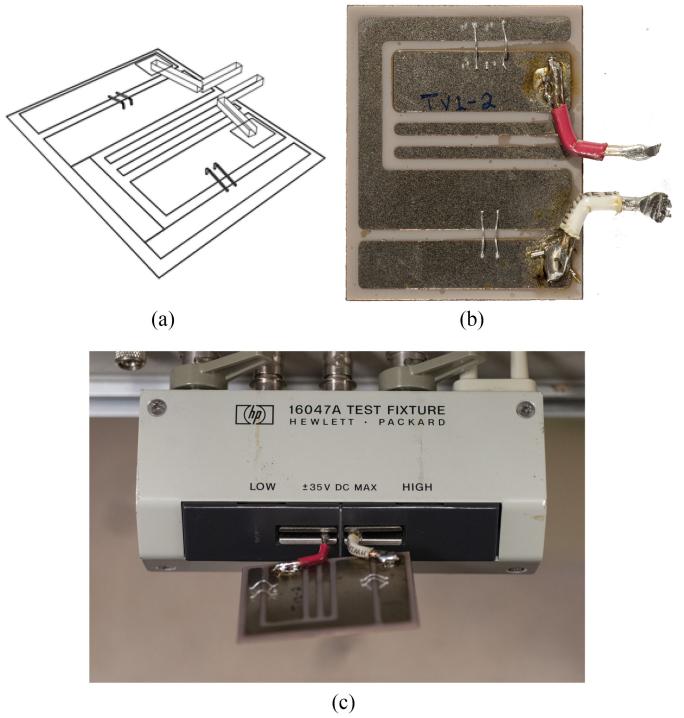


Fig. 8. (a) Electrical test vehicle layout in FastHenry. (b) Electrical parasites measurement test vehicle with wire bonds and attached leads. (c) Test vehicle inserted into the test fixture of the *LCR* meter.

For the electrical measurement test vehicles, no active device is attached to the substrate. Instead, a pair of $300 \mu\text{m}$ diameter aluminum wire bonds are bonded to each location corresponding to where a device would be. In this case, we are considering a single device per switching. Leads are soldered to the substrate where the dc-positive and negative terminals would be to interface *LCR* meter equipment as shown in Fig. 8(b).

2) *Electrical Parasitics Simulation:* The electrical test vehicle is modeled in FastHenry for simulation as illustrated in Fig. 8(a) and with a similar methodology to that outlined in Section III. Here the traces, substrate backside metallization, and soldered test leads are modeled as copper elements with conductivity $\sigma = 5.96 \times 10^7 \text{ S}\cdot\text{m}^{-1}$. Likewise, the wirebonds are modeled as aluminum elements with electrical conductivity $\sigma = 3.77 \times 10^7 \text{ S}\cdot\text{m}^{-1}$.

Simulation of the overall structure is conducted at the same frequency points as those in the *LCR* meter measurement in Section III-B.3—from 10 kHz to 1 MHz. In order to accurately capture the skin effect, the smallest filament size used to discretize the mesh is calculated using the skin depth at 1 MHz. Additionally, in order to correctly model the image current on the backside of the DBC, the backside metallization layer is modeled as a densely meshed grid. The total mesh size for this setup yields 6500 elements.

Using this setup, the simulation is run as a frequency sweep with excitation between the two soldered test leads to extract the parasitic inductance and resistance of the dc loop of the half-bridge layout. However, since PowerSynth does not currently support these types of test leads, a second FastHenry simulation was performed to account for this. In this simulation, the test

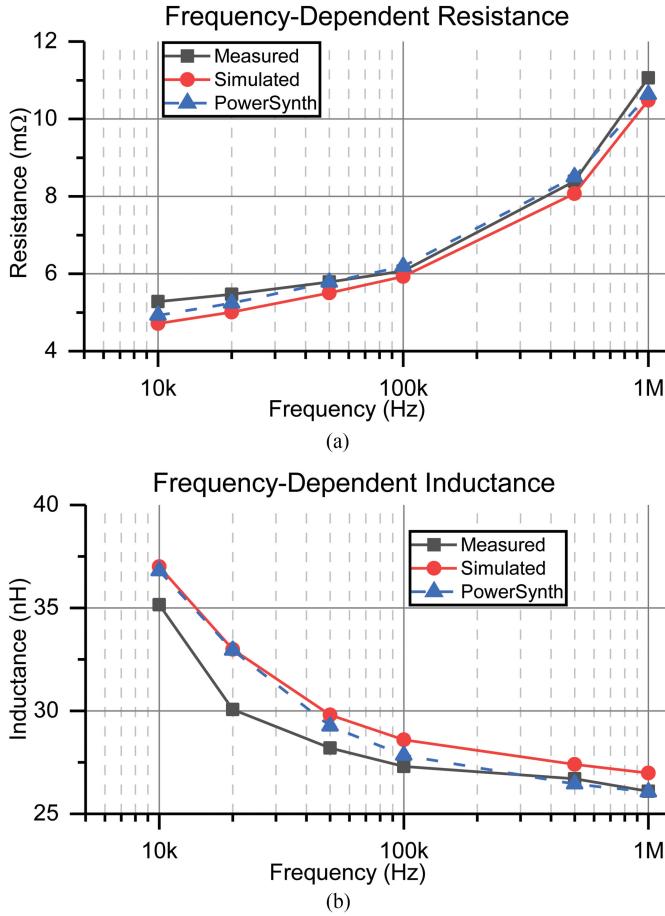


Fig. 9. Results for (a) frequency-dependent resistance and (b) inductance from measurement, simulation, and PowerSynth.

leads are removed and the parasitics are extracted between their respective landing pads. The difference between the FastHenry simulation with and without test leads is added to each calculated value from PowerSynth. The results of these simulations and from PowerSynth are compared with the measured values in Section III-B-3) and shown in Fig. 9.

3) Electrical Parasitics Measurement and Comparison: Electrical parasitics of the test vehicle are measured using an *LCR* meter, model HP4284A, with sample inserted into an HP 16047A test fixture. This setup is used to simultaneously measure both inductance and resistance at several frequency points from 10 kHz to 1 MHz. Prior to measurement, both short- and open-circuit conditions are calibrated at each frequency point. Then, the soldered leads of the DUT are inserted into the test fixture of the *LCR* meter as shown in Fig. 8(c) and inductance and resistance values at each frequency are recorded. Results of this measurement over the frequency range are presented in Fig. 9 where they are compared with those from FastHenry and the RSM used by PowerSynth.

When comparing these results, PowerSynth shows excellent agreement with the values produced by both FastHenry and *LCR* measurements on the test vehicle. In estimating resistance, the average error of the electrical model is only 3% and 4%, respectively, when compared with the measured and simulated

values. The PowerSynth inductance model also closely follows that of the simulated results with an average error of only 2% across the entire frequency range.

Compared with the *LCR* meter inductance results, there is slightly more discrepancy in the low-frequency range where the maximum error is 9.5%. However, these results converge with increasing frequency and an error of only 0.15% at 1 MHz. Furthermore, calculation of parasitics using this methodology shows a significant improvement in evaluation time when compared with FastHenry. Each parasitic calculation using this model takes only 50 ms whereas the simulations took over 300 s to perform, indicating a speed increase of 6000 times. Overall, these results verify that the reduced-order parasitic models PowerSynth uses are sufficiently accurate to serve as a cost function for layout optimization.

IV. THERMAL MODELING

A. Fast Thermal Modeling Methodology

Modeling of MCPMs using thermal resistance networks derived from FEA is a widely accepted practice for which theoretical proofs have been given [44], [45]. For fast evaluation of die temperatures within the MCPM, the module is modeled as a lumped element heat transfer system using thermal resistances. These resistances are initially characterized using the finite element method (FEM) and then the spatial superposition of die temperature and heat flux is employed to predict changes in thermal resistance and heat spreading. The method employed here is presented in detail in [31] and summarized in this section.

The module itself is treated as a stack of different layers corresponding to the materials used, as illustrated in Fig. 10. Heat transfer through the stack is dominated by heat conduction through the various layers. Heat removal due to convection is considered at the backside of the bottom layer—in this case, the baseplate or heat spreader—and is modeled using an effective heat transfer coefficient. For these calculations, the effects due to radiation are minimal and therefore assumed to be negligible. Furthermore, only steady-state thermal conditions are considered in this method.

To begin with, material thermal resistance is defined as follows:

$$R_{\text{TH},i} = \frac{T_i - T_{i+1}}{P_i} \quad (3)$$

where T_i and T_{i+1} are the average temperatures at the start and end of a layer and P_i is the average heat flow in Watts through the layer. Each layer is shown in Fig. 10 with their corresponding thermal resistances. Every resistance value in this thermal circuit is constant except for those pertaining to spread resistance R_{sp} . The devices are modeled as heat sources with a constant power dissipation and a series material resistance and die-to-trace spread resistance $R_{sp,j}$. The die spread resistance varies based on die position and trace layout. Similarly, $R_{sp,trace}$ is the spread resistance of the traces, but only depends on trace geometry. The remaining resistances define the thermal resistance of the traces and sublayers.

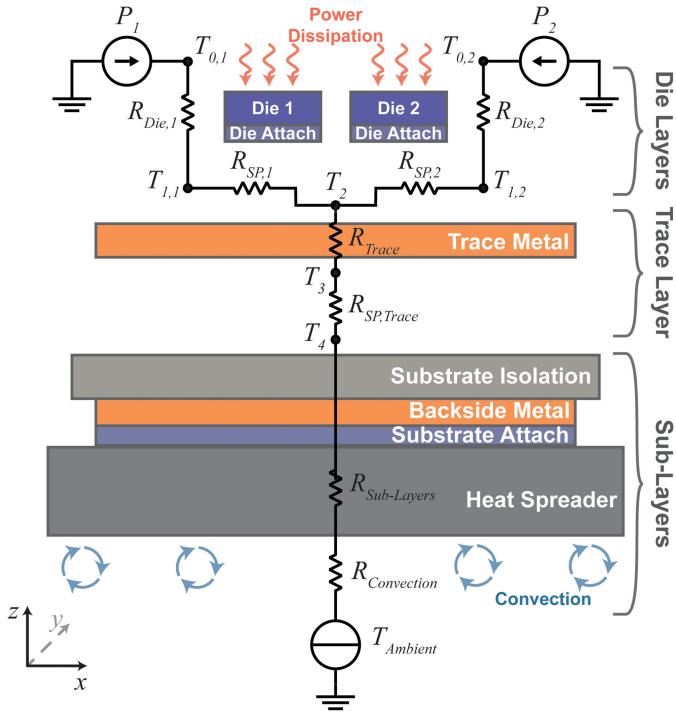


Fig. 10. Exploded cross-section of the MCPM layer structure for thermal modeling with thermal-equivalent circuit overlaid.

To ascribe values to each of these resistances, an FEM model is automatically generated to run a single, steady-state thermal simulation on the module layers for characterization for each device type. An individual die is considered at the center of the top layer of the module stack. The two substrate metal layers are treated as rectangular prisms without trace etching. A constant heat source is placed on the die surface and temperature and flux values at the top side of the isolation layer are mapped to a regular grid. This mapped data is used to construct a set of rectangular contours S_n for both temperature and heat flux magnitude as shown in Fig. 11(a). This format allows for an efficient representation of the temperature and heat flux distributions, enabling fast calculation at the contour intersections during the superposition calculation. The height, or value, of each contour is defined as the average of the distribution contained within it. This value is calculated via numerical integration by simply averaging the mapped values.

For each device, the value of $R_{SP,n}$ changes with die placement and trace layout and is defined as follows:

$$R_{SP,j} = R_{C,j} + R_{E,j} \quad (4)$$

where $R_{E,j}$ is the edge-effect resistance and $R_{C,j}$ is the thermal coupling resistance for each device j . $R_{E,n}$ captures the effect of increased thermal resistance due to a decrease in thermal conduction as a device is positioned closer to an edge. $R_{C,j}$ then defines the increase in thermal resistance of a die as devices are placed closer together and their respective mutual heating effects increase die temperature. The superposition of neighboring die temperature distributions is used to calculate this value. As the device temperature contours are translated into position, the intersection of these contours with a die footprint is used to find

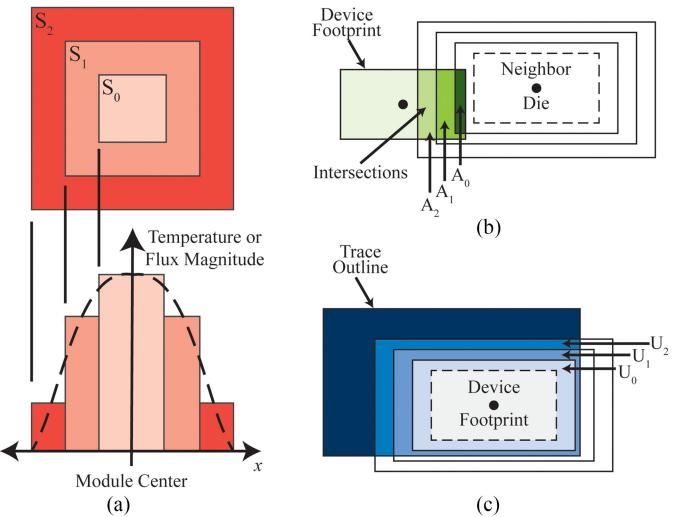


Fig. 11. Thermal modeling illustrations. (a) Rectangular contour representation with temperature and flux distribution. (b) Thermal coupling intersections. (c) Edge effect intersections.

the average contribution to the device under consideration as shown in Fig. 11(b). $R_{E,j}$ is determined in several steps. First, the heat flux distribution is again used to determine the heat conduction around the device. Next, heat flux contours for each die are translated to their respective die positions and checked for intersection with a set of trace rectangles representing the module layout Fig. 11(c). This trace scaling data is used to calculate the effective heat flux through intersecting contours and provide the value of $R_{E,j}$.

Once all the thermal resistance values are known, an impedance matrix is built using the topology of the heat transfer circuit in Fig. 10. A vector comprised of heat flows from their respective devices is used with the thermal impedance matrix using linear algebra techniques to solve for the average temperature of each device during the optimization routine.

B. Thermal Model Validation

While the thermal model developed in this paper is inherently one-dimensional, the inclusion of R_{SP} ensures that trace-edge-to-die proximity and thermal coupling among devices can be captured and accounted for during optimization. To verify the accuracy of this method, both single- and multi-chip per switch position versions of the same test vehicle are simulated, fabricated, and experimentally measured to compare with the fast-thermal model in PowerSynth. Furthermore, since cooling of MCPMs can be accomplished in many ways, these trials also consider both natural convection and forced-air heat sinks. This section also details the steps necessary to provide an equivalent heat transfer coefficient that can be used in PowerSynth, regardless of heat sink type.

1) *Thermal Test Vehicle Design:* The thermal measurement test vehicle [see Fig. 12(b)] employs discrete, TO-252-packaged thick-film resistors soldered directly to the same DBC substrate as in Section III-B.1) in lieu of active devices. This was done for several reasons, but primarily because they eliminate the need

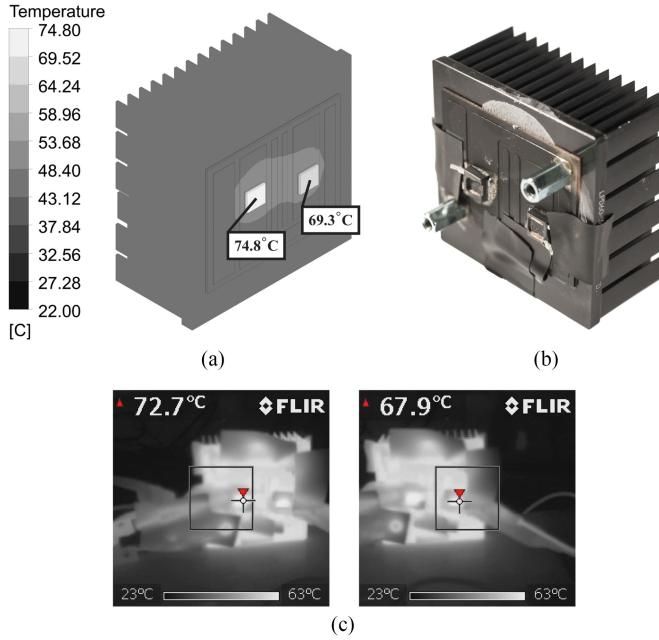


Fig. 12. (a) Thermal simulation model and results at 10 W total power dissipation and 22 °C ambient temperature. (b) Photograph of the thermal test vehicle. (c) IR camera data for the test vehicle under the same conditions in (a).

for complicated temperature calibration required when measuring transistors. These resistors each have a value of $470\text{ m}\Omega$. To ensure proper temperature measurement via the IR camera, each package was first milled out to expose the thick-film layer and eliminate the high thermal resistance over-mold compound. As a final preparation step, the resistors and substrate are coated with a light application of matte-black spray paint (emissivity, $\varepsilon \approx 0.90$) for use in calibrating the IR camera during measurement. The substrate is then mounted to a passive, air-cooled heatsink using a thermal interface grease for measurement. This heatsink is made of black-anodized, extruded aluminum with base dimensions of $60\text{ mm} \times 60\text{ mm} \times 4\text{ mm}$ and is comprised of 84 regularly spaced fins of dimensions $8.35\text{ mm} \times 0.85\text{ mm} \times 26\text{ mm}$.

2) Thermal Simulation: The thermal test vehicle shown in Fig. 12(a) is simulated using ANSYS Icepak computational fluid dynamics (CFD) software. The entire test vehicle structure, including the heat sink and fins, are modeled in 3-D and within an air box of dimensions $160\text{ mm} \times 360\text{ mm} \times 175\text{ mm}$. The air box is modeled as having openings everywhere except immediately below the test vehicle—where it is modeled as an impermeable, adiabatic boundary.

Boundary conditions for this setup also include power dissipation from the two resistors, a gravity vector of 1.0 g in the negative y -direction, radiative heat transfer of the heat sink, and an ambient temperature of $22\text{ }^{\circ}\text{C}$. A summary list of layers, dimensions, and materials used is presented in Table II. Here, an approximate thermal conductivity for the resistors is calculated from the dimensions and thermal conductivity ($R_{TH,J-C} = 5\text{ KW}^{-1}$) given in the datasheet [46]. Power dissipation for each heater resistor is determined by the thermal measurement results in Section IV-B.4). The solver is set to

TABLE II
THERMAL SIMULATION LAYERS, DIMENSIONS, AND MATERIALS

Layer	Material	Area (mm^2)	Thickness (mm)	Thermal Conductivity ($\text{Wm}^{-1}\text{K}^{-1}$)
Heat Sink Base	Al	60×60	4.0	205
TIM	Thermal Grease	50×40	0.025	4.5
Substrate Backside Metal	Cu	50×40	0.2	387.6
Substrate Isolation	AlN	50×40	0.635	180
Traces	Cu	Varies	0.2	387.6
Die Attach	SnPb	6.82×6.35	0.1	50
Resistor	--	6.82×6.35	1.0	4.62

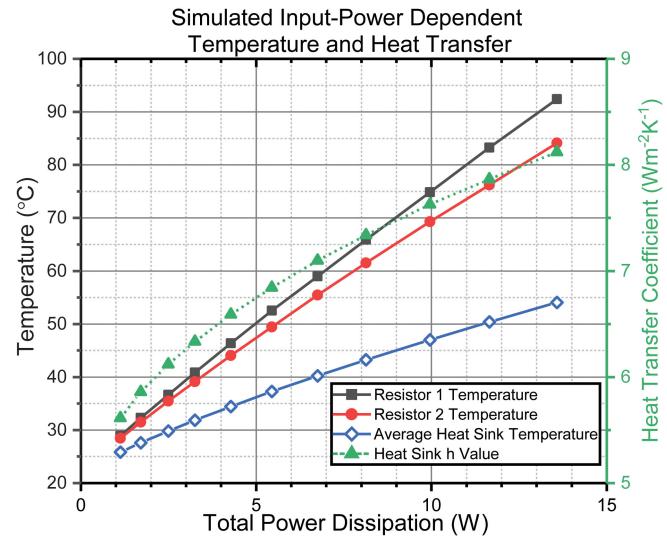


Fig. 13. CFD simulation results for the test vehicle showing resistor temperatures, average heat sink temperatures, and the heat transfer coefficient of the heat sink all as a function of total power dissipation. Ambient temperature is $22\text{ }^{\circ}\text{C}$.

calculate steady-state temperature and pressure using natural convection and turbulent-flow conditions. The results of these simulations are shown in Fig. 13 where the temperatures of each resistor, the average temperature of the heatsink, and the heat transfer coefficient of the heat sink are presented as they change with overall power dissipation.

3) Equivalent Heat Transfer Coefficient Determination: It should be noted that while the CFD simulation accounts for convection and radiation for a detailed 3-D heat sink, PowerSynth does not. Rather, PowerSynth uses the bottom surface of the baseplate layer as a planar boundary for which the user may supply an equivalent heat transfer coefficient representing the setup of their thermal management system. For example, given the surface area of the heat sink ($A_{HS} = 4.83 \times 10^{-2}\text{ m}^2$) and the baseplate surface area ($A_{BP} = 3.6 \times 10^{-3}\text{ m}^2$), an equivalent heat transfer coefficient can be determined using a ratio of these two surface areas and defined as $\Gamma_A = A_{HS}/A_{BP}$. Given this surface area ratio, the equivalent heat transfer coefficient to

use in PowerSynth can be computed from the simulated data as follows:

$$h_{\text{equiv}} = \frac{P_{\text{total}}}{A_{HS} \Delta T_{HS-A}} \cdot \Gamma_A \quad (5)$$

where P_{total} is the total power dissipation in W and ΔT_{HS-A} is the temperature difference (K) between the heat sink and the surrounding air. In this example, h_{equiv} is approximately 13.4 times that of the value of h_{HS} from the simulation and the results of using this value PowerSynth are shown in Section IV-B.4).

As an aside, it is important to note that the process of computing h_{equiv} from CFD simulation is performed here to provide the closest comparison possible when validating the PowerSynth thermal model. In practice and using the steps above, users may easily convert known heat transfer coefficients or thermal resistance values from simulations or datasheets pertaining to their chosen thermal management system. Once layout optimization in PowerSynth is complete, users may then export a chosen solution for final validation using FEA.

4) *Thermal Measurement and Comparison*: Thermal measurements are conducted in an open lab environment with the sample on a test bench. Temperature readings of the resistors are taken using a FLIR i7 infrared camera. During measurement, ambient temperature is recorded using a K-type thermocouple placed approximately 30 cm from the heat sink fins so that the change in resistor temperature relative to ambient can be determined.

In this setup, the two resistors are connected in parallel with an Agilent E3634A bench-top power supply providing the heating current to each device. The thermal measurements are conducted over a range of total input currents varying between 2 and 7 A. A Tektronix TPS 2024 oscilloscope is used to measure the voltage across and current through each resistor with Tektronix P2220 and A622 voltage and current probes, respectively. Readings from these probes are used to accurately calculate the power dissipation in each resistor due to Joule heating at the time of temperature measurement.

Due to the large thermal capacitance of the test vehicle heat sink, an initial calibration step is necessary to determine the proper amount of dwell time between sampling intervals required for the resistor temperatures to reach saturation. This is done by fixing the input current at 7 A and checking the temperature at regular time intervals. From these data, it is determined that saturation is reached after 30 min. Therefore, all subsequent readings are taken at 30-min intervals by measuring and recording the ambient temperature via thermocouple and the temperatures of the left- and right-side resistors with the IR camera. Example results for these measurements—alongside those from the CFD simulation—at 10 W total power dissipation are shown in Fig. 12(c). Additionally, a summary comparison of the simulation and measurement results with the PowerSynth approximations are presented in Fig. 14. Here, the temperature rise for each resistor is shown versus the total power dissipation between them at each test condition.

Comparing the simulation and measurement results of these tests to those of PowerSynth shows the accuracy of the fast-thermal model used to approximate die temperature. This model has an average relative-error between simulation and

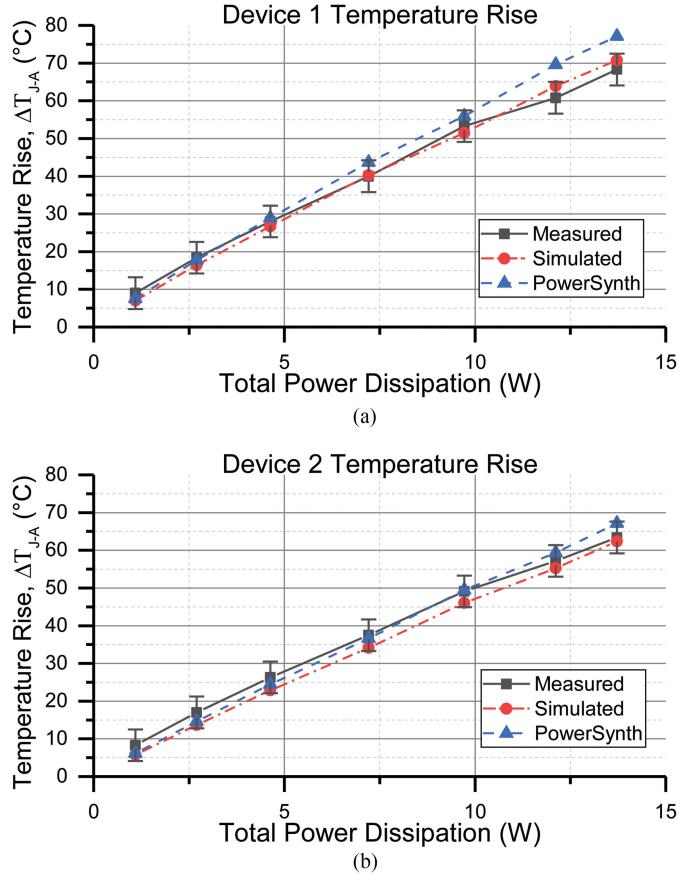


Fig. 14. Results for temperature rise in resistor device (a) 1 and (b) 2 from measurement, simulation, and PowerSynth.

measurement of approximately 4%. The maximum error occurs at higher input power between PowerSynth and the measurement. In this case, errors for device 1 and device 2 are approximately 10% and 6.5%, respectively. For reference, the main sources of error in the measurement setup include the accuracy of the IR camera and thermocouple which is ± 2 °C and ± 2.2 °C, respectively. Additionally, evaluation of a single data point using CFD software takes, on average, 520 s. However, the fast-thermal model in PowerSynth only requires 60 ms for evaluation. Like the electrical modeling results in the preceding sections show, this thermal modeling approach is well suited to provide quick junction temperature estimation for use in an optimization cost function.

5) *Thermal Coupling of Multichip Modules*: In order to verify the thermal coupling of the fast thermal model in PowerSynth, a second test vehicle is fabricated to compare this model among simulated and experimental results. This test vehicle has two devices per switch position and utilizes the same footprint and layout as the two-device version above. Additionally, trials of this four-device module have been conducted using both passive and active heatsinks. The passive heatsink remains the same as above while the forced air heatsink uses a fan for heat removal. A picture showing the four-device module and forced air heatsink are shown in Fig. 15. In comparison, test results where each device is dissipating approximately 4 W of power are compiled in Table III. Throughout these trials, simulation



Fig. 15. Multichip thermal test vehicle mounted onto forced-air heatsink and fan.

TABLE III
TEMPERATURE RISE COMPARISON

				Temperature Rise (°C)		
Cooling	Device Count	Device Position	Power	Measure	Sim	Power Synth
Natural	Two	1	4.5	43.4	43.9	47.4
		2	3.6	39.5	39.5	42.1
	Four	1	3.5	55.7	53.8	53.6
		2	3.6	56.4	53.1	52.0
		3	3.8	55.1	54.3	52.0
		4	3.8	56.5	55.1	55.0
	Forced	1	3.6	15.3	20.0	20.6
		2	3.9	15.5	21.6	22.1
		3	3.6	14.7	20.2	20.8
		4	3.9	16.0	21.5	22.1

and measurement are in close agreement. However, a slightly wider margin of error between simulation and measurement can be found between the simulated and measured results that employ active cooling. Regardless, PowerSynth is able to closely approximate the simulated results with an average error of 3.2% and a maximum error of 8.0%. These data indicate that the model PowerSynth uses to approximate die temperature preserves thermal coupling among devices.

V. LAYOUT OPTIMIZATION

A. Multiobjective Optimization

Due to the multidisciplinary nature of power module design, PowerSynth uses an *a posteriori*, multiobjective optimization framework when evaluating the design variables of an MCPM layout. Here, the electrical and thermal performance models described in Sections III and IV, respectively, are used within the cost function as a way of measuring performance for a particular layout selection. This approach eliminates the need

to manually explore the design space by producing a Pareto frontier of solutions.

The NSGA-II [47] algorithm was chosen for the optimization routine, since the objective function can be formulated algorithmically without the need for closed-form equations. Implementation is achieved through the use of the DEAP library [48] in Python. This implementation requires several parameters to be passed to it, including, but not limited to: a list of design variables with initialization and constraints; the number of objective functions, the population size for a generation, the size of the offspring population, the number of generations for the algorithm to run, the probability of mutation, and the probability of crossover.

The constraints for each design variable are defined on a range by providing a minimum and maximum value. Design variables are then initialized randomly from a normal distribution formed on the interval of their constraints. These values form a vector for each design variable that is used to create the genetic information for each individual in a generation of constant population size. The individuals with the best fit are chosen for reproduction, forming the next generation. Mutations randomly perturb a given design variable for an individual solution while crossovers swap values between the variables of two individuals. The NSGA-II algorithm allows for quick sorting of nondominated individuals and best fit is determined through crowding—where individuals in more sparsely populated regions of the Pareto frontier have higher fitness.

One of the requirements of the chosen optimizer is that the number of design variables must be known beforehand. It should be noted that the number of design variables can be reduced if the user opts to specify design correlation parameters. This lets the user select different components or traces and assign symmetrical positioning or spacing among them. The number of design variables is then extracted from the symbolic layout. For devices, this is a straightforward count of the number of devices. However, for the traces, a trace-specific matrix must be analyzed to determine the number of trace-related design variables. For this to occur, the substrate dimensions are user-specified and fixed. This puts boundaries on the trace specifications as they are all contained within the substrate extends. Additionally, user-specified design rules dictate the minimum spacing between traces and offset from the substrate edge. Traces are then assumed to expand as much as possible within these constraints. Analysis of this trace-specific matrix is done via an algorithm separated into horizontal and vertical scans of the columns and rows of this matrix, respectively. Upon completion, the algorithm provides a list of design variables for the traces, an example of which can be seen in Fig. 16. Once the design variables are extracted, trace layout generation is accomplished in a similar fashion to the analysis algorithm.

After trace layout generation, component placement is carried out. Each device-position design variable is defined on the interval $[0, 1]$ where its center is then placed proportionally along the length of its parent trace. Signal and power bondwires are then placed relative to their parent device and contain no design variables. Finally, leads are placed relative to their position on the symbolic layout. After layout and placement, the solution goes through a design rule check process. The design rule

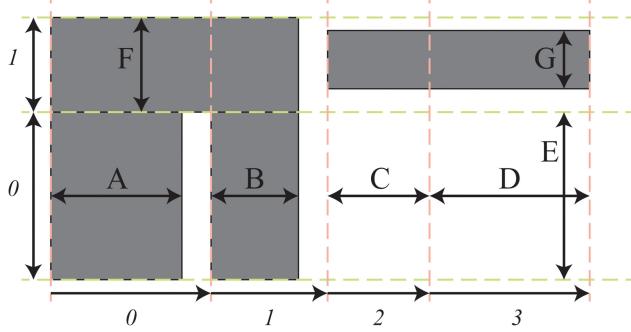


Fig. 16. Sample trace layout matrix with design variables labeled A–G.

TABLE IV
MCPM DESIGN RULES

Design Rule Description	Label
Min. trace-to-trace (gap) width	A
Min. trace width	B
Min. die-to-die distance	C
Min. die-to-trace distance	D
Min. power bondwire landing-to-trace distance	E
Min. signal bondwire landing-to-trace distance	F
Min. power bondwire landing-to-component distance	G
Min. signal bondwire landing-to-component distance	H

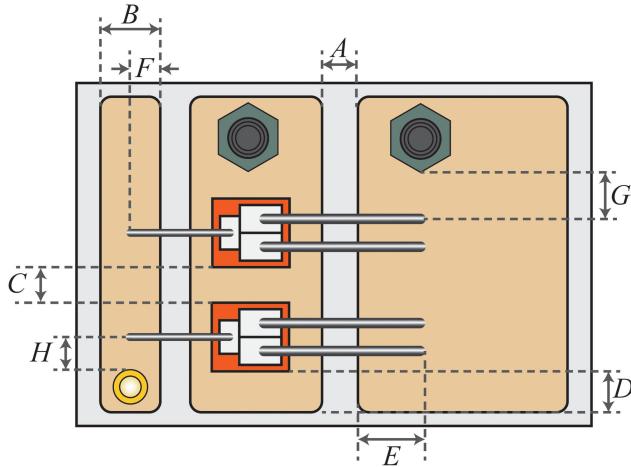


Fig. 17. Illustration of the MCPM design rules in Table IV.

checker first ensures that the sum of trace widths horizontally and vertically is equal to the layout boundaries.

Then, the design rule checker goes through a set of conventional design rules for MCPMs (Table IV and Fig. 17). Once the solution meets all these design rules, it is ready for thermal and electrical parasitics evaluation.

B. Layout Optimization Example

As a use-case example of the capabilities in PowerSynth, the area optimization of a simple half-bridge layout with four devices per switching position is explored. In this case, the switching frequency of the module is specified to be 100 kHz and there are 8 devices with each one dissipating 50 W. A

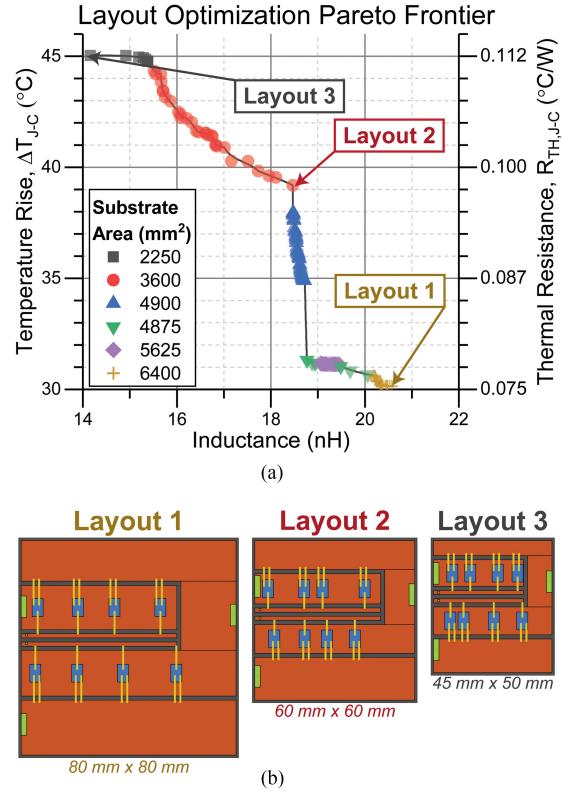


Fig. 18. (a) Layout optimization results showing maximum junction temperature rise and thermal resistance versus loop inductance for 170 candidate solutions. (b) Three solutions selected from the graph in (a) and drawn to relative scale, showing their respective layout dimensions.

constant temperature of 300 K is applied to the backside of the baseplate. In this study several optimization runs are performed, varying substrate area between 45 mm \times 50 mm and 80 mm \times 80 mm and combining the results to form a single Pareto front. The baseplate is set to be 15 mm larger than the substrate in both dimensions for each condition.

The multiobjective optimization routine is set to use loop inductance and maximum device temperature as goals for the cost function. The design constraints applied include a fixed width of 2 mm for the signal traces and a correlation of their lengths. Additionally, traces with power terminals are constrained so that their minimum widths are greater than the width of the power terminals mounted onto them.

Results of this layout optimization are shown in Fig. 18 where the overall Pareto frontier is presented along with three sample layouts. In total, 803 layouts are generated in approximately 20 min of run-time on a 3.4 GHz Intel Core i7-3770 with 8 GB of RAM. Of these, 170 are nondominated and plotted. Overall, these layouts span a difference in inductance and temperature of 7 nH and 15 $^{\circ}\text{C}$, respectively. Layout 1 in Fig. 18(b) corresponds to one that has the lowest temperature rise, but the highest loop inductance. Likewise, layout 3 has the smallest loop inductance, but its decreased footprint results in the highest maximum temperature. Layout 2 represents a near-equal tradeoff between these two extremes.

While changing the overall footprint of a layout has a significant impact on temperature rise and loop inductance,

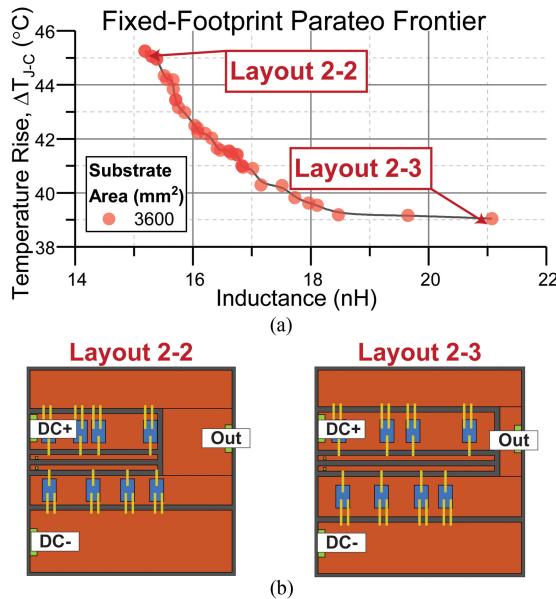


Fig. 19. (a) Pareto frontier for a fixed substrate size from this case study. (b) Example layouts from the graph in (a).

PowerSynth strives to optimize die placement and trace geometry within a fixed area to minimize these performance criteria. To illustrate this, the graph in Fig. 19(a) shows the complete Pareto frontier for candidates belonging to the same group as Layout 2 in Fig. 18—this includes solutions that were dominated in the preceding chart. In these examples, the total inductance range spans 5.9 nH with a 6.2 °C difference in maximum temperature across the solutions. For Layout 2-3, the traces corresponding to both the negative dc and output terminals are narrower than their counterparts in Layout 2-2. For Layout 2-3, this means that the loop inductance from the positive to negative dc terminals is relatively higher. However, the high-side devices can spread out more along the dc positive trace and the low-side devices are situated over a greater trace area, both promoting lower temperatures under the same operating conditions. Conversely, the wider output and negative dc traces found in Layout 2-2 yield a lower loop inductance at the cost of higher temperature due to crowding of the high-side devices and less metal area underneath the low-side devices.

VI. CONCLUSION AND FUTURE WORK

This paper has presented an overview of the MCPM design tool PowerSynth, the first hardware-validated power module layout tool. The models that PowerSynth uses to rapidly approximate both electrical parasitics and device temperature were presented. By employing response surface modeling to estimate parasitics, the inaccuracies associated with using microstrip formulae for MCPMs have been overcome without increasing computational effort significantly. Additionally, the thermal model presented in this paper results in a reduced-order thermal resistor network that can still account for thermal coupling among devices as well as changes in heat spreading associated with trace geometry. Furthermore, it was shown that these models correlate well to FEA simulations and measurements, and thus are certainly sufficiently accurate in the context

of layout generation to assess tradeoffs. The fast evaluation of these models (approximately three to four orders of magnitude faster than FEA) allows them to be used as cost functions within a multiobjective optimization framework that was implemented using a genetic algorithm. The parasitics are accurate enough that they can be back annotated on the original circuit netlist for subsequent circuit simulation analysis aimed at signal integrity.

The symbolic layout representation introduced in this tool is a unique extension of stick diagrams used in VLSI design. By starting with a symbolic layout, PowerSynth is able to assign design variables and perform this optimization—generating hundreds of candidate solutions in minutes and presenting them to designers in a manner that allows them to quickly choose ones for further evaluation. Layout optimization within this framework is matrix-based with the explicit goals of minimizing temperature along with inductance and resistance. This is opposed to grid-based place-and-route methods that focus on compaction, where temperature or parasitic reduction is only a side effect. Also, with the inclusion of the MDK and design rule checks, PowerSynth ensures that only manufacturable designs are presented to the user. Furthermore, PowerSynth is an open software architecture allowing the incorporation of alternate thermal modeling methods, electrical parasitic modeling methods, and optimization algorithms.

Since the end goal is to produce a tool that will help bridge the gap between circuit design and packaging engineers, research efforts are constantly expanding on current capabilities. Upcoming endeavors include extending the layout representation to include heterogeneous component integration and 3-D layout optimization along with an improved fidelity of the electrical and thermal models. Continued development of the electrical models will allow for better optimization for balanced branch-currents among paralleled devices and conducted EMI. Additionally, collaboration has already begun with other groups to bring improvements to the thermal model, leading to thermomechanical reliability optimization and lifetime prediction including stress/strain analysis. This model can then be used to optimize the thickness of the substrate, attachment, and other related material layers to produce more reliable modules. Finally, techniques that will allow complete synthesis of the layout from a circuit netlist—further narrowing the technical divide between systems design and converter manufacturing – are under investigation.

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REFERENCES

- [1] J. Rabkowski, D. Peftitsis, and H. Nee, "Silicon carbide power transistors: A new era in power electronics is initiated," *IEEE Trans. Ind. Electron. Mag.*, vol. 6, no. 2, pp. 17–26, Jun. 2012, doi: [10.1109/MIE.2012.2193291](https://doi.org/10.1109/MIE.2012.2193291).
- [2] J. Millan, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014, doi: [10.1109/TPEL.2013.2268900](https://doi.org/10.1109/TPEL.2013.2268900).
- [3] P. Gueguen, "Market & technology trends in wide BandGap power packaging," in *Proc. Appl. Power Electron. Conf. Expo.*, 2015. [Online]. Available at: <https://www.psmra.com/sites/default/files/uploads/tech-forums-semiconductor/presentations/11-market-and-technology-trends-wbg-power-module-packaging.pdf>
- [4] B. Whitaker *et al.*, "A high-density, high-efficiency, isolated on-board vehicle battery charger utilizing silicon carbide power devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2606–2617, May 2014, doi: [10.1109/TPEL.2013.2279950](https://doi.org/10.1109/TPEL.2013.2279950).
- [5] S. Seal and H. A. Mantooth, "High performance silicon carbide power packaging—Past trends, present practices, and future directions," *Energies*, vol. 10, no. 3, pp. 1–30, 2017, Art. no. 341.
- [6] H. A. Mantooth, M. D. Glover, and P. Shepherd, "Wide Bandgap technologies and their implications on miniaturizing power electronic systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 3, pp. 374–385, Sep. 2014, doi: [10.1109/JESTPE.2014.2313511](https://doi.org/10.1109/JESTPE.2014.2313511).
- [7] B. K. Bose, *Power Electronics and Motor Drives: Advances and Trends*. Amsterdam, The Netherlands: Elsevier, 2010.
- [8] B. K. Bose, "Global warming: Energy, environmental pollution, and the impact of power electronics," *IEEE Ind. Electron. Mag.*, vol. 4, no. 1, pp. 6–17, Mar. 2010, doi: [10.1109/MIE.2010.935860](https://doi.org/10.1109/MIE.2010.935860).
- [9] R. W. Johnson, J. L. Evans, P. Jacobsen, J. R. Thompson, and M. Christopher, "The changing automotive environment: high-temperature electronics," *IEEE Trans. Electron. Packag. Manuf.*, vol. 27, no. 3, pp. 164–176, Jul. 2004, doi: [10.1109/TEPM.2004.843109](https://doi.org/10.1109/TEPM.2004.843109).
- [10] J. Hornberger, A. B. Lostetter, K. J. Olejniczak, T. McNutt, S. M. Lal, and H. A. Mantooth, "Silicon-carbide (SiC) semiconductor power electronics for extreme high-temperature environments," in *Proc. IEEE Aerosp. Conf.*, 2004, vol. 4, pp. 2538–2555.
- [11] S. Tanimoto and K. Matsui, "High junction temperature and low parasitic inductance power module technology for compact power conversion systems," *IEEE Trans. Electron Dev.*, vol. 62, no. 2, pp. 258–269, Feb. 2015, doi: [10.1109/TED.2014.2359978](https://doi.org/10.1109/TED.2014.2359978).
- [12] Z. Liang, P. Ning, F. Wang, and L. Marlino, "Reducing parasitic electrical parameters with a planar interconnection packaging structure," in *Proc. 7th Int. Conf. Integr. Power Electron. Syst.*, 2012, pp. 374–379.
- [13] J. B. Forsythe *et al.*, "Paralleling of power MOSFETs for higher power output," in *Proc. Conf. Rec.—Ind. Appl. Soc. 1981 Annu. Meet.*, 1981, pp. 777–796. [Online]. Available at: <https://www.infineon.com/dgdl/para.pdf?fileId=5546d462533600a401535744b4583f79>
- [14] D. P. Sadik, J. Colmenares, D. Peftitsis, J. K. Lim, J. Rabkowski, and H. P. Nee, "Experimental investigations of static and transient current sharing of parallel-connected silicon carbide MOSFETs," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, 2013, pp. 1–10.
- [15] F. Merienne, J. Roudet, and J. L. Schanen, "Switching disturbance due to source inductance for a power MOSFET: Analysis and solutions," in *Proc. 27th Annu. IEEE Power Electron. Spec. Conf.*, 1996, vol. 2, pp. 1743–1747.
- [16] K. Takao, T. Shinohe, T. Yamamoto, K. Hasegawa, and M. Ishida, "1200 V-360 A SiC power module with phase leg clustering concept for low parasitic inductance and high speed switching," in *Proc. 8th Int. Conf. Integr. Power Syst.*, 2014, pp. 1–7.
- [17] N. Oswald, P. Anthony, N. McNeill, and B. H. Stark, "An experimental investigation of the tradeoff between switching losses and EMI generation with hard-switched All-Si, Si-SiC, and All-SiC device combinations," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2393–2407, May 2014, doi: [10.1109/TPEL.2013.2278919](https://doi.org/10.1109/TPEL.2013.2278919).
- [18] G. Busatto, C. Abbate, F. Iannuzzo, L. Fratelli, B. Cascone, and G. Giannini, "EMI Characterisation of high power IGBT modules for traction application," in *Proc. IEEE 36th Power Electron. Spec. Conf.*, 2005, vol. 2005, pp. 2180–2186.
- [19] A. Dutta and S. S. Ang, "Electromagnetic interference simulations for wide-bandgap power electronic modules," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 757–766, Sep. 2016, doi: [10.1109/JESTPE.2016.2573315](https://doi.org/10.1109/JESTPE.2016.2573315).
- [20] A. Domurat-Linde and E. Hoene, "Analysis and reduction of radiated EMI of power modules," in *Proc. 7th Int. Conf. Integr. Power Electron. Syst.*, 2012, vol. 9, pp. 1–6.
- [21] E. Hoene, A. Ostrmann, B. T. Lai, C. Marczok, A. Müsing, and J. W. Kolar, "Ultra-low-inductance power module for fast switching semiconductors current sensor DC-link capacitor semiconductor," in *Proc. PCIM Europe*, 2013, pp. 198–205.
- [22] R. Bayerer and D. Domes, "Power circuit design for clean switching," in *Proc. 6th Int. Conf. Integr. Power Electron. Syst.*, 2010, pp. 1–6.
- [23] L. Qiao *et al.*, "Performance of a 1.2 kV, 288A full-SiC MOSFET module based on low inductance packaging layout," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 3038–3042.
- [24] B. Grummel, R. McClure, L. Zhou, A. P. Gordon, L. Chow, and Z. J. Shen, "Design consideration of high temperature SiC power modules," in *Proc. 34th Annu. IEEE Conf. Ind. Electron.*, 2008, pp. 2861–2866.
- [25] X. Perpiñà, L. Navarro, X. Jordà, M. Vellvehi, J.-F. Serviere, and M. Mermet-Guyennet, *Reliability and Lifetime Prediction for IGBT Modules in Railway Traction Chains*. InTech, 2012, doi: [10.5772/38268](https://doi.org/10.5772/38268).
- [26] N. Hingora, X. Liu, Y. Feng, B. McPherson, and H. A. Mantooth, "Power-CAD: A novel methodology for design, analysis and optimization of power electronic module layouts," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 2692–2699.
- [27] T. Hubing, C. Su, H. Zeng, and H. Ke, "Software table of contents," *Cvel-08-011.2*, pp. 1–56, 2008.
- [28] U. Drofenik, D. Cottet, A. Müsing, J.-M. Meyer, and J. W. Kolar, "Modelling the thermal coupling between internal power semiconductor dies of a water-cooled 3300V/1200A HiPak IGBT module," in *Proc. Conf. Power Electron., Intell. Motion, Power Qual.*, Nuremberg, Germany, May 2007, pp. 22–24.
- [29] B. Du, J. L. Hudgins, E. Santi, A. T. Bryant, P. R. Palmer, and H. A. Mantooth, "Transient electrothermal simulation of power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 237–248, Jan. 2010, doi: [10.1109/TPEL.2009.2029105](https://doi.org/10.1109/TPEL.2009.2029105).
- [30] M. Hammadi, J. Y. Choley, O. Penas, J. Louati, A. Rivière, and M. Haddar, "Layout optimization of power modules using a sequentially coupled approach," *Int. J. Simul. Model.*, vol. 10, no. 3, pp. 122–132, 2011, doi: [10.2507/IJSIMM10\(3\)2.183](https://doi.org/10.2507/IJSIMM10(3)2.183).
- [31] B. W. Shook, Z. Gong, Y. Feng, A. M. Francis, and H. A. Mantooth, "Multi-chip power module fast thermal modeling for layout optimization," *Comput. Des. Appl.*, vol. 9, no. 6, pp. 837–846, 2012, doi: [10.3722/cadaps.2011.837-846](https://doi.org/10.3722/cadaps.2011.837-846).
- [32] B. W. Shook, A. Nizam, Z. Gong, A. M. Francis, and H. A. Mantooth, "Multi-objective layout optimization for multi-chip power modules considering electrical parasitics and thermal performance," in *Proc. IEEE 14th Work. Control Model. Power Electron.*, 2013, pp. 1–4, doi: [10.1109/COMPEL.2013.6626450](https://doi.org/10.1109/COMPEL.2013.6626450).
- [33] P. Ning, F. Wang, and K. D. T. Ngo, "Automatic layout design for power module," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 481–487, Jan. 2013, doi: [10.1109/TPEL.2011.2180739](https://doi.org/10.1109/TPEL.2011.2180739).
- [34] P. Ning, X. Wen, Y. Mei, and T. Fan, "A fast universal power module layout method," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 4132–4137.
- [35] P. Ning, X. Wen, Y. Li, and X. Ge, "An improved automatic layout method for planar power module," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, May 2016, vol. 2016, pp. 3080–3085.
- [36] B. Ji, X. Song, E. Sciberras, W. Cao, Y. Hu, and V. Pickert, "Multiobjective design optimization of IGBT power modules considering power cycling and thermal cycling," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2493–2504, May 2015, doi: [10.1109/TPEL.2014.2365531](https://doi.org/10.1109/TPEL.2014.2365531).
- [37] J. Main, "A manufacturer design kit for multi-chip power module layout synthesis," M.S. thesis, Dept. Elect. Eng., Univ. of Arkansas, Fayetteville, AR, USA, 2017.
- [38] A. Hagberg, P. Swart, D. S Chult, Aric A. Hagberg, Daniel A. Schult, and Pieter J. Swart, "Exploring network structure, dynamics, and function using NetworkX," in *Proc. 7th Python Sci. Conf.*, Pasadena, CA, USA, 2008, pp. 11–15.
- [39] B. W. Shook, "The design and implementation of a multi-chip power module layout synthesis tool," M.S. thesis, Dept. Elect. Eng., Univ. of Arkansas, Fayetteville, AR, USA, 2014.
- [40] L. W. Nagel, "SPICE 2, a computer program to simulate semiconductor circuits," Univ. California, Berkeley, CA, USA, Tech. Rep. UCB/ERL M520, 1975.
- [41] A. Madry, *From Graphs to Matrices, and Back: New Techniques for Graph Algorithms*. MIT: Cambridge, MA, USA, 2011.

- [42] Q. Le, T. Evans, S. Mukherjee, Y. Peng, T. Vrotsos, and H. A. Mantooth, "Response surface modeling for parasitic extraction for multi-objective optimization of multi-chip power modules (MCPMs)," in *Proc. IEEE 5th Workshop Wide Bandgap Power Devices Appl.*, 2017, pp. 327–334.
- [43] W. C. M. Van Beers and J. P. C. Kleijnen, "Kriging for interpolation in random simulation," *J. Oper. Res. Soc.*, vol. 54, no. 3, pp. 255–262, 2003.
- [44] A. Amrous, S. Ghedira, B. Allard, H. Morel, and D. Renault, "Choosing a thermal model for electrothermal simulation of power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 14, no. 2, pp. 300–307, Mar. 1999, doi: [10.1109/63.750183](https://doi.org/10.1109/63.750183).
- [45] Z. Luo, H. Ahn, and M. A. E. Nokali, "A thermal model for insulated gate bipolar transistor module," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 902–907, Jul. 2004, doi: [10.1109/TPEL.2004.830089](https://doi.org/10.1109/TPEL.2004.830089).
- [46] Vishay, "Surface Mounted Power Resistor D2TO35." DTO25 Datasheet, pp. 1–6, 2002.
- [47] K. Deb, A. Pratap, S. Agarwal, and T. Meyarivan, "A fast and elitist multiobjective genetic algorithm: NSGA-II," *IEEE Trans. Evol. Comput.*, vol. 6, no. 2, pp. 182–197, Apr. 2002, doi: [10.1109/4235.996017](https://doi.org/10.1109/4235.996017).
- [48] F.-A. Fortin, F.-M. De Rainville, M.-A. Gardner, M. Parizeau, C. Gagné, and C. Gagné, "DEAP: Evolutionary algorithms made easy," *J. Mach. Learn. Res.*, vol. 13, pp. 2171–2175, Jul. 2012. [Online]. Available at: <http://jmlr.csail.mit.edu/papers/volume13/fortin12a/fortin12a.pdf>



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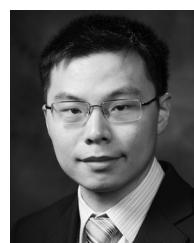
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