

Research on Losses of PCB Parasitic Capacitance for GaN-Based Full Bridge Converters

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Abstract—The utilization of wide band-gap semiconductor devices provides the possibility of higher switching frequency and power density for power converters. However, the influence of parasitic parameters becomes more significant. It deteriorates the converter performance and leads to extra loss. In this article, the extra loss caused by the parasitic capacitance of printed circuit boards (PCBs) is studied. The mechanism is explained, and the model of full bridge topology with PCB parasitic capacitance is proposed as an example. Both the capacitance in power loops and control circuits are considered in the proposed model. Besides the capacitive loss in power loops, losses are also introduced by the capacitive coupling between the power and control circuits due to the potential pulsation of the control ground. This potential pulsation is analyzed and the calculation method of corresponding losses is presented. The formation of PCB parasitic capacitance is analyzed in detail and corresponding layout optimization methods are proposed. Theoretical analyses are verified on a gallium nitride based full bridge prototype with calorimetric loss measurement. The comparison of calculated and measured losses is presented, which shows a switching loss deviation of 26% without the consideration of parasitic capacitance and a 40% reduction on the extra losses after the proposed optimization.

Index Terms—Bridge circuits, capacitance, gallium nitride (GaN), losses, parasitic, temperature measurement.

I. INTRODUCTION

AS THE characteristics of power semiconductor devices based on silicon (Si) material are reaching its inherent limits after decades of development, wide band-gap devices, such as gallium nitride (GaN) transistors, become more and more widely concerned [1]–[4]. GaN high electron mobility transistors (HEMTs) have shown superiorities of low ON-state resistance, ultra-low junction capacitance, fast switching speed, and the absence of body-diode reverse recovery over Si counterparts. This benefits the increase of switching frequency and switching speed for the devices and leads to reduced conduction

loss, switching loss, and the volume of passive components in power conversion systems. Thus, the efficiency and power density of the systems is further improved [5]–[8].

Loss analysis is one of the significant processes in power conversion system designs, as the basis for device selection, efficiency pre-estimation, and the optimization of the cooling systems [7], [9], [10]. The losses of GaN HEMTs usually consist of conduction loss, switching loss, dead-time loss, driving loss, and others. As the switching loss is in proportion with switching frequency, it becomes more noticeable and occupies most of the losses in high-frequency applications [11].

Turn-ON and turn-OFF energies ($E_{\text{on}}/E_{\text{off}}$) are the direct reflection of the switching loss for GaN HEMTs and the key parameters in switching loss estimation. Lots of researches have been published on the study of $E_{\text{on}}/E_{\text{off}}$ for GaN HEMTs. Various calculation and measurement approaches are proposed and could be categorized into double-pulse testing (DPT) [12]–[16], theoretical calculations based on the switching behaviors [17]–[19], SPICE model simulation [20], and calculation methods with multivariable scaling [21]. Although $E_{\text{on}}/E_{\text{off}}$ can be accurately extracted with these proposed approaches, most of them concentrate on the characteristics of the devices. The external parasitic parameters in practical converters may deteriorate the performance of the devices, making the loss calculation results based on $E_{\text{on}}/E_{\text{off}}$ data less accurate, especially in higher switching frequency and power density applications.

As one of the common nonideal factors, parasitic capacitance can no longer be neglected with the increase of switching frequency, leading to extra losses on the devices. It is reported in [22] that a mismatch is observed between the calculated and measured results of the switching energy due to parasitic parameters. Liu *et al.* [23] studied the extra loss of nonactive devices in three-level converters. Due to the switching actions of the active devices, the pulsating energy in the junction capacitance of the nonactive devices leads to extra capacitive losses, which will cause an error of 15% in loss calculation. The capacitive loss caused by the passive devices in bridge topologies has also been studied in [24]. Extra loss is introduced as the energy stored in the parasitic capacitance is eventually dissipated in two-dimensional electron gas of the active device when it is turned ON. It is also explained that the parasitic capacitance of the printed circuit board (PCB) and filter inductor is repeatedly charged and discharged as the midpoint voltage changes [25]. Thus, the equivalent output capacitance of the passive device is increased, as well as the

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corresponding capacitive loss. Q3D extractions of the parasitic capacitance and the modified switching energy calculation are also presented in [24].

Although parasitic capacitance loss is noticed in these literatures, there is little further discussion on it. Moreover, most of the published researches only focus on the parasitic capacitance in the power circuits. None of the control circuits, sensing circuits, and isolated power supplies is involved. For a phase-leg in bridge-type topologies, the midpoint also performs as the return of the top gate driving circuit. Parasitic capacitance is found between the output side of the driver IC and not only the power loops but also the control circuits. Unfortunately, few quantitative analyses are published on this. Significant losses could be observed especially with dense PCB layouts.

The extra capacitive losses caused by PCB parasitic capacitance are investigated in detail in this article. The model of full bridge topology with parasitic capacitance is proposed, which considers both the power loops and the control and sensing circuits from the system level. Theoretical analysis and experimental results show that a switching loss deviation of 26% occurs without the consideration of parasitic capacitance. The organization of this article is as follows. The PCB parasitic capacitance in power loops and the mechanism of this extra loss are explained in Section II. Also, the parasitic capacitance related to the control circuits is modeled, and the voltage pulsation of the control ground is investigated. In Section III, the methods of PCB parasitic capacitance measurement and loss calculation are proposed. Some key parts that are responsible for the parasitic capacitance are analyzed according to the PCB layouts. The principle to reduce the discussed capacitance is proposed along with some examples of layout optimization. In Section IV, the theoretical analysis is verified on a GaN-based full bridge converter. The power losses on GaN devices are measured with a calorimetric method. A loss breakdown approach is proposed, and the comparison of the calculated and measured results is presented. Finally, the conclusion is drawn in Section V.

II. PCB PARASITIC CAPACITANCE LOSS MECHANISM AND MODELING

A. PCB Parasitic Capacitance in Power Loops

Bridge-type topologies, including half bridge, full bridge, synchronous buck units, etc. are commonly used in power conversion systems. Fig. 1 shows a GaN-based full bridge converter and the parasitic capacitance in power loops. S_1 and S_4 are defined as active devices. S_2 and S_3 are passive devices, which are turned on complementarily with S_1 and S_4 , respectively. L_f is the output filter inductor and I_L is the current of L_f . V_{bus} and V_o are the dc bus voltage and the output voltage, respectively.

Parasitic capacitance exists inevitably between different nodes of the power loops in practical converters. The two midpoints in Fig. 1 are regarded as the voltage pulsation nodes. On the contrary, dc+ and dc- are defined as static nodes. Fig. 2 shows the schematic diagram of the parasitic capacitance between the midpoints and dc buses as an example. Due to the symmetry of the full bridge converter, only Phase-leg I is analyzed hereinafter, and the same method can be applied

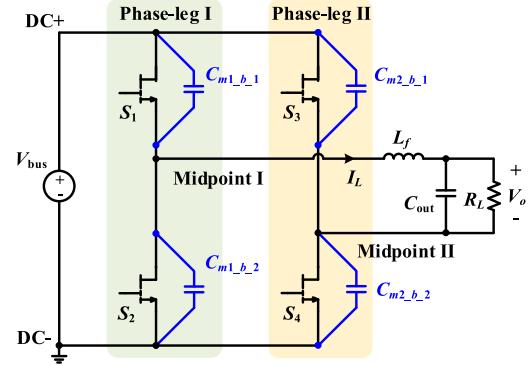


Fig. 1. Topology of full bridge converter with parasitic capacitance in power loops.

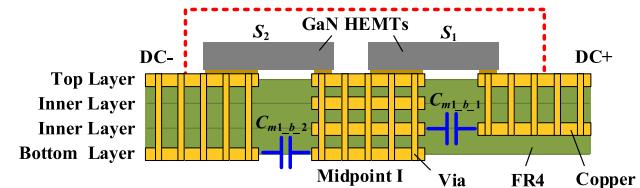


Fig. 2. Schematic diagram of the parasitic capacitance in a phase-leg. $C_{m1_b_1}$ and $C_{m1_b_2}$ are the PCB parasitic capacitance and introduced by the adjacent coppers that act like plate capacitors.

to Phase-leg II. Fig. 2 illustrates the formation mechanism of the midpoint-to-bus capacitance $C_{m1_b_1}$ and $C_{m1_b_2}$ in a four-layer PCB. They are introduced by the adjacent coppers which act like plate capacitors.

The diagram of Phase-leg I and the typical turn-ON waveforms of S_1 are depicted in Fig. 3. As the gate-to-source voltage v_{gs} reaches the threshold voltage V_{th} at t_1 , the channel current i_{chan} starts to rise along with v_{gs} . During the current rise time of t_1-t_2 , a small drop occurs on the drain-to-source voltage v_{ds} of S_1 because of the loop inductance L_d .

At the instant of t_2 , i_{chan} reaches I_L , and v_{ds} starts to fall. The output capacitance C_{oss1} of S_1 is discharged during voltage falling time, while the output capacitance C_{oss2} of S_2 is charged. With the charging and discharging current, i_{chan} keeps rising and exceeds I_L . It should be noted that C_{oss1} discharging current goes directly through the channel of S_1 and cannot be spotted in the drain current i_d from the outside of the device.

The power loss on the device during the turn-ON transient could be divided into two parts, which are defined as $V-I$ overlap loss and capacitive loss. $V-I$ overlap loss is introduced by the overlap of v_{ds} and i_d , which is highlighted as shown in Fig. 3(a) and derived as

$$E_{overlap} = \int_{t_1}^{t_3} v_{ds} i_d dt \approx \frac{1}{2} V_{bus} I_L t_{on}, \quad (1)$$

where t_{on} is the turn-ON time of the device. It is the sum of current rising time t_{cr} and voltage falling time t_{vf} as shown in the following equation:

$$t_{on} = t_{cr} + t_{vf}. \quad (2)$$

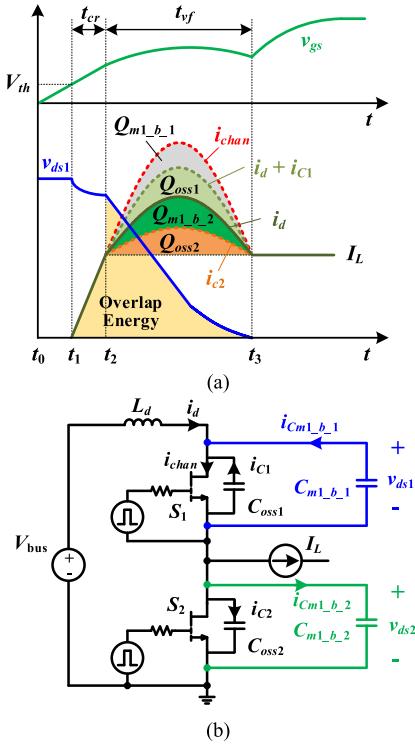


Fig. 3. Topology of Phase-leg I and typical turn-ON waveforms of the active device. (a) Typical turn-ON waveforms of GaN HEMTs. The highlighted areas represent the overlap energy, the output charge of the devices, and the charge corresponding to the parasitic capacitance. (b) Diagram of Phase-leg I with GaN HEMTs. S_1 is the active device and S_2 is the passive device. $C_{m1_b_1}$ and $C_{m1_b_2}$ are considered as in parallel with S_1 and S_2 , respectively.

The other part of the loss is the capacitive loss. As illustrated in Fig. 3(b), there are five components in i_{chan} during the time interval of t_2-t_3 , namely, the load current I_L , C_{oss1} discharging current i_{C1} , C_{oss2} charging current i_{C2} , $C_{m1_b_1}$ discharging current $i_{Cm1_b_1}$, and $C_{m1_b_2}$ charging current $i_{Cm1_b_2}$. Given that the voltage drop on L_d is negligible compared with the dc bus voltage, the drain-to-source voltage rising slew rate of S_1 is identical with the drain-to-source voltage falling slew rate of S_2 . Thus, the channel current is derived as

$$\begin{aligned} i_{chan} &= I_L + i_{C1} + i_{C2} + i_{Cm1_b_1} + i_{Cm1_b_2} \\ &= I_L + (C_{oss1} + C_{oss2} + C_{m1_b}) \left| \frac{dv_{ds1}}{dt} \right|, \end{aligned} \quad (3)$$

where C_{oss1} and C_{oss2} are expressed as (4) according to the voltage-dependent C_{oss} curve of GaN HEMTs and C_{m1_b} is the sum of $C_{m1_b_1}$ and $C_{m1_b_2}$, which is expressed as (5)

$$\begin{cases} C_{oss1} = C_{oss}(v_{ds1}) \\ C_{oss2} = C_{oss}(V_{bus} - v_{ds1}) \end{cases} \quad (4)$$

$$C_{m1_b} = C_{m1_b_1} + C_{m1_b_2}. \quad (5)$$

As presented in Fig. 3(b), $C_{m1_b_1}$ and $C_{m1_b_2}$ are in parallel with GaN HEMTs; thus, the voltage across them will follow the drain-to-source voltage of devices. Therefore, the equivalent junction capacitance of the devices is enlarged and higher current

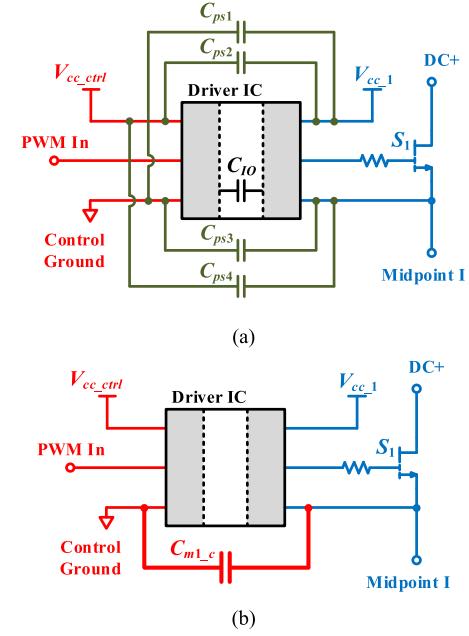


Fig. 4. Schematic diagrams of a top device and the gate driving circuit with midpoint-to-control parasitic capacitance. (a) Parasitic capacitance between the input and output sides of the driver IC. (b) Equivalent model of midpoint-to-control parasitic capacitance.

overshoot will occur on i_d and i_{chan} , as illustrated in Fig. 3(a). According to (3)–(5), the total capacitance of the phase-leg is

$$C_{total} = C_{oss}(v_{ds1}) + C_{oss}(V_{bus} - v_{ds1}) + C_{m1_b}. \quad (6)$$

As the PCB parasitic capacitance is voltage-independent, the corresponding charge and capacitive energy of C_{total} are derived as

$$\begin{aligned} Q_{total} &= \int_0^{V_{bus}} (C_{oss}(v_{ds1}) + C_{oss}(V_{bus} - v_{ds1})) dv_{ds1} \\ &\quad + C_{m1_b} V_{bus} \end{aligned} \quad (7)$$

$$\begin{aligned} E_{total} &= \int_0^{V_{bus}} (C_{oss}(v_{ds1}) + C_{oss}(V_{bus} - v_{ds1})) v_{ds1} dv_{ds1} \\ &\quad + \frac{1}{2} C_{m1_b} V_{bus}^2. \end{aligned} \quad (8)$$

It is indicated in (8) that extra switching loss is introduced evidently by PCB parasitic capacitance C_{m1_b} .

Moreover, larger C_{total} leads to an increased t_{vf} . It has been reported in [12] that t_{vf} is approximately proportional to $\sqrt{Q_{total}}$. Therefore, higher overlap energy is caused by PCB parasitic capacitance as well according to (1) and (2).

B. Control-Related Parasitic Capacitance

Besides the midpoint-to-bus capacitance, parasitic capacitance is also found between the control circuits and the power nodes in practical converters, which makes the actual parasitic capacitance even larger.

Fig. 4(a) and (b) shows a top device and its gate driving circuit. The midpoint of the phase-leg and the return of the gate driving

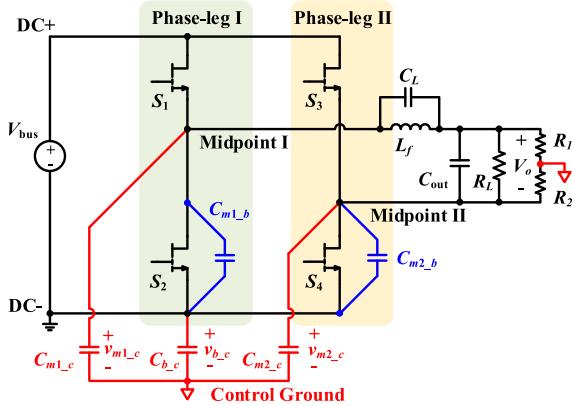


Fig. 5. Full bridge converter with PCB parasitic capacitance. Both midpoint-to-bus and control-related capacitance are included.

circuit share the same node. Meanwhile, the return of the input side of the driver IC is connected to the control ground. The potential of the output side of the driver IC pulsates with the switching actions of the device. Fig. 4(a) shows the parasitic capacitance between the input and output sides of the driver IC. C_{IO} is the inner input-to-output isolation capacitance of the driver IC, which is usually provided by the manufacturers [26]. The value of C_{IO} is around 1 pF for optocouplers and could be as low as 0.1 pF for digital isolated drivers as reported in [27]. In addition, C_{ps1} to C_{ps4} indicate the parasitic capacitance between the PCB strays of the input and output sides. They are highly dependent on the layout and can be found in both power supply and returns strays of the driving circuits, the control circuits, and even the isolated power supplies. It is noteworthy that the capacitance tends to become higher in high power density designs. With the steady supply voltage for both V_{cc_ctrl} and V_{cc_1} , all the capacitance is equivalent to one capacitance across the driver IC, connecting the control ground and the midpoint, as illustrated in Fig. 4(b).

Parasitic capacitance also exists between the control circuits and the dc buses. It is caused by the capacitive coupling of the input-side PCB strays of the driver ICs, sensing circuits, and the coppers of the dc buses. In fact, the voltage between the control ground and the dc buses pulsates with the switching actions of the GaN HEMTs instead of being constant, making the loss of control-to-bus capacitance easy to be overlooked. This will be discussed in the next section.

The full bridge topology with PCB parasitic capacitance is redrawn in Fig. 5, where not only the midpoint-to-bus capacitance but also the midpoint-to-control and control-to-bus capacitance are included. C_{m1_b} , C_{m2_b} , C_{m1_c} , C_{m2_c} , and C_{b_c} represent the Midpoint-I-to-bus, Midpoint-II-to-bus, Midpoint-I-to-control, Midpoint-II-to-control, and control-to-bus parasitic capacitance, respectively. Because of the constant voltage between the dc+ and dc- buses, they can be treated as one node in switching transients. Therefore, an equivalent capacitance C_{m1_b} is obtained between Midpoint I and the dc buses for simplicity as the paralleling of $C_{m1_b_1}$ and $C_{m1_b_2}$, which

is expressed as (5). Note that C_{m1_b} could be set in parallel with either S_1 or S_2 , and it does not change the following analysis. The same equivalent method can be applied to C_{m2_b} as well. Similar to the PCB parasitic capacitance, extra power losses could be introduced by the equivalent paralleled capacitance (EPC) C_L of the filter inductor, which is also presented in Fig. 5.

It is demonstrated in the previous work that differential or isolated sensing methods are recommended to deal with the common-mode noise [28]. If isolated sensing methods are adopted, the input-to-output capacitance of the sensing IC or the isolated amplifier should also be considered as part of C_{m2_c} . If the differential voltage sensing method is adopted for the output voltage sensing, the control ground is connected to the neutral point of the voltage dividing resistor network, which is simplified as R_1 and R_2 in Fig. 5. A high-impedance state between the control ground and the power circuits is established because of the high resistance of the voltage dividing network. Therefore, the potential of the control ground is determined by the parasitic capacitance. With dc+ and dc- treated as the static nodes, the rising and falling of midpoint voltage lead to the potential variation of the control ground referring to the dc buses. The energy stored in the capacitance will also be dissipated in the channels of the active devices during their turn-ON processes, and thus extra losses are produced.

C. Potential Pulsation of Control Ground

The dc input side and the output side of the converter could both be considered as shorted due to the large input and output capacitance. Therefore, the simplified ac and dc models of Fig. 5 are obtained, as shown in Fig. 6(a) and (b). All the GaN HEMTs are treated as pulsating voltage sources according to their switching actions.

It is shown in Fig. 6(a) that C_{m1_b} and C_{m2_b} are in parallel with the bottom devices. Therefore, they are charged from 0 V to V_{bus} in the turn-OFF transients of S_2 and S_4 , and discharged back to 0 V when they are turned ON, during which time the energy stored in C_{m1_b} and C_{m2_b} is dissipated in the channels of the devices. However, the voltage variations on C_{m1_c} , C_{m2_c} , and C_{b_c} are more complicated instead of pulsating between 0 V and V_{bus} . There will be five voltage levels in one switching cycle as depicted in Fig. 7, which will be explained in the following demonstration.

The carrier phase-shifted (CPS) pulsewidth modulation (PWM) doubles the equivalent frequency of the filter inductor, providing the possibility of shrinking the passive components without increasing the switching loss. Detailed control themes and analysis of the circuit modes have been reported in [29]. A full bridge converter with CPS PWM is adopted in this article. Fig. 7 shows the key waveforms of the converter. The inductor current ripples twice in one switching cycle. Therefore, it is reasonable to separate one switching cycle (T_s) into two equivalent cycles (T_{s_eq}). There is only one pair of turn-ON and turn-OFF actions in a single equivalent cycle.

As for the dc model, all the mean values of the voltage across the devices and parasitic capacitance are easy to be derived and

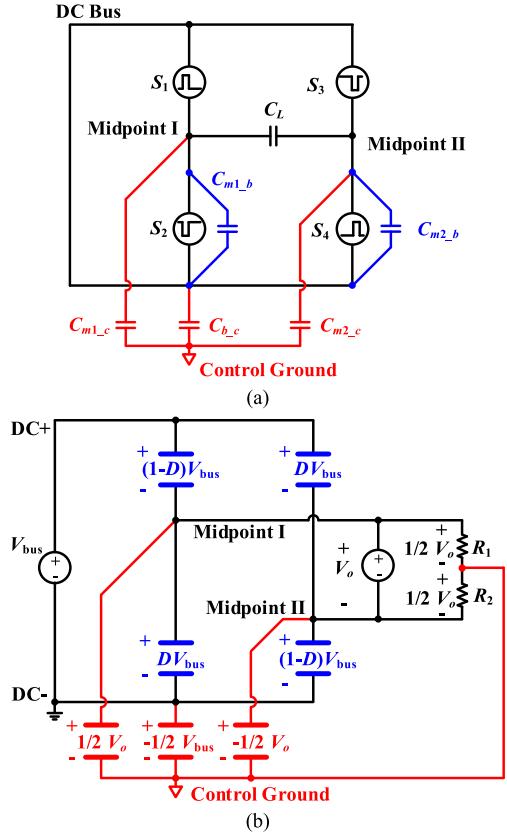
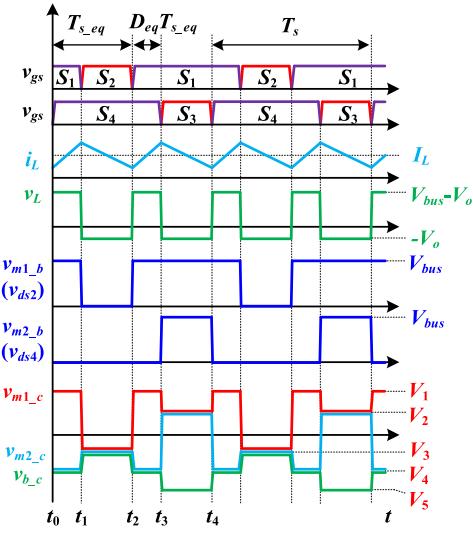
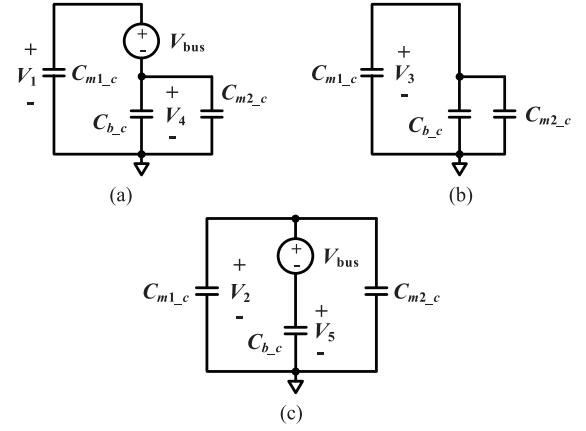


Fig. 6. Simplified ac and dc models of Fig. 5. (a) AC model. (b) DC model.

Fig. 7. Key waveforms of CPS full bridge converter. The inductor current ripples twice in one switching cycle. T_s is the switching period and T_{s_eq} is the equivalent switching period. D_{eq} is the equivalent duty ratio.

marked, as shown in Fig. 6(b). The voltage drops on R_1 and R_2 are both $1/2 V_o$ owing to the symmetry of the differential voltage dividing resistor network. The relation of the dc bus voltage and the output voltage is derived as

$$V_o = D_{eq} V_{bus} = (2D - 1) V_{bus} \quad (9)$$

Fig. 8. Further simplified ac models of Fig. 6 in one equivalent switching cycle. (a) t_0-t_1 and t_2-t_3 . S_1 and S_4 are in ON-state. (b) t_1-t_2 . S_2 and S_4 are in ON-state. (c) t_3-t_4 . S_1 and S_3 are in ON-state.

where D is the duty ratio of the active devices and D_{eq} is the equivalent duty ratio.

According to the switching actions of the devices, Fig. 6(a) is further simplified into three modes as shown in Fig. 8. As illustrated in Fig. 7, S_1 and S_4 are both in ON-state during t_0-t_1 and t_2-t_3 , and the equivalent circuit is shown as Fig. 8(a). It transforms to Fig. 8(b) after t_1 since S_2 and S_4 are ON at the same time. With the turn-ON action of S_3 at t_3 , the equivalent ac model turns from Fig. 8(a) into Fig. 8(c). The voltage on the parasitic capacitance satisfies

$$\begin{cases} V_1 = V_{bus} + V_4 \\ V_2 = V_{bus} + V_5. \end{cases} \quad (10)$$

According to charge conservation at t_1 and t_3 , the equations could also be given as

$$\begin{cases} C_{m1_c} (V_1 - V_3) + (C_{m2_c} + C_{b_c}) (V_4 - V_3) = 0 \\ C_{m1_c} (V_2 - V_1) + C_{m2_c} (V_2 - V_4) + C_{b_c} (V_5 - V_4) = 0. \end{cases} \quad (11)$$

Fig. 7 shows that there are three levels on all the voltage of C_{m1_c} , C_{m2_c} , and C_{b_c} . For the mean values of these voltages that correspond to the proposed dc model in Fig. 6(b), three equations are obtained as presented in the following equation:

$$\begin{cases} V_{m1_c_avg} = \frac{2D_{eq}V_1 + (1-D_{eq})(V_2 + V_3)}{2} = \frac{1}{2}V_o \\ V_{m2_c_avg} = \frac{2D_{eq}V_4 + (1-D_{eq})(V_2 + V_3)}{2} = -\frac{1}{2}V_o \\ V_{b_c_avg} = \frac{2D_{eq}V_4 + (1-D_{eq})(V_3 + V_5)}{2} = -\frac{1}{2}V_{bus}. \end{cases} \quad (12)$$

By combining (10)–(12), the voltage levels V_1-V_5 are calculated and presented in Table I, where Δ is defined as

$$\Delta = C_{m1_c} + C_{m2_c} + C_{b_c}. \quad (13)$$

Also, the voltage variations on all the parasitic capacitance are listed in Table II.

TABLE I
VOLTAGE LEVELS OF CONTROL RELATED CAPACITANCE

Voltage Levels	Expressions
V_1	$\frac{D_{eq}C_{m1_c} + (2 - D_{eq})C_{m2_c} + C_{b_c}}{2\Delta} V_{bus}$
V_2	$\frac{D_{eq}C_{m1_c} - D_{eq}C_{m2_c} + C_{b_c}}{2\Delta} V_{bus}$
V_3	$\frac{D_{eq}C_{m1_c} - D_{eq}C_{m2_c} - C_{b_c}}{2\Delta} V_{bus}$
V_4	$\frac{(D_{eq} - 2)C_{m1_c} - D_{eq}C_{m2_c} - C_{b_c}}{2\Delta} V_{bus}$
V_5	$\frac{(D_{eq} - 2)C_{m1_c} - (D_{eq} + 2)C_{m2_c} - C_{b_c}}{2\Delta} V_{bus}$

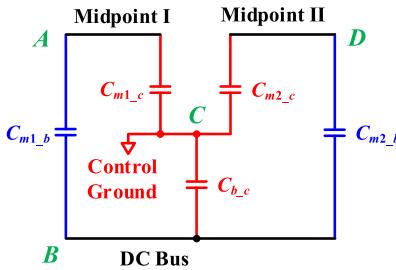


Fig. 9. Selection of testing points in capacitance measurement. $A-D$ are chosen as the nodes of Midpoint I, dc bus, the control ground, and Midpoint II on the power board.

III. CALCULATION AND REDUCTION OF PCB PARASITIC CAPACITANCE LOSS

A. PCB Parasitic Capacitance Measurement and Loss Calculation

An L/C/R is used in this article to measure the discussed parasitic capacitance, which can be directly measured on PCBs due to the voltage independence. The filter inductor and all the GaN HEMTs are removed to diminish their influence on the measurement results. Also, the dc+ and dc- buses, as well as the output port, are shorted to imitate the ac model in Fig. 6(a). Four testing points A to D are chosen on the nodes of Midpoint I, DC-, the control ground, and Midpoint II as shown in Fig. 9, and the measurement results are presented in Table III. All the values are measured at the switching frequency f_s , which is 160 kHz in this design. As a matter of fact, the PCB parasitic capacitance with certain overlap areas shows little correlation with the frequency because of the flat permittivity-frequency curve of the FR4 material [30], leading to high credibility of the measured results. Note that the measured values are the equivalent capacitance of the capacitor networks in Fig. 9 instead of the desired capacitance. The relations between the measurement results and the desired capacitance are listed in Table III as well. The values of each capacitance are solved accordingly and given in Table IV. Moreover, the value of EPC of the filter inductor is measured as 6.37 pF with a network analyzer.

According to Table II and Fig. 7, the voltage on C_{m1_b} and C_{m2_b} pulsates between 0 V and V_{bus} with the frequency as

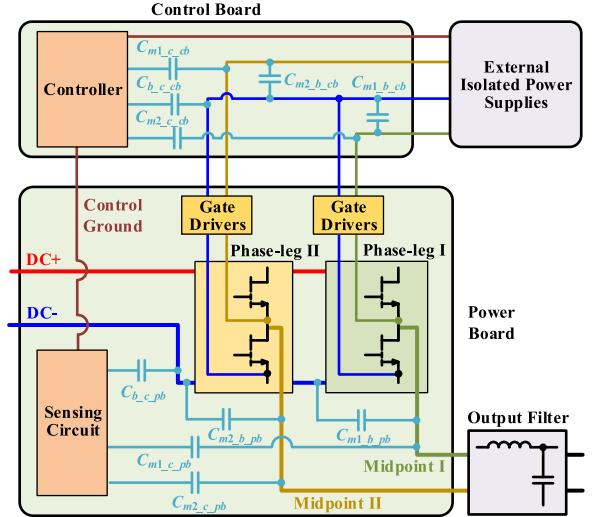


Fig. 10. Configuration diagram of the discussed converter system. $C_{m1_b_pb}$, $C_{m2_b_pb}$, $C_{m1_c_pb}$, $C_{m2_c_pb}$, and $C_{b_c_pb}$ are the PCB parasitic capacitance on the power board. $C_{m1_b_cb}$, $C_{m2_b_cb}$, $C_{m1_c_cb}$, $C_{m2_c_cb}$, and $C_{b_c_cb}$ are the PCB parasitic capacitance on the control board.

same as the switching frequency f_s , while the voltage on C_L pulsates between $-V_o$ and $V_{bus} - V_o$ with $2f_s$. Therefore, the corresponding losses of C_L , C_{m1_b} , and C_{m2_b} are calculated as follows, in which f_s , V_{bus} , and V_o are assumed to be 160 kHz, 400 V, and 80 V, respectively:

$$P_{CL} = 2f_s \frac{C_L}{2} \left((V_{bus} - V_o)^2 + V_o^2 \right) = 0.111 \text{ W} \quad (14)$$

$$P_{Cm1_b} = f_s \frac{C_{m1_b}}{2} V_{bus}^2 = 0.072 \text{ W} \quad (15)$$

$$P_{Cm2_b} = f_s \frac{C_{m2_b} V_{bus}^2}{2} = 0.188 \text{ W}. \quad (16)$$

Also, the power losses on C_{m1_c} , C_{m2_c} , and C_{b_c} could be calculated based on the voltage variations by combining Table I and Fig. 7 and presented as follows:

$$P_{Cm1_c} = f_s \frac{C_{m1_c}}{2} [(V_1^2 + V_3^2) + (V_1^2 - V_2^2)] = 0.166 \text{ W} \quad (17)$$

$$P_{Cm2_c} = f_s \frac{C_{m2_c}}{2} [(V_4^2 - V_3^2) + (V_2^2 + V_4^2)] = 0.141 \text{ W} \quad (18)$$

$$P_{Cb_c} = f_s \frac{C_{b_c}}{2} (V_5^2 - V_3^2) = 0.366 \text{ W}. \quad (19)$$

The measured parasitic capacitance and loss calculation results in Table IV and (14)–(19) show that C_{b_c} is the highest among all the PCB parasitic capacitance and contributes to nearly one-third of the total extra losses. Also, it is observable that C_{m2_b} is larger than C_{m1_b} , while C_{m1_c} is much larger than C_{m2_c} .

TABLE II
VOLTAGE VARIATIONS OF PARASITIC CAPACITANCE

Time intervals	C_L	Voltage on the parasitic capacitance			
		C_{m1_b}	C_{m2_b}	C_{m1_c}	C_{m2_c}
$t_0 \sim t_1$	$V_{bus} - V_o$	V_{bus}	0	V_1	V_4
$t_1 \sim t_2$	$-V_o$	0	0	V_3	V_3
$t_2 \sim t_3$	$V_{bus} - V_o$	V_{bus}	0	V_1	V_4
$t_3 \sim t_4$	$-V_o$	V_{bus}	V_{bus}	V_2	V_5

TABLE III
MEASURED CAPACITANCE BETWEEN TESTING NODES

Capacitance	Values /pF	Expressions
C_{BD}	28.40	$C_{m2_b} + C_{m2_c} \parallel (C_{b_c} + (C_{m1_c} \parallel C_{m1_b}))^a$
C_{AB}	29.68	$C_{m1_b} + C_{m1_c} \parallel (C_{b_c} + (C_{m2_c} \parallel C_{m2_b}))^a$
C_{CD}	29.14	$C_{m2_c} + C_{m2_b} \parallel (C_{b_c} + (C_{m1_c} \parallel C_{m1_b}))^a$
C_{AC}	40.60	$C_{m1_c} + C_{m1_b} \parallel (C_{b_c} + (C_{m2_c} \parallel C_{m2_b}))^a$
C_{BC}	80.16	$C_{b_c} + C_{m1_c} \parallel C_{m1_b} + C_{m2_c} \parallel C_{m2_b}^a$

^a“+” means parallel connections and “||” means series connections.

TABLE IV
VALUES OF PCB PARASITIC CAPACITANCE

Capacitance	C_{m1_b}	C_{m2_b}	C_{m1_c}	C_{m2_c}	C_{b_c}
Values /pF	5.61	14.68	35.38	16.94	67.46

B. Causes of High PCB Parasitic Capacitance

Fig. 10 shows the configuration diagram of the discussed converter system. Only the ground connections of the control, sensing, and gate driving circuits, along with the power loops, are presented for simplicity. As illustrated in Fig. 10, the returns of bottom gate driving power supplies are connected to the dc–bus, and those of the top gate driving power supplies are connected to Midpoint I and II, respectively.

Parasitic capacitance exists on the power board (noted with the postfix of “pb”) and control board (noted with the postfix of “cb”), as well as the external isolated power supplies and the connecting wires between the PCBs. The capacitance on one of the boards is considered as in parallel with its counterparts from the other boards, and the parasitic capacitance presented in Fig. 5 is the corresponding lumped result. For instance, C_{b_c} is the equivalent capacitance of the parallel of $C_{b_c_pb}$, $C_{b_c_cb}$, and the bus-to-control parasitic capacitance from other positions all over the converter system.

As mentioned in Section II, the values of the discussed parasitic capacitance are highly dependent on the PCB layout of the converter and distributed on the PCBs, connectors, and wires between them. They are difficult to be accurately calculated in practice. Nevertheless, some key coppers and strays are found responsible for the high values in Table IV and could reveal their trends.

In this design, C_{b_c} is mainly introduced by the overlap of the coppers of the control ground and the dc bus nodes from two aspects. On one hand, an oversized control ground plane in the sensing circuit overlaps with the dc bus on the inner layers of the power board as shown in Fig. 11(a) and (b), leading to a

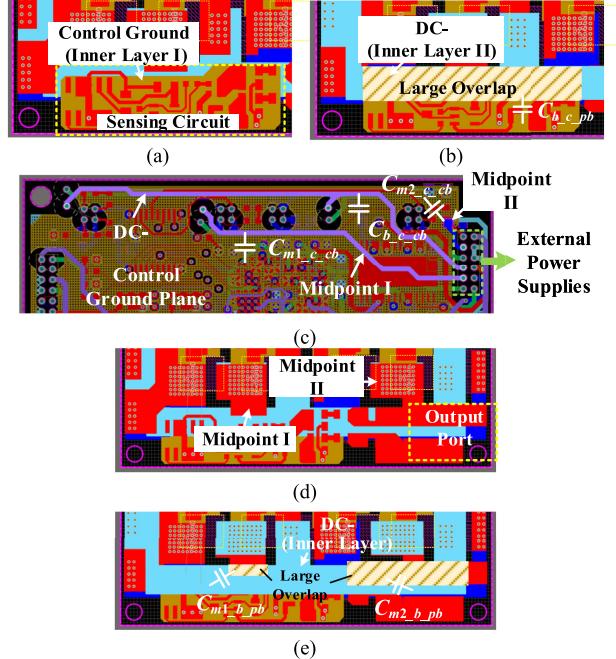


Fig. 11. PCB layouts and the formation of parasitic capacitance. (a) Top view of the sensing circuit on the power board. (b) Inner layer of the sensing circuit. The control ground plane overlaps with the copper of dc bus on the adjacent layer. (c) Return strays of the gate driver power supplies on the control board. DC–, Midpoint I, and Midpoint II correspond to the return strays of the gate driving power supplies of the bottom devices, S1, and S3, respectively. (d) Top view of the power loops. (e) Inner layer of the power loops. More overlap is found between dc bus and Midpoint II than I.

high $C_{b_c_pb}$. On the other hand, Fig. 11(c) shows the long return strays of the bottom driving power supply on the control board, which is in one of the inner layer adjacent to the control ground plane, leading to a high $C_{b_c_cb}$. Although the power loops are usually intentionally separated with the gate driving and control circuits to diminish the noise coupling between the power loops and the signal loops, attention should also be paid to the overlap between the output side power supply of the driving ICs and the control circuits.

Because Midpoint II also acts as the return terminal of the output port, a larger overlap area is found between the coppers of Midpoint II and dc buses comparing with that between the coppers of Midpoint I and dc buses, which are illustrated in Fig. 11(d) and (e) as $C_{m2_b_pb}$ and $C_{m1_b_pb}$. This leads to a higher C_{m2_b} than C_{m1_b} . Fig. 11(c) also shows that high C_{m1_c} is mainly caused by the overlap between the long return strays

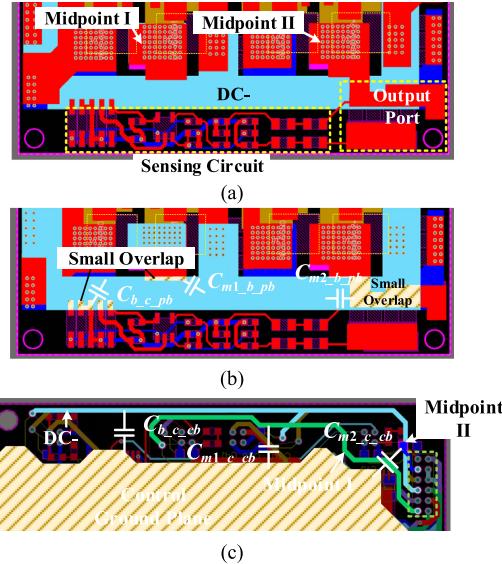


Fig. 12. Optimized PCB layouts. (a) Top view of the power loops and the sensing circuit on the power board. (b) Inner layer of the power board. The overlaps between dc bus and the sensing circuit, and Midpoint II are reduced. (c) Return strays of the gate driver power supplies and the control ground plane on the control board. The power supply and return strays are separated from the control ground plane.

of the top driving power supply of Phase-leg I and the control ground plane, which is marked as $C_{m1_c_cb}$.

C. Layout Optimization and Comparison

Some optimization methods could be employed for the PCB layouts in order to reduce the PCB parasitic capacitance and corresponding losses. One of the most vital concerns for the optimization is to minimize the overlap between different nodes, including not only the midpoints of phase-legs and dc buses in the power loops but also the gate driving power supply strays for all the GaN HEMTs, sensing circuits and control ground plane in the control circuits.

Fig. 12(a)–(c) shows some examples of PCB optimization based on the original design of Fig. 11. As shown in Fig. 12(a) and (b), the oversized control ground plane is removed from the sensing circuit. Meanwhile, the sensing circuit is squeezed up to the border to avoid direct overlap with the dc buses in the inner layers. The power supply and return strays of the gate drivers are separated from the control ground plane in the control board, which is indicated in Fig. 12(c). Both these approaches benefit for the reduction of C_{b_c} , while the latter could also remarkably reduce C_{m1_c} and C_{m2_c} . Fig. 12(b) also shows the layout optimization of Midpoint II and the output terminal. The overlap area of the cooper is reduced by around 56% and will lead to a smaller C_{m2_b} .

The parasitic capacitance shown in Figs. 11 and 12 are extracted by Ansoft Q3D to verify the proposed optimization approaches. The extraction results are presented in Table V. The measured values of parasitic capacitance with optimized layouts are listed in Table VI. Most of the parasitic capacitance is reduced comparing with Table IV, especially for C_{b_c} and

TABLE V
COMPARISON OF Q3D EXTRACTION RESULTS

Capacitance	Q3D extraction results /pF Before optimization	Q3D extraction results /pF After optimization
$C_{b_c_pb}$	33.64	1.96
$C_{b_c_cb}$	27.61	3.08
$C_{m1_b_pb}$	1.80	1.80
$C_{m2_b_pb}$	10.48	6.43
$C_{m1_c_cb}$	15.6	2.99
$C_{m2_c_cb}$	0.41	2.15

TABLE VI
VALUES AND LOSSES OF PARASITIC CAPACITANCE AFTER OPTIMIZATION

Capacitance	C_{m1_b}	C_{m2_b}	C_{m1_c}	C_{m2_c}	C_{b_c}
Values /pF	11.52	11.55	7.81	7.75	16.42
Losses/W ^a	0.160	0.159	0.047	0.046	0.098

^aThe losses are calculated at $f_s = 160$ kHz.

TABLE VII
KEY PARAMETERS OF THE PROTOTYPE

Parameters	Values
Input voltage V_{bus}	400 V
Output voltage V_o	80V
Nominal output power P_o	100 W
Switching frequency f_s	160 kHz
Output filter inductance L_f	110 μ H
GaN HEMTs	GS66502B
Gate driving IC	Si8274
Core of filter inductor	PQ2020

C_{m1_c} , which are reduced by 76% and 78%, respectively. C_{m1_b} is slightly increased because of the closer distance between S_1 and S_2 gate driving power supply strays, which is the cost of the separation between power supply strays and the control ground plane. Table VI also shows the power losses of each parasitic capacitance, and significant reductions are observed on the power losses of C_{m1_b} , C_{m2_b} , and C_{b_c} .

It should be noted that, due to the high sensitivity of the gate driving for GaN HEMTs, special attentions are usually paid to the gate driving layouts to reduce loop inductance and eliminate the unexpected coupling between power loops and the gate driving loops. Gate driving circuits with vertical structures are usually employed for high speed GaN HEMTs [31], [32]. However, the midpoint-to-bus parasitic capacitance tends to increase if there are large overlaps between the coppers of midpoints and dc buses. Moreover, the midpoint-to-control and control-to-bus capacitance must be taken into consideration as the potential of the control ground is also pulsating referring to the dc bus. It is recommended to reduce the overlaps of the coppers between all the static nodes and voltage pulsating nodes with enough distance to reduce this capacitive loss.

IV. EXPERIMENTAL VERIFICATION

A. Implementation of Prototype and Testing Platform

Two full bridge converter prototypes are built to verify the proposed analysis. The key parameters and the photographs of

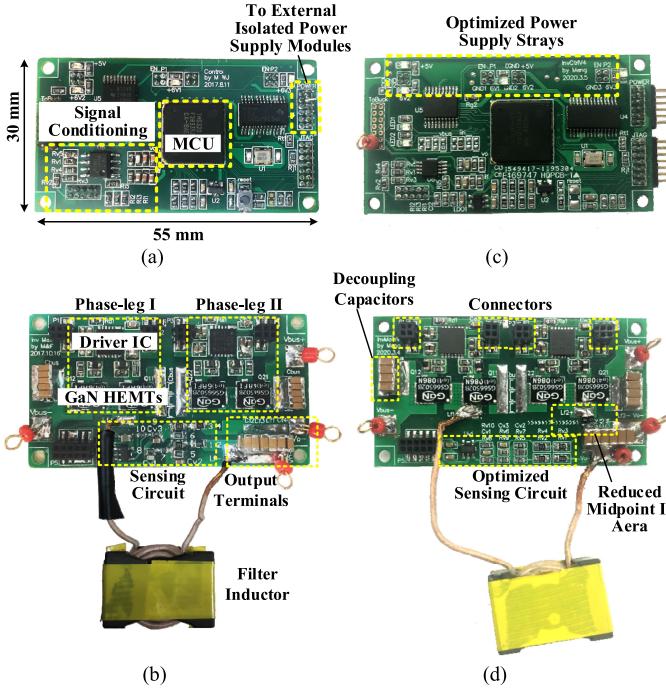


Fig. 13. Photographs of the converter prototypes. (a) and (b) Control board and power board before layout optimization. (c) and (d) Control board and power board after layout optimization. The layouts are kept as same as possible except for the changes mentioned in Fig. 12 to provide fair comparisons.

TABLE VIII
INSTRUMENTS USED FOR MEASUREMENT

Equipment	Model
LCR meter	Agilent 4285A
Network analyzer	Agilent E5061B
Thermocouples	Omega TT-T-36
Data Acquisition Unit	Agilent 34970A
Oscilloscope	Yokogawa DLM2034
Differential Voltage Probe	Sunrise SRS2050
Current Probe	Keysight N2783B

the prototypes are given in Table VII and Fig. 13. The instruments used for measurement are listed in Table VIII. Fig. 13(a) and (b) is the control board and the power board before layout optimization, while Fig. 13(c) and (d) is of those after layout optimization. The control boards and the power boards are connected through several pairs of connectors. The control and sensing circuits and the gate driving ICs are supplied by external isolated power modules. The layouts are kept as same as possible except for the changes mentioned in Fig. 12 in order to provide fair comparisons. Therefore, other parameters of the converter, such as the parasitic inductance, are barely changed.

Fig. 14(a) and (b) shows the experimental waveforms of the voltage across the inductor, midpoints to dc bus voltage, midpoints to control ground voltage, and control ground to dc-voltage. The waveforms show agreement with the theoretical waveforms depicted in Fig. 7.

It is commonly known that the power losses on the devices lead to temperature rises. The temperature rise of the device is approximately in proportion to its power loss if the thermal

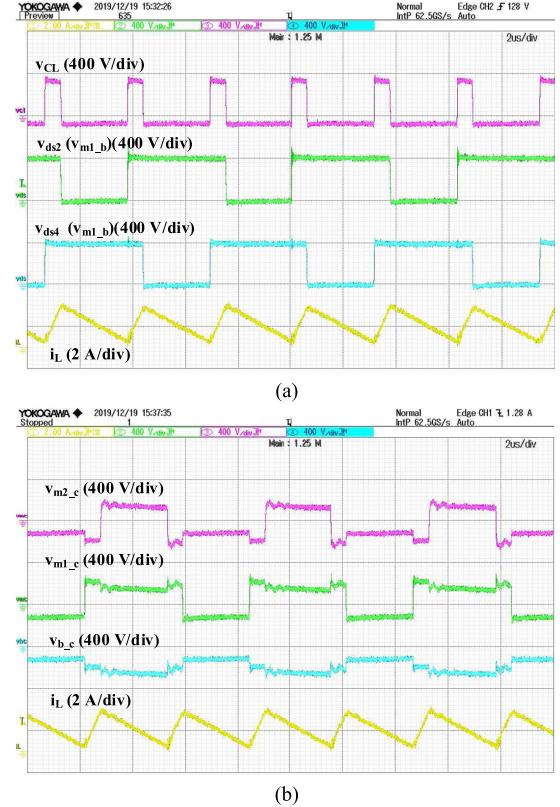


Fig. 14. Experimental waveforms of the voltage across the inductor, midpoint-to-control capacitance, midpoint-to-bus voltage, and control-to-bus capacitance.

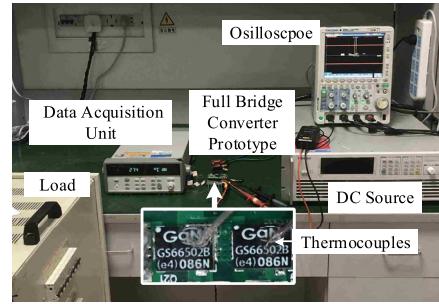


Fig. 15. Testing platform and the prototype. The temperature is measured with Agilent 34970A data acquisition unit and Omega TT-T-36 thermocouples. The thermal-couplers are stuck on the cases of the devices.

resistance is assumed to be constant in the same cooling conditions. As for the converter prototype in this article, most of the losses are produced by GaN HEMTs and the filter inductor. In fact, the temperature of the inductor shows little effect on the devices for the large distance separation between the inductor and the power board. Therefore, the losses of the devices could be measured by monitoring their temperature [33], [34].

Power devices are usually characterized by the junction temperature T_j by the manufacturers. However, T_j is difficult to be measured for practical power converters. Therefore, the case temperature T_c is measured instead of T_j in this article. The testing platform is shown in Fig. 15. The temperature monitoring

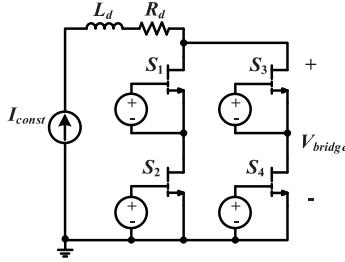


Fig. 16. Loss calibration circuit. The filter inductor is disconnected and all the GaN HEMTs are set to ON-state with a constant current source. The case temperature of GaN HEMTs is measured and the total power losses are calculated with I_{const} and V_{bridge} .

system consists of an Agilent 34970A data acquisition unit and Omega TT-T-36 thermocouples. The thermocouples are stuck on the cases of the devices, which are air-cooled with a heatsink using the bottom side cooling method [35].

B. Loss Calibration and Measurement Methods

The loss calibration circuit is shown in Fig. 16 and the calibration procedures are as follows.

- 1) The filter inductor is disconnected from the power loop.
- 2) The gate-to-source voltage is set at a high level to guarantee the ON-state for all the GaN HEMTs. Meanwhile, a current limiting resistor R_d is added.
- 3) The dc input voltage source is replaced with a constant current source. With the conduction of a suitable current I_{const} , T_c is measured until its thermal steady-state value $T_{c,st}$.
- 4) The voltage drop on the phase-legs V_{bridge} is measured at the same time with the data acquisition unit.
- 5) The total power loss on the devices is then calculated.

By repeating Steps 3) and 4) with different I_{const} , the curve of P_{loss} versus $T_{c,st}$ is obtained.

$$P_{\text{loss}} = V_{\text{bridge}} I_{\text{const}}. \quad (20)$$

Note that V_{bridge} is increasing along with the device temperature during Step 4), owing to the positive temperature coefficient of the ON-state resistance. Therefore, the value of V_{bridge} at thermal steady-state should be utilized for P_{loss} calculation.

Fig. 17(a) shows the measured T_c at $I_{\text{const}} = 4.3$ A as an example. $T_{c,st}$ can be easily obtained from the T_c curve. The measurement results of $T_{c,st}$ and P_{loss} with different I_{const} are presented in Fig. 17(b) as triangular marks. A strong linear relationship is observed between $T_{c,st}$ and P_{loss} , and the linear fitting result is shown as the solid line, which is expressed as

$$T_{c,st} = 7.488 P_{\text{loss}} + 35.71^\circ\text{C}. \quad (21)$$

When the converter operates in normal conditions, the power losses on GaN HEMTs consist of conduction loss, turn-ON loss, turn-OFF loss, parasitic capacitance loss, dead-time loss, etc. Although the loss calibration is based on the conduction loss, it is believed that a certain amount of loss will generate identical temperature rising in the same cooling conditions, regardless of the causes of the losses. Therefore, the total losses of the devices

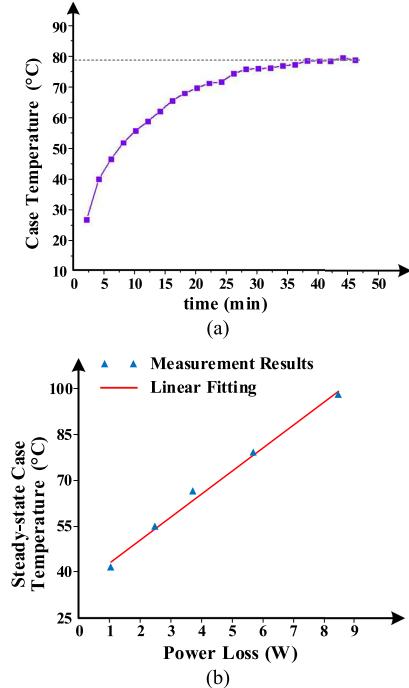


Fig. 17. Case temperature measurement results of the loss calibration. (a) Measured T_c curve at $I_{\text{const}} = 4.3$ A. T_c reaches its thermal steady-state after about 45 min. (b) Relation between $T_{c,st}$ and the P_{loss} . The triangle marks are the measurement results. The solid line is the linear curve fitting result.

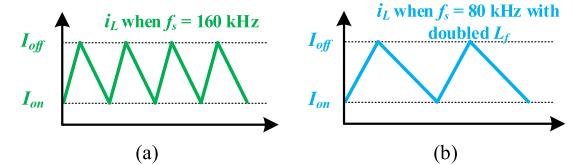


Fig. 18. Schematic waveforms of the inductor current. (a) $f_s = 160$ kHz. (b) $f_s = 80$ kHz and doubled filter inductance. The peak and valley values of the inductor current remain the same when the switching frequency is reduced by half and filter inductance is doubled.

are obtained referring to Figs. 17(b) and (21) by monitoring $T_{c,st}$ of the devices in normal operating conditions.

Among all the loss components, conduction loss is independent of the switching frequency, while the others are in proportion to it. Therefore, the switching-related loss is defined as the sum of the loss components that are related to the switching frequency, including turn-ON loss, turn-OFF loss, parasitic capacitance loss, dead-time loss, etc. The former three occupy most of the switching-related loss in this design, making the other parts negligible. In order to separate the conduction and switching-related loss from the total losses, $T_{c,st}$ is also measured at the switching frequency of 80 kHz, other than the original design of 160 kHz. Two filter inductors are connected in series to provide a doubled inductance and guarantee the same turn-ON and turn-OFF current as illustrated in Fig. 18, and therefore the same $E_{\text{on}}/E_{\text{off}}$ for the devices. The measured total losses P_{loss} when the switching frequency is 160 and 80 kHz are

expressed as

$$\begin{aligned} P_{\text{loss}(160\text{kHz})} &\approx P_{\text{sw}(160\text{kHz})} + P_{\text{cond}(160\text{kHz})} \\ &= P_{\text{sw_other}(160\text{kHz})} + P_{\text{CL}(160\text{kHz})} \\ &\quad + P_{\text{cond}(T_{c_st1})} \end{aligned} \quad (22)$$

$$\begin{aligned} P_{\text{loss}(80\text{kHz})} &\approx P_{\text{sw}(80\text{kHz})} + P_{\text{cond}(80\text{kHz})} \\ &= P_{\text{sw_other}(80\text{kHz})} + P_{\text{CL}(80\text{kHz})} + P_{\text{cond}(T_{c_st2})} \end{aligned} \quad (23)$$

where P_{cond} is the conduction loss and P_{sw} represents the switching-related loss, which is divided as the capacitive loss of C_L (P_{CL}), and other parts of the switching-related loss ($P_{\text{sw_other}}$). T_{c_st1} and T_{c_st2} are the corresponding steady-state case temperature of the devices in each case. It should be noted that $P_{\text{sw_other}}$, which consists of $V-I$ overlap loss, junction capacitance loss, and PCB parasitic capacitance loss as described in Section II, is in proportion to the switching frequency f_s . Therefore, $P_{\text{sw_other}}$ satisfies

$$P_{\text{sw_other}(160\text{kHz})} = 2P_{\text{sw_other}(80\text{kHz})}. \quad (24)$$

With the same turn-ON and turn-OFF current, P_{cond} only depends on the temperature-related $R_{ds(\text{on})}$ of GaN HEMTs. $R_{ds(\text{on})}$ at a certain temperature T_c could be easily obtained during Step 4) of the loss calibration with

$$R_{ds(\text{on})(T_c)} = \frac{V_{\text{bridge}(T_c)}}{I_{\text{const}}}. \quad (25)$$

Therefore, P_{cond} in each case satisfies

$$P_{\text{cond}(160\text{kHz})} = \frac{R_{ds(\text{on})(T_{c_st1})}}{R_{ds(\text{on})(T_{c_st2})}} P_{\text{cond}(80\text{kHz})}. \quad (26)$$

Moreover, the relation of the capacitive loss of C_L in each case is expressed as (27) according to (14) for C_L is cut by half with doubled inductance

$$P_{\text{CL}}(160\text{kHz}) = 4P_{\text{CL}}(80\text{kHz}). \quad (27)$$

By combining (22)–(27), P_{sw} and P_{cond} in each case could be calculated. The switching and conduction losses are therefore separated from the total losses of the devices.

C. Comparison of Calculated and Measured Losses

With the aforementioned calorimetric method, the total losses on the GaN devices of the original prototype when $f_s = 160$ and 80 kHz are measured as 5.2 and 3.17 W, respectively. Meanwhile, the total losses on the GaN devices of the optimized prototype when $f_s = 160$ and 80 kHz are measured as 4.46 and 2.76 W, respectively. The loss separation results based on (22)–(27) and the calculated losses are presented in Fig. 19. Fig. 19(a) shows the loss breakdown without the consideration of PCB parasitic capacitance. Fig. 19(b) and (c) shows the comparison of measured losses and modified calculated results before layout optimization, while Fig. 19(d) and (e) shows that after optimization. The turn-ON and turn-OFF losses in Fig. 19(a) are obtained according to the $E_{\text{on}}/E_{\text{off}}$ curves from DPT simulation with GS66502B LTSpice model. On one hand, the capacitive losses in the modified turn-ON and turn-OFF losses are calculated

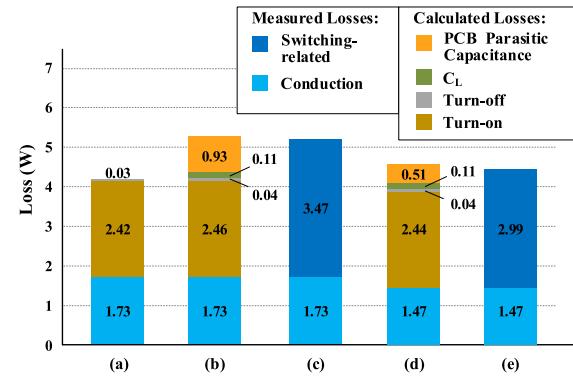


Fig. 19. Comparison of the calculated and measured losses at $f_s = 160$ kHz. Parasitic capacitance causes 26% extra loss of the switching-related loss in the original design. It is significantly reduced with the proposed optimization methods. (a) Calculated losses without the consideration of parasitic capacitance. (b) Modified calculated losses of the original design. (c) Measured losses of the original design. (d) Modified calculated losses after layout optimization. (e) Measured losses after layout optimization.

based on the values in Tables I, IV, and VI, and (14)–(19). On the other hand, the overlap loss is modified according to the relation between t_{vf} and Q_{total} as described in Section II.

It is indicated in Fig. 19 that the capacitive loss of parasitic capacitance is 0.93 W and the calculated switching-related loss is 3.54 W before layout optimization, which means that the extra loss caused by parasitic capacitance occupies as high as 26% of the switching-related loss. After layout optimization, the parasitic capacitance loss is reduced by around 40% and down to 0.51 W for the calculated results. Also, a reduction of 0.44 W is noticed on the sum of calculated parasitic capacitance loss, turn-ON loss, and turn-OFF loss and of 0.48 W on the measured switching-related loss with the proposed optimization methods. The calculated switching-related losses show agreement with the measured results within error permissibility. It is proved that PCB parasitic capacitance needs to be taken into consideration for accurate loss analysis of GaN HEMTs, especially in high switching frequency and high power density applications.

V. CONCLUSION

The extra switching loss caused by PCB parasitic capacitance is studied in this article. The mechanism of parasitic capacitance loss is demonstrated and the full bridge model with PCB parasitic capacitance, in which both the power loops and the control circuits are included, is proposed. Theoretical analysis shows that remarkable loss is introduced by this parasitic capacitance due to the voltage pulsation. The cause of high PCB parasitic capacitance is analyzed in detail according to the layouts, and some optimization methods are proposed to reduce it. The theoretical analysis is verified on two full bridge converter prototypes. The measurement method of the capacitance is presented, along with the waveforms of the voltage across the parasitic capacitance. The losses of the GaN HEMTs are measured with a calorimetric method. The comparison of calculated and measured results shows the validity of the proposed analysis.

Conclusions could be drawn as follows.

- 1) PCB parasitic capacitance exists between different nodes in the converter system. As the voltage across the parasitic capacitance pulsates with the switching actions of the GaN HEMTs, the energy of the capacitance is dissipated in the channels of GaN HEMTs, therefore leading to extra losses.
- 2) PCB parasitic capacitance is found not only between the pulsating nodes and the static nodes in the power loops but also between the strays in the control circuits, sensing circuits, and the isolated power supplies, which may easily be omitted.
- 3) The voltage between the control ground and the static nodes of power loops is also pulsating in practical converters. It is determined by the PCB parasitic capacitance network. The voltage pulsation on each capacitance could be drawn from the ac and dc models. Thus, the capacitive loss is calculated.
- 4) The overlaps between different nodes lead to high parasitic capacitance, which could be effectively reduced by layout optimization. An extra loss reduction of 40% is observed in this design when the PCB parasitic capacitance is reduced.
- 5) Experimental results show that the extra loss caused by PCB parasitic capacitance could be as high as 26% of the total switching-related loss. The overlook of PCB parasitic capacitance will lead to a significant deviation in loss calculation.

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