An Optimized Layout with Low Parasitic Inductances for GaN HEMTs Based DC-DC Converter

Wang Kangping, Ma Huan, Li Hongchang, Guo Yixuan, Yang Xu, Zeng Xiangjun, and Yu Xiaoling
State Key Laboratory of Electrical Insulation and Power Equipment
Xi'an Jiaotong University
Shaanxi, Xi'an, China
zengxj@mail.xjtu.edu.cn

***Abstract*—Reducing parasitic inductances are critical for improving efficiency and safety in Gallium Nitride (GaN) based DC-DC Converter. This paper aims at reducing the driver loop inductance and power loop inductance by optimizing the PCB layout. Firstly, this paper compares three different kinds of driver loop layouts by Maxwell 3D simulation. The results show that the driver loop inductances of single-layer layout with a shielding layer and double-layers layout are much smaller than that of the conventional single-layer layout. Then a novel double-sided layout is proposed, which has a small power loop inductance because the magnetic field is significantly canceled by the interleaved current. Finally, the design is verified by a buck converter operating at an input voltage of 12 V, an output voltage of 3.3 V, and an output current of 8 A. Experimental results show that the power loop inductance is about 0.1nH, which reduces 75% than that of the reported best layout.**

Keywords—Gallium Nitride; layout; DC-DC Converter; parasitic inductance

I. INTRODUCTION

In recent years, the Gallium Nitride high electron mobility transistors (GaN HEMTs) have emerged as promising devices for high frequency, high efficiency, and high density power conversion due to a better figure of merit (FOM) than that of comparable Si transistors[1, 2]. However, unavoidable parasitic inductances limit the excellent switching performance of GaN transistors.

On the one hand, the gate's breakdown voltage of enhancement mode Gallium Nitride (eGaN) transistors is 6V. However, the devices are designed to achieve optimal performance with a gate drive voltage about 5V. This leaves a very small margin for driver overshoot to ensure safe operation. The driver loop inductance is critical and it needs to be strictly controlled. On the other hand, the power loop parasitic inductances increase switching losses, cause ringing and voltage spike [3-6]. To enable the high switching speed, low parasitic packaging and PCB layout are required. The eGaN transistors have a land grid array (LGA) package, which contributes little parasitic inductances[7]. PCB layout then is the major contributor and it needs to be optimized carefully.

Much work has been carried out on reducing the parasitic inductances by optimizing the layout. Youhao Xi[8] empirically gives an optimized driver loop layout by reducing the wire length and the area of driver loop. However, a large gate resistor is used to reduce the overshoot of gate voltage, which will reduce the switching speed and increase switching losses. Recently, three different kinds of power loop layouts are compared in[9]. The power loop inductance of the best layout is about 0.4nH. The ringing is still obvious. So it is necessary to further reduce the parasitic inductances to get a better performance.

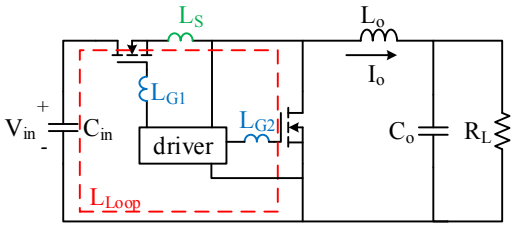


Fig. 1 Typical circuit of a buck converter

This paper aims at reducing the parasitic inductances of driver loop and power loop by optimizing PCB layout. Firstly, three different kinds of driver loop layouts are compared. Then a double-sided layout is proposed that can reduce the power loop inductance effectively. Finally, a buck converter is applied to verify the design.

II. EFFECTS OF PARASITIC INDUCTANCES ON CIRCUIT PERFOREMANCE

Fig.1 is a typical circuit of a buck converter. There are three critical parasitic inductances that have a significant impact on DC-DC converter's performance. The common source inductance L_S is the inductance shared by power loop and driver loop. It increases the switching loss by lowering the switching speed of the switching devices. It mainly comes from the package parasitic inductance. The high-frequency power loop inductance L_{Loop} is composed of the series inductance of the input capacitor C_{in}, the PCB trace parasitic inductance, and the package inductances of the top switching device (TS) and the bottom switching device (BS). It induces a spike voltage on the devices and ringing by resonance with the output

This work was supported by Delta Environmental & Educational Foundation.

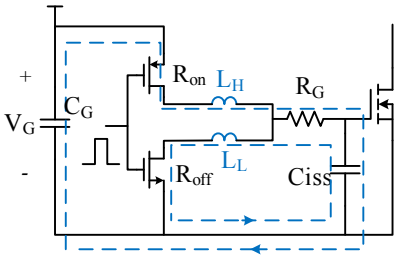


Fig. 2 Simplified equivalent circuit for the gate driver

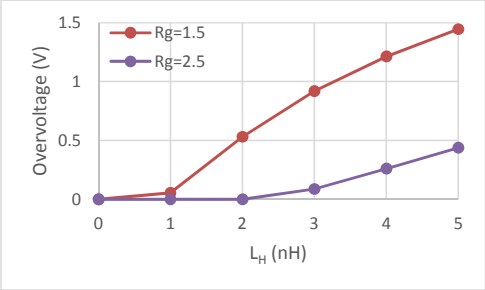


Fig. 3 The relationship between gate overvoltage and driver loop inductance

capacitance of the switching devices. Besides, the ringing in power loop will be coupled to the gate-source voltage through common source inductance L_S and miller capacitance. Therefore, reducing the high-frequency power loop inductance L_{Loop} helps reduce the ringing of drain-source and gate-source voltage.

Fig.2 is the simplified equivalent circuit for the gate driver circuit. If the gate resistance is small, the driver loop inductance will resonate with the input capacitance C_{iss} during turn-on/turn-off transition. The gate overvoltage during turn on transition may exceed gate's breakdown voltage, resulting in the failure of GaN HEMTs. The gate ringing voltage during turn off transition may exceed threshold voltage, resulting in false turn-on of GaN HEMTs. As a result, the power loss is increased. Increasing gate resistance can reduce the gate overvoltage and ringing, but the switching losses are increased. Reducing driver loop inductance can reduce the gate overvoltage and ringing without increasing switching losses.

Let's take the driver LM5113 and GaN HEMT EPC2015 as an example. The total turn-on gate resistance is about 2.5Ω and the input capacitance is about 1.2nF. Because the safety margin of gate voltage is very small, so we need to strictly control the overvoltage. The relationship between gate overvoltage and driver loop inductance is shown in Fig.3. There is no overvoltage when L_H <1.9nH. If the gate resistance decreases to 1.5Ω, there is no overvoltage when L_H <0.7nH.

III. Layout Optimizing of Driver Loop

Fig.4 shows a conventional single layer layout of the driver circuit. The driver is LM5113. The top switch (TS) and bottom switch (BS) are EPC2015. The blue loop shows the gate

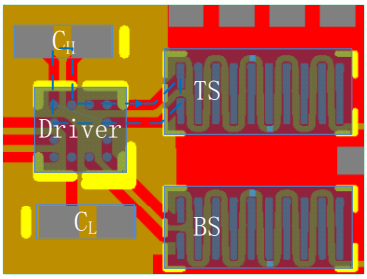


Fig. 4 Conventional single layer layout of the driver loop

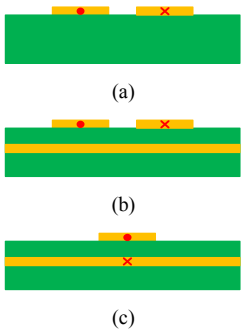


Fig. 5 Three different kinds of driver loop layout (a) single-layer layout (b) single-layer layout with a shielding layer (c) double-layers layout

current path when top switch is turned on. Three different kinds of driver loop layouts are compared. Fig.5 shows the schematic diagrams. The yellow parts represent conductor and the green parts represent isolator. The layouts are as follows:

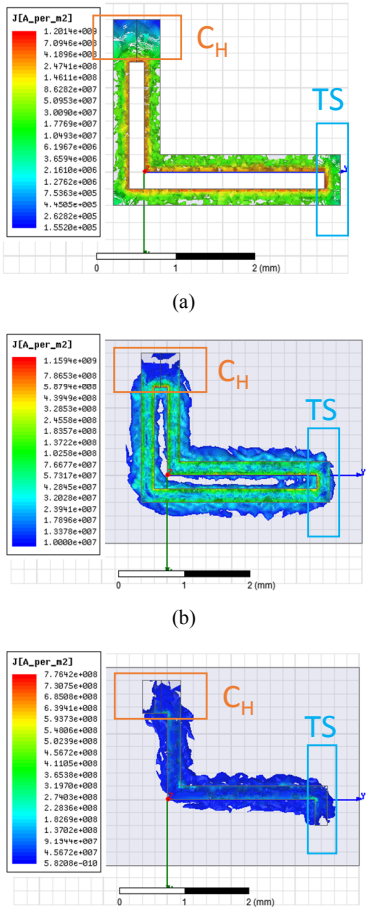
1) *Single-layer layout:* the gate current path only exists in the top layer (see Fig.5a).

2) *Single-layer layout with a shielding layer:* a complete inner layer conductor is used as shielding layer. An opposite current is induced on the shielding layer when the gate current changes. The induced current plays a role in cancelling the magnetic field generated by the gate current, which helps reducing the driver loop inductance (see Fig.5b).

3) *Double-layers layout:* the gate current flows through the top layer and inner layer. The layout has a small driver loop inductance due to a small loop area and a decentralized current (see Fig.5c).

In the layouts, copper thickness is 2oz and the distance between top layer and inner layer is 5mil. Fig.6 shows the high-frequency power loop current distribution among three different kinds of driver loop layout, which are obtained by Maxwell 3D simulation.

The simulation results of driver loop inductance are shown in Table I. The driver loop inductance of single-layer layout are 4.3nH. If a shielding layer is added, the driver loop inductance is 2.2nH, reduced by 48.8%. The driver loop inductance of double-layer layout are 1.4nH, reduced by 67.4% over that of single-layer layout.



(a)

(b)

(c)

Fig. 6 Current distribution among three different kinds of driver loop layout (a) single-layer layout (b) single-layer layout with a shielding layer (c) double-layers layout

TABLE I. SIMULATION RESULTS OF DRIVER LOOP INDUCTANCE

	Single layer layout	Single layer layout with a shielding layer	Double layer layout
L_H (nH)	4.3	2.2	1.4

IV. LAYOUT OPTIMIZING OF POWER LOOP

In order to reduce the high-frequency power loop inductance, the layout is carefully considered. The proposed layout of power loop is shown in Fig.7. TS locates on the one side of the PCB substrate and BS locates on the other side. The input capacitors C_{in} are placed close to TS in parallel. The positive terminals of C_{in} are connected to the drain electrodes of TS. Then the source electrodes of TS are directly connected to the drain electrodes of BS by via holes. The source electrodes of BS are connected to L2 by via holes. L2 is connected back to the negative terminals of C_{in}. The switching node (SW) can connect to the output inductor (Lo) through L3 or L4. The red line with arrows represents the high frequency current path.

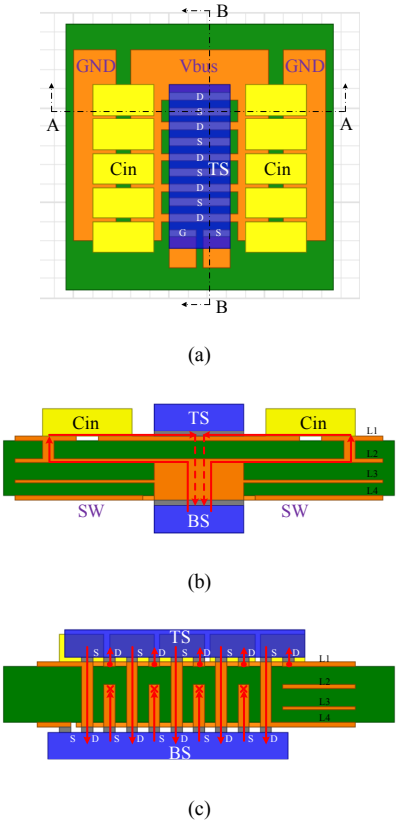


Fig. 7 Proposed layout of power loop (a) Top view (b) Sectional view of A-A plane (c) Sectional view of B-B plane

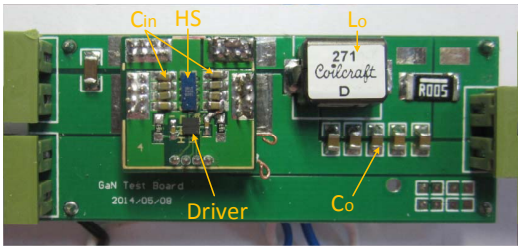
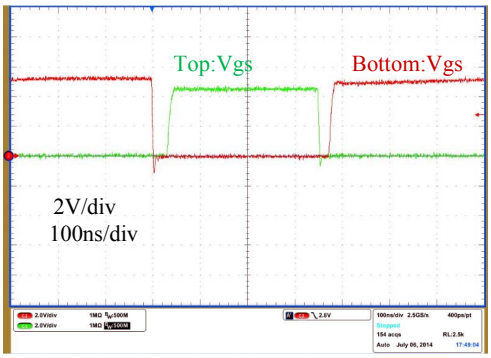


Fig. 8 Experimental prototype of a buck converter

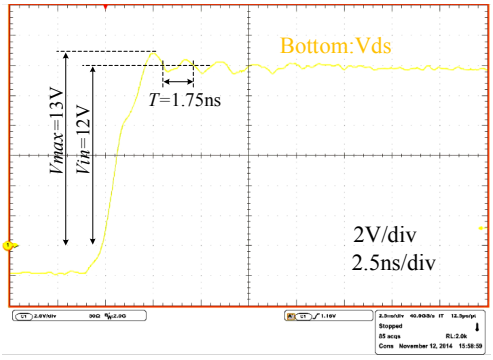
The proposed layout has the following characteristics:

1) Taking full advantage of GaN HEMTs' LGA package, the layout forms some interleaved current paths between L2 and L4 layer, as shown in Fig.7c. The interleaved currents can cancel magnetic field by themselves effectively, resulting in a small high-frequency power loop inductance.

2) The input capacitors are placed in the left and right sides of TS in order to form two current paths, as shown in Fig.7b. The equivalent high frequency power loop inductance in each current path is connected in parallel, therefore the total high frequency power loop inductance is further reduced.



(a)



(b)

Fig. 9 (a) Gate-source voltage waveform. Top switch: blue line; Bottom switch: red line (b) Drain-source voltage waveform of bottom switch

V. Experiment Verification

A buck converter is tested, which operates at a switching frequency of 1 MHz, an input voltage of 12V, an output voltage of 3.3 V, and an output current of 8 A. Fig. 8 shows the experimental prototype. The TS and BS devices are EPC2015 and the driver is LM5113. The PCB board is composed of four layers and its thickness is 1mm. The distance between L1 and L2 is 5mil. The copper thickness of each layer is 2oz.

The driver loop layout of TS and BS are double layer layout and single layer layout with a shielding layer respectively. No gate resistor is added between the driver and switching devices. The gate-source voltage waveforms are measured when the input voltage is 0V, shown in Fig.9a (top switch: green line; bottom switch: red line). The gate overvoltages of top switch and bottom switch are almost zero.

The drain-source voltage waveform of bottom switch is measured by the probe with a high bandwidth, as shown in Fig.9b. The bandwidth of oscilloscope is set to 2GHz. The overshoot is about 8.3% and the ringing period is about 1.75ns.

The high frequency power loop inductance can be calculated by:

$$L_{Loop} = \frac{T_{ring}^{\ 2}}{4\pi^2 C_{oss@V_{in}}} \quad (1)$$

where $C_{oss@V_{in}}$ is the output capacitance of bottom switch at input voltage V_{in} and T_{ring} is the ringing period of the drain-source voltage. The high-frequency power loop inductance is about 0.1nH calculated from (1), which reduces by 75% over that of the reported best PCB layout.

VI. Conclusions

This paper aims at reducing the driver loop inductance and power loop inductance by optimizing the PCB layout. Three different kinds of driver loop layouts are compared. The results show that single-layer layout with a shielding layer or double-layers layout can reduce the driver loop inductance by 48.8%, 67.4% over that of single-layer layout respectively. A novel double-sided layout is proposed, providing a 75% decrease in high-frequency power loop inductance over the reported best layout because the magnetic field is significantly cancelled by the interleaved currents.

References

[1] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," *Power Electronics, IEEE Transactions on,* vol. 29, pp. 2155-2163, 2014.

[2] F. C. Lee and L. Qiang, "High-Frequency Integrated Point-of-Load Converters: Overview," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 4127-4136, 2013.

[3] D. Reusch, F. C. Lee, D. Gilham, and Y. Su, "Optimization of a high density gallium nitride based non-isolated point of load module," presented at the Energy Conversion Congress and Exposition (ECCE), 2012.

[4] J. Wang, H. Chung, and R. Li, "Characterization and Experimental Assessment of the Effects of Parasitic Elements on the MOSFET Switching Performance," *Power Electronics, IEEE Transactions on,* 2013.

[5] Y. Ren, M. Xu, J. Zhou, and F. C. Lee, "Analytical loss model of power MOSFET," *Power Electronics, IEEE Transactions on,* vol. 21, pp. 310-319, 2006.

[6] W. Kangping, Y. Xu, Z. Xiangjun, Y. Xiaoling, L. Hongchang, G. Yixuan, *et al.*, "Analytical loss model of low voltage enhancement mode GaN HEMTs," in *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE*, 2014, pp. 100-105.

[7] D. Reusch, D. Gilham, Y. Su, and F. C. Lee, "Gallium Nitride based 3D integrated non-isolated point of load module," in *Applied Power Electronics Conference and Exposition (APEC)*, 2012, pp. 38-45.

[8] Y. Xi, M. Chen, K. Nielson, and R. Bell, "Optimization of the drive circuit for enhancement mode power GaN FETs in DC-DC converters," in *Applied Power Electronics Conference and Exposition (APEC)*, 2012, pp. 2467-2471.

[9] D. Reusch and J. Strydom, "Understanding the Effect of PCB Layout on Circuit Performance in a High-Frequency Gallium-Nitride-Based Point of Load Converter," *Power Electronics, IEEE Transactions on,* vol. 29, pp. 2008-2015, 2014.