Paralleling GaN E-HEMTs in 10kW-100kW Systems

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***Abstract*— Industry is adopting GaN HEMT in 10kW-100kW and higher power systems due to the ultra-fast switching capabilities of GaN. Paralleling GaN HEMT transistors is an appealing idea to further increase the power capability and reduce conduction losses of systems. The characteristics of E-mode GaN HEMT, such as positive temperature coefficient of $R_{DS(ON)}$ and a temperature independent threshold voltage, are very suitable for paralleling devices. However, the main challenge for parallel operation is thought to be the diverse parasitics of the power stage and gate driver circuits, which are very sensitive to the high di/dt and dv/dt during the switching process.**

In this paper, an analytic model for the switching process of paralleled GaN HEMT transistors is built to analyze the effects of parasitics and device characteristics on paralleling, and the design consideration for gate driver and layout is also presented. A half bridge power stage consisting of four high-side and four low-side 60 A / 650 V GaN HEMTs in parallel is designed to undertake 240 A / 400 V hard switching on and off. Double pulse testing results are presented to confirm GaN paralleling capability.

Keywords—GaN HEMT; paralleling; parasitics; gate driver design； PCB Layout

I. INTRODUCTION

GaN E-HEMTs (high electron mobility transistors) are being designed into many power electronics applications, including travel adapters, wireless chargers, smart home appliances, high efficiency AC-DC datacenter power supplies, industrial motor drives, distributed energy generation and storage systems, aerospace, automotive traction inverters, on-board EV battery chargers, DC-DC converters and etc.

This is exemplified by the lowest figure of merit ($R_{DS(on)}$ x Q_G) of all power transistor technologies available today as shown in Figure 1. The ultra-fast switching capabilities of GaN, combined with low on-resistance and superior thermal performance, enables higher efficiency and power density in these applications.

Industry is also applying GaN transistors in 10kW-100kW and higher power systems. Currently the commercially available GaN HEMT with highest current capability is GS66516T (60 A / 650 V) from GaN Systems Inc. Paralleling GaN HEMTs is a must to further increase the power capability and efficiency of high power systems.

The characteristics of E-mode GaN HEMT are very suitable for paralleling. Using GaN Systems' GS66516T as an example, the I-V curve at different temperatures is shown in Figure.2, where obvious positive dependency on temperature is shown. In parallel applications, the junction temperature of HEMTs of lower $R_{DS(ON)}$ devices will increase to balance the current sharing during on-state.

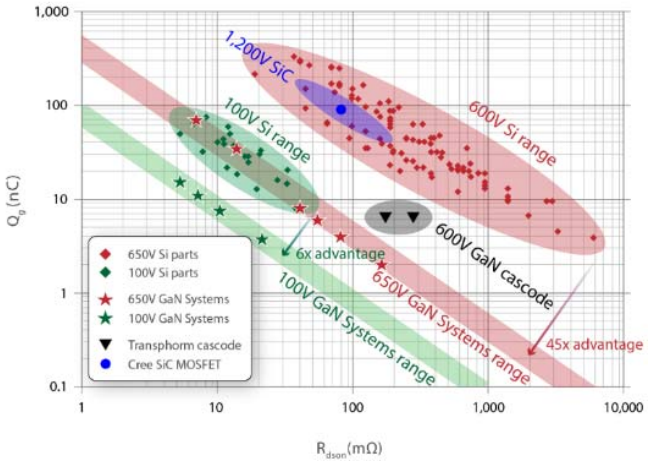


Figure. 1. Figure of merit comparison between different technologies

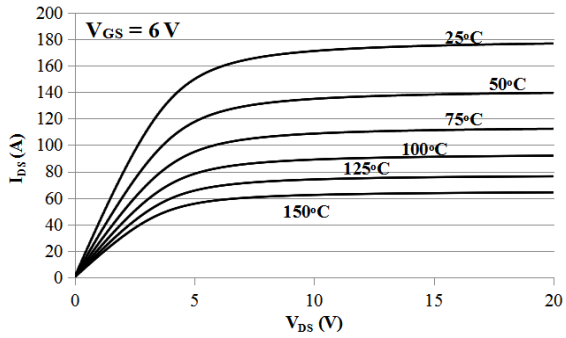


Figure. 2. V-I Curve of GS66516T vs. Temperature

Furthermore, the threshold voltage (V_{th}) of the GS66516T is nearly constant as a function of junction temperature as shown in Figure 3. The device with lower V_{th} will turn on earlier and turn off earlier which will result in a higher turn-on switching loss and a lower turn-off switching loss. The dynamic current sharing and switching loss distribution will not be effected by unbalanced temperature distribution of paralleled transistors.

The main challenge for parallel operation is thought to be the diverse parasitics of the power stage and gate driver circuits, which are very sensitive to the high di/dt and dv/dt during the switching process. Although the effect of parasitics on single device switching has been thoroughly discussed in the previous

work [1][2][3][4], there is very little previous work focusing on the dynamic performance of paralleled GaN HEMTs [5][6], and paralleling of more than 2 GaN HEMTs is thought to be extremely difficult to realize [7].

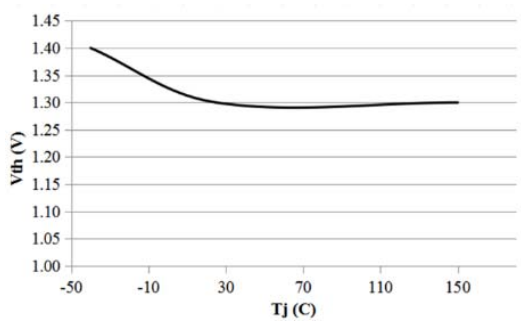


Figure. 3. Vth of GS66516T vs. Temperature

Zero Voltage Switching (ZVS) technology could relieve the high di/dt stress during the hard turn-on switching process, facilitating GaN HEMT paralleling. A 4x GS66516T in parallel based 7.2 kW On-board Charger has been successfully developed [8] with 97% efficiency, and 3.3 kW/L Power density, in which a 400 V / 92 A hard turn-off switching was reliably demonstrated.

The aim of this paper is to remove bottlenecks of applying GaN HEMT to ~100 kW power electronics systems, which are not only limited to ZVS typologies but also hard switching applications. In Section II, an analytic model for switching process of paralleled GaN HEMTs is built, and the design rules for gate driver and PCB layout are concluded based on the quantitative analysis of parasitics. In Section III, the design of 240 A / 650 V half bridge power stage with 4x GS66516T in parallel is detailed with the parasitics fully extracted. In Section IV, the experimental result of 240 A / 400 V hard switching is presented to verify the design.

II. Effects and Design Rules of Parasitics for Paralleled GaN HEMTs

Compared with the analytical loss model on Si MOSFET[12], the unique characteristics of GaN HEMT, e.g. absence of body diode, have been taken into consideration. Special attention is paid on the additional parasitics introduced by the paralleled transistors.

The equivalent circuit of a half bridge power stage consisting of two high-side and two low-side GaN HEMTs in parallel is shown as Figure 4, in which all the parasitic inductance in the gate drive loop and power commutation loop is included.

Instead of trying to predict the switching waveform of paralleled transistors, the aim of this section is to understand the effects of parasitics and device characteristics on paralleled transistors paralleling during the switching process via the built analytical model in this section. Numerical methods, e.g. SPICE simulation, will be a more efficient way to precisely model the non-linear trans-conductance and parasitic capacitance of power switches.

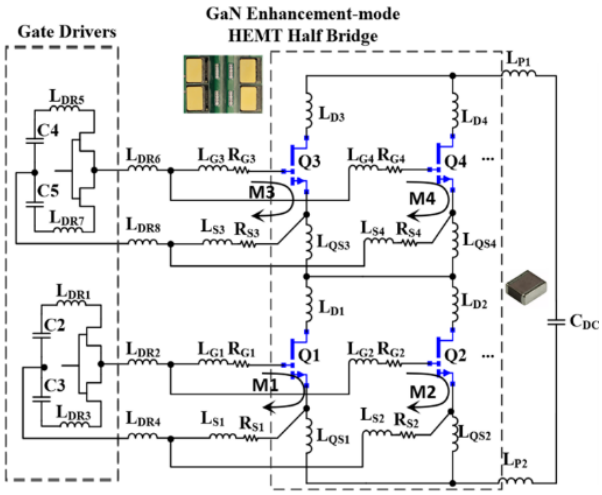


Figure.4. Equivalent Ciruit of Half Bridge with 2x GaN HEMTs in Parallel

A. Switching-on Process

The state of GaN HEMT as well as the waveform of V_{ds}, I_{ds} during switching on is shown in Figure 5. The switching on process of paralleled GaN HEMTs is divided into four periods to ease the analysis, P1-delay period, P2-di/dt period, P3-dv/dt period, P4-remaining switching period.

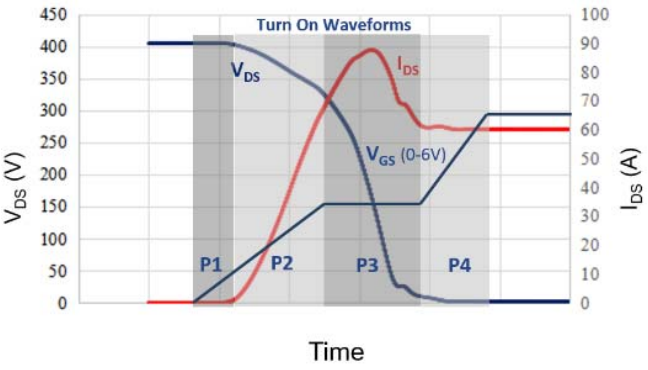


Figure.5.a Vds, Ids Waveform During Switching on

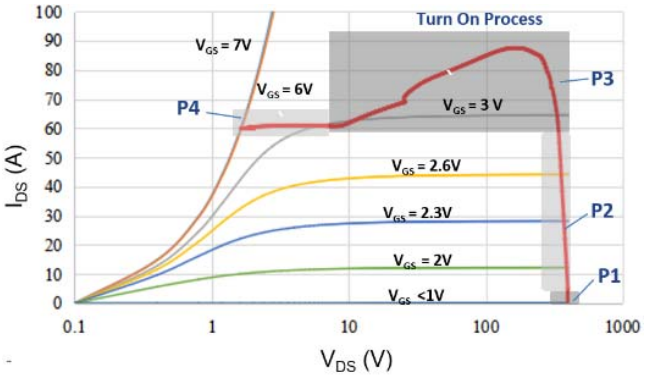


Figure. 5.b State of GaN HEMT During Switching on

1) P1:Delay Period

When controller signal is added to the low side gate driver, the higher switch of totem pole circuit in gate driver chip is turned on. The gate driver capacitor begins to charge the C_{ISS} ($C_{GS}+C_{GD}$) of paralleled HEMT. When $V_{GS}<V_{th}$ (threshold voltage of GaN HEMT), the 2-Dimensional Electron Gas (2DEG) is not conducting as shown in Figure 5.

Gate current I_G charges C_{iss} exponentially through the gate resistors and parasitics. This period ends when v_{GS} of either of the paralleled HEMTs reaches the threshold voltage.

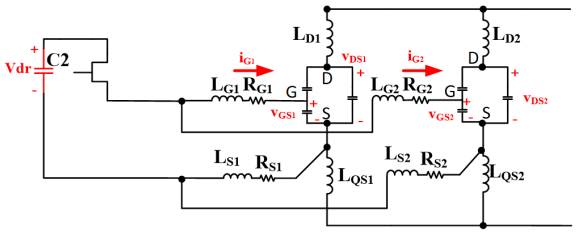


Figure. 6. Equivalent Circuit during Delay Period of Switching on Process

Only taking the low side gate driver circuit into consideration, the equivalent circuit of this period could be simplified as shown in Figure 6. To ease the derivation, we only list the equations for the left one(Q1) of two paralleled transistors.

The circuit equations of Q1 are expressed by (1)~(2).

$$V_{dr}=L_1\cdot\frac{di_{G_1}}{dt}+R_1\cdot\frac{di_{G_1}}{dt}+v_{GS_1} \quad (1)$$

$$i_{G_1}=C_{ISS_1}\cdot\frac{dv_{GS_1}}{dt} \quad (2)$$

Where, $R_1=R_{G1}+R_{S1}$, $L_1=L_{G1}+L_{S1}$.

So, V_{GS} could be derived as (3).

$$v_{GS_1}=V_{dr}\cdot\left(1+\frac{S_2}{S_1-S_2}\cdot e^{S_1\cdot t}+\frac{S_1}{S_2-S_1}\cdot e^{S_2\cdot t}\right) \quad (3)$$

Where, $S_{1,2}=\frac{\pm\sqrt{R_1^2-4\frac{L_1}{C_{ISS_1}}}-R_1}{2\cdot L_1}$.

According to equation (3), unbalanced gate driver loop (L_1) will result in different slew rate of gate driver voltage, which will eventually cause unsynchronized switching of paralleled transistors. Generally speaking, the delay time could be ~nS level if there is a 10 nH gate drive loop inductance difference for two paralleled HEMTs, which is not critical.

So, for PCB design, we always want to make the gate driver loops as symmetric and small as possible.

In this period, the extra-small parasitic capacitance of GaN HEMT will result in a small delay time and gate driver loss compared with Si transistors.

2) P2:di/dt Period

After either of the paralleled HEMTs reaches the threshold voltage, the impedance of 2DEG begins to decrease. As shown in Figure 5, in this period the HEMT operates in the saturation region. The 2DEG current is controlled by V_{GS} as (6).

$$i_D=g\cdot(v_{GS}-V_{th}) \quad (4)$$

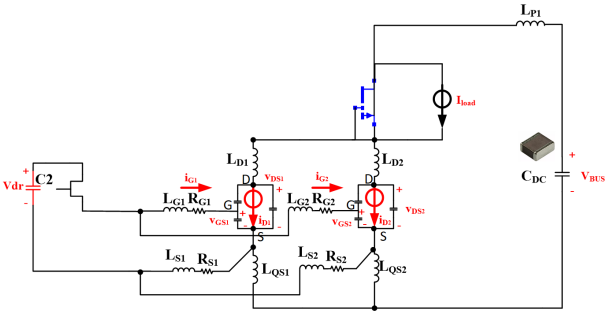


Figure.7. Equivalent Circuit during di/dt Period of Switching on Process

As v_{GS} increase, $\frac{di_D}{dt}$ will start to affect v_{GS} via mutual inductance and common source inductance between gate driver loop and power commutation loop as described in many previous works. To minimize this effect, the Kelvin terminal is usually employed in high-frequency applications to bypass the common source inductance.

However, though the paralleled transistors will share the same gate driver chip and employ Kelvin connections in the design, $\frac{di_D}{dt}$, as shown in Figure 6, could still potentially be problematic due to the existence of the quasi-common-source inductance (L_{QS_1} and L_{QS_2} as shown in Figure 7). The imbalanced quasi-common source inductance or di/dt will eventually cause a resultant feedback voltage across the v_{GS} as described in equation (5).

$$v_{QS_1}=\left(L_{QS_1}\cdot\frac{di_{D_1}}{dt}-L_{QS_2}\cdot\frac{di_{D_2}}{dt}\right)\cdot\frac{Z_{S2}}{Z_{S1}+Z_{S2}} \quad (5)$$

So, based on KCL and KVL, the circuit equations are expressed as (6) ~ (8).

$$C_{GD_1}\cdot\frac{dv_{GS_1}}{dt}+C_{GS_1}\cdot\frac{dv_{GS_1}}{dt}=\frac{1}{R_1}\left(V_{dr}-v_{GS_1}-v_{QS_1}-M_1\cdot\frac{di_{D_1}}{dt}-L_1\cdot\frac{di_{G_1}}{dt}\right) \quad (6)$$

$$v_{DS_1}=V_{BUS}-L_P\cdot\left(\frac{di_{D_1}}{dt}+\frac{di_{D_2}}{dt}\right)-M_1\cdot\frac{di_{G_1}}{dt}-\left(L_{D_1}+L_{QS_1}\right)\cdot\frac{di_{D_1}}{dt} \quad (7)$$

$$i_{G_1}=C_{ISS_1}\cdot\frac{dv_{GS_1}}{dt}+C_{RSS_1}\cdot\frac{dv_{GD_1}}{dt} \quad (8)$$

This period ends when i_{D_1} or i_{D_2} reaches I_{load}. The v_{GS_1} is derived as (9) assuming $\frac{di_{D_1}}{dt}=\frac{di_{D_2}}{dt}$.

$$v_{GS_1}=V_{dr}+(V_{dr}-V_{th_1})\cdot\left(\frac{s_2\cdot e^{s_1t}-s_1\cdot e^{s_2t}}{s_1-s_2}\right) \quad (9)$$

Where $s_{1,2}=\frac{\pm\sqrt{b^2-4a}-b}{2a}$, $a=R_1\cdot C_{GD_1}\cdot\left(L_D+M1+L_{QS_1}-L_{QS_2}\right)+C_{ISS_1}\cdot(M1+L_{QS_1}-L_{QS_2}+L_G)$, $b=1+L_{QS_1}-L_{QS_2}\cdot g+R_G\cdot C_{ISS}$.

The v_{DS1} and i_{DS1} could be derived according to (4), (7), (9).

According to equation (6)(9), the quasi-common source inductance (L_{QS_1}, L_{QS_2}) has the same effect as M_1 (mutual inductance and common source inductance between gate driver loop and power commutation loop). On one hand, the unbalanced quasi-common will help balance dynamic current distribution by lowering the transistor v_{GS} of higher transition speed. On the other hand, the feedback voltage might potentially cause overshoot or undamped ringing on v_{GS}.

So, for layout design, it is suggested to minimize and evenly distribute the quasi-common source inductance, which is so critical that an unsynchronized gate driver circuit is proposed to solve unbalanced quasi-common source inductance issue [5]. In this paper, a symmetric power loop and gate driver loop layout is proposed to achieve reliable switching.

3) P3:dv/dt Period

Because of the absence of body diode for high side HEMT, once i_D reaches i_{load}, the voltage across drain and source of low side transistor begin to build, and $C_{OSS}$of high side and low side begins to be discharged and charged through 2DEG of lower HEMTs exponentially as Figure 8.

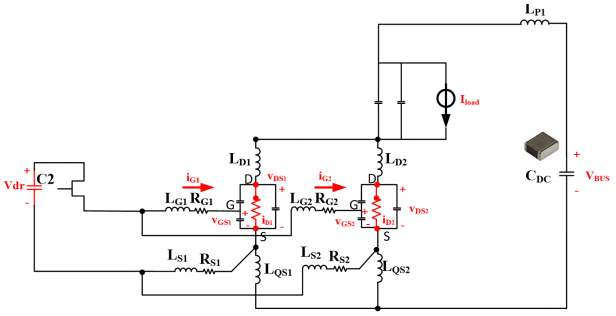


Figure. 8. Equivalent Circuit during dv/dt Period of Switching on Process

The impedance of 2DEG is controlled by the v_{GS} as (10). Assume $\frac{dv_{GS_1}}{dt} = 0$ during the miller plateau, so v_{GS_1} is a constant value($v_{GS_{1\_miller}}$) in this period.

$$R_{2DEG} = \frac{v_{DS}}{g\cdot(v_{GS}-V_{th})} \tag{10}$$

This period ends when v_{ds} reaches zero. The circuit equation could be expressed as (11) ~ (12).

$$C_{GD_1}\cdot\frac{dv_{DS_1}}{dt} = \frac{1}{R_1}\left(V_{dr} - v_{GS_1} - v_{QS_1} - M_1\cdot\frac{di_{D_1}}{dt} - L_1\cdot C_{GD_1}\cdot\frac{d^2v_{DS_1}}{dt^2}\right) \tag{11}$$

$$\left(I_{load} + C_{OSS_{total}}\cdot\frac{dv_{DS}}{d_t}\right)\cdot R_{2DEG} + L_{LOOP}\cdot C_{OSS_{total}}\cdot\frac{d^2v_{DS}}{{d_t}^2} = V_{BUS} \tag{12}$$

Where, $L_{LOOP} = L_{P1} + (L_{D1} + L_{QS_1})//(L_{D2} + L_{QS_2})$, $C_{oss_{total}}$ is the total output capacitance of both high side and lower side transistors, R_{2DEG} is the 2DEG resistance of low side transistors.

The $v_{DS_1}$and v_{GS_1} of low side HEMT could be derived as (13) and (14).

$$v_{DS_1} = V_{BUS}\cdot\left(1 - \frac{S_2}{S_2-S_1}\cdot e^{S_1\cdot t} + \frac{S_1}{S_2-S_1}\cdot e^{S_2\cdot t}\right) \tag{13}$$

Where, $S_{1,2} = \frac{\pm\sqrt{R_{2DEG}^2 - 4\frac{L_{LOOP}}{C_{OSS_{total}}}} - R_{2DEG}}{2\cdot L_{LOOP}}$.

$$v_{GS_{1\_miller}} = \frac{1}{R_1}\left(V_{dr} - R_1\cdot C_{GD_1}\cdot\frac{dv_{DS_1}}{dt} - v_{QS_1} - M_1\cdot C_{GD_1}\cdot\frac{d^2v_{DS_1}}{dt^2} - L_1\cdot C_{GD_1}\cdot\frac{d^2v_{DS_1}}{dt^2}\right) \tag{14}$$

Where, $v_{QS_1} = \left(L_{QS_1}\cdot\frac{di_{D_1}}{dt} - L_{QS_2}\cdot\frac{di_{D_2}}{dt}\right)\cdot\frac{Z_{S2}}{Z_{S1}+Z_{S2}}$, $R_1 = R_{G1} + R_{S1}$, $L_1 = L_{G1} + R_{S1}$.

According to (10) and (13), the miller plateau voltage ($v_{GS_{1\_miller}}$) determines R_{2DEG} so as to control the slew rate of the exponential drain and source voltage. According to (14) the larger the gate resistance, the lower $v_{GS_{1\_miller}}$ will drop, which will result in a higher overlapping loss. Increasing the gate driver voltage also could be a potentially solution to reduce the switching loss as long as v_{GS} does not exceed the maximum V_{GS} of transistors.

Current spike on the low side transistor happens in this period, and the total charge is $C_{OSS_{total}}\cdot V_{BUS}$. Further analysis will be detailed in next section.

4) P4: Remaining Period

In this period, both v_{DS} and i_D have finished transition, there might be some undamped ringing remaining in the circuit. The gate driver capacitor will continue to charge the C_{ISS} to the rated driving voltage. Very similar to the delay period, v_{GS_1} is derived as (15).

$$v_{GS_1} = \left(V_{dr} - v_{GS_{1miller}}\right)\cdot\left(\frac{S_2}{S_1-S_2}\cdot e^{S_1\cdot t} + \frac{S_1}{S_2-S_1}\cdot e^{S_2\cdot t}\right) + V_{dr} \tag{15}$$

Where, $S_{1,2} = \frac{\pm\sqrt{R_1^2 - 4\frac{L_1}{C_{ISS_1}}} - R_1}{2\cdot L_1}$.

So, when $R_1 < 2\cdot\sqrt{\frac{L_1}{C_{ISS_1}}}$, there will be voltage over shoot on v_{GS}, which might cause device failure.

Compared with Si MOSFET, the gate of E-mode GaN HEMT is more fragile as most E-HEMT could undertake ~5V maximum voltage for v_{GS}.

Generation II E-HEMT from GaN Systems have the most robust gate which could undertake 10V maximum v_{GS}. In order to prevent potential gate failure, -3 V/ +6 V v_{GS} is suggested for GaN Systems' generation II E-HEMTs. Most of existing Si MOSFET/IGBT gate driver chip could be applied.

B. Switching-off Process

The state of GaN HEMT as well as the waveform of v_{DS}, i_D during switching off is shown in Figure 9. The switching off process could be also divided into three periods to ease the analysis, P1-delay period, P2-dv/dt period, P3-di/dt period.

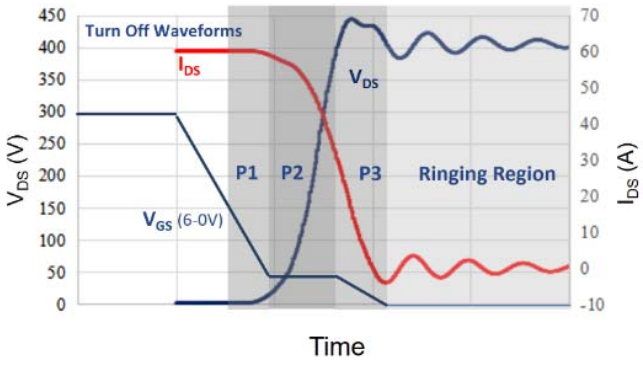


Figure.9.a Vds, Ids Waveform During Switching on

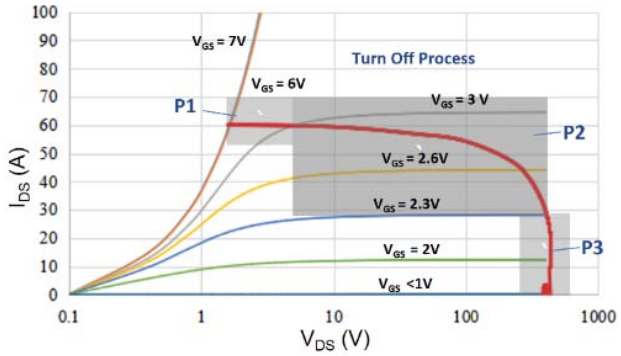


Figure. 9.b State of GaN HEMT During Switching off

1) P1:Delay Period

Very similar to the delay period of Switching-on process, after driver output starts to actively pull down, the C_{ISSS} begins to be discharged exponentially through the lower switch of totem pole circuit.

The 2DEG on-resistance is increasing as the decrease of gate-source voltage as shown in Figure 9. The drain-source voltage and drain current does not change in this period. Also, the paralleled transistors will not affect each other in this periods.

v_{GS_1} is expressed as (16).

$$v_{GS_1} = -V_{neg} + (V_{dr} + V_{neg}) \cdot \left(\frac{S_2}{S_2 - S_1} \cdot e^{S_1 \cdot t} + \frac{-S_1}{S_2 - S_1} \cdot e^{S_2 \cdot t}\right) \quad (16)$$

Where, $S_{1,2} = \frac{\pm\sqrt{R_1^2 - 4\frac{L_1}{C_{ISS_1}}} - R_1}{2 \cdot L_1}$, V_{neg} is the absolute value of the switching off voltage of gate driver circuit.

This period ends when $v_{GS_1} < V_{th} + \frac{I_{load}}{g}$

2) P2:dv/dt Period

In this period, as the increase of 2DEG impedance, part of the load current (I_{load}) begins to charge and discharge high side and low side output capacitance ($C_{OSS_{total}}$).

The v_{DS_1} and v_{GS_1} (a miller voltage plateau $v_{GS_{1miller}}$,is usually observed) of low side HEMT could be derived, as (17) and (18).

$$v_{DS_1} = V_{BUS} \cdot \left(1 - e^{\frac{-t}{R_{2DEG} \cdot C_{OSS_{total}}}}\right) \quad (17)$$

$$v_{GS_{1\_miller}} = \frac{1}{R_1}\left(-V_{neg} + R_1 \cdot C_{GD_1} \cdot \frac{dv_{DS_1}}{dt} + v_{QS_1} + M_1 \cdot C_{GD_1} \cdot \frac{d^2 v_{DS_1}}{dt^2} + L_1 \cdot C_{GD_1} \cdot \frac{d^2 v_{DS_1}}{dt^2}\right) \quad (18)$$

Where, $v_{QS_1} = \left(L_{QS_1} \cdot \frac{di_{D_1}}{dt} - L_{QS_2} \cdot \frac{di_{D_2}}{dt}\right) \cdot \frac{Z_{S2}}{Z_{S1}+Z_{S2}}$, $R_1 = R_{G1} + R_{S1}$, $L_1 = L_{G1} + R_{S1}$.

According to (17) and (18), the miller plateau voltage ($v_{GS_{1\_miller}}$) determines the slew rate of the exponential drain and source voltage. The larger the gate resistance, the higher $v_{GS_{1\_miller}}$ will go, which will result in a higher overlapping loss. Increasing the negative switching off voltage also could be a potential solution to reduce the switching loss. When the miller plateau voltage is lower than the threshold voltage, all the load current will charge the output capacitance, and the switching-off loss is minimum (close to zero).

This period ends, when the drain-source voltage reaches the bus voltage.

3) P3:di/dt Period

After the phase voltage is higher than the bus voltage, the high side transistor begins to freewheeling. The low side 2DEG will be completely depleted in this period. This period ends when i_{D_1}or i_{D_2}reaches I_{load}. The v_{GS_1}, i_{D_1},and v_{DS_1} is derived as (19), (20) and (21) assuming $\frac{di_{D_1}}{dt} = \frac{di_{D_2}}{dt}$.

$$v_{GS_1} = -V_{neg} - (-V_{neg} - v_{GS_{1miller}}) \cdot \left(\frac{s_2 \cdot e^{s_1 t} - s_1 \cdot e^{s_2 t}}{s_1 - s_2}\right) \quad (19)$$

$$i_{D1} = g \cdot \left(-V_{neg} - (-V_{neg} - v_{GS_{1miller}}) \cdot \frac{s_2 \cdot e^{s_1 t} - s_1 \cdot e^{s_2 t}}{s_1 - s_2}\right) - V_{th_1}) \quad (20)$$

$$v_{DS_1} = V_{BUS} - L_P \cdot \left(\frac{di_{D_1}}{dt} + \frac{di_{D_2}}{dt}\right) - M_1 \cdot \frac{di_{G_1}}{dt} - (L_{D_1} + L_{QS_1}) \cdot \frac{di_{D_1}}{dt} \quad (21)$$

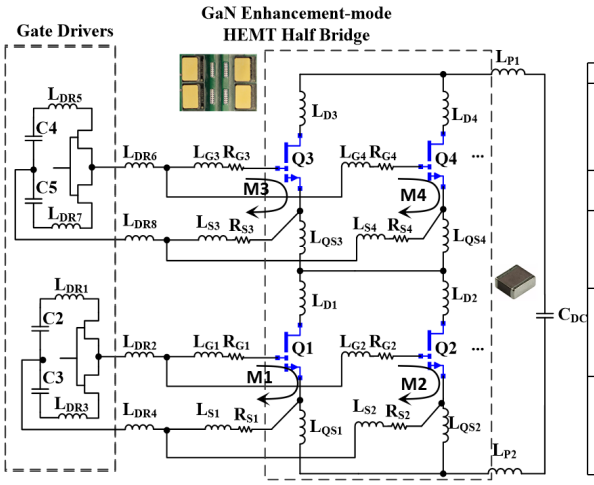
Where $s_{1,2} = \frac{\pm\sqrt{b^2 - 4a} - b}{2a}$, $a = R_1 \cdot C_{GD} \cdot \left(L_D + M_1 + L_{QS_1} - L_{QS_2}\right) + C_{iss} \cdot (M_1 + L_{QS_1} - L_{QS_2} + L_G)$, $b = 1 + L_{QS_1} - L_{QS_2} \cdot g + R_G \cdot C_{ISS}$.

Voltage overshoot over $v_{DS}$of lower side transistors will happen in this period.

After both v_{DS} and i_{DS} have finished transition, there might be some undamped ringing remaining in the circuit.

C. Conclusion

The effects and design rules of various parasitics existing in the gate drive loop and power loop, can be concluded as shown in Figure 10.



Effects of Parasitics

Parameter	Description	Effect	Priority	Design Rules
L_{P1},L_{P2} L_{D1-4}	Commutation Loop Inductance	Increase Vds spike during P3 of Switching off	High	Smaller the better
L_{DR1}-L_{DR8}	Gate drive loop inductance	Increase Vgs ringing and overshoot	Medium	Smaller the better
L_{G1}-L_{G4} L_{S1}-L_{S4}		1. Increase Vgs ringing and overshoot, 2. susceptible to gate oscillation if very unbalanced	Medium	Smaller the better, as equal as possible for paralleled devices
M1-4	Mutual Inductance between power loop and gate loop	1.Feedback di/dt to Vgs, 2. Slowdown switching 3. potentially cause gate oscillation	Extremely High	
L_{QS1-6}	Quasi-common source inductance	1. Feedback the difference of di/dt to Vgs, 2. Balance current sharing 3. Potentially cause gate oscillation	Extremely High	

Figure. 10. Effects and Design Rules of Parasitic Parameters

III. Design Consideration of 240 A / 650 V E-mode GaN HEMT Based Power Stage

A. Parasitic Inducatance

As described in last section, the short rising and falling time during commutation will result in a high di/dt, which will cause a voltage across stray loop inductance in the power loop. Because of the extremely small C_{ISS} of GaN HEMT, a >5 Ohm gate resistors sometimes have to be applied slowing down transition in order to eliminate the voltage spike on the drain and source voltage during switching off, which will definitely increase the switching loss.

Reducing commutation loop inductance to ~sub-nH level, is probably the best solution to get rid of voltage spike on Vds without compromising on the switching speed. Significant effort in power module design has been previously aimed at reducing the commutation loop inductance and reducing the drain-source overshoot, [6] [10] [11].

The parasitic inductance is a function of the magnetic flux generated by current as (22).

$$L = \frac{\Psi}{I} = \frac{\int \dot{B} * d\dot{S}}{I} \tag{22}$$

According to the law of electromagnetic induction, with the multi-layer magnetic-flux-canceling design strategy, the parasitics of the trace could be greatly reduced – the direction of the commutation current on two adjacent layers are opposite so that the generated flux outside the loop are canceling each other.

Compared to Direct Bonded Copper (DBC) substrate, the PCB could easily adopt the multi-layer structure and smaller distance between layers to achieve a better magnetic flux canceling effect.

A half bridge power stage consisting of four high-side and four low-side GaN HEMTs in parallel rated at 240A/650V has been designed as shown in Figure 11.

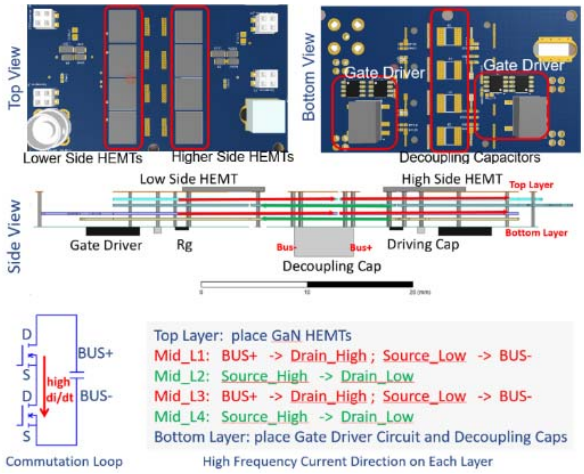


Figure. 11. Layout of 240A/650V GaN HEMTs based Half Bridge

On the other hand, the GaNPX™ packaging of GaN Systems with no leads or bonding wires as shown in Figure 12 also tremendously merits the design. Compared with traditional TO-247 package, the stray inductance is reduced by >80%.

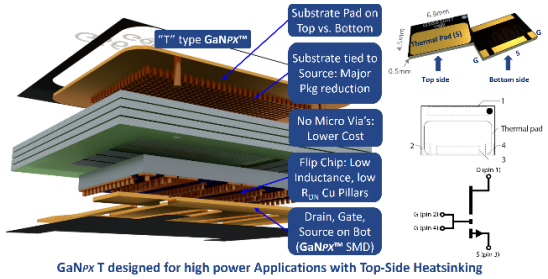


Figure. 12. GaNpxTM packaging

The half bridge with four GaN HEMTs in parallel is modeled in Ansys Q3D, and the power loop and gate-driver loop inductance are evaluated by Finite Element Analysis,. The commutation loop inductance of the proposed design is only 0.7 nH, 1/4 of the best E-mode GaN HEMT based power module [9]. For each paralleled GaN HEMT, quasi-common source inductance is <0.2 nH, and gate drive loop inductance is 4.2 nH.

B. *Parasitic Capacitance*

Parasitic capacitance is another design consideration as depicted in Section II. During switch-on process, C_{oss} as well as the reverse recovery charge (as seen in Si/SiC MOSFETs) will increase the current spike and switching loss. Generally speaking, in hard switching application, the more transistors we parallel, the higher switching loss we will have. So, there will be an optimum number of paralleled HEMTs to reach the highest efficiency for a certain application.

In Zero Voltage Switching application, during the dead time, the reactive energy stored on magnetic components begins to discharge and charge the parasitic capacitance.

To secure ZVS, the reactive power has to be higher than the stored energy in the parasitic capacitance of GaN HEMTs and PCB board and the dead time loss of GaN HEMTs. On the other hand, in order to increase the efficiency of system, the reactive power needs to be controlled as close to the required energy as possible, which will require a precise modelling of parasitic capacitance.

The output capacitance of GaN HEMT (GS66516T) at different voltage is measured by curve tracer. According to (23), the equivalent parasitic output capacitance of single GaN HEMT at 400V could be derived as 0.28 nF.

$$C_{oss_{eq}} = \frac{\int_0^{400V} Coss(V_{ds}) \cdot dV_{ds}}{V_{ds}} \qquad (23)$$

Parasitic capacitance of PCB and magnetic components is not ignorable compared with the ultra-small C_{oss} of GaN HEMT. The parasitic capacitance in a half bridge module is extracted by ANSYS Q3D as Figure 13, indicating the parasitic capacitance in one leg is 0.6 nF (0.4 nF to BUS+ and 0.2 nF to BUS- node). And measured by Impedance Analyzer, inter-winding capacitance of transformer is less than 50 pF.

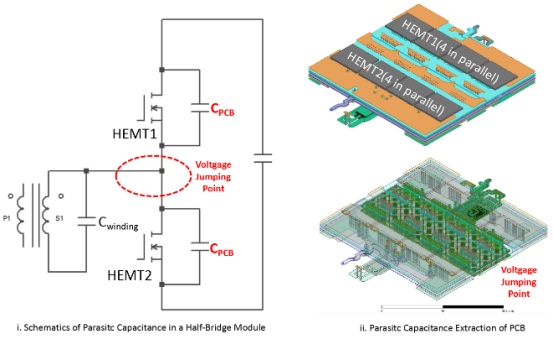


Figure. 13. Parasitic Capacitance Extraction in Q3D

So, the total parasitic capacitance of the half-bridge power stage is 3.2 nF (1.73 nF to BUS+ node, 1.48 nF to BUS- node).

As the equivalent circuit of double pulse test circuit and switching waveform shown in Figure 14, the current spike measured during the hard switching on process in the lower switches is contributed by the displacement charge current of the parasitic capacitance between voltage jumping point and BUS+ node.

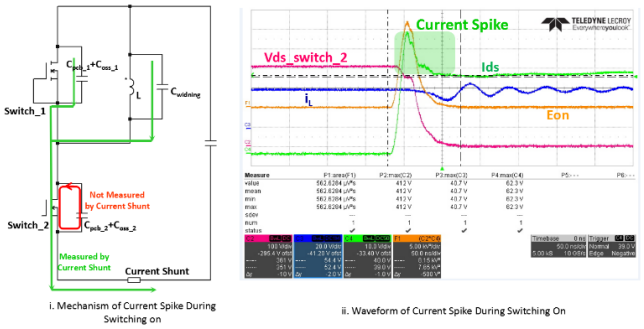


Figure. 14. Current Spike Measurement with Double Pulse Test Platform

The displacement charge form high side transistors and parasitics were measured as shown in Figure 15. The measured equivalent capacitance is about 2 nF. The error between measurement and estimation is about 13.5%, which is reasonable considering the measurement and simulation accuracy.

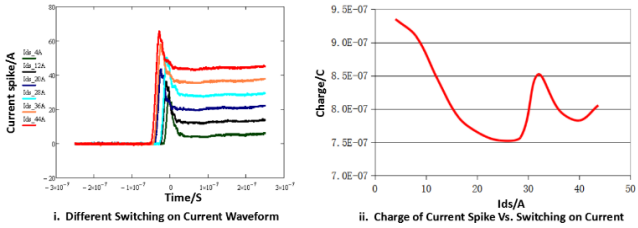


Figure. 15. C_{oss} Charge @ Different Load Current

IV. Experimental Verification

A half bridge power stage consisting of four high-side and four low-side GaN HEMTs in parallel rated at 240 A / 650 V has been prototyped as shown in Figure 16 and has been experimentally verified by double pulse test.

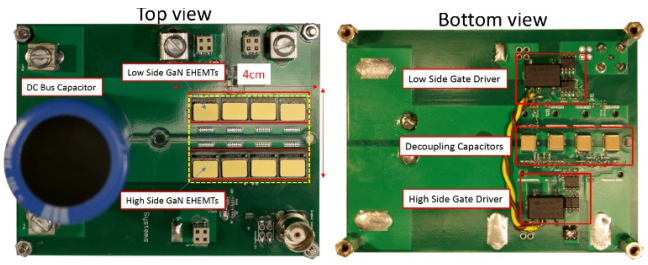


Figure. 16. Prototype of 240A/650V GaN HEMTs based Half Bridge

As shown in Figure 17, reliable hard switching on and off are realized at the rated power, 240 A/400 V with clean

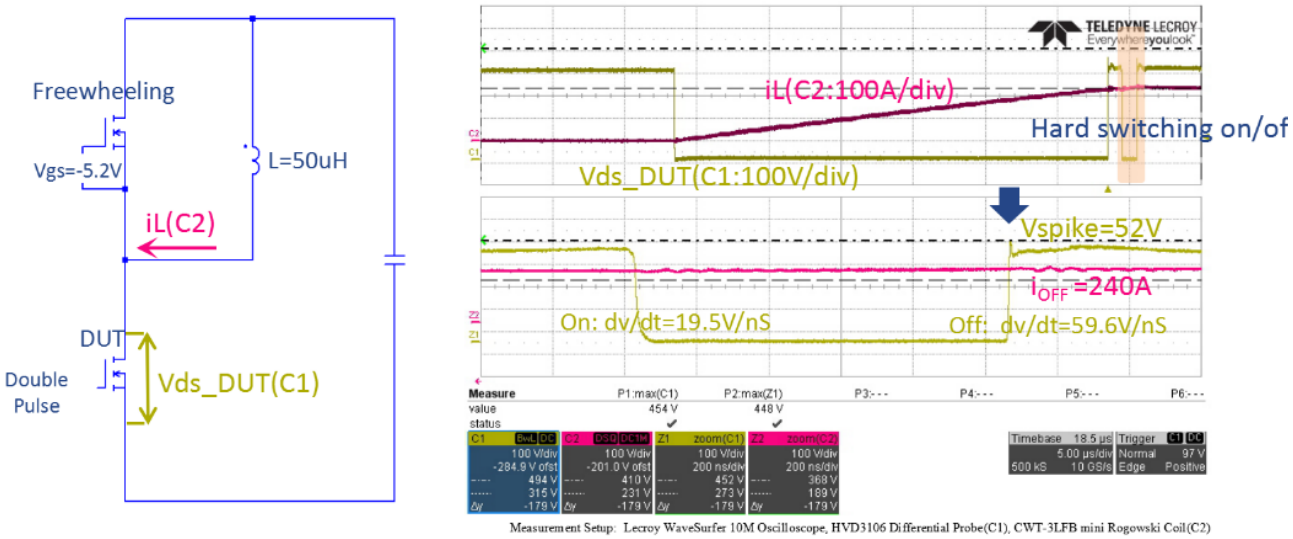


Figure. 17. Double Pulse Test Waveform @240 A/400 V

transition waveforms, while the spike on Vds during switching off is only 52 V even with close to 60 V/ns turn-off speed, which shows the benefit of low power loop inductance.

V. Conclusion

An analytic model of paralleled GaN HEMTs is built to understand the effects of parasitics. And the design rules for gate driver circuit and layout that effects the parallel operation are detailed.

A half bridge power stage consisting of four high-side and four low-side GaN HEMTs in parallel, rated at 240 A/400 V, has been prototyped and experimentally verified by double pulse test.

The paralleling techniques in this paper can be scaled up to 100 kW with proper packaging considerations including thermal management and module assembly.

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