A study on parasitic inductance reduction design in GaN-based power converter for high-frequency switching operation

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***Abstract*— This report studies the influence of printed circuit board (PCB) design on voltage overshoot and ringing oscillation in switching operation of gallium nitride gate injection transistor (GaN-GIT) for high-frequency DC-DC converter. The parasitic inductances in the main power loop have been identified based on moment of method (MoM) analysis and frequency characteristics of impedance measured with 2-port shunt-thru method. The measured switching characteristics of GaN-GIT in a 5 MHz DC-DC boost converter shows that a small-ESL ceramic capacitor connected across the DC-link can reduce the effective power loop inductances and can improve both voltage overshoot and the damping of ringing oscillation.**

Index Terms*—; GaN gate injection transistor; parasitic inductnce; dynamic characteristics; DC-DC converter

I. INTRODUCTION

The gallium nitride (GaN) power semiconductor devices are expected to achieve high-frequency switching operations and high-power density of power converters [1 – 3]. However, fast switching operation of power transistors also induce voltage overshoot and parasitic ringing oscillation during hard-switching transient [4 – 6]. This report studies the identification of parasitic inductances for three-types wiring layout of printed circuit board (PCB) using electromagnetic (EM) analysis and impedance measurement with 2-port shunt-thru method. This report also investigates the influence of PCB design on the switching characteristics of commercially-available GaN gate injection transistor (GIT) [7] in a tested 100 W DC-DC boost converter operating at a megahertz switching frequency.

II. STATIC CHARACTERISTICS OF GAN POWER TRANSISTOR

Fig. 1 (a) shows the transfer characteristics of studied GaN-GIT (Panasonic PGA26E19BA, 600V, 10A) and conventional Si super junction MOSFET with surface mount discrete (SMD) package (Infineon IPL60R199CP, 650V, 10A) at room temperature (25 °C) measured by a curve tracer (Agilent, B1505A). GaN-GIT has dual-flat no-leads (DFN) 8x8 package. The GIT has a p-type AlGaN layer over AlGaN/Gan hetero junction. The channel under the gate is depleted at the zero gate bias, i.e., GIT shows normally-off characteristics [7]. The GIT shows relatively lower gate threshold voltage (approximately 1.2 V) than Si SJMOSFET, as shown in Fig. 1 (a). Therefore, negative gate to source voltage is applied in the off-state to avoid its self-turn on operation [8]. Fig. 1 (b) depicts the conduction

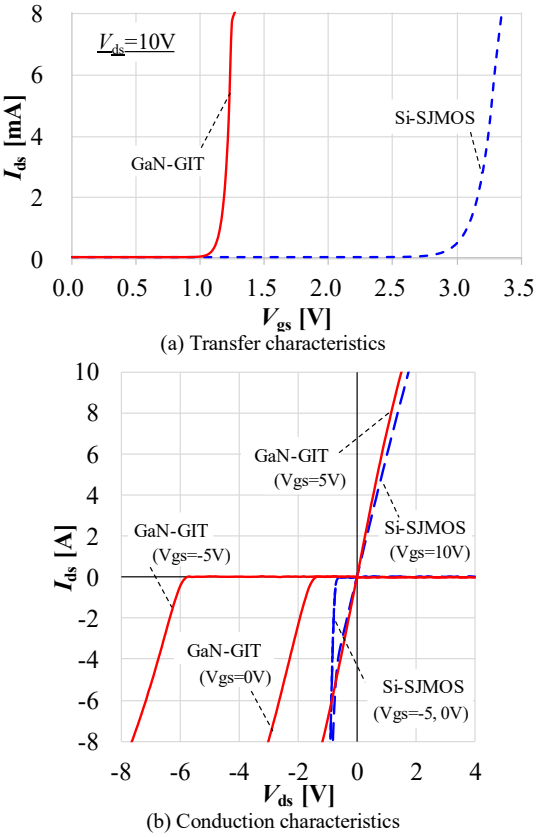

Figure 1. Static I-V characteristics of transistors.

characteristics. The forward characteristics of GaN-GIT is almost the same with Si-SJMOSFET. GaN-GIT can conduct in both direction; however, a negative gate voltage increases the voltage drop. This suggests that the reverse conduction time in body diode mode (e.g. during dead time in half bridge configuration) has to be as short as possible to avoid the large conduction losses.

Fig. 2 shows the C-V characteristics of the studied transistors at room temperature. GaN-GIT exhibits relatively small input capacitance C_{iss}. Small C_{iss} enables fast switching operation of transistor. The output capacitance C_{oss} determines the frequency of the ringing oscillation in transient voltage and current, which is due to the resonance with the power loop parasitic inductances.

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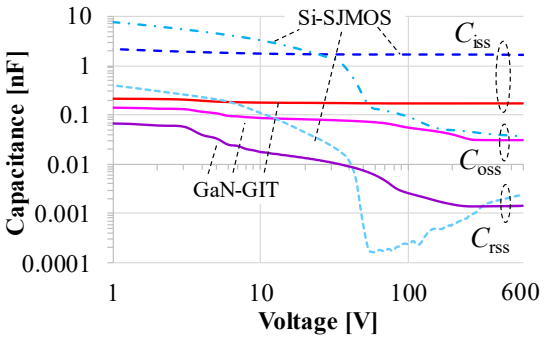


Figure 2. C-V characteristics of transistors (OSC=100 mV, 1 MHz).

III. IDENTIFICATION OF PARASITIC INDUCTANCES ON PCB WIRING PATTERN

This section studies the identification of parasitic inductances on PCB wiring pattern by using EM analysis and impedance measurement with 2-port shunt-thru method. Fig. 3 shows the tested three-types PCB design of the GaN-GIT-based DC-DC converter. The power loop is the path from the DC-link smoothing capacitor C through the high-side and low-side transistor, $Q1$ and $Q2$, and back to the capacitor, as shown in Fig. 3. The layout "Type I" uses only single layer copper foil for power loop. The area size of power loop is determined by the body of smoothing film capacitor. The SMD ceramic capacitor was used as smoothing capacitor for the layout "Type II-A". Four capacitors were connected in parallel for decreasing the parasitic inductances of the smoothing capacitor. The return path of power loop in this design is located directly underneath the top layer power loop path. The layout "Type II-B" has the same size PCB with type II-A and also has the same double layer power loop structure. The low-side transistor $Q2$ for type II-B was mounted in a back side. An additional snubber ceramic capacitor C_{sn} placed in close to the high-side transistor $Q1$ to minimize the physical loop size.

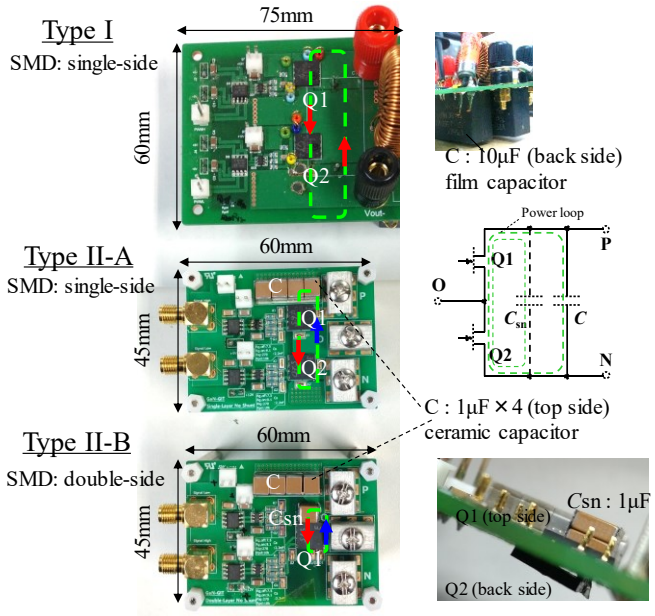
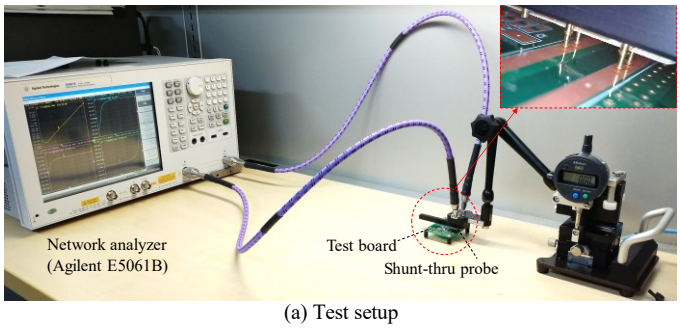
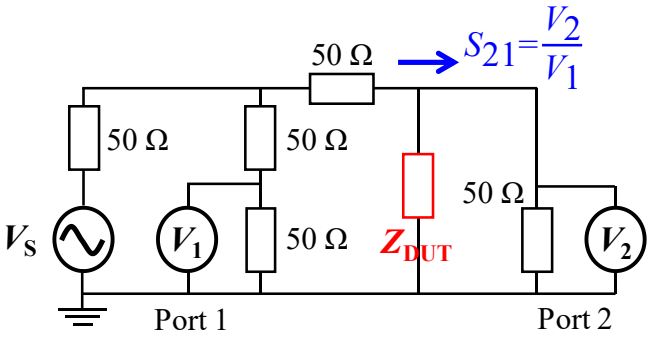


Figure 3. Studied three-types PCB design.



(a) Test setup



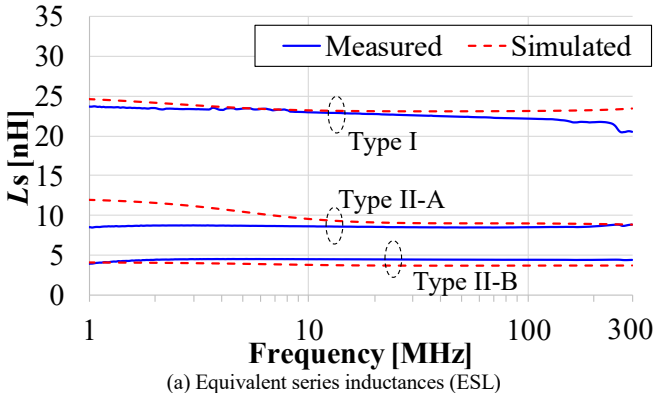
(b) Equivalent circuit

Figure 4. Test setup for power loop inductances measurement by shunt-thru method.

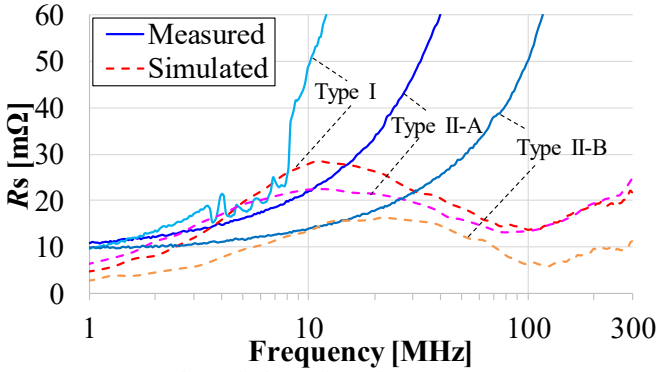
Fig. 4 (a) shows the test setup for loop inductances measurement by 2-port S_{21} shunt-thru method. This configuration can measure a low-impedance (milliohm order) of device under test (DUT). The equivalent circuit of the vector network analyzer ports connected to the DUT is shown in Fig. 4 (b). Port 1 drives the current through the DUT. This current creates a small voltage across the low impedance DUT, and it is measured at port 2. The analyzer calculates the gain from Port 1 to Port 2, i.e., $S_{21}=V_2/V_1$. The impedance of DUT Z_{DUT} can be expressed as [9]

$$Z_{DUT} = \frac{25S_{21}}{1-S_{21}} \quad (1).$$

The parasitic inductances of each power loop can also be calculated by EM analysis. This study used Keysight Momentum EM simulator that is based on the Method of Moments (MoM) technology for calculating S-parameter of planar conductors. The measured and simulated frequency characteristics of equivalent series inductances (ESL) and equivalent series resistances (ESR) for short circuit condition of power loop are shown in Fig. 5. The dielectric substrate (FR-4) thickness was 1.6mm, and its copper foil thickness was 35 μm. The wiring layout type II-A and II-B have much less loop inductance than type I . The identified power loop ESL and ESR for type II-B wiring layout is the path from the additional snubber capacitor C_{sn} through the $Q1$ and $Q2$, and back to the C_{sn}, and it yields the smallest loop inductance. The frequency characteristics of ESL measured by shunt-thru method are almost identical to the simulation results of MoM in the entire intended frequency range. However, the measured and simulated frequency characteristics of ESR do not correspond, especially in higher than 10 MHz. Further study is needed to realize accurate EM modeling for evaluating very small resistance.



(a) Equivalent series inductances (ESL)



(b) Equivalent series resistance (ESR)

Figure 5. Frequency characteristics of ESL and ESR of power loop for studied three-types PCB wiring layout.

IV. Influence of Parasitic Inductances on Dynamic Characteristics of GaN Power Transistor

This section presents the measured switching characteristics of GaN-GIT in a tested DC-DC boost converter to investigate the influence of power loop parasitic inductances on dynamic characteristics of transistor. Fig. 6 depicts the circuit diagram of the tested converter. The GaN-GIT of $Q2$ was operated at 1 MHz and 5 MHz switching frequency with 45% duty cycle for 100 V DC output voltage and 94 Ω resistive load. The gate and source of $Q1$ was shorted and it used as a free-wheeling diode.

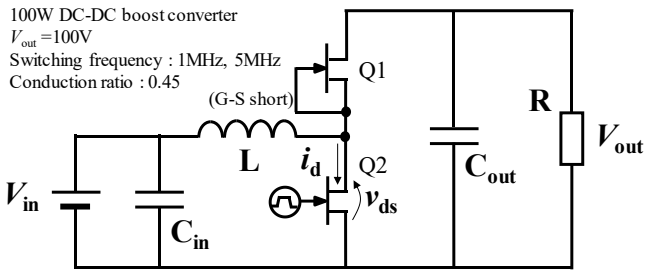


Figure 6. A tested DC-DC boost converter configuration.

Fig. 7 shows the measurd time responce of $Q2$ voltage and current at 1 MHz switching frequency for type I PCB design. The digital oscilloscope (Keysight, DSOS104A) were used for measurement. The drain to source voltage v_{ds} was measured by a 300 MHz high-voltage differential probe (Keysight, N2804A). The drain current i_d was measured by a 10 mΩ coaxial current shunt (T&M Research Products Inc., SDN-414-01) and its voltage drop was captured with a power rail probe (Keysight,

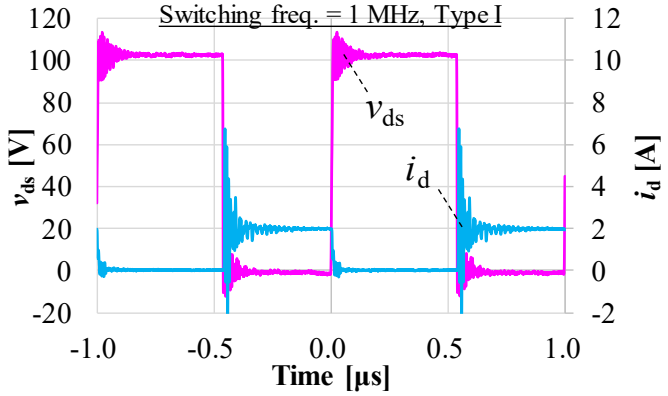
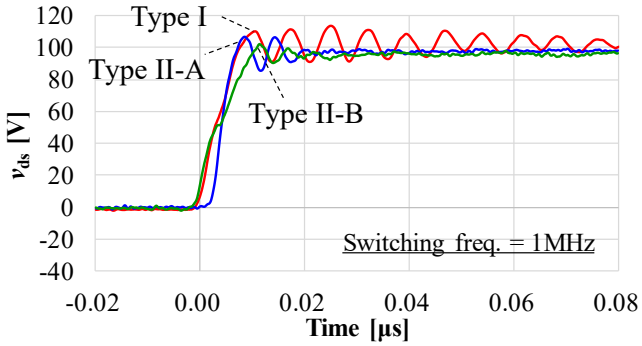
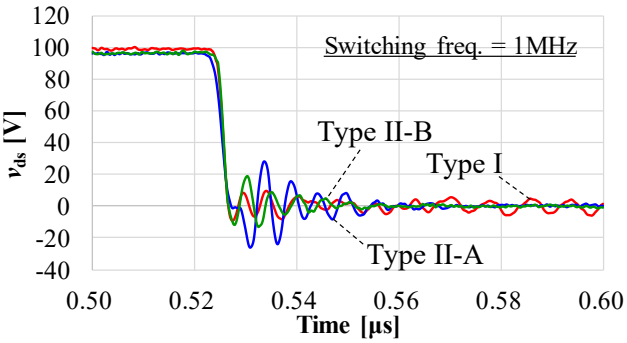


Figure 7. Time response of $Q2$ voltage and current. (Switching frequency = 1 MHz, PCB design : Type I)



(a) $Q2$ turn off operation



(b) $Q2$ turn on operation

Figure 8. Switching characteristics of $Q2$ voltage (Switching freqency = 1 MHz).

N7020A). The turn off voltage of $Q2$ shows overshoot, which are caused by interaction with high di/dt and power loop inductances. The transient voltage and current show ringing oscillation. These are caused by the resonance with output capacitance of the $Q2$ and parasitic inductances of power loop. An inductor current commutates from $Q1$ to $Q2$ and $Q1$ induces reverse current when $Q2$ turns on. It results in large turn on current peak of $Q2$.

Fig. 8 depicts the measured switching characteristics of $Q2$ voltage for studied three-types wiring layout of PCB. The switching frequency was 1 MHz. Fig. 9 shows the time response of $Q2$ voltage at 5 MHz switching operation. The small power loop inductances of type II-A and II-B layouts improve both voltage overshoot and the attenuation of ringing oscillation than for using type I wiring layout in turn on and off operation.

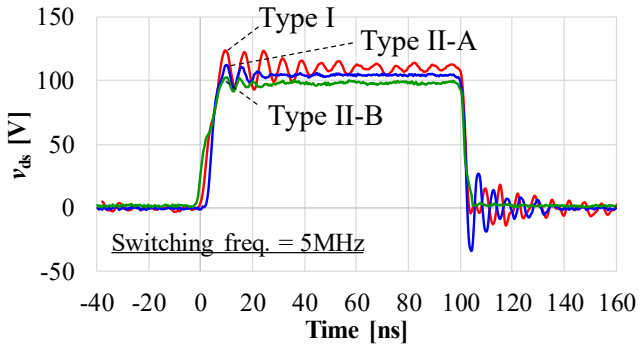


Figure 9. Time response of $Q2$ voltage at 5 MHz switching operation.

This study applies Prony analysis to model dynamic characteristics of voltage in turn on and turn off operation for $Q2$, shown in Fig. 8. Prony analysis identifies the mathematical model of a dynamical system with the sampled time domain data as a linear superposition of multiple oscillation modes. The damping, frequency, magnitude, and initial phase information of the respective modes are estimated directly [10].

Assuming the N data samples k=0,1,2,⋯, N-1 (sampling period Δt), the investigated signal can be approximated by n exponential functions, which are expressed by initial value B_i and eigenvalue λ_i.

$$y(k) = \sum_{i=1}^{n} B_i \, (e^{\lambda_i \Delta t})^k \tag{2}$$

$$B_i = A_i e^{j\theta_i} \tag{3}$$

$$\lambda_i = \alpha_i + j(2\pi f_i) \tag{4},$$

where α_i is damping factor, f_i is frequency, A_i is amplitude, and θ_i denotes initial phase for i^{th} mode.

Table I shows the extracted damping factor and oscillation frequency of dominant ringing oscillation mode in $Q2$ transient voltage. The parasitic inductances L_{loop} of power loop is estimated from the oscillation frequency f and the output capacitance of off-state GaN-GIT C_{oss} as

$$L_{\text{loop}} = \frac{1}{4\pi^2 f^2 C_{\text{oss}}} \tag{5}.$$

The loop inductances are calculated by using (5) as 26.5 nH, 12.6 nH, and 11.7 nH for type I, II-A, and II-B, respectively. The identified f shown in Table I (a) and measured C_{oss} = 56.6 pF at 100 V bias voltage (depicted in Fig. 2.) were used in these calculation. The differences between type I and II-A almost correspond with the identified power loop inductances shown in Fig. 5 (a). The results shown in Table I also indicate the smaller power loop inductances have effect on the faster damping of ringing oscillation. The oscillation frequency which is extracted by Prony analysis and calculated loop inductances for type II-B show little difference from that of type II-A. This result suggests that the partial inductances of a half-bridge leg for type II-B is smaller than for type II-A due to the smaller physical loop. However, there is almost no difference between the impedance of an output smoothing capacitor C_{out} and an additional snubber capacitor C_{sn} in higher-frequency range, i.e. C_{sn} in this experiment has little effect for bypassing the high-frequency component. The optimization of C_{out} and C_{sn} remain to be future task.

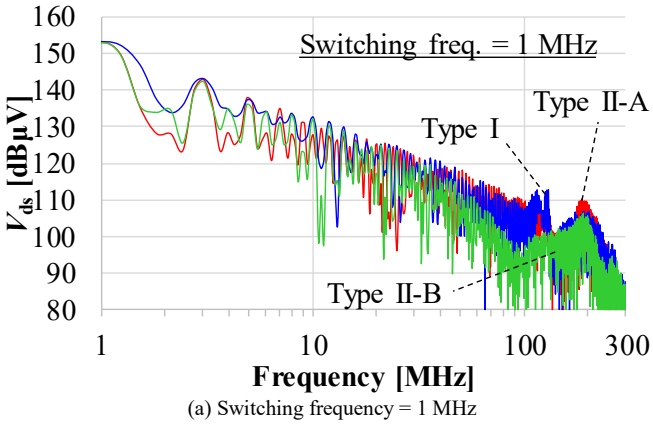
TABLE I. EVALUATION OF THE DYNAMIC CHARACTER OF GAN-GIT BY PRONY ANALYSIS (SWITCHING FREQUENCY = 1 MHZ)

(a) turn on voltage

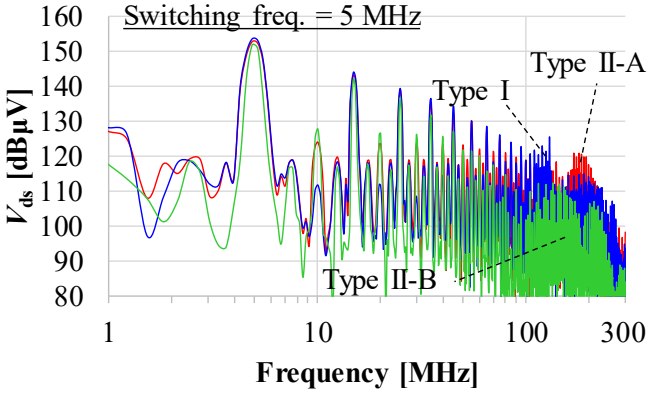
Board type	Damping factor α [1/sec.]	Oscillation frequency f [MHz]
Type I	4.527×10^7	129.0
Type II-A	8.523×10^7	186.1
Type II-B	1.022×10^8	196.5

(b) turn off voltage

Board type	Damping factor α [1/sec.]	Oscillation frequency f [MHz]
Type I	3.013×10^7	120.3
Type II-A	1.088×10^8	187.4
Type II-B	1.943×10^8	190.6



(a) Switching frequency = 1 MHz



(b) Switching frequency = 5 MHz

Figure 10. Frequency spectrum of GaN-GIT ($Q2$) voltage.

Fig. 10 shows the frequency spectrum of $Q2$ voltage for 1 – 300 MHz. The spectrum peaks correspond with the theoretical harmonic components of the integral multiple of the switching frequency up to tens of megahertz. The relatively high level spectrum peak exhibits around 120 – 130 MHz for type I layout, which stems from the ringing oscillation in the transient response. The smaller power loop inductances of type II-A and II-B wiring layout results in a shift of the spectrum peak towards higher frequency (around 200 MHz) and 5 – 10 dB lower peak level than for type I. These differences agree with the results of the damping and the ringing oscillation frequency extracted by Prony analysis. Thus, it is clear that the wiring layout of PCB has significant influence on parasitic inductances and it affects the overshoot voltage level and ringing oscillation character.

V. CONCLUSION

This report studies the PCB design for reducing power loop parasitic inductances of GaN power device-based power converter to realize high-frequency switching operation. The parasitic inductances in the main power loop identified by EM simulation analysis and frequency characteristics of impedance measured with 2-port shunt-thru method. The measured and simulated frequency characteristics of ESL are almost identical, and these two methods are validated. This report also experimentally evaluated the influence of power loop inductances on dynamic characteristics of GaN-GIT in a MHz switching operation 100 W DC-DC converter. It is confirmed that the small-ESL capacitor connected across the DC-link can reduce the power loop inductances effectively and can improve both voltage overshoot and the damping of ringing oscillation. Future work will evaluate the parasitic inductances in gate drive circuit and its influence on dynamic characteristics of gate to source voltage. Further study is also needed to optimize design for passive component to achieve high frequency switching operation, high power density, and low EMI noise level of GaN-based power converter.

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