Extraction of Parasitic Inductances of SiC MOSFET Power Modules Based on Two-Port S-Parameters Measurement

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Abstract— **With silicon carbide (SiC) MOSFETs becoming commercial available, high switching frequency is a prevailing trend to increase the power density and efficiency in power converters. Nevertheless, the device performance is critically determined by the values of parasitic inductances, where negative effects such as switching oscillations are usually presented. It is more likely troublesome for power modules due to complex interconnect structures and higher current levels operation property. A parasitic inductances extraction technique based on two-port scattering (S) parameters measurement for SiC MOSET power modules is introduced in this paper. Floating errors in the conventional measurement methods can be avoided and accurate results are revealed from a step by step analysis. The practical utility of the two-port approach is demonstrated through a case study of a 1200V SiC MOSFET power module.**

Keywords—Parasitic inductances; Power modules; SiC MOSFETs; S-parameters; Two-port network; Z-parameters.

I. INTRODUCTION

SiC power devices for high switching frequency, high voltage and high temperature applications are currently become more commercial available thanks to the continued maturation of wide bandgap (WBG) semiconductor technology [1][2]. However, the device performance mainly depends on the parasitic inductances, where negative effects including switching oscillations, electromagnetic interface (EMI) noise and extra power losses are accompanied with the high *di/dt* and *dv/dt* characteristics [3][4]. It is necessary to parallel SiC MOSFETs together in a packaging structure to form a power module for managing electrical, mechanical and thermal requirements. The side effects are more likely pronounced in power modules because (1) more complex interconnect structures thus more parasitic inductances; (2) higher current operating level where more energy could be stored; and (3) the tradeoff between electrical and thermal performance [5]. As a result, it is essential to have accurate technique for characterizing the parasitic inductances in order to model and mitigate these non-ideal effects.

The methods for parasitic inductances extraction reported in the literature can be divided into calculation-based and measurement-based. Software tools using the finite element analysis (FEA) or the partial element equivalent circuit (PEEC) method are utilized in the calculation-based approach, such as ANSYS Q3D [6]-[8]. This software application requires internal geometry and material property of the package for modeling and extraction purposes, while such detailed information is usually not available for commercial power modules. In addition, the calculation is time consuming and suffers from convergence issue for complex structures. Measurement-based is an alternative approach, which can be further summarized in time domain and frequency domain. Time domain reflectometry (TDR) method is application of the transmission line theory and extracts the parasitic parameters in time domain [9][10]. A disadvantage of TDR measurement is that the accuracy may be affected from the impedance mismatching between the measured transmission line structure and the TDR instrument. The impedance measurement method in frequency domain utilizing an impedance analyzer or a vector network analyzer (VNA) brings more accuracy and gains considerable acceptance [11]-[13]. However, as will be shown in Section II, this technique has previously been applied with one-port configuration with the disadvantage of inducing floating errors. Scattering (S) parameters measurement are used to extract equivalent circuit of microwave field effect transistors and this technique was applied on silicon power MOSFETs [14][15], but the tedious iterative matching process limits its application. Therefore, we proposed a simple and accurate two-port S-parameters measurement technique, and this method has been applied on discrete power MOSFETs [16] and an IGBT power module [17].

In this paper, we further validate our methodology in three different ways. Firstly, a justification is carried out by extracting an equivalent circuit using Keysight Advanced Design System (ADS) circuit simulator in comparison with known values. Moreover, besides the inductances extraction, we also include the device capacitances characterization under zero biasing condition and compare with the datasheet values, demonstrating the efficacy of the extraction procedures. Lastly, the two-port approach is applied to a commercial SiC MOSFET power module from Wolfspeed (CAS120M12BM2) to ensure that it offers a general solution for the parasitics extraction. The analysis, simulation and experimental results indicate that the two-port method is an accurate and general approach for the parasitic inductances extraction.

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II. Prior Art One-port Extraction Method

A. Discrete Devices

The conventional impedance measurement method for power MOSFET parasitic inductances extraction can be categorized a one-port configuration, as shown in Fig. 1. The MOSFET small-signal equivalent circuit under zero biasing condition is illustrated in the shaded box. The impedance measurement can be taken three times in the three terminal pairs (D-G, G-S, and D-S), forming three equations and resulting three individual inductance values (L_G , L_D and L_S). However, there are two serious concerns in this technique that can be identified as inaccuracy and uncertainty. In the first place, inaccuracy comes from the unintended coupling effect between the floating terminal and ground. For example, when measuring the D-G inductances in Fig. 1, the Source terminal is floating in the air and non-contacted parasitic will be coupled through this floating terminal, thus may induce a significant error. Fig.1 illustrates the coupling path between the floating Source terminal and ground as a coupling impedance in red. Moreover, there are six combinations (D-G, G-D, G-S, S-G, D-S, and S-D) for the three terminals and eight (2^3) possible results could be obtained. This represents the uncertainty issue, where none of these results are accurate because floating errors are always included in each measurement.

The prior art one-port extraction is repeated to show its limitation on a 1200V SiC power MOSFET (Wolfspeed's C2M0280120D) with a Keysight VNA (E5061B) between 100 kHz to 200 MHz. We measured each terminal pair twice with the second time been connected reversely (e.g. first time D-G and second time G-D). Fig. 2 shows the impedance plot of D-G and G-D connection with the extracted combined impedance equal to $L_{\mathrm{D-G}} = 12.28$ nH in Fig. 2(a) and $L_{\mathrm{G-D}} = 13.96$ nH in Fig. 2(b) respectively. The same terminal pair extraction has a difference of 1.68 nH , indicating the floating errors coupled from the floating Source terminal.

B. Power Modules

The inaccuracy and uncertainty concerns associated with one-port extraction are more likely troublesome in power modules with more complex interconnect structures. As it is noted, one-port impedance analysis can be performed on a discrete MOSFET with 3 terminals by 6 (A_3^2) combinations and a total of 8 (2^3) results. There are 7 terminals in a half-bridge power module topology, which means the measurement could be carried out as much as 42 (A_7^2) times and 128 (2^7) results could be obtained. Therefore, it is even more critical to develop accurate characterization technique to extract the parasitic inductances for power modules.

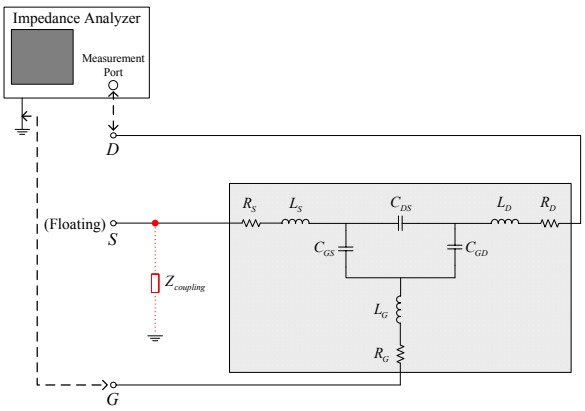


Fig. 1. Prior art one-port extraction of Drain-Gate (D-G) parasitic inductances with Source terminal floating. The MOSFET small-signal equivalent circuit under zero biasing condition is shown in the shaded box.

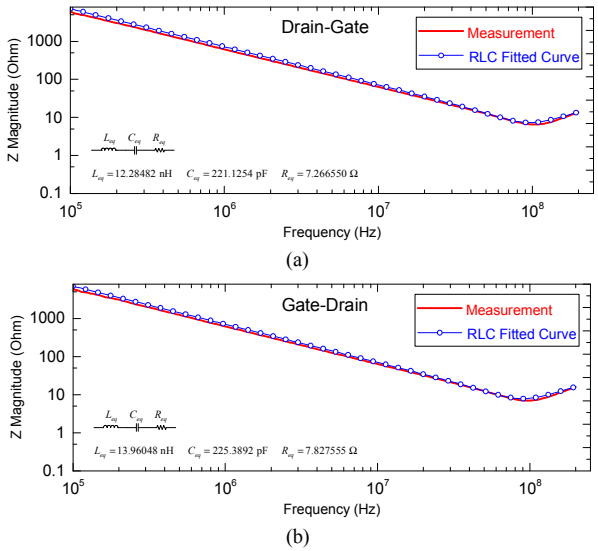


Fig. 2. Limitation of the one-port extraction: (a) $L_{\mathrm{D-G}} = 12.28$ nH from D-G connection; (b) $L_{\mathrm{G-D}} = 13.96$ nH from G-D connection.

III. Proposed Two-port Extraction Method

We proposed a more accurate technique for discrete power devices and power modules extraction based on two-port S-parameters measurement. The methodology will be introduced in this section followed by a simulation validation.

A. Two-port Network Analysis for Discrete MOSFET

A single device in the MOSFET power module is shown as a two-port network in Fig. 3 with S-G connected as Port 1 and D-G as Port 2.

For a second order series RLC circuit, the impedance plot is frequency dependent and the capacitor C_{eq} will dominate at

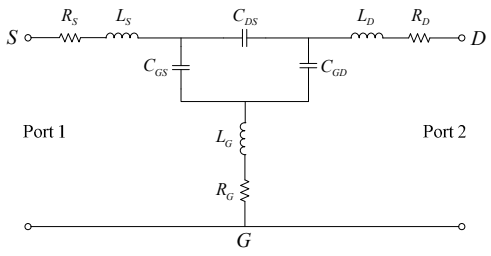


Fig. 3. Two-port network representation of the MOSFET.

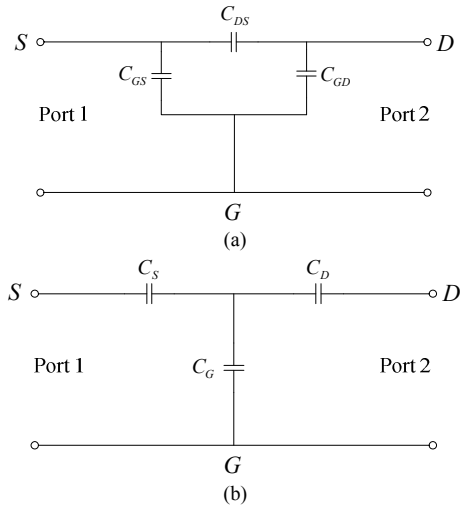


Fig. 4. Two-port network representation of the MOSFET for capacitance contribution at low frequency: (a) Delta connection, (b) Star connection.

low frequency range. The minimum magnitude value is observed at the self-resonant frequency (SRF) which is determined by the resistor R_{eq}. Above the SRF, the inductance L_{eq} contributes the increase of the magnitude plot and can be calculated from the SRF expression $\omega_{\mathrm{SRF}} = 1/\sqrt{L_{eq}C_{eq}}$ [18]. Applying impedance analysis to the two-port network will produce the equivalent RLC circuit in each of the Z-parameters (Z_{11}, Z_{12}, Z_{21} and Z_{22}), from which all the parasitic elements shown in the network will be obtained accurately without floating errors.

The three terminal resistances and three parasitic inductances in Fig. 3 are both in star connection, while the three capacitances are connected in delta connection. Converting the capacitances from delta connection to star connection would simplify the two-port impedance analysis. The conversion is shown in Fig. 4 through (1)-(3).

$$X_{C_G} = \left(X_{C_{GS}} \cdot X_{C_{GD}}\right) \Big/ \left(X_{C_{GS}} + X_{C_{GD}} + X_{C_{DS}}\right) \tag{1}$$

$$X_{C_D} = \left(X_{C_{DS}} \cdot X_{C_{GD}}\right) \Big/ \left(X_{C_{GS}} + X_{C_{GD}} + X_{C_{DS}}\right) \tag{2}$$

$$X_{C_S} = \left(X_{C_{DS}} \cdot X_{C_{GS}}\right) \Big/ \left(X_{C_{GS}} + X_{C_{GD}} + X_{C_{DS}}\right) \tag{3}$$

Therefore, the two-port network can be modified with all

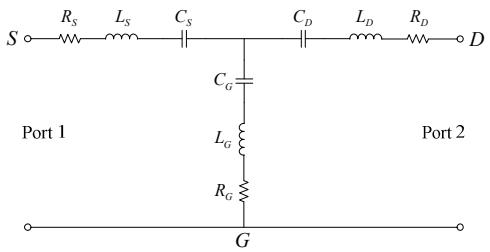


Fig. 5. Modified two-port network representation of the MOSFET with components in star connection.

the components in star connection, as shown in Fig. 5. The Z-parameters for this modified two-port network are defined by all the individual components with (4)-(7),

$$Z_{11} = V_1/I_1\big|_{I_2=0} = \left(X_{C_S} + X_{C_G}\right) + \left(X_{L_S} + X_{L_G}\right) + \left(X_{R_S} + X_{R_G}\right) \tag{4}$$

$$Z_{12} = V_1/I_2\big|_{I_1=0} = X_{C_G} + X_{L_G} + X_{R_G} \tag{5}$$

$$Z_{21} = V_2/I_1\big|_{I_2=0} = X_{C_G} + X_{L_G} + X_{R_G} \tag{6}$$

$$Z_{22} = V_2/I_2\big|_{I_1=0} = \left(X_{C_D} + X_{C_G}\right) + \left(X_{L_D} + X_{L_G}\right) + \left(X_{R_D} + X_{R_G}\right) \tag{7}$$

In each of the Z-parameters (Z_{11}, Z_{12}, Z_{21} and Z_{22}), the impedance is composed from the combined capacitances, inductances and resistances. All the individual components could be extracted from these Z-parameters. It is noted that Fig. 5 should be a reciprocal two-port network, which is also verified from equation (5) and (6).

Based on the analysis, the two-port characterization of parasitic elements in a single discrete MOSFET from its Z-parameters can be summarized as: (1) At low frequency (1 MHz), extract the capacitances C_{GS}, C_{GD} and C_{DS} under zero DC biasing; (2) At SRF, extract the terminal resistances R_G, R_D and R_S; and (3) At high frequency ($>$SRF), extract the parasitic inductances L_G, L_D and L_S.

Last but not least, since the VNA is a test system that enables the measurement in terms of S-parameters. It is required to convert the measured S-parameters into Z-parameters for the extraction purpose. The conversion can be done from (8)-(11) for a standard two-port network, where Z_0 is the characteristic impedance equals to $50\ \Omega$ [19].

$$Z_{11} = \left[\frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}\right] Z_0 \tag{8}$$

$$Z_{12} = \left[\frac{2S_{12}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}\right] Z_0 \tag{9}$$

$$Z_{21} = \left[\frac{2S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}\right] Z_0 \tag{10}$$

$$Z_{22} = \left[\frac{(1+S_{22})(1-S_{11}) + S_{12}S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}\right] Z_0 \tag{11}$$

B. Two-port Network Analysis for MOSFET Module

The two-port extraction technique can be also applied on power modules by the same token. Fig. 6(a) is the circuit diagram of a SiC MOSFET half-bridge power module, and its

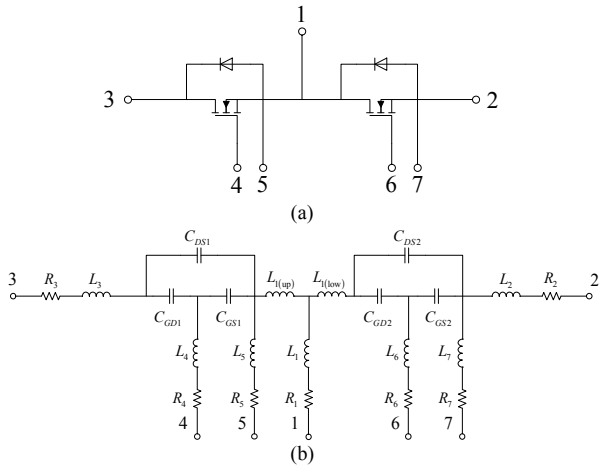


Fig. 6. SiC MOSFET half-bridge power module: (a) Circuit diagram; (b) Small-signal circuit model under zero biasing condition.

small-signal circuit model under zero biasing with all the parasitic components is presented in Fig. 6(b).

The S-parameters can be measured with the VNA and Z-parameters can be converted accordingly; while all the parasitics can be extracted. The SiC MOSFET half-bridge power module has 7 terminals with 9 parasitic inductances and 6 capacitances. They must be extracted with a step by step approach as the following:

Step 1: Port 1 (Terminal 3), Port 2 (Terminal 5, 1, 6, 7 and 2 connected together) and ground (Terminal 4). The individual inductances L_3, L_4, and the capacitances from the upper device C_{GS1}, C_{GD1}, C_{DS1} are extracted, where the circuit connection is illustrated in Fig. 7.

Step 2: Port 1 (Terminal 3 and 4), Port 2 (Terminal 1, 6, 7 and 2) and ground (Terminal 5). The individual inductance L_5 is extracted in this step. The connection can be constructed likewise as Fig. 7.

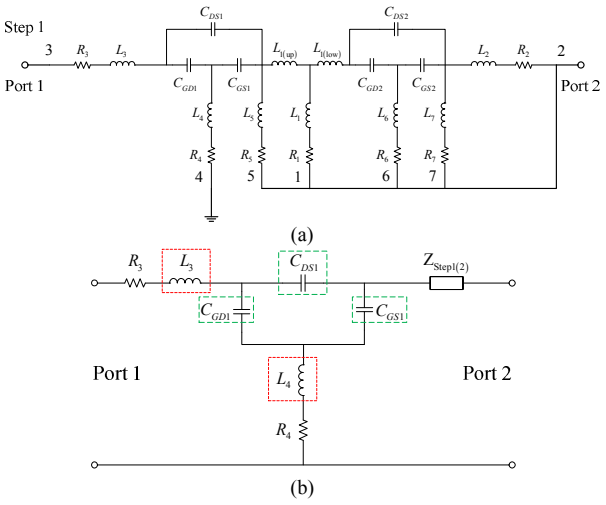


Fig. 7. SiC MOSFET half-bridge power module extraction Step 1: (a) circuit connection; (b) equivalent circuit for L_3, L_4 and C_{GS1}, C_{GD1}, C_{DS1} extraction. Similar diagrams for Step 2, 3, 4 and 5 can be constructed.

Step 3: Port 1 (Terminal 3, 4 and 5), Port 2 (Terminal 6, 7 and 2) and ground (Terminal 1). The individual inductances $L_{1(up)}$, L_1 and $L_{1(low)}$ are extracted in this step.

Step 4: Port 1 (Terminal 3, 4, 5 and 1), Port 2 (Terminal 7 and 2) and ground (Terminal 6). The individual inductance L_6, and the capacitances from the lower device C_{GS2}, C_{GD2}, C_{DS2} are extracted in this step.

Step 5: Port 1 (Terminal 3, 4, 5, 1 and 6), Port 2 (Terminal 2) and ground (Terminal 7). The individual inductances L_7 and L_2 are extracted in this step.

C. Simulation Validation

To validate the proposed two-port extraction technique, we simulate a SiC MOSFET half-bridge power module equivalent circuit (Fig. 6) with a set of pre-determined inductance, capacitance and resistance values to generate a set of S-parameters for all the five steps, and then extract the parasitic elements from the converted Z-parameters. The extracted values are compared with the given simulation values to verify our methodology. We utilize the Keysight Advanced Design System (ADS), a radio frequency (RF) and microwave design automation software, for this validation. Table I shows the set of pre-determined values using in the simulation, and the proposed five steps two-port extraction technique are utilized to extract the parasitic inductances and capacitances. The comparison between the extracted values and the initial simulation values are carried out with a largest difference of 2.25% noted in the $L_{1(low)}$ extraction, which is because the

TABLE I. ADS SIMULATION VERIFICATION RESULTS

ADS Simulation	Pre-determined	Two-port Extraction	Difference
L_3 (nH)	15	15.007	0.047%
L_4 (nH)	30	29.986	0.047%
L_5 (nH)	40	40.000	0%
$L_{1(up)}$ (nH)	16	16.023	0.14%
L_1 (nH)	20	20.000	0%
$L_{1(low)}$ (nH)	2	2.045	2.25%
L_6 (nH)	45	44.980	0.044%
L_7 (nH)	50	50.000	0%
L_2 (nH)	15	15.000	0%
C_{GS1} (nF)	6	6.001	0.017%
C_{GD1} (nF)	3	3.000	0%
C_{DS1} (nF)	15	15.004	0.027%
C_{GS2} (nF)	6	6.002	0.033%
C_{GD2} (nF)	3	3.000	0%
C_{DS2} (nF)	15	15.008	0.053%

original value (2 nH) is already very small in the beginning. This reasonably good agreement indicates that the two-port extraction method is applicable for power modules, and it is a simple yet accurate extraction technique.

IV. Experimental Validation

To further validate the our methodology, we applied it on a SiC MOSFETs half-bridge power module for inductances and capacitances extraction to show the it is a general solution for power modules extraction.

A. Experimental Setup

The S-parameters characterization is performed using a VNA (Keysight's E5061B) in this work, as shown in Fig. 8. Before the two-port measurement, two critical steps are required: test fixture design and VNA calibration. On the one hand, a good test fixture can provide a transparent connection between the VNA and the device under test (DUT) with negligible loss and flat frequency response. Fig. 8 shows the designed PCB based test fixture, and two female SMA female adaptors are used for interfacing the VNA cable and the DUT [20]. On the other hand, calibration is crucial to ensuring the accuracy and repeatability of VNA measurements. Prior the S-parameters measurement, a full 2-port Short-Open-Load-Through (SOLT) calibration procedures are executed. The VNA compares the measured calibration values with the known values of SOLT standard, from which the correction factor for each frequency point can be calculated. These correction factors are then applied to remove the errors and recover the intrinsic characteristics of the DUT. The Short, Open and Load calibration steps are carried out using the calibration kit provided by Keysight; while the Through step is performed by the PCB based on the designed test fixture [21].

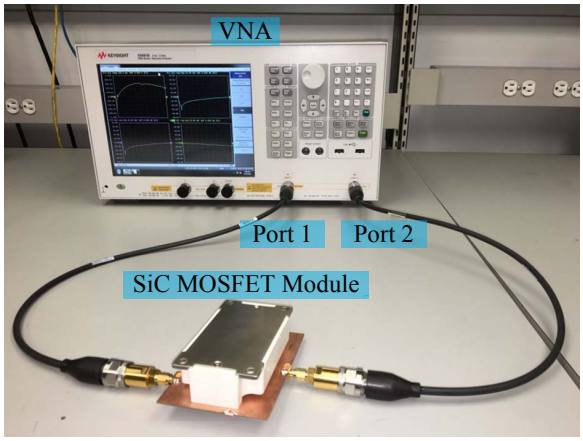
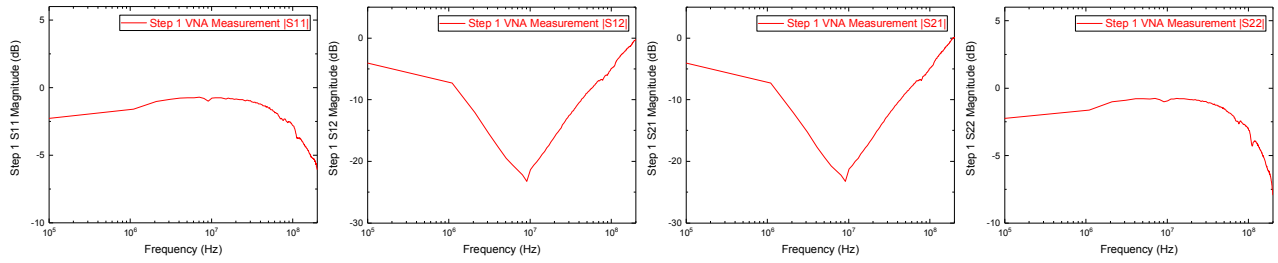


Fig. 8. Two-port extraction experimental setup showing the test fixture and the SiC MOSFET half-bridge power module.

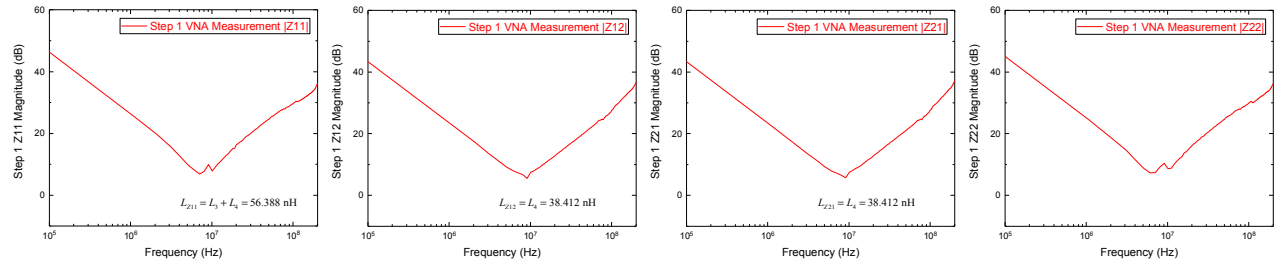
B. 1200V SiC MOSFET Half-bridge Power Module

A commercial 1200V SiC MOSFET half-bridge power module (Wolfspeed's CAS120M12BM2) is selected for a case study and its device schematic is shown in Fig. 6(a). The log-spaced frequency sweep is from 100 kHz to 200 MHz. The five steps extraction procedure is carried out one by one to reveal all the 9 parasitic inductances and 6 capacitances in Fig. 6(b). As an illustration, Fig. 9 shows the VNA measured S-parameters for Step 1, from which the Z-parameters are converted through equations (8)-(11) and the results are shown in Fig. 10. According to Step 1, the inductances L_3 and L_4, as well as the capacitances from the upper MOSFET C_{GS1}, C_{GD1}, C_{DS1} are extracted. Similar procedure can be also performed for Step 2, 3, 4 and 5 with the converted Z-parameters



(a) (b) (c) (d)

Fig. 9. Measured S-parameters (Step 1). (a) $|S_{11}|$; (b) $|S_{12}|$; (c) $|S_{21}|$; (d) $|S_{22}|$.

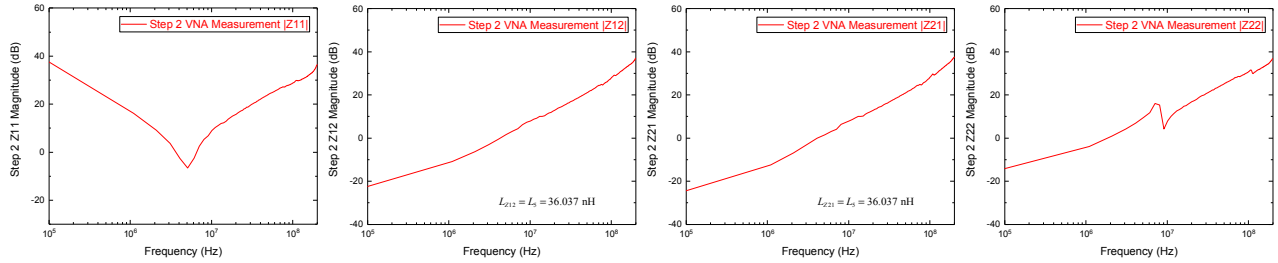


(a) (b) (c) (d)

Fig. 10. Converted Z-parameters (Step 1). (a) $|Z_{11}|$; (b) $|Z_{12}|$; (c) $|Z_{21}|$; (d) $|Z_{22}|$. Extracted inductances: L_3 = 17.976 nH and L_4 = 38.412 nH.

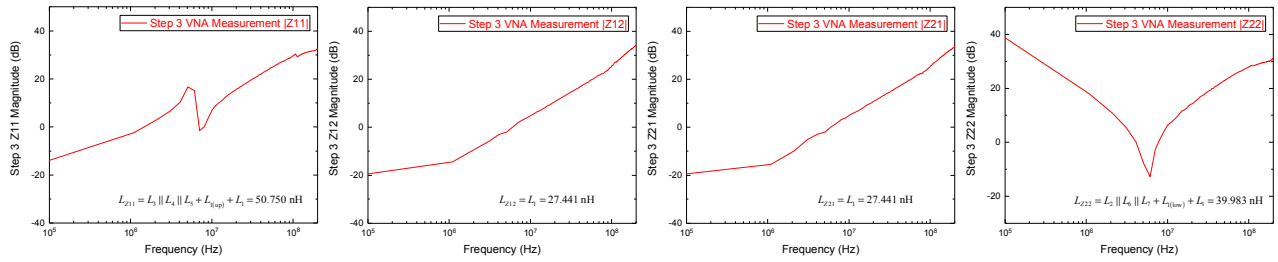
represented in Fig. 11, 12, 13 and 14 respectively.

Terminal 5, 1, 6, 7 and 2 are connected together as Port 2 in Step 1 extraction, where high-order resonance will present in Z_{22} because $Z_{\text{Step1(2)}}$ (in Fig. 7) contains multiple inductances and capacitances. This high-order resonance for Step 1 can be noted and verified in Fig. 10(d) above the SRF. Based on the connect configuration, high-order resonance are also presented in Step 2 for Z_{11} and Z_{22}, in Step 3 for Z_{11} and Z_{22}, in Step 4 for Z_{11}, and in Step 5 for Z_{11}. However, the resonance might not be noticed in the impedance plot when the high-order resonance is near the self-resonant frequency, such as Fig. 11(a) in Step 2, Fig. 12(d) in Step 3 and Fig. 13(a) in Step 4. Moreover, the two-port network reciprocal property can be also verified in all the five steps through Fig. 10 to Fig. 14, which is consistent with equation (5) and (6) in section III.



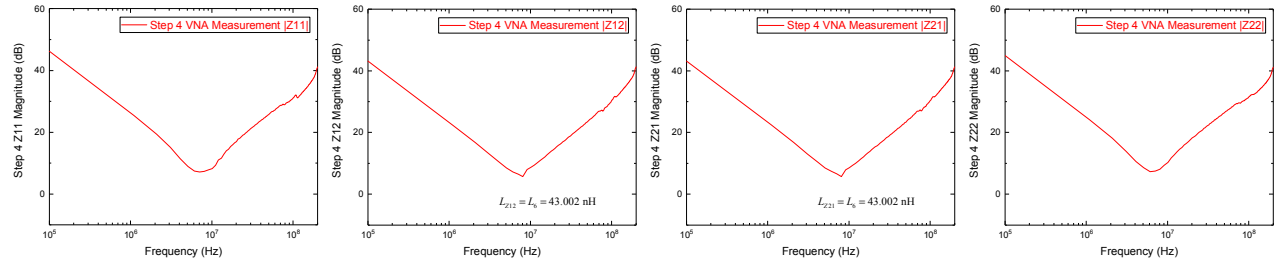
(a) (b) (c) (d)

Fig. 11. Converted Z-parameters (Step 2). (a) $|Z_{11}|$; (b) $|Z_{12}|$; (c) $|Z_{21}|$; (d) $|Z_{22}|$. Extracted inductance: L_5 = 36.037 nH.



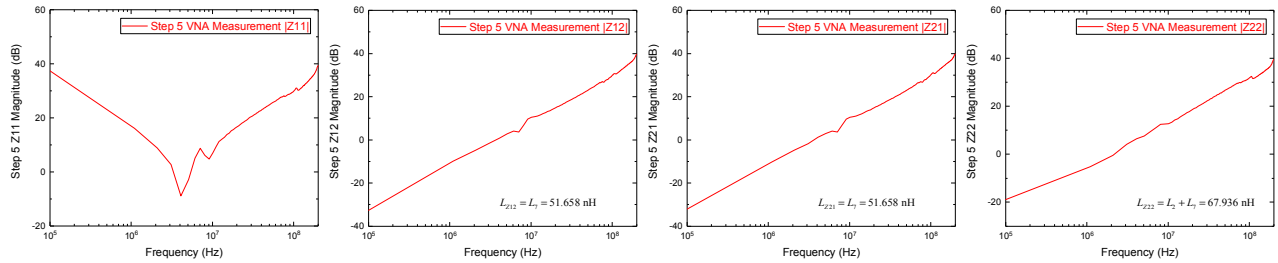
(a) (b) (c) (d)

Fig. 12. Converted Z-parameters (Step 3). (a) $|Z_{11}|$; (b) $|Z_{12}|$; (c) $|Z_{21}|$; (d) $|Z_{22}|$. Extracted inductances: $L_{1(\text{up})}$ = 14.182 nH, L_1 = 27.441 nH, $L_{1(\text{low})}$ = 2.931 nH.



(a) (b) (c) (d)

Fig. 13. Converted Z-parameters (Step 4). (a) $|Z_{11}|$; (b) $|Z_{12}|$; (c) $|Z_{21}|$; (d) $|Z_{22}|$. Extracted inductance: L_6 = 43.002 nH.



(a) (b) (c) (d)

Fig. 14. Converted Z-parameters (Step 5). (a) $|Z_{11}|$; (b) $|Z_{12}|$; (c) $|Z_{21}|$; (d) $|Z_{22}|$. L_7 and L_2 are extracted: L_7 = 51.658 nH and L_2 = 16.278 nH.

TABLE II. EXTRACTED PARASITIC INDUCTANCES AND CAPACITANCES OF THE SIC MOSFET HALF-BRIDGE POWER MODULE

Inductance	L_3 (nH)	L_4 (nH)	L_5 (nH)	$L_{1(up)}$ (nH)	L_1 (nH)	$L_{1(low)}$ (nH)	L_6 (nH)	L_7 (nH)	L_2 (nH)
Two-port Extraction	17.976	38.412	36.037	14.182	27.441	2.931	43.002	51.658	16.278

Capacitance	C_{GS1} (nF)	C_{GD1} (nF)	C_{DS1} (nF)	C_{GS2} (nF)	C_{GD2} (nF)	C_{DS2} (nF)
Two-port Extraction	6.062	3.262	15.897	6.310	3.246	15.661
Datasheet Value	6	3	16	6	3	16
Difference	1.03%	8.73%	0.64%	5.17%	8.20%	2.12%

The extracted parasitic inductances and capacitances from the two-port characterization technique through the five steps procedure are summarized in Table II. Larger inductances values are observed in the four gate terminals L_4, L_5, L_6 and L_7 as long wires are usually connected in the module package. It is reasonable to note that $L_{1(low)}$ is the smallest because the upper and lower MOSFET are directly attached. The extraction of $L_{1(low)}$ is another important contribution of this paper as it was usually neglected in prior research [9][12][13]. Furthermore, the extracted upper and lower MOSFET capacitances with zero DC biasing are compared with datasheet values in Table II. The datasheet capacitances are obtained from the CV curves when the Drain-Source voltage is 0V. Considering reading errors from the compact log-spaced plot, the extracted capacitances are consistent with the datasheet values and the maximum difference is 8.73%. It is worth pointing out that the MOSFET capacitances are voltage dependent and we only extracted with one voltage level at zero voltage biasing (i.e. 0V). These capacitances extracted from our two-port characterization are just one way we used to verify the proposed technique. The main purpose of this work, however, is to use the two-port approach to extract the parasitic inductances, which will avoid the inaccuracy and uncertainty concerns in the prior art one-port method.

According to the simulation and experimental studies, applying the proposed two-port extraction technique to determine the parasitic elements in power devices is effective and accurate. This approach is now verified with a commercial available 1200V SiC MOSFET half-bridge power module (Wolfspeed's CAS120M12BM2), indicating itself as a general method and can be generally applied for power modules. More importantly, this method is capable to be applied on other multi-chip power modules with more complex interconnect structures.

V. CONCLUSION

Parasitic inductances play an important role in determining the SiC MOSFETs performance for the high frequency and high power density applications. This paper presents a new and accurate two-port extraction methodology for extracting values of parasitic inductances in power modules. This proposed technique resolves the inaccuracy and uncertainty concerns exist in the prior art one-port configuration. We further verified the approach in three aspects: (1) extracting a power MOSFET module equivalent circuit using Keysight ADS simulator and compare with the initial simulation values; (2) determining the MOSFET power module capacitances and compare with the datasheet values; and (3) demonstrating by the execution of a experimental study on a SiC MOSFET half-bridge power module. The resulting validation suggests that the proposed methodology is a general approach and capable for accurate extraction of the parasitic inductances in high speed discrete power devices and power modules.

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