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-- Company: İstanbul Üniversitesi - Cerrahpaşa
-- Engineer: Buse Dağıdır
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-- Create Date: 20:37:50 11/05/2020
-- Design Name:
-- Module Name: devre - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
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-- Dependencies:
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-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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library IEEE;

use IEEE.STD_LOGIC_1164.ALL;



entity and_gate is

        port( and_g1: in STD_LOGIC;

                        and_g2: in STD_LOGIC;

                        and_x: out STD_LOGIC);

end and_gate;



architecture Behavioral of and_gate is



begin

        and_x <= and_g1 and and_g2;

end Behavioral;



----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD_LOGIC_1164.ALL;
```

```
entity or_gate is
        port( or_g1, or_g2: in STD_LOGIC;
                        or_x: out STD_LOGIC);
end or_gate;

architecture Behavioral of or_gate is

begin
        or_x <= or_g1 or or_g2;
end Behavioral;


-------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity dff is
        port( D: in STD_LOGIC;
                  Q: inout STD_LOGIC;
                        Qn: inout STD_LOGIC;
                        Clock: in STD_LOGIC;
                        Clear: in STD_LOGIC);
end dff;

architecture Behavioral of dff is

begin
        process(Clock) --eğer clock değişirse alttaki begin-end process i çalıştır --
        begin
                if(rising_edge(Clock)) then
```

```
                    if(Clear='0') then
                        Q <= '0';
                        Qn <= '1';
                    else
                        Q <= D;
                        Qn <= not(D);
                    end if;
                end if;
            end process;

end Behavioral;

------------------------------------------------------------------------------
Library IEEE;
USE IEEE.Std_logic_1164.all;

entity dff_and_or is
            port(     X: in STD_LOGIC;
                    Clock: in STD_LOGIC;
                    Z: out STD_LOGIC);
end dff_and_or;

architecture Behavioral of dff_and_or is

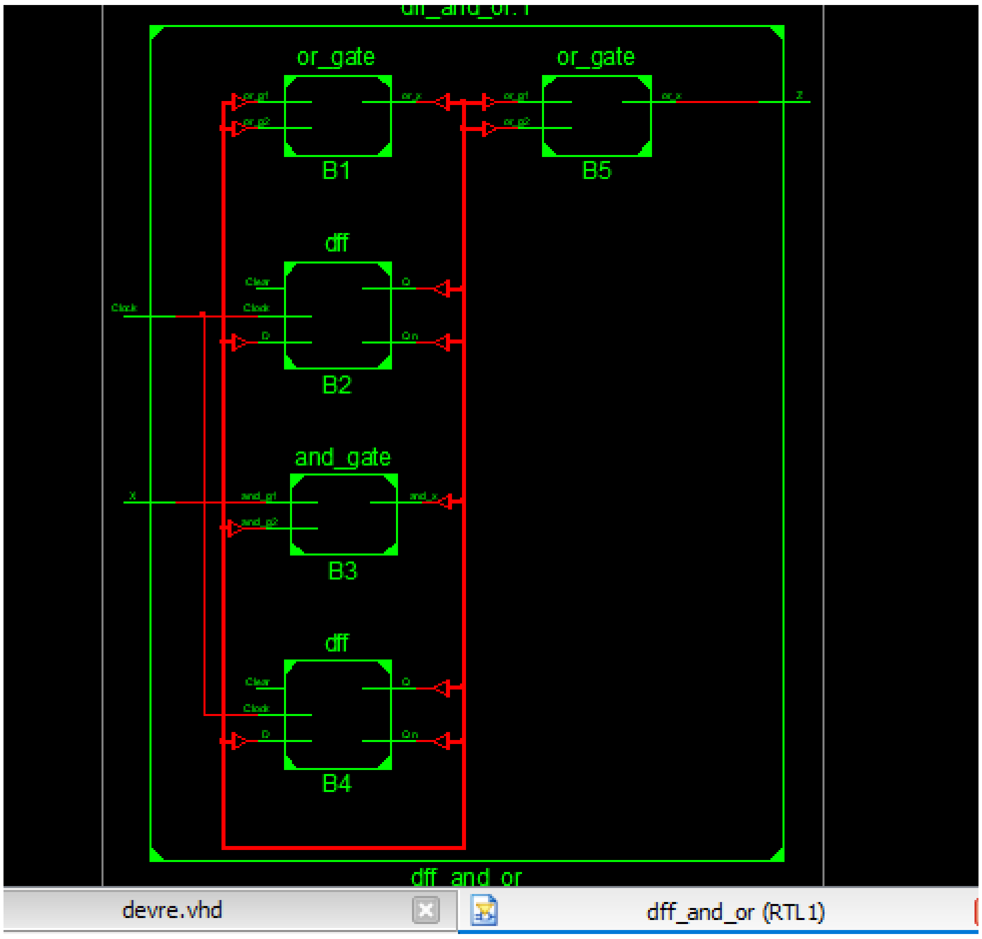
            component or_gate is
                port( or_g1, or_g2: in STD_LOGIC;
                        or_x: out STD_LOGIC);
            end component;

            component dff is
                port(     Q: inout STD_LOGIC;
                              Qn: inout STD_LOGIC;
                              Clock: in STD_LOGIC;
                              Clear: in STD_LOGIC;
                              D: in STD_LOGIC);
          end component;

          component and_gate is
                    port( and_g1: in STD_LOGIC;
                              and_g2: in STD_LOGIC;
                              and_x: out STD_LOGIC);
          end component;

          signal K: STD_LOGIC_VECTOR(5 downto 0);

begin
                    B1: or_gate port map(K(0), K(1), K(2));
                    B2: dff port map(K(3), K(0), Clock, '0', K(2));
                    B3: and_gate port map(X, K(4), K(5));
                    B4: dff port map(K(1), K(4), Clock, '0', K(5));
                    B5: or_gate port map(K(3), K(5), Z);
end Behavioral;
```



| Clock | X | Z |
|---|---|---|
| 0 | 0 | - |
| 1 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 1 | 1 |