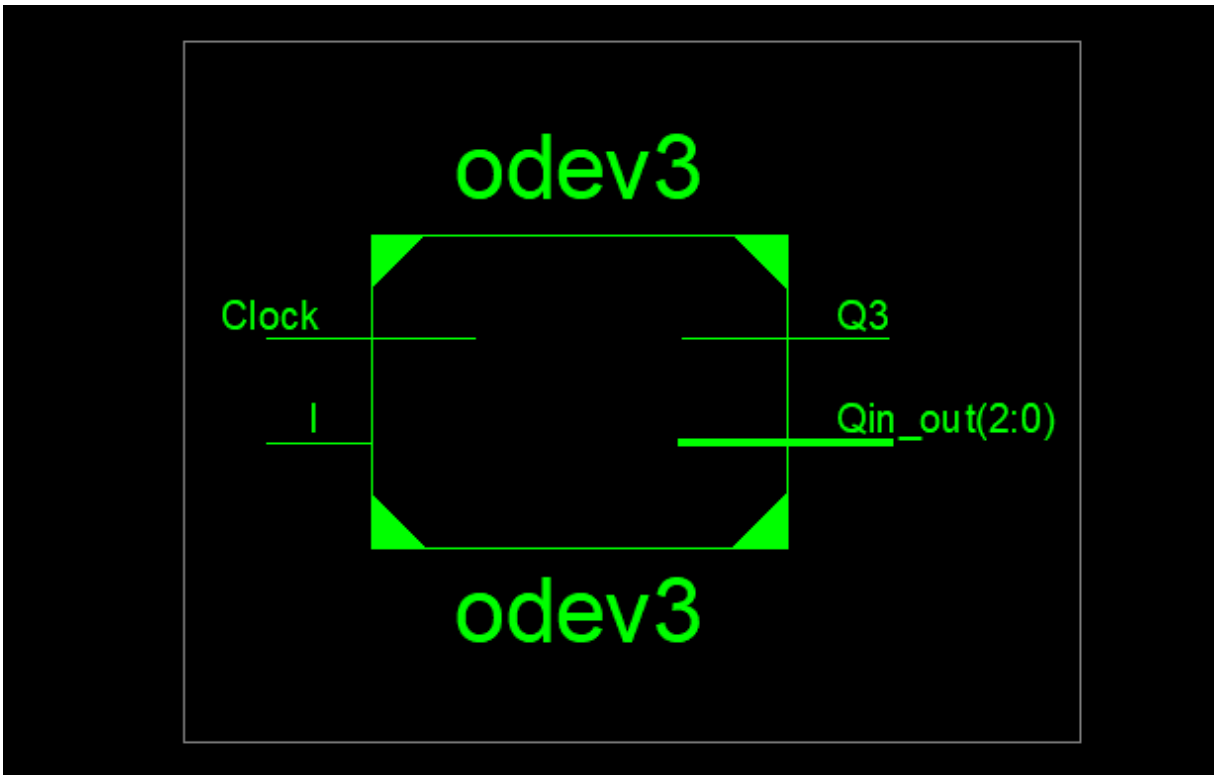
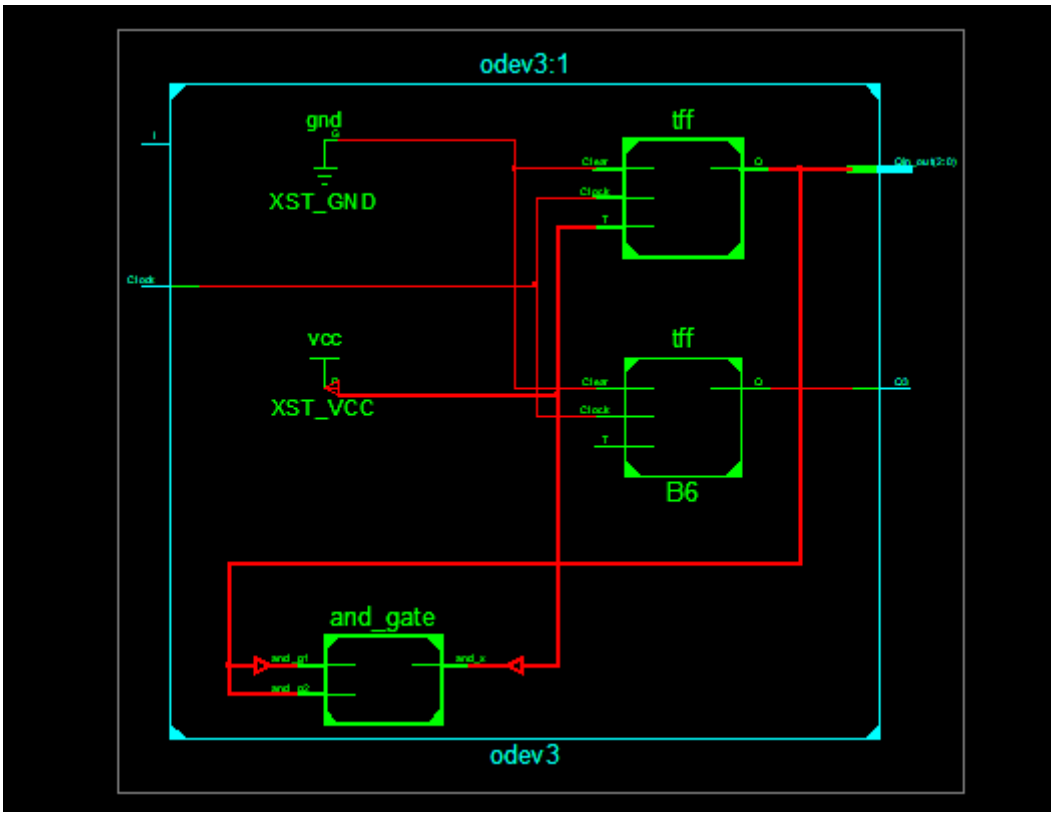
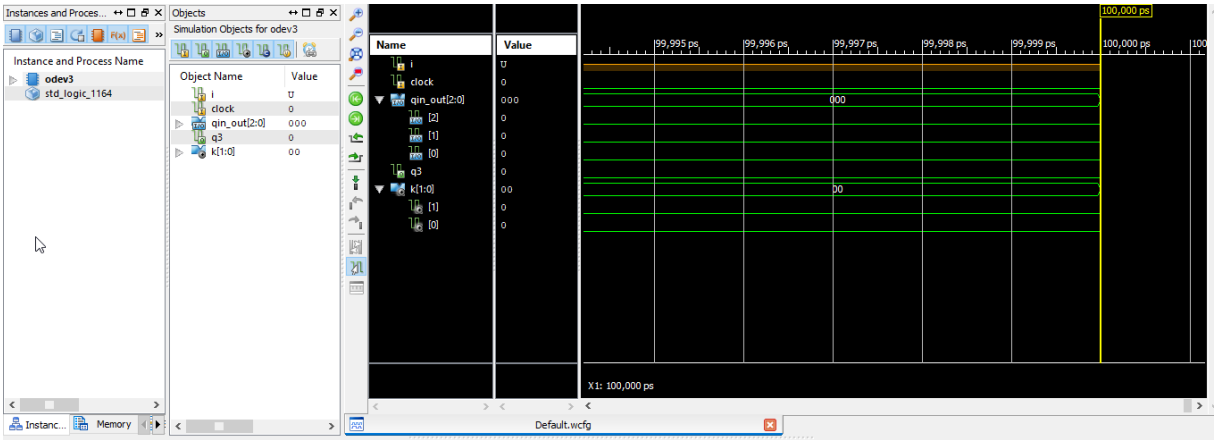
```
Library IEEE;
USE IEEE.Std_logic_1164.all;
entity tff is
	port( T: in STD_LOGIC;
			Clock: in STD_LOGIC;
			Clear: in STD_LOGIC;
			Q: out STD_LOGIC);
end tff;
architecture Behavioral of tff is
begin
	toggle: process(T, Clock, Clear) is
	variable m: std_logic := '0';
	begin
		if (Clear = '1') then
			m := '0';
		elsif (rising_edge(Clock)) then
			if(T = '1') then
				m := not m;
			end if;
		end if;
		Q <= m;
	end process toggle;
end Behavioral;
----------------------------------------------------------------------------
Library IEEE;
USE IEEE.Std_logic_1164.all;

entity odev3 is
	port( I: in STD_LOGIC;
			Clock: in STD_LOGIC;
			Qin_out: inout STD_LOGIC_VECTOR (2 downto 0);
			Q3: out STD_LOGIC);
end odev3;
```

```
architecture Behavioral of odev3 is
	component tff is
		port( T: in STD_LOGIC;
			Clock: in STD_LOGIC;
			Clear: in STD_LOGIC;
			Q: out STD_LOGIC);
	end component;

	component and_gate is
		port( and_g1: in STD_LOGIC;
			and_g2: in STD_LOGIC;
			and_x: out STD_LOGIC);
	end component;

	signal K: STD_LOGIC_VECTOR(1 downto 0);
	begin
		B1: tff port map('1', Clock, '0', Qin_out(0));
		B2: tff port map(Qin_out(0), Clock, '0', Qin_out(1));
		B3: and_gate port map(Qin_out(0), Qin_out(1), K(0));
		B4: tff port map(K(0), Clock, '0', Qin_out(2));
		B5: and_gate port map(K(0), Qin_out(2), K(1));
		B6: tff port map(K(1), Clock, '0', Q3);
end Behavioral;
```

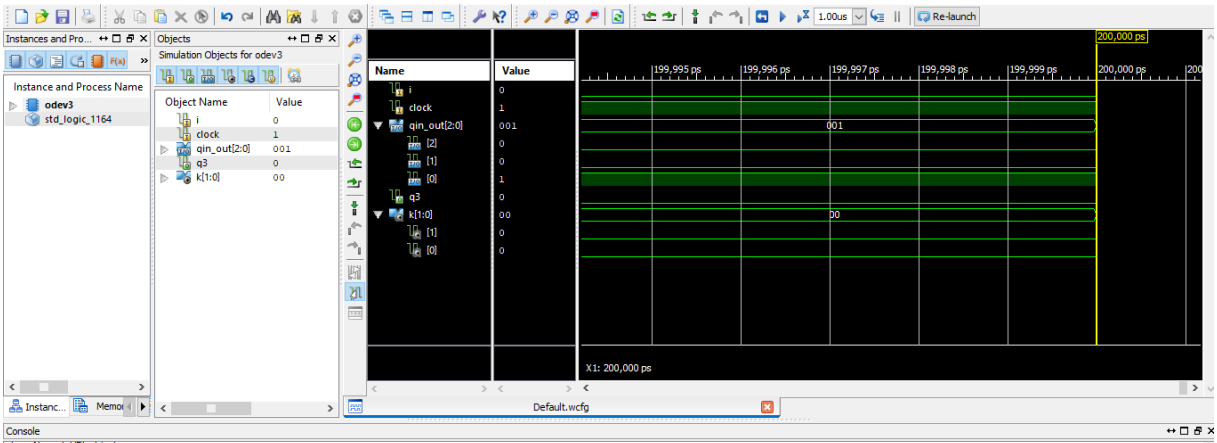

odev3
Clock
I
Q3
Qin_out(2:0)
odev3


odev3:1
gnd
XST_GND
tff
vcc
XST_VCC
tff
B6
and_gate
odev3

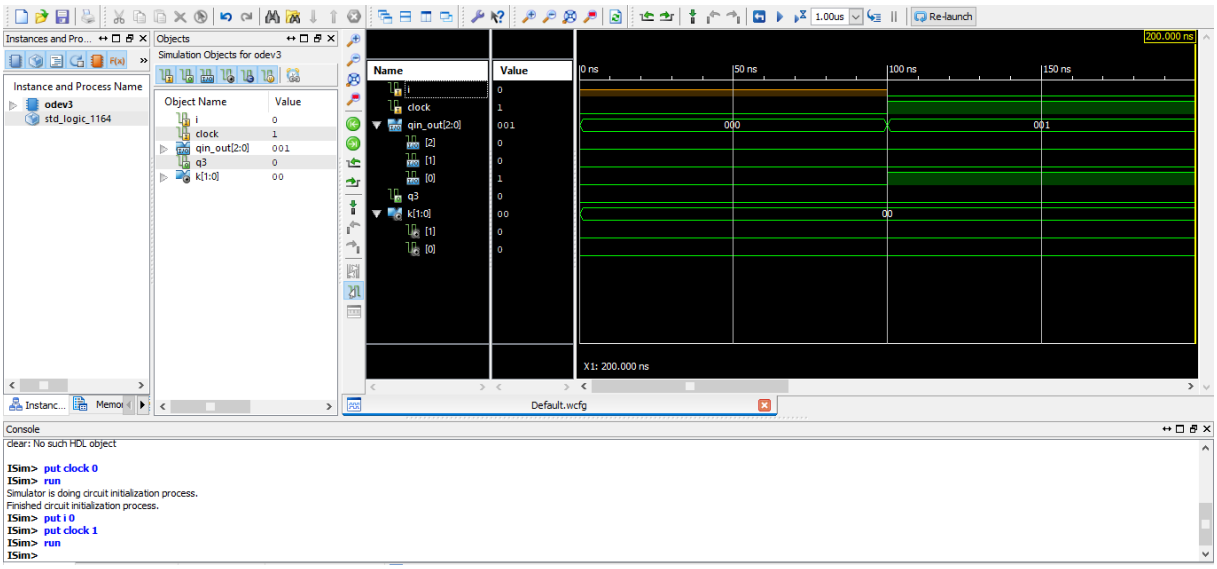

```
im P.28xd (signature 0xa0883be4)
ARNING: A WEBPACK license was found.
ARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
ARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
is is a Lite version of ISim.
ne resolution is 1 ps
nulator is doing circuit initialization process.
ished circuit initialization process.
im> restart
im>
```

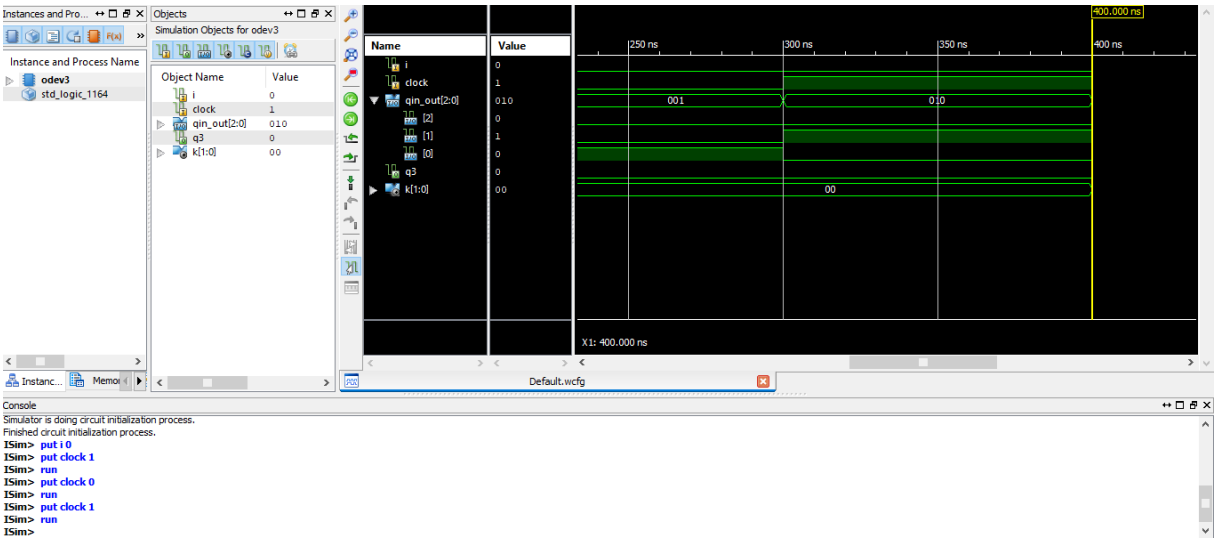



```
ISim> put clock 0
ISim> run
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
```




```
clear: No such HDL object

ISim> put clock 0
ISim> run
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim> put i 0
ISim> put clock 1
ISim> run
ISim>
```





Clock'a bir kaç defa 0 ve 1 değerlerini verince: