

Microcontroladores

Laboratorio Sesión 6

Semestre: 2021-2

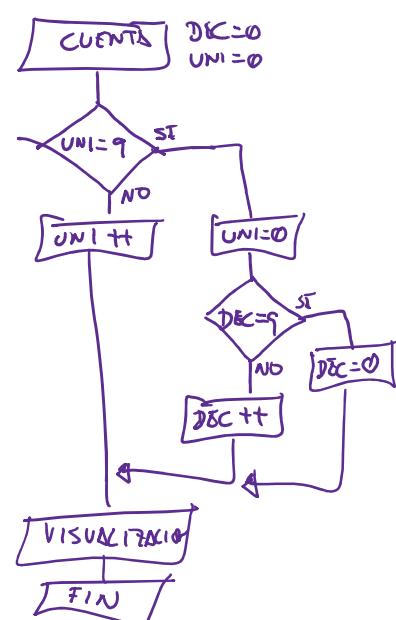
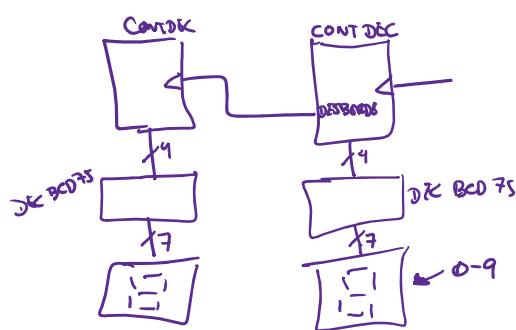
Profesor: Kalun José Lau Gan

1

Preguntas previas (alzar la mano durante la consulta)

Algoritmo para cuenta 00-99:

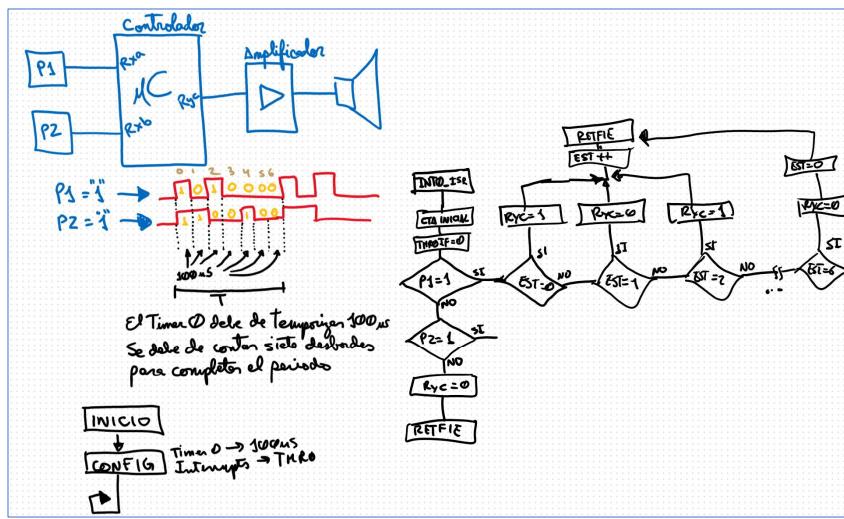
Idea:



2

Preguntas previas (alzar la mano durante la consulta)

- Tuve dificultades para desarrollar la onda requerida en la última pregunta de la PC1



3

Preguntas previas (alzar la mano durante la consulta)

- ?

4

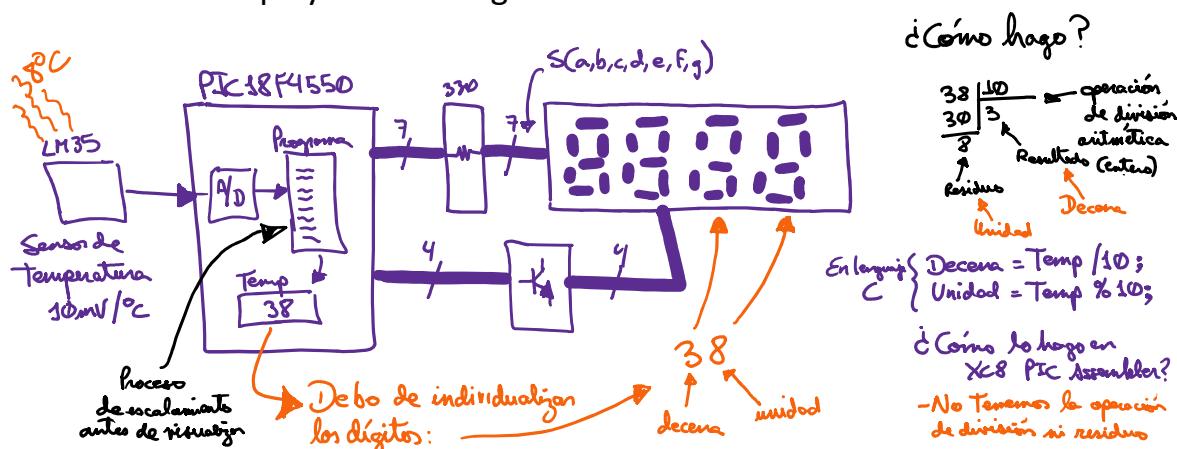
Agenda

- Rutina para obtener los dígitos centena, decena y unidad de un registro de 8 bits
- Timer 1 para aplicaciones en tiempo real (RTC)
 - Referencia: Unidad 12 de la hoja técnica del PIC18F4550
- Interrupciones con el Timer 1
- Ejemplos con el Timer 1

5

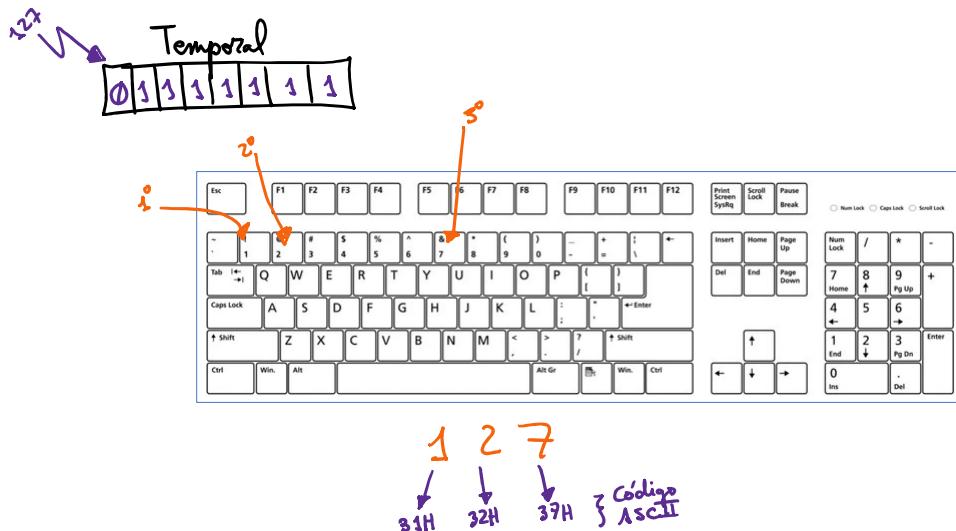
Rutina para obtener los dígitos centena, decena y unidad de un registro de 8 bits

- Sirve para individualizar los dígitos de un registro para así visualizarlos en cada display de siete segmentos.



6

Idea: ¿Cómo ingresas el número 127 a la PC?



7

Rutina para obtener los dígitos centena, decena y unidad de un registro de 8 bits

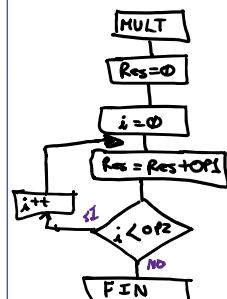
Ejemplo:

$$\begin{array}{r}
 \text{OP1} \quad \text{OP2} \quad \text{Res} \\
 \downarrow \quad \downarrow \quad \downarrow \\
 8 \times 4 = 32 \\
 \begin{array}{r}
 8+ \\
 8 \\
 8 \\
 8 \\
 \hline
 32
 \end{array}
 \qquad
 \begin{array}{r}
 8 \times 6 = 48 \\
 \begin{array}{r}
 8+ \\
 8 \\
 8 \\
 8 \\
 8 \\
 8 \\
 \hline
 48
 \end{array}
 \end{array}
 \\
 \begin{array}{r}
 (8 \times 1 = 8) \\
 8
 \end{array}
 \qquad
 \begin{array}{r}
 8 \times 2 = 16 \\
 \begin{array}{r}
 8+ \\
 8 \\
 \hline
 16
 \end{array}
 \end{array}
 \end{array}$$

Recordando:

```

For (i=0; i<9; i++) {
    } Se va a repetir 9 veces
    → OP1 = 8
    OP2 = 4
    Res = 0
    For (i=0; i<OP2; i++) {
        Res = Res + OP1;
    }
  
```



8

Rutina para obtener los dígitos centena, decena y unidad de un registro de 8 bits

Tomo el número 133, obtener centena, decena y unidad:

$$\begin{array}{r} \text{Temp} = 133 - \\ \hline 100 \\ 33 - \\ 100 \\ \hline -67 \end{array}$$

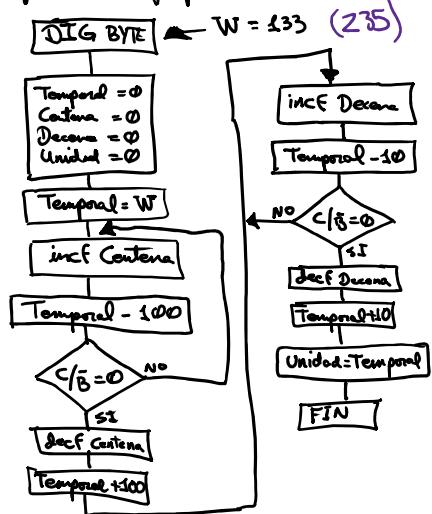
¿Cuántas veces he restado 100?
- Dos veces → centena
Restar uno a centena

$$\begin{array}{r} -67 + \\ 100 \\ \hline 33 - \\ 10 \\ \hline 23 - \\ 10 \\ \hline 13 - \\ 10 \\ \hline 3 - \\ 10 \\ \hline -7 \end{array}$$

¿Cuántas veces he restado 10?
- Cuatro veces.
→ Restar uno y obtengo la decena

Nota:
El bit C/B de STATUS:
Suma: C
Resta: B

Diagrama de flujo:



Módulo Timer 1

- Tres fuentes de reloj para contar: Fosc/4, cristal 32.768KHz y pulsos externos en T13CKI (pin 15)
- Resolución de 16 bits (registros de cuenta TMR1H:TMR1L)
 - Total de cuentas: 65536
 - Cuentas van desde el 0 hasta 65535
- Cuenta ascendente
- Al desbordarse (overflow) puede generar evento de interrupción (TMR1IF)
 - El desborde ocurre en 65535 -> 0
- **Exclusivo para aplicaciones de RTC (empleando 32.768KHz)**
- Opción de reinicio de cuenta con el módulo periférico CCP (modo comparación evento especial de disparo)
- Política de carga de datos en la cuenta: primero TMR1H y luego TMR1L

Observaciones en el Proteus con respecto al uso del Timer1

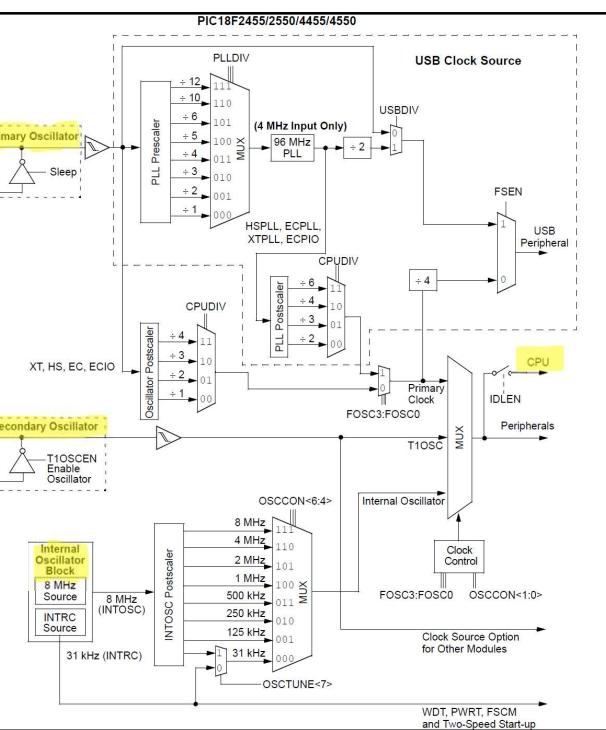
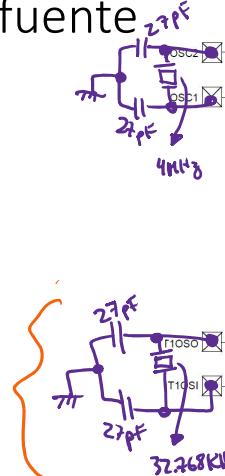
- No se simula correctamente el uso del cristal de 32.768KHz
- Para la simulación usaremos pulsos externos de reloj a la entrada T13CKI



11

Recordando la configuración de fuente de reloj del CPU

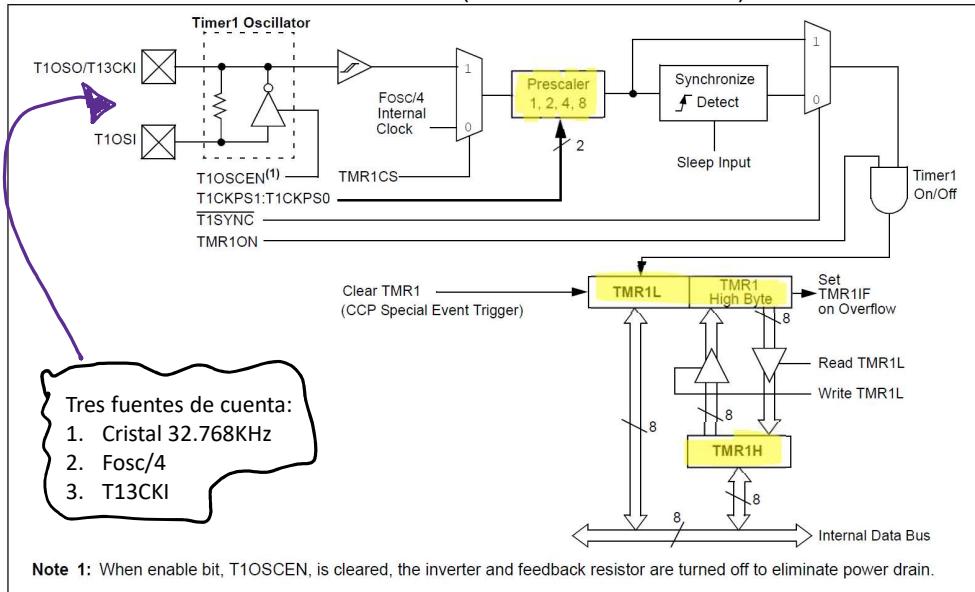
Se usa exclusivamente para el Timer1, pero en algunos casos este oscilador también puede ser direccionado para el CPU



12

Diagrama de bloques del Timer1

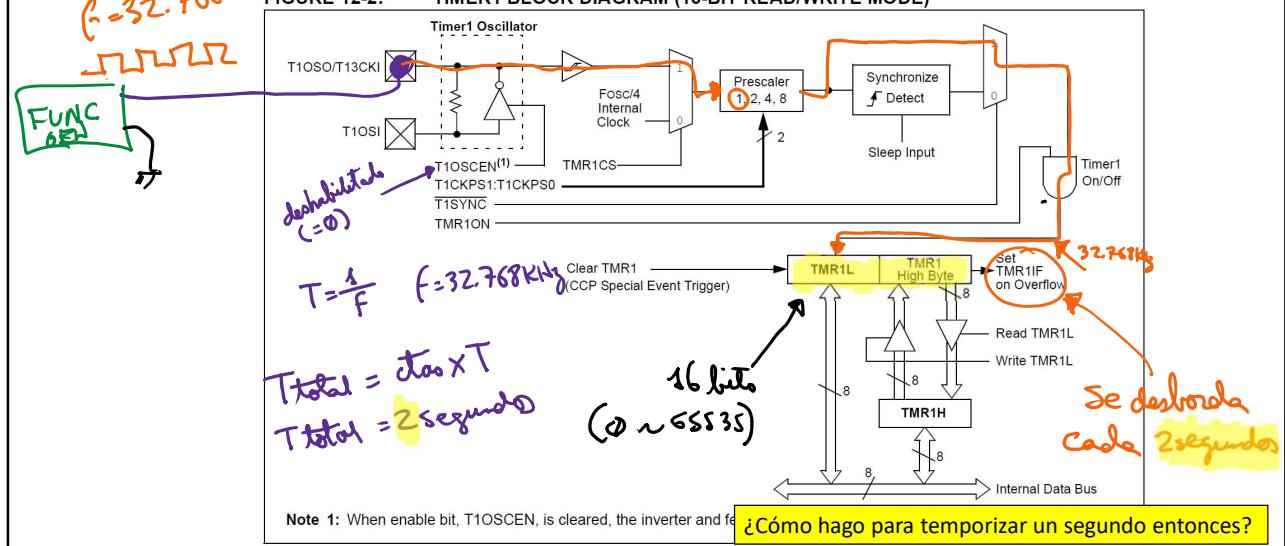
FIGURE 12-2: TIMER1 BLOCK DIAGRAM (16-BIT READ/WRITE MODE)



13

Opción 1: Ingreso de pulsos de reloj a través de T13CKI

FIGURE 12-2: TIMER1 BLOCK DIAGRAM (16-BIT READ/WRITE MODE)



14

Opción 1: Ingreso de pulsos de reloj a través de T13CKI

- Según la configuración anterior, el Timer1 se está desbordando cada 2 segundos
- Si necesitamos que se desborde cada segundo debemos de precargar la cuenta en 32768
- Para precargar la cuenta necesitamos escribir en TMR1H y TMR1L el valor de 32768, este proceso de carga le toma un tiempo al uC para ejecutarlo:

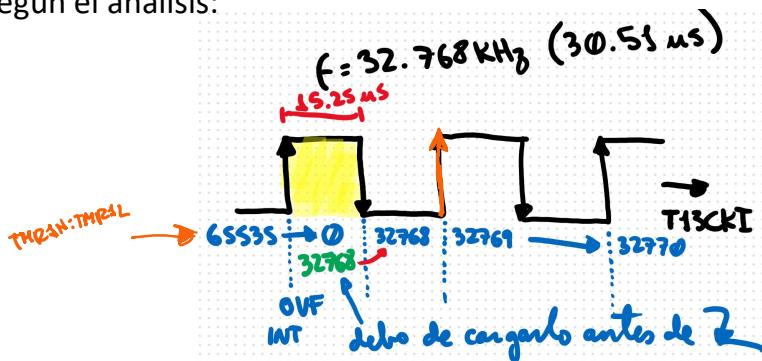


- Tener en cuenta lo estipulado en 12.6 y 12.7 de la hoja técnica

15

Opción 1: Ingreso de pulsos de reloj a través de T13CKI

- Según el análisis:



- Se tiene una ventana de tiempo de 15.25us (antes de que haya el flanko negativo de la señal de reloj) para cargar una cuenta inicial en TMR1 luego de producirse una interrupción por desborde de TMR1. El proceso de carga se realizará en el flanko negativo.
- Para que esto funcione se debe de cumplir con lo estipulado en el último párrafo del 12.6 de la hoja técnica: Modo asíncrono, interrupciones habilitadas y fuente de reloj funcionando todo el tiempo

16

Ejemplo 1: Obtener una señal de reloj de 1Hz empleando el Timer1 en modo RTC.

- Hardware

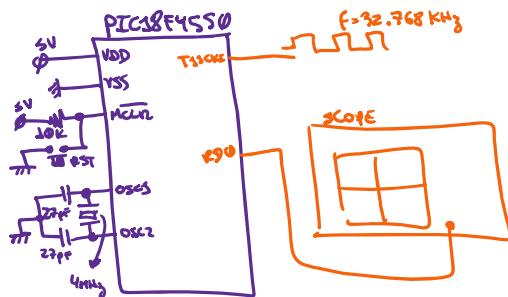
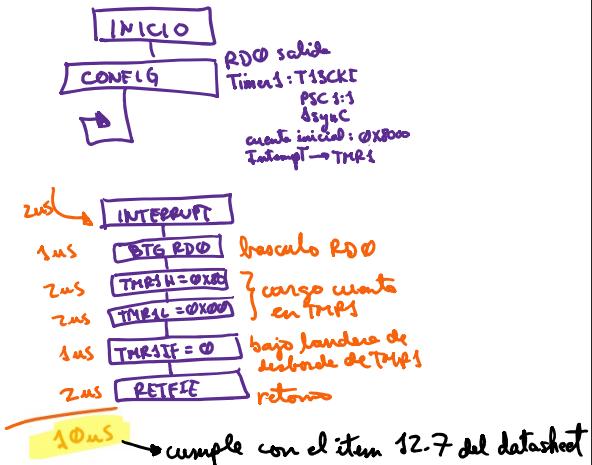


Diagrama de Flujo:



17

Ejemplo 1: Obtener una señal de reloj de 1Hz empleando el Timer1 en modo RTC.

- Configuración de TMR1
(registro T1CON)

$\textcircled{0} \times 07$
 07H

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER							
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
bit 7	bit 6	bit 5-4	bit 3	bit 2	bit 1	bit 0	
T1CON: Timer1 Control Register							
Legend: R = Readable bit W = Writable bit -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown							
bit 7: RD16: 16-Bit Read/Write Mode Enable bit 0 = Enables register read/write of Timer1 in one 16-bit operation 1 = Enables register read/write of Timer1 in two 8-bit operations	bit 6: T1RUN: Timer1 System Clock Status bit 0 = Device clock is derived from Timer1 oscillator 1 = Device clock is derived from another source	bit 5-4: T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits 11 = 1:8 Prescale value 10 = 1:4 Prescale value 01 = 1:2 Prescale value 00 = 1:1 Prescale value	bit 3: T1OSCEN: Timer1 Oscillator Enable bit 0 = Timer1 oscillator is enabled 1 = Timer1 oscillator is shut off The oscillator inverter and feedback resistor are turned off to eliminate power drain.	bit 2: T1SYNC: Timer1 External Clock Input Synchronization Select bit When TMR1CS = 1: 0 = Do not synchronize external clock input 1 = Synchronize external clock input When TMR1CS = 0: This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.	bit 1: TMR1CS: Timer1 Clock Source Select bit 0 = Internal clock (Fosc/4) 1 = External clock from RCO/T1OSC/T13CKI pin (on the rising edge)	bit 0: TMR1ON: Timer1 On bit 1 = Enables Timer1 0 = Stops Timer1	

18

Ejemplo 1: Obtener una señal de reloj de 1Hz empleando el Timer1 en modo RTC.

- Configuración de la interrupción del TMR1 (TMR1IF se encuentra en PIR1)

REGISTER 9-1: INTCON: INTERRUPT CONTROL REGISTER							
R/W-A	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-A	R/W-0
GIE/H	PEIESEL	TMR0IE	INSE	SB	TMR0IF	TOIE	RFIF
bit 7	1	1	0	0	0	0	0
Legend:	R = Readable bit -n = Value at POR	W = Writable bit '1' = Bit is set	U = Unimplemented bit, read as '0'	0 = Bit is cleared	x = Bit is unknown		
bit 7	GIIE/GIEH: Global Interrupt Enable bit When IPEN=0: 1 = Enables all unmasks interrupts 0 = Disables all interrupts When IPEN=1: 1 = Enables all high-priority interrupts 0 = Disables all interrupts	PIE1IE: Peripheral Interrupt Enable bit When IPEN=0: 1 = Enables all unmasks peripheral interrupts 0 = Disables all peripheral interrupts When IPEN=1: 1 = Enables all low-priority peripheral interrupts (if GIE/GIEH = 1) 0 = Disables all low-priority peripheral interrupts	INTCON: 0x C0				
bit 6	PIE1IE: Peripheral Interrupt Enable bit When IPEN=0: 1 = Enables all unmasks peripheral interrupts 0 = Disables all peripheral interrupts When IPEN=1: 1 = Enables all low-priority peripheral interrupts (if GIE/GIEH = 1) 0 = Disables all low-priority peripheral interrupts	TMR0IE: TMR0 Overflow Interrupt Enable bit 1 = Enables the TMR0 overflow interrupt 0 = Disables the TMR0 overflow interrupt					
bit 5	INT0IE: INT0 External Interrupt Enable bit 1 = Enables the INT0 external interrupt 0 = Disables the INT0 external interrupt	INT0IF: INT0 External Interrupt Flag bit 1 = The INT0 external interrupt occurred (must be cleared in software) 0 = The INT0 external interrupt did not occur					
bit 4	RBIE: RB Port Change Interrupt Enable bit 1 = Enables the RB port change interrupt 0 = Disables the RB port change interrupt	RBIF: RB Port Change Interrupt Flag bit 1 = The RB port change interrupt occurred (must be cleared in software) 0 = The RB port change interrupt did not occur					
bit 3							
bit 2							
bit 1							
bit 0							

REGISTER 9-6: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1							
R/W-A	R/W-0	R/W-0	R/W-A	R/W-A	R/W-A	R/W-A	R/W-0
SPPIE	ADIE	P0IE	TXIE	SPIE	CCP1IE	TMRIE	TMR1IE
bit 7	0	0	0	0	0	0	1
Legend:	R = Readable bit -n = Value at POR	W = Writable bit '1' = Bit is set	U = Unimplemented bit, read as '0'	0 = Bit is cleared	x = Bit is unknown		
bit 7	SPPIE: Streaming Parallel Port Read/Write Interrupt Enable bit ⁽¹⁾ 1 = Enables the SPP read/write interrupt 0 = Disables the SPP read/write interrupt	ADIE: A/D Converter Interrupt Enable bit 1 = Enables the A/D interrupt 0 = Disables the A/D interrupt					
bit 6		RCIE: USART Receive Interrupt Enable bit 1 = Enables the USART receive interrupt 0 = Disables the USART receive interrupt					
bit 5		TXIE: USART Transmit Interrupt Enable bit 1 = Enables the USART transmit interrupt 0 = Disables the USART transmit interrupt					
bit 4		SSPIE: Master Synchronous Serial Port Interrupt Enable bit 1 = Enables the MSSP interrupt 0 = Disables the MSSP interrupt					
bit 3		CCP1IE: CCP1 Interrupt Enable bit 1 = Enables the CCP1 interrupt 0 = Disables the CCP1 interrupt					
bit 2							
bit 1		TMR2IE: TMR2 to PR2 Match Interrupt Enable bit 1 = Enables the TMR2 to PR2 match interrupt 0 = Disables the TMR2 to PR2 match interrupt					
bit 0		TMR1IE: TMR1 Overflow Interrupt Enable bit 1 = Enables the TMR1 overflow interrupt 0 = Disables the TMR1 overflow interrupt					

19

Ejemplo 1: Obtener una señal de reloj de 1Hz empleando el Timer1 en modo RTC.

- Código en MPASM

```

17      org 0x0000
18      goto init_conf
19
20      org 0x0008
21      goto TMRI_ISR
22
23      ;Aqui se pueden declarar las constantes en la memoria de programa
24
25      org 0x0020
26      init_conf:
27          bcf TRISD, 0      ;RD0 como salida
28          movlw 0x07
29          movwf TICON       ;TMRI on, 1:1PSC, T13CKI
30          movlw 0x01
31          movwf PIE1         ;Interrupcion de TMRI habilitado
32          movlw 0xC0
33          movwf INTCON       ;Interrupciones habilitadas (globales y de perifericos)
34
35      loop:
36          nop
37          goto loop
38
39      TMRI_ISR:
40          btg LATD, 0      ;Basculo la salida RD0
41          movlw 0xC0
42          movwf TMRIH
43          clrf TMRL        ;Cargo 49152 como cuenta inicial
44          bcf PIR1, TMRIIF   ;Bajo la bandera de desborde de TMRI
45          retfie
46          end

```

20

Ejemplo 1: Obtener una señal de reloj de 1Hz empleando el Timer1 en modo RTC.

- Código en XC8 PIC Assembler
- Empleando RD7 como salida de señal.
- Opción para implementación física (líneas 21-22)
- La basculación la está haciendo a 1Hz, si se requiere obtener una señal de reloj se deberá de disminuir la cantidad de cuentas a contar de 16384 en el Timer1 (cuenta inicial de 49152 en TMR1H:TMR1L, líneas 33-35).

```

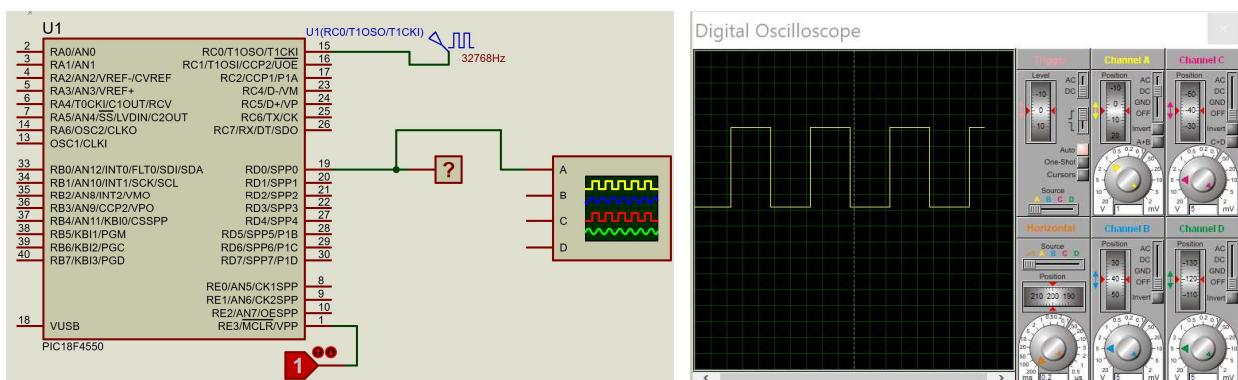
4      PROCESSOR 10f4550
5      #include "cabecera.inc"
6
7      FSECT erretece,class=CODE,reloc=2,abs
8
9      ORG 00000H          ;Vector de reset
10     erretece:    goto configuracion
11
12     ORG 00008H          ;Vector de interrupcion
13     vector_hp:   goto TMRL_ISR
14
15     ORG 00020H
16     configuracion:
17         bcf TRISD, 7      ;RD7 como salida
18         movlw 07H
19         movwf T1CON        ;Tmrl ON, PSC 1:1, T13CKI (T1OSCEN=0) sin cristal para Proteus
20         movlw 0FH
21         ;      movwf T1CON        ;Tmrl ON, PSC 1:1, XTAL32K (T1OSCEN=1) con cristal 32K
22         ;      movlw 01H
23         ;      movwf PIE1        ;TMRIIE=1
24         ;      movlw 0C0H
25         ;      movwf INTCON       ;GIE=1, PEIE=1
26
27     loop:
28         nop
29         goto loop
30
31     TMRL_ISR:
32         btg LATD, 7      ;Basculando RD7
33         movlw 080H
34         movwf TMR1H
35         clrf TMR1L        ;49152 ;32768
36         bcf PIR1, 0
37         retfie
38     end erretece

```

21

Ejemplo 1: Obtener una señal de reloj de 1Hz empleando el Timer1 en modo RTC.

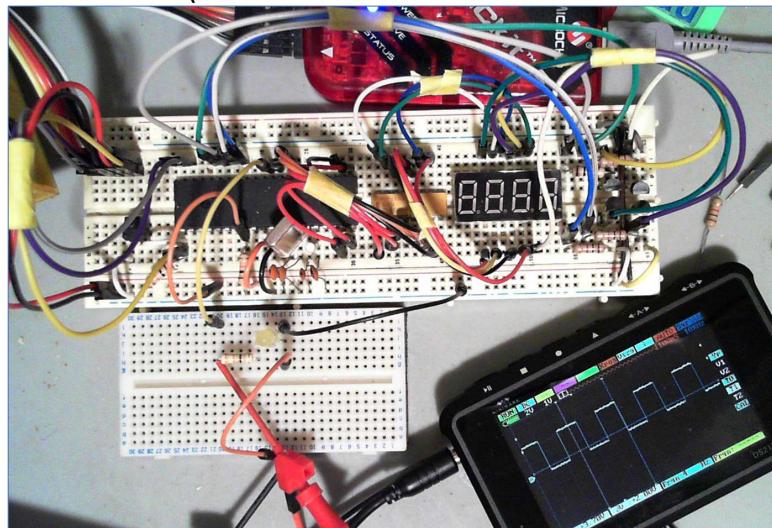
- Simulación



22

Ejemplo 1: Obtener una señal de reloj de 1Hz empleando el Timer1 en modo RTC.

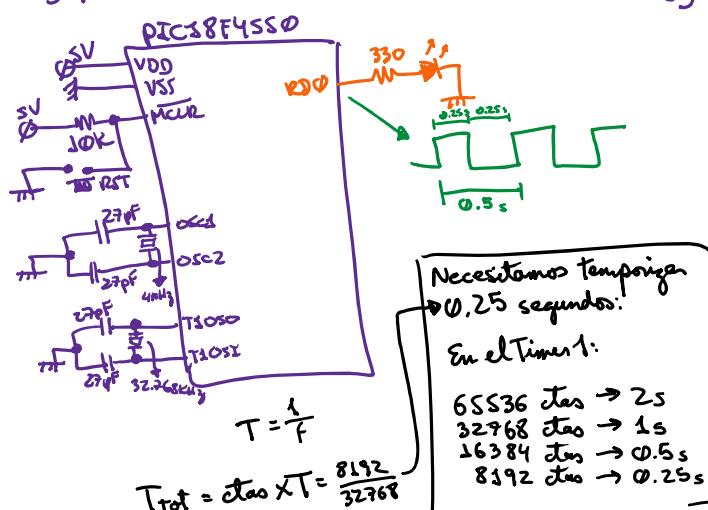
- Implementación (mostrando señal de 4Hz – cuenta inicial E000H)



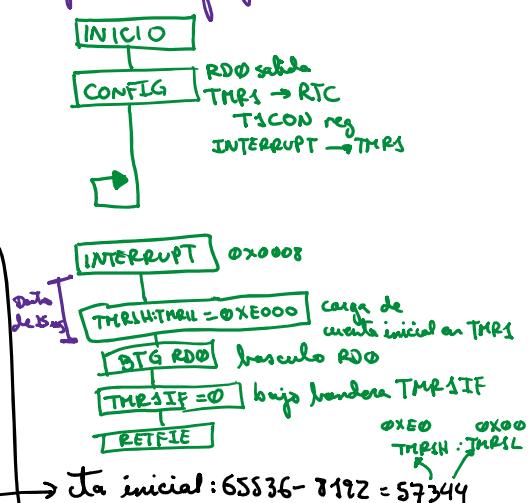
23

Ejemplo 2: Desarrollar un titileo de LED con periodo de 0.5s (RTC) empleando TMR1

a) Hardware

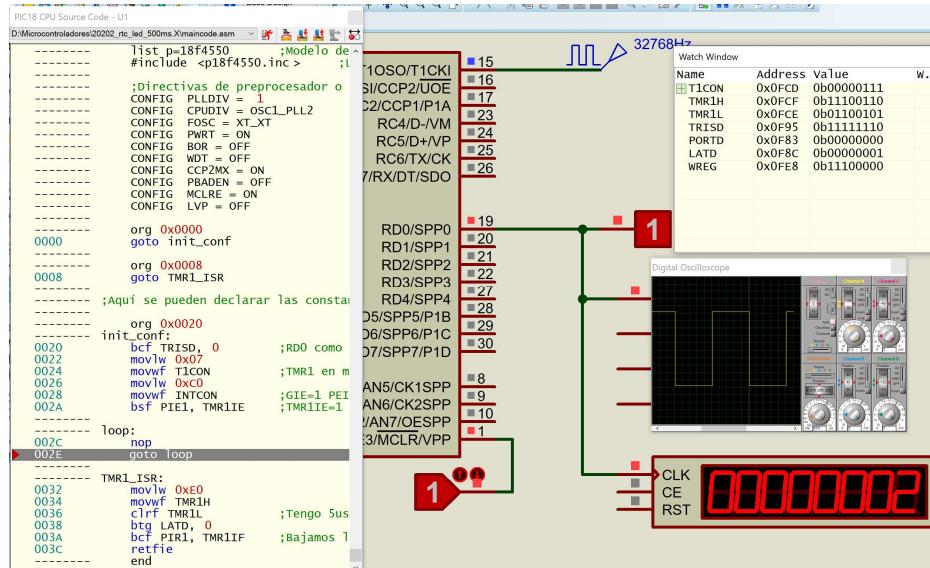


b) Diagrama de flujo:



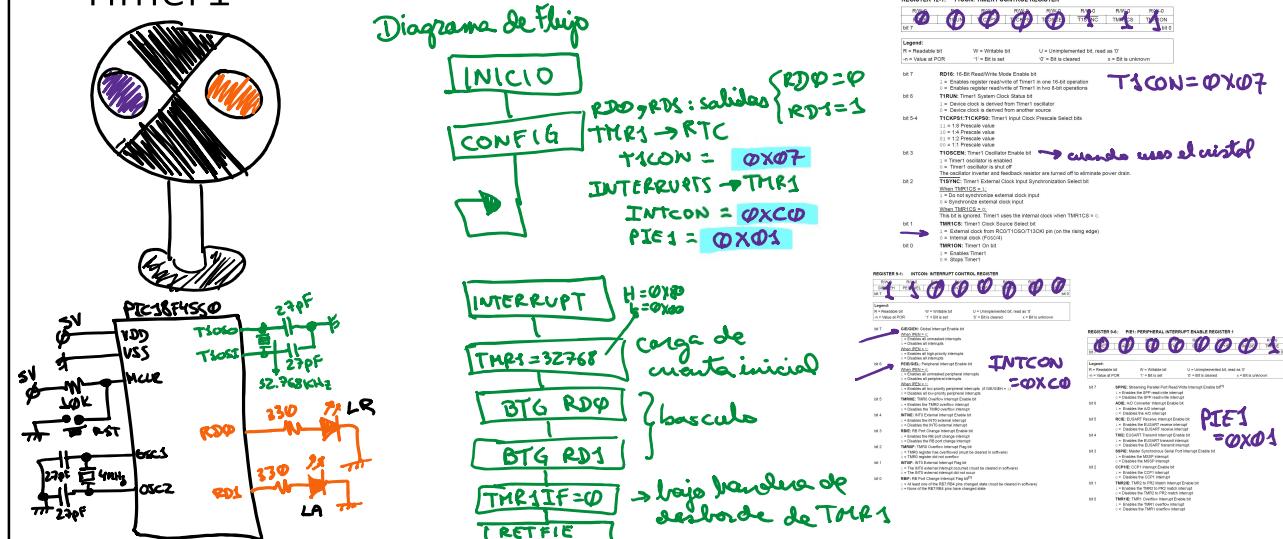
24

Ejemplo 2: Desarrollar un titileo de LED con periodo de 0.5s (RTC) empleando TMR1



25

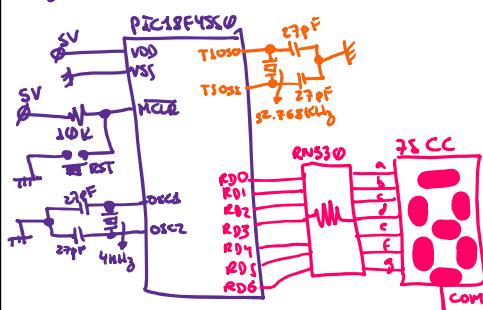
Ejemplo 3: Desarrollar una señal de tren con periodo de alternancia de 1s (RTC) empleando Timer1



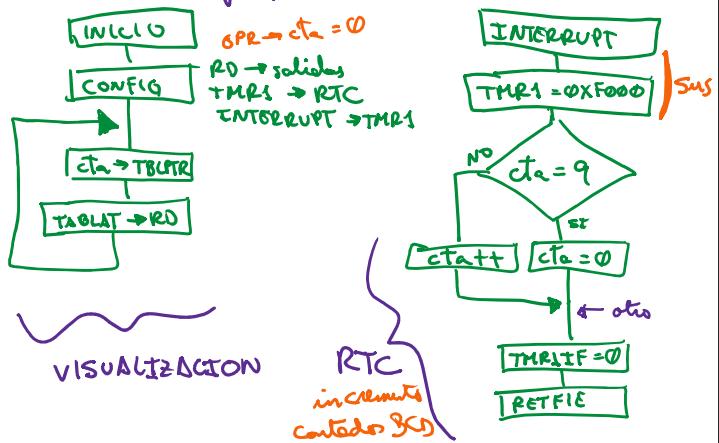
26

Ejemplo 4: Desarrollar un contador BCD (0-9) con periodo de cuenta de 0.125segundos

a) Hardware:



b) Diagrama de flujo



27

Ejemplo 4: Desarrollar un contador BCD (0-9) con periodo de cuenta de 0.125segundos

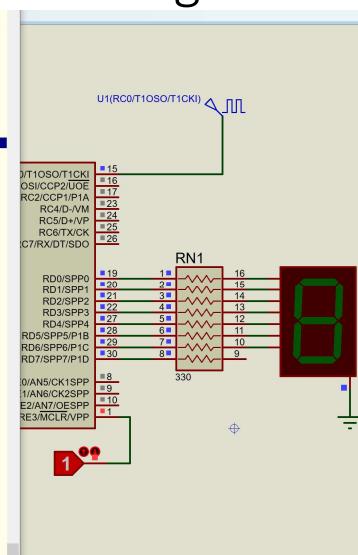
```

----- org 0x400
0400 tabla_7s db 0xBF, 0x86, 0xDB, 0xCF, 0xE6, 0xED, 0xFD, 0x87, 0xFF, 0xE
----- ;Aqui va el cblock o declaracion de nombres de GPR
        cblock 0x000
-----         cta
        endc
----- org 0x0000
0000     goto init_conf
----- org 0x0008
0008     goto TMRL1_ISR
----- ;Aqui se pueden declarar las constantes en la memoria de programa
----- org 0x0020
----- init_conf:
0020     movlw TRISD ;RD como salidas para manejar el display
0022     movlw 0x07
0024     movlw 0x00
0026     movlw 0xC0 ;GIE=1 y PEIE=1
0028     movwf INTCON
002A     movlw 0x01
002C     movwf PIR1 ;TMRL1IE=1
002E     movlw HIGH tabla_7s
0030     movwf TBLPTRH
0032     movlw LOW tabla_7s
0034     movwf TBLPTRL ;TBLPTR apuntando a 0x0400

----- loop:
0036     movf cta, W
0038     movwf TABLPTRL
003A     TABLPRD
003C     movff TABLAT, LATD
0040     goto loop

----- TMRL1_ISR:
0044     movlw 0xF0
0046     movwf TMRL1H ;Carga cuenta inicial en TMRL1
0048     clrf TMRL1L
004A     movf cta, W
004C     cpfsq cta
004E     goto noescierto
0052     clrf cta
0054     goto otro
0056     noescierto:
0058     incf cta, F
005A     otro:
005B     lcf PIR1, TMRL1IF
005C     retfie
----- end

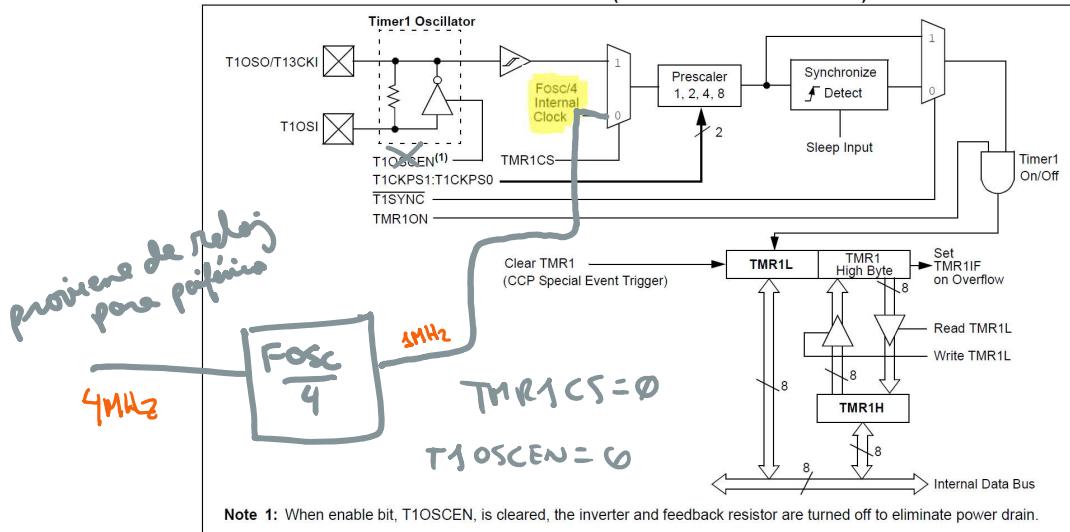
```



28

Opción 2: Usando fuente de reloj principal del microcontrolador Fosc/4

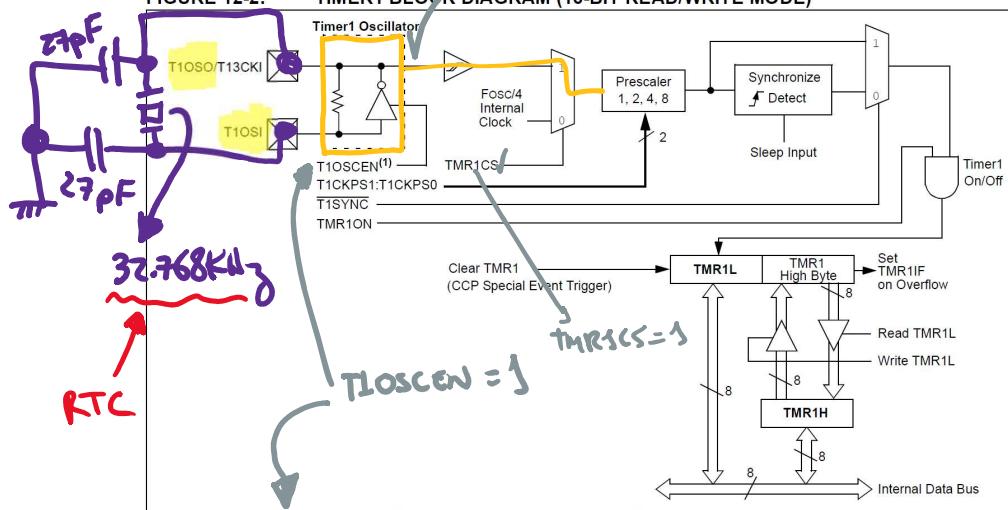
FIGURE 12-2: TIMER1 BLOCK DIAGRAM (16-BIT READ/WRITE MODE)



29

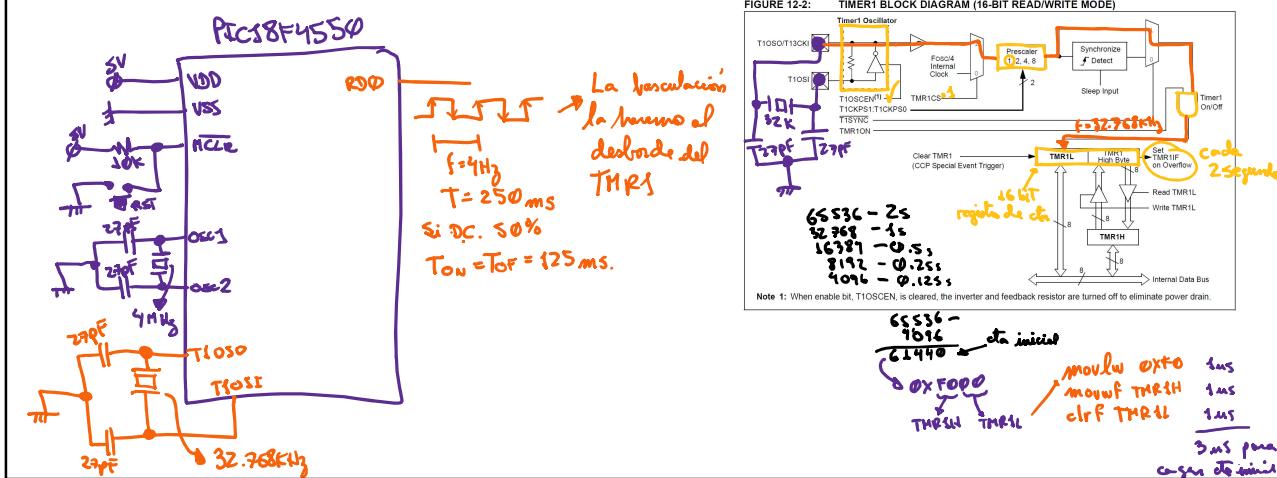
Opción 3: Empleando cristal de cuarzo de 32.768KHz

FIGURE 12-2: TIMER1 BLOCK DIAGRAM (16-BIT READ/WRITE MODE)



30

Ejemplo 5: El Timer 1 configurado como RTC y empleando el cristal 32K para generar una señal cuadrada de 4Hz a través de RDO



31

(cont...)

- Configuración del Timer1

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER							
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RW0	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON
bit 7							bit 0
Legend:							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				
bit 7	RD16: 16-Bit Read/Write Mode Enable bit						
	1 = Enables register read/write of Timer1 in one 16-bit operation	0 = Enables register read/write of Timer1 in two 8-bit operations					
bit 6	T1RUN: Timer1 System Clock Status bit						
	1 = Device clock is derived from Timer1 oscillator	0 = Device clock is derived from another source					
bit 5-4	T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits						
11	= 1:8 Prescale value						
10	= 1:4 Prescale value						
01	= 1:2 Prescale value						
00	= 1:1 Prescale value						
bit 3	T1OSCEN: Timer1 Oscillator Enable bit						
1	= Timer1 oscillator is enabled						
0	= Timer1 oscillator is shut off						
	The oscillator inverter and feedback resistor are turned off to eliminate power drain.						
bit 2	T1SYNC: Timer1 External Clock Input Synchronization Select bit						
When TMR1CS = 1:	1 = Do not synchronize external clock input						
	0 = Synchronize external clock input						
When TMR1CS = 0:	This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.						
bit 1	TMR1CS: Timer1 Clock Source Select bit						
1	= External clock from RC0/T1OSO/T13CKI pin (on the rising edge)						
0	= Internal clock (Fosc/4)						
bit 0	TMR1ON: Timer1 On bit						
1	= Enables Timer1						
0	= Stops Timer1						

32

(cont...)

- Configuración de las interrupciones con el Timer1

REGISTER 9-4: PIR1: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1							
R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPIPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7							b7D
Legend:	R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR	-1 = Bit is set '0' = Bit is cleared x = Bit is unknown					
bit 7	SPIPIF: Streaming Parallel Port Read/Write Interrupt Flag bit ⁽¹⁾	1 = A read or a write operation has taken place (must be cleared in software) 0 = No read or write has occurred					
bit 6	ADIF: A/D Converter interrupt Flag bit	1 = An A/D conversion completed (must be cleared in software) 0 = No A/D conversion completed					
bit 5	RCIF: USART Receive Interrupt Flag bit	1 = The USART receive buffer, RCREG, is full (cleared when RCREG is read) 0 = The USART receive buffer is empty					
bit 4	TXIF: USART Transmit Interrupt Flag bit	1 = The USART transmit buffer, TXREG, is empty (cleared when TXREG is written) 0 = The USART transmit buffer is full					
bit 3	SSPIF: Master Synchronous Serial Port Interrupt Flag bit	1 = The transmission/reception is complete (must be cleared in software) 0 = Waiting to transmit/receive					
bit 2	CAPTURE: Capture interrupt Flag bit	Capture mode: 1 = A TMR1 register capture occurred (must be cleared in software) 0 = No TMR1 register capture occurred					
bit 1	COMPARE: Compare interrupt Flag bit	Compare mode: 1 = A TMR1 register compare match occurred (must be cleared in software) 0 = No TMR1 register compare match occurred					
bit 0	UNDEF: undefined in this mode						
	TMR2IF: TMR2 to PR2 Match Interrupt Flag bit	1 = TMR2 to PR2 match occurred (must be cleared in software) 0 = TMR2 register overflowed (must be cleared in software)					
	TMR1IF: TMR1 Overflow Interrupt Flag bit	1 = TMR1 register overflowed (must be cleared in software) 0 = TMR1 register did not overflow					

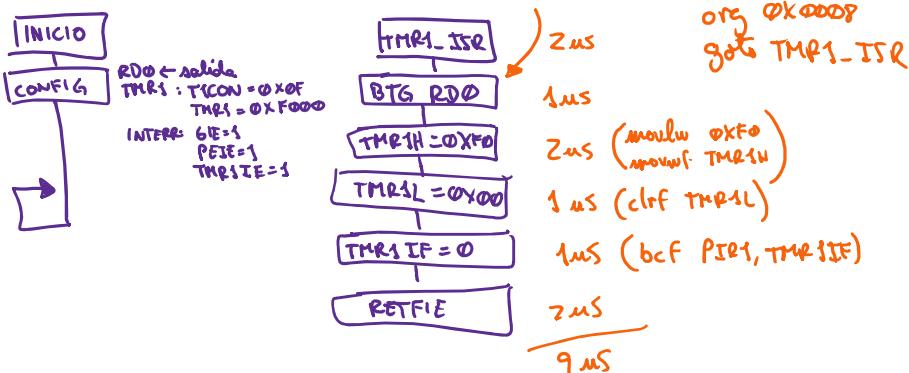
REGISTER 9-6: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPIPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit 7							b7D
Legend:	R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR	-1 = Bit is set '0' = Bit is cleared x = Bit is unknown					
bit 7	SPIPIE: Streaming Parallel Port Read/Write Interrupt Enable bit ⁽¹⁾	1 = Enables the SPIP read/write interrupt 0 = Disables the SPIP read/write interrupt					
bit 6	ADIE: A/D Converter Interrupt Enable bit	1 = Enables the A/D converter interrupt 0 = Disables the A/D converter interrupt					
bit 5	RCIE: USART Receive Interrupt Enable bit	1 = Enables the USART receive interrupt 0 = Disables the USART receive interrupt					
bit 4	TXIE: USART Transmit Interrupt Enable bit	1 = Enables the USART transmit interrupt 0 = Disables the USART transmit interrupt					
bit 3	SSPIE: Master Synchronous Serial Port Interrupt Enable bit	1 = Enables the MSSP interrupt 0 = Disables the MSSP interrupt					
bit 2	CAPPIE: CCP1 Interrupt Enable bit	1 = Enables the CCP1 interrupt 0 = Disables the CCP1 interrupt					
bit 1	TMR2IE: TMR2 to PR2 Match Interrupt Enable bit	1 = Enables the TMR2 to PR2 match interrupt 0 = Disables the TMR2 to PR2 match interrupt					
bit 0	TMR1IE: TMR1 Overflow Interrupt Enable bit	1 = Enables the TMR1 overflow interrupt 0 = Disables the TMR1 overflow interrupt					

REGISTER 9-1: INCON: INTERRUPT CONTROL REGISTER							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE/GIEH	PEIE/PEIEL	TMR0IE	INT0IE	R0IE	TMR0IF	INT0IF	R0IF ⁽¹⁾
bit 7							
Legend:	R = Readable bit W = Writable bit -n = Value at POR	-1 = Bit is set '0' = Bit is cleared x = Bit is unknown					
bit 7	GIE/GIEH: Global Interrupt Enable bit When IPEN = 0:	1 = Enables all unmasked interrupts 0 = Disables all interrupts					
bit 6	PEIE/PEIEL: Peripheral Interrupt Enable bit When IPEN = 1:	1 = Enables all unmasked peripheral interrupts 0 = Disables all peripheral interrupts					
bit 5	TMR0IE: TMR0 Overflow Interrupt Enable bit When IPEN = 1:	1 = Enables all low-priority peripheral interrupts (if GIE/GIEH = 1) 0 = Disables all low-priority peripheral interrupts					
bit 4	INT0IE: INT0 External Interrupt Enable bit	1 = Enables the INT0 external interrupt 0 = Disables the INT0 external interrupt					
bit 3	R0IE: RB Port Change Interrupt Enable bit	1 = Enables the RB port change interrupt 0 = Disables the RB port change interrupt					
bit 2	TMR0IF: TMR0 Overflow Interrupt Flag bit	1 = TMR0 register has overflowed (must be cleared in software) 0 = TMR0 register did not overflow					
bit 1	INT0IF: INT0 External Interrupt Flag bit	1 = The INT0 external interrupt was detected (must be cleared in software) 0 = The INT0 external interrupt did not occur					
bit 0	R0IF: RB Port Change Interrupt Flag bit ⁽¹⁾	1 = At least one of the RB7/RB4 pins changed state (must be cleared in software) 0 = None of the RB7/RB4 pins have changed state					

33

(cont...)

- Algoritmo en diagrama de flujo del ejemplo



(cont...)

- Código en MPASM

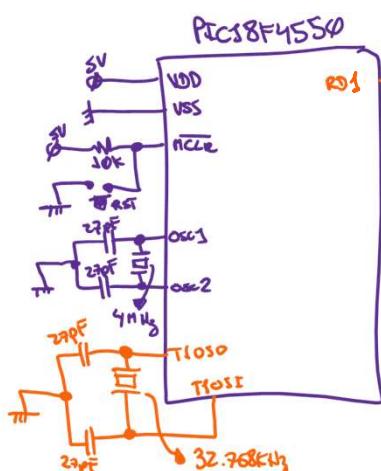
```

17      org 0x0000      ;vector de reset
18      goto init_conf
19
20      org 0x0008      ;vector de interrupcion
21      goto TMR1_ISR
22
23  init_conf: bcf TRISD, 0
24      movlw 0x0F
25      movwf T1CON
26      movlw 0x80
27      movwf TMR1H
28      clrf TMR1L
29      bsf INTCON, GIE
30      bsf INTCON, PEIE
31      bsf PIE1, TMR1IE
32
33  loop:   nop
34      goto loop
35
36  TMR1_ISR: btg LATD, 0
37      movlw 0x80
38      movwf TMR1H
39      clrf TMR1L
40      bcf PIR1, TMR1IF
41      retfie
42      end

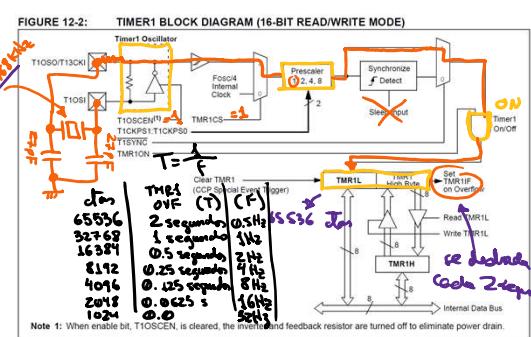
```

35

Ejemplo 6: Generar una onda cuadrada de 16Hz exactos a través del puerto RD1 empleando el Timer1 en RTC



Debo de los pulsos RD1 a 32Hz para cumplir con la frecuencia solicitada de la onda cuadrada.



cuenta inicial:

$$\frac{65536 - 1024}{64512} = 0x\text{FC00}$$

36

(cont...)

• Configuración del Timer1

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER							
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	T1RUN	T1CKPS	T1CKPS0	T1OCEN	T1ONC	TM1CS	TMR1ON
bit 7							
Legend:							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared					
							x = Bit is unknown
bit 7	RD16: 16-Bit Read/Write Mode Enable bit						
	1 = Enables register read/write of Timer1 in one 16-bit operation						
	0 = Enables register read/write of Timer1 in two 8-bit operations						
bit 6	T1RUN: Timer1 System Clock Status bit						
	1 = Device clock is derived from Timer1 oscillator						
	0 = Device clock is derived from another source						
bit 5-4	T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits						
	11 = 1:8 Prescale value						
	10 = 1:4 Prescale value						
	01 = 1:2 Prescale value						
	00 = 1:1 Prescale value ✓						
bit 3	T1OSCEN: Timer1 Oscillator Enable bit						
	1 = Timer1 oscillator is enabled						
	0 = Timer1 oscillator is shut off						
	The oscillator inverter and feedback resistor are turned off to eliminate power drain.						
bit 2	T1SYNC: Timer1 External Clock Input Synchronization Select bit						
	When TMR1CS = 1:						
	1 = Do not synchronize external clock input ✓						
	0 = Synchronize external clock input ✓						
	When TMR1CS = 0:						
	This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.						
bit 1	TMR1CS: Timer1 Clock Source Select bit						
	1 = External clock from RC0/T1SO/T1CKI pin (on the rising edge) ✓						
	0 = Internal clock (Fosc/4)						
bit 0	TMR1ON: Timer1 On bit						
	1 = Enables Timer1 ✓						
	0 = Stops Timer1						

37

(cont...)

• Configuración de las interrupciones con el Timer1

REGISTER 9-4: PIR1: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1							
R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPIPI(R1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7							
Legend:							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared					x = Bit is unknown
bit 7	SPIPI: Streaming Parallel Port Read/Write Interrupt Flag bit ¹						
	1 = A read or a write operation has taken place (must be cleared in software)						
	0 = No read or write has occurred						
bit 6	ADIF: ADC Interrupt Flag bit						
	1 = The A/D conversion complete (must be cleared in software)						
	0 = The A/D conversion is not complete						
bit 5	RCIF: USART Receive Interrupt Flag bit						
	1 = The USART receive buffer, RCREG, is full (cleared when RCREG is read)						
	0 = No USART receive interrupt						
bit 4	TXIF: USART Transmit Interrupt Flag bit						
	1 = The USART transmit buffer, TXREG, is empty (cleared when TXREG is written)						
	0 = The USART transmit buffer is full						
bit 3	SSPIF: Master Synchronous Serial Port Interrupt Flag bit						
	1 = The master synchronous serial port receive complete (must be cleared in software)						
	0 = Waiting to transmit/receive ²						
bit 2	CCP1IF: CCP1 Interrupt Flag bit						
	Capture mode:						
	1 = A CCP1 register capture occurred (must be cleared in software)						
	0 = No CCP1 register capture occurred						
	Compare mode:						
	1 = A CCP1 register compare match occurred (must be cleared in software)						
	0 = No CCP1 register compare match occurred						
	PWM mode:						
	Unused in this mode.						
bit 1	TMR2IF: TMR1 to PR2 Match Interrupt Flag bit						
	1 = A TMR2 register match occurred (must be cleared in software)						
	0 = No TMR2 to PR2 match occurred						
bit 0	TMR1IF: TMR1 Overflow Interrupt Flag bit						
	1 = TMR1 register overflowed (must be cleared in software)						
	0 = TMR1 register did not overflow						

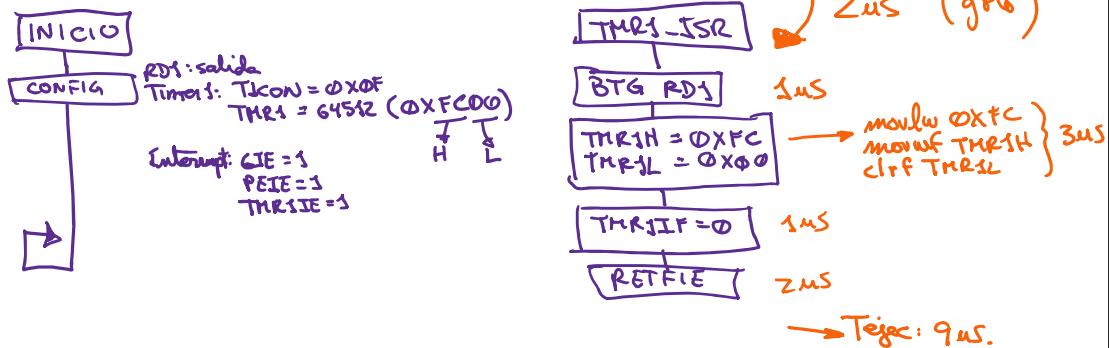
REGISTER 9-5: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPIPE(R1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit 7							
Legend:							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared					x = Bit is unknown
bit 7	SPIPE: Streaming Parallel Port Read/Write Interrupt Enable bit ¹						
	1 = Enables the SPIP interrupt						
	0 = Disables the SPIP read/write interrupt						
bit 6	ADIE: A/D Converter Interrupt Enable bit						
	1 = Enables the A/D interrupt						
	0 = Disables the A/D interrupt						
bit 5	RCIE: USART Receive Interrupt Enable bit						
	1 = Enables the USART receive interrupt						
	0 = Disables the USART receive interrupt						
bit 4	TXIE: USART Transmit Interrupt Enable bit						
	1 = Enables the USART transmit interrupt						
	0 = Disables the USART transmit interrupt						
bit 3	SPIE: Master Synchronous Serial Port Interrupt Enable bit						
	1 = Enables the MSSP interrupt						
	0 = Disables the MSSP interrupt						
bit 2	CCP1IE: CCP1 Interrupt Enable bit						
	1 = Enables the CCP1 interrupt						
	0 = Disables the CCP1 interrupt						
bit 1	TMR2IE: TMR2 to PR2 Match Interrupt Enable bit						
	1 = Enables the TMR2 to PR2 match interrupt						
	0 = Disables the TMR2 to PR2 match interrupt						
bit 0	TMR1IE: TMR1 Overflow Interrupt Enable bit						
	1 = Enables the TMR1 overflow interrupt						
	0 = Disables the TMR1 overflow interrupt						

REGISTER 9-6: INTC1: INTERRUPT CONTROL REGISTER							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GIE/GIEH	PEIE/PEIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF ¹
bit 7							
Legend:							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared					x = Bit is unknown
bit 7	GIE/GIEH: Global Interrupt Enable bit						
	When IPEN = 0:						
	1 = Enables all unmasked interrupts						
	0 = Disables all interrupts						
bit 6	PEIE/PEIEL: Peripheral Interrupt Enable bit						
	When IPEN = 1:						
	1 = Enables all peripheral interrupts						
	0 = Disables all peripheral interrupts						
bit 5	TMR0IE: TMR0 Overflow Interrupt Enable bit						
	1 = Enables the TMR0 overflow interrupt						
	0 = Disables the TMR0 overflow interrupt						
bit 4	INT0IE: INT0 External Interrupt Enable bit						
	1 = Enables the INT0 external interrupt						
	0 = Disables the INT0 external interrupt						
bit 3	RBIE: RB Change Interrupt Enable bit						
	1 = Enables the RB change interrupt						
	0 = Disables the RB port change interrupt						
bit 2	TMR0IF: TMR0 Overflow Interrupt Flag bit						
	1 = TMR0 register has overflowed (must be cleared in software)						
	0 = TMR0 register did not overflow						
bit 1	INT0IF: INT0 External Interrupt Flag bit						
	1 = The INT0 external interrupt occurred (must be cleared in software)						
	0 = The INT0 external interrupt did not occur						
bit 0	RBIF: RB Port Change Interrupt Flag bit ¹						
	1 = At least one of the RB7/RB4 pins changed state (must be cleared in software)						
	0 = None of the RB7/RB4 pins have changed state						

38

(cont...)

- Algoritmo en diagrama de flujo



39

(cont...)

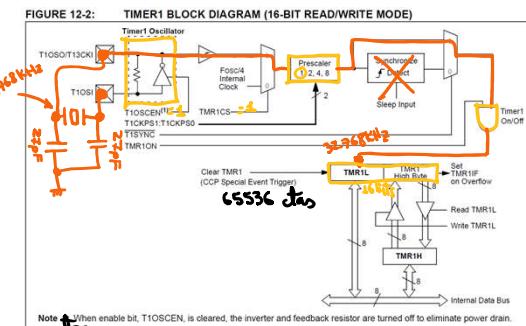
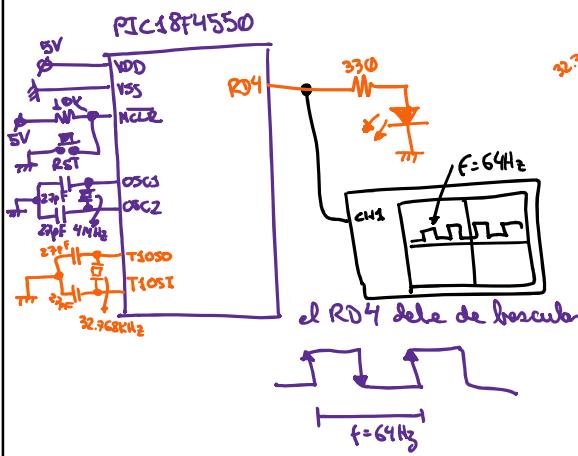
- Código en MPASM

```

2      list p=18f4550      ;Modelo del microcontrolador
3      #include <p18f4550.inc>      ;Llamada a la librería
4
5      ;Directivas de preprocesador o bits de configuración
6      CONFIG PLLDIV = 1          ; PLL Prescaler
7      CONFIG CFUDIV = OSC1_FLL2 ; System Clock
8      CONFIG FOSC = XT_XT       ; Oscillator
9      CONFIG FWRT = ON          ; Power-up Timer
10     CONFIG BOR = OFF          ; Brown-out Reset
11     CONFIG WDT = OFF          ; Watchdog Timer
12     CONFIG CCP2MX = ON         ; CCP2 MUX bit
13     CONFIG PBADEN = OFF        ; PORTB A/D Enable
14     CONFIG MC1RRE = ON         ; MCLR Pin Enable
15     CONFIG LVP = OFF          ; Single-Supply
16
17     org 0x0000                ;vector de reset
18     goto init_conf
19
20     org 0x0008                ;vector de interrupción
21     goto TMRI_ISR
22
23     init_conf:
24     bcf TRISD, 1
25     movlw 0x0F
26     movwf T1CON
27     movlw 0xFC
28     movwf TMR1H
29     clrf TMR1L
30     bsf INTCON, GIE
31     bsf INTCON, PEIE
32     bsf PIE1, TMRIIE
33
34     loop:    nop
35     goto loop
36
37     TMRI_ISR:   btg LATD, 1
38     movlw 0xFC
39     movwf TMR1H
40     bcf PIR1, TMRIIF
41     retfie
42     end
  
```

40

Ejemplo 7: Generar una señal cuadrada de 64Hz exactos a través del puerto RD4 y empleando el Timer1 en RTC



Note: When enable bit, T1OSCEN, is cleared, the inverter and feedback resistor are turned off to eliminate power drain.

$65536 \rightarrow 25\text{seg.} \rightarrow 0.5\text{Hz}$
 $32768 \rightarrow 1\text{seg.} \rightarrow 1\text{Hz}$
 $16384 \rightarrow 0.5\text{seg.} \rightarrow 2\text{Hz}$
 $8192 \rightarrow 0.25\text{seg.} \rightarrow 4\text{Hz}$
 $4096 \rightarrow 0.125\text{seg.} \rightarrow 8\text{Hz}$
 $2048 \rightarrow 0.0625\text{seg.} \rightarrow 16\text{Hz}$
 $1024 \rightarrow ? \rightarrow 32\text{Hz}$
 $512 \rightarrow ? \rightarrow 64\text{Hz}$
 $256 \rightarrow ? \rightarrow 128\text{Hz}$

$\frac{65536}{256} = 256$ cuenta inicial
 $0xFF00 \leftarrow TMR1L$
 $TMR1H$

41

(cont...)

- Configuración del Timer1

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER							
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	T1RUN	T1CKPS	TICKPS0	T1OSCEN	T1OSCNC	TMR1CS	TMR1ON
bit 7	RD16: 16-Bit Read/Write Mode Enable bit 1 = Enables register read/write of Timer1 in one 16-bit operation 0 = Enables register read/write of Timer1 in two 8-bit operations						
bit 6	T1RUN: Timer1 System Clock Status bit 1 = Device clock is derived from Timer1 oscillator 0 = Device clock is derived from another source						
bit 5-4	T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits 11 = 1:8 Prescale value 10 = 1:4 Prescale value 01 = 1:2 Prescale value 00 = 1:1 Prescale value						
bit 3	T1OSCEN: Timer1 Oscillator Enable bit 1 = Timer1 oscillator is enabled 0 = Timer1 oscillator is shut off The oscillator inverter and feedback resistor are turned off to eliminate power drain.						
bit 2	T1OSCNC: Timer1 External Clock Input Synchronization Select bit When TMR1CS = 1: 1 = Do not synchronize external clock input 0 = Synchronize external clock input When TMR1CS = 0: This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.						
bit 1	TMR1CS: Timer1 Clock Source Select bit 1 = External clock from RC0/T1OSO/T13CKI pin (on the rising edge) 0 = Internal clock (Fosc/4)						
bit 0	TMR1ON: Timer1 On bit 1 = Enables Timer1 0 = Stops Timer1						

42

(cont...)

- Configuración de las interrupciones con el Timer1

REGISTER 9-4: PIR1: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1							
R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
SPIPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7							b7D

Legend:
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 SPIPIF: Streaming Parallel Port Read/Write Interrupt Flag bit⁽¹⁾
1 = A read or a write operation has taken place (must be cleared in software)
0 = No read or write has occurred
ADIF: A/D Converter interrupt Flag bit
1 = An A/D conversion completed (must be cleared in software)
0 = No A/D conversion completed
bit 5 RCIF: USART Receive Interrupt Flag bit
1 = The USART receive buffer, RCREG, is full (cleared when RCREG is read)
0 = The USART receive buffer is empty
bit 4 TXIF: USART Transmit Interrupt Flag bit
1 = The USART transmit buffer, TXREG, is empty (cleared when TXREG is written)
0 = The USART transmit buffer is full
bit 3 SSPIF: Master Synchronous Serial Port Interrupt Flag bit
1 = The transmission/reception is complete (must be cleared in software)
0 = Waiting to transmit/receive
bit 2 CCP1IF: CCP1 interrupt Flag bit
Capture mode:
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare mode:
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
Overflow mode:
1 = TMR1 register overflowed (must be cleared in software)
0 = TMR1 register did not overflow
Unused in this mode:
TMR2IF: TMR2 to PR2 Match Interrupt Flag bit
1 = TMR2 to PR2 match occurred (must be cleared in software)
0 = TMR2 to PR2 match did not occur
TMR1IF: TMR1 Overflow Interrupt Flag bit
1 = TMR1 register overflowed (must be cleared in software)
0 = TMR1 register did not overflow

REGISTER 9-6: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPIPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit 7							b7D

Legend:
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 SPIPIE: Streaming Parallel Port Read/Write Interrupt Enable bit⁽¹⁾
1 = Enables the SPIP read/write interrupt
0 = Disables the SPIP read/write interrupt
bit 6 ADIE: A/D Converter Interrupt Enable bit
1 = Enables the A/D converter interrupt
0 = Disables the A/D interrupt
bit 5 RCIE: USART Receive Interrupt Enable bit
1 = Enables the USART receive interrupt
0 = Disables the USART receive interrupt
bit 4 TXIE: USART Transmit Interrupt Enable bit
1 = Enables the USART transmit interrupt
0 = Disables the USART transmit interrupt
bit 3 SSPIE: Master Synchronous Serial Port Interrupt Enable bit
1 = Enables the MSSPI interrupt
0 = Disables the MSSPI interrupt
bit 2 CCP1IE: CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt
bit 1 TMR2IE: TMR2 to PR2 Match Interrupt Enable bit
1 = Enables the TMR2 to PR2 match interrupt
0 = Disables the TMR2 to PR2 match interrupt
bit 0 TMR1IE: TMR1 Overflow Interrupt Enable bit
1 = Enables the TMR1 overflow interrupt
0 = Disables the TMR1 overflow interrupt

REGISTER 9-1: INCON: INTERRUPT CONTROL REGISTER							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE/GIEH	PIE1/GIEL	TMR0IE	INT0IE	RBIIE	TMR0IF	INT0IF	RBIIF ⁽¹⁾
bit 7							b7D

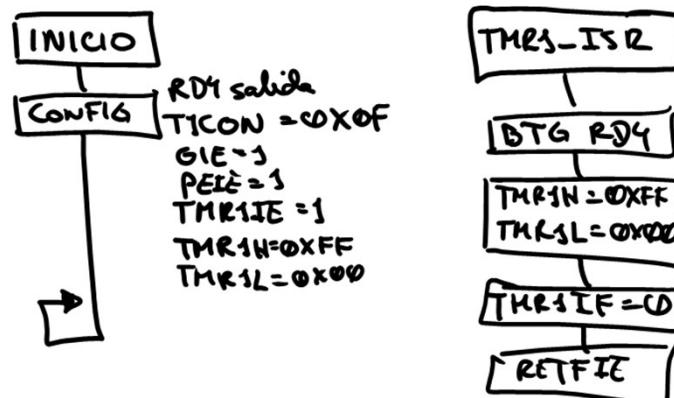
Legend:
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 GIE/GIEH: Global Interrupt Enable bit
When IPEN = 0:
1 = Enables all unmasked interrupts
0 = Disables all interrupts
When IPEN = 1:
1 = Enables all priority peripheral interrupts
0 = Disables all interrupts
PIE1/GIEL: Peripheral Interrupt Enable bit
When IPEN = 0:
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts
When IPEN = 1:
1 = Enables all priority peripheral interrupts (if GIE/GIEH = 1)
0 = Disables all low-priority peripheral interrupts
bit 6 TMR0IE: TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 overflow interrupt
0 = Disables the TMR0 overflow interrupt
INT0IE: INT0 External Interrupt Enable bit
1 = Enables the INT0 external interrupt
0 = Disables the INT0 external interrupt
bit 5 RBIIE: RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt
bit 4 TMR0IF: TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow
bit 3 INT0IF: INT0 External Interrupt Flag bit
1 = The INT0 external interrupt has occurred (must be cleared in software)
0 = The INT0 external interrupt did not occur
bit 2 RBIIF: RB Port Change Interrupt Flag bit⁽¹⁾
1 = At least one of the RB7/RB4 pins changed state (must be cleared in software)
0 = None of the RB7/RB4 pins have changed state

43

(cont...)

- Algoritmo en diagrama de flujo



44

(cont...)

- Código en MPASM

```
;Este es un comentario, se le antecede un punto y coma
list p18f4550      ;Modelo del microcontrolador
#include <p18f4550.inc>    ;Llamada a la librería de nombre de los registros

;Directivas de preprocesador o bits de configuración
CONFIG PLLDIV = 1          ; PLL Prescaler Selection bits (No prescale (4)
CONFIG CPUDIV = OSC1_PLL2   ; System Clock Postscaler Selection bits ([P]
CONFIG FOSC = XT_XT        ; Oscillator Selection bits (XT oscillator (XT)
CONFIG FWRT = ON            ; Power-up Timer Enable bit (PWRT enabled)
CONFIG BOR = OFF            ; Brown-out Reset Enable bits (Brown-out Reset
CONFIG WDT = OFF            ; Watchdog Timer Enable bit (WDT disabled (cont
CONFIG CCP2MX = ON           ; CCP2 MUX bit (CCP2 input/output is multiplexe
CONFIG PBADEN = OFF          ; PORTB A/D Enable bit (PORTB<4:0> pins are con
CONFIG MCLE = ON            ; MCLR Pin Enable bit (MCLR pin enabled: RE3 in
CONFIG LVP = OFF             ; Single-Supply ICSP Enable bit (Single-Supply

        org 0x0000      ;vector de reset
        goto init_conf

        org 0x0008      ;vector de interrupcion
        goto TMRI_ISR

        org 0x0020      ;zona de programa de usuario

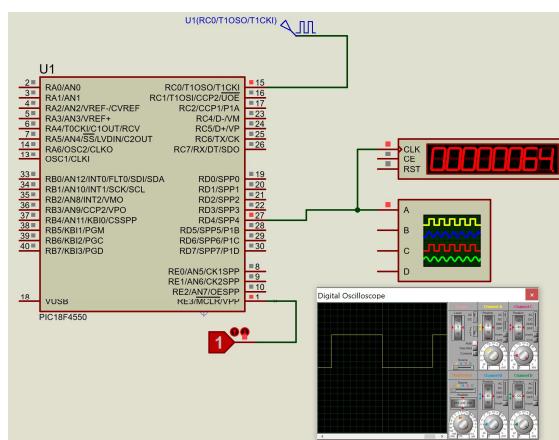
init_conf: bcf TRISD, 4      ;RD4 como salida
        movlw 0x0F
        movwf TICON        ;Timer on, pac 1:1. cristal 3K habilitado, asyn
        bcf TICON, TIOSCEN ;Si es que vas a usar el Proteus
        bsf PIE1, TMRIIE   ;Interrupción de TMRII activada
        bsf INTCON, PEIE   ;Habilitador de int de perifericos activo
        bsf INTCON, GIE    ;interruptor global de interrupciones activado
        setf TMRIH
        clrf TMRL          ;Cuenta inicial en TMRI
loop:    goto loop

TMRI_ISR: btg LATD, 4        ;basculo RD4
        setf TMRIH
        clrf TMRL          ;Cuenta inicial en TMRI
        bcf PIR1, TMRIIF   ;Bajamos la bandera de desborde del TMRI
        retfie
end
```

45

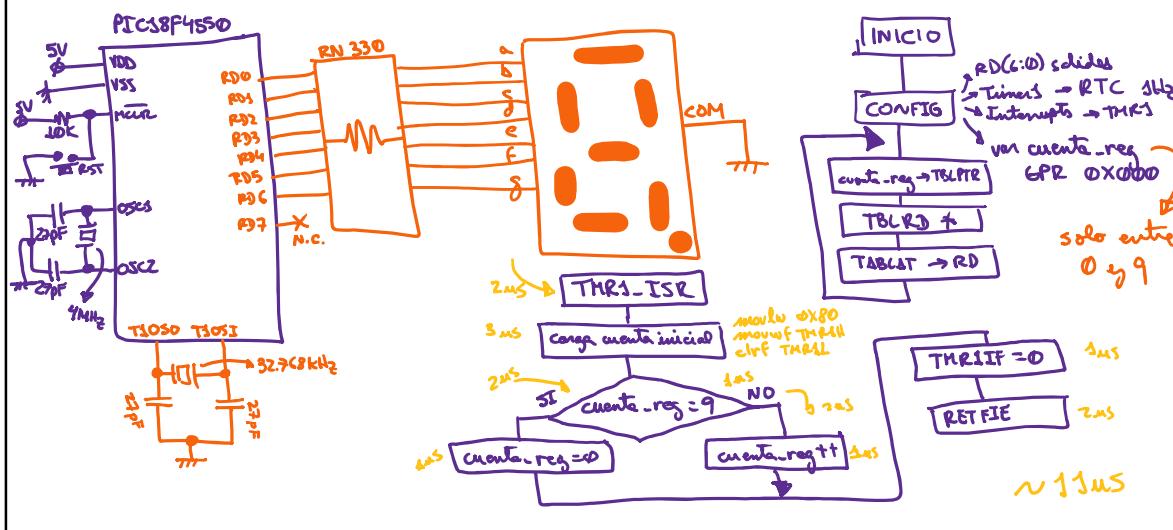
(cont...)

- Simulación en Proteus (T1OSCEN = 0)



46

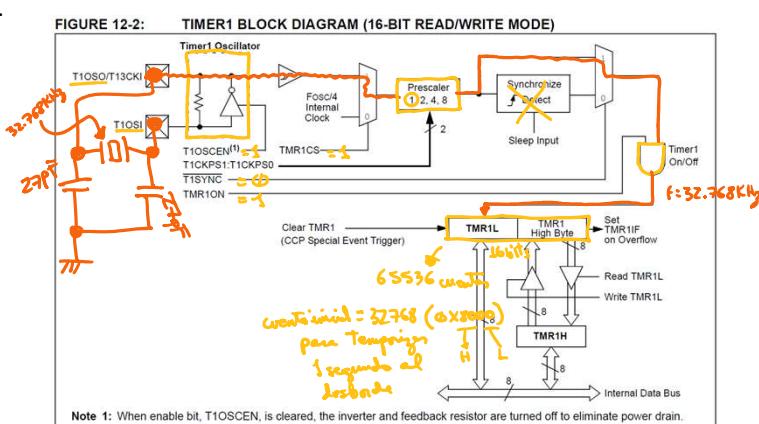
Ejemplo 8: Realizar una cuenta automática 0-9 con un display de siete segmentos cátodo común donde el periodo de cuenta sea de 1Hz dado por el Timer1 en RTC con cristal de 32.768KHz



47

(cont...)

- Configuración del Timer1 para RTC 1Hz con cristal 32.768KHz



48

(cont...)

• Configuración del Timer1

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER							
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	T1RUN	T1CKPS	T1CKPS0	T1OCEN	T1ONC	TM1CS	TMR1ON
bit 7							bit 0
Legend:							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared					x = Bit is unknown
bit 7	RD16: 16-Bit Read/Write Mode Enable bit						
	1 = Enables register read/write of Timer1 in one 16-bit operation	0 = Enables register read/write of Timer1 in two 8-bit operations					
bit 6	T1RUN: Timer1 System Clock Status bit						
	1 = Device clock is derived from Timer1 oscillator	0 = Device clock is derived from another source					
bit 5-4	T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits						
	11 = 1:8 Prescale value	10 = 1:4 Prescale value	01 = 1:2 Prescale value	00 = 1:1 Prescale value			
bit 3	T1OSCEN: Timer1 Oscillator Enable bit						
	1 = Timer1 oscillator is enabled	0 = Timer1 oscillator is shut off					
	The oscillator inverter and feedback resistor are turned off to eliminate power drain.						
bit 2	T1SYNC: Timer1 External Clock Input Synchronization Select bit						
	When TMR1CS = 1: 1 = Do not synchronize external clock input	0 = Synchronize external clock input					
	When TMR1CS = 0: This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.						
bit 1	TMR1CS: Timer1 Clock Source Select bit						
	1 = External clock from RC0/T1SO/T1CKI pin (on the rising edge)	0 = Internal clock (Fosc/4)					
bit 0	TMR1ON: Timer1 On bit						
	1 = Enables Timer1	0 = Stops Timer1					

49

(cont...)

• Configuración de las interrupciones con el Timer1

REGISTER 9-4: PIR1: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1							
R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPIPI(R1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7							bit 0
Legend:							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared					x = Bit is unknown
bit 7	SPIPI: Streaming Parallel Port Read/Write Interrupt Flag bit ¹						
	1 = A read or a write operation has taken place (must be cleared in software)	0 = No read or write has occurred					
bit 6	ADIF: ADC Interrupt Flag bit						
	1 = The A/D conversion complete (must be cleared in software)	0 = The A/D conversion is not complete					
bit 5	RCIF: USART Receive Interrupt Flag bit						
	1 = The USART receive buffer, RCREG, is full (cleared when RCREG is read)	0 = The USART receive buffer, RCREG, is empty					
bit 4	TXIF: USART Transmit Interrupt Flag bit						
	1 = The USART transmit buffer, TXREG, is empty (cleared when TXREG is written)	0 = The USART transmit buffer is full					
bit 3	SSPIF: Master Synchronous Serial Port Interrupt Flag bit						
	1 = The master synchronous serial port reception is complete (must be cleared in software)	0 = Waiting to transmit/receive ²					
bit 2	CCP1IF: CCP1 Interrupt Flag bit						
	Capture mode: 1 = A timer register capture occurred (must be cleared in software)	0 = No timer register capture occurred					
	Compare mode: 1 = A timer register compare match occurred (must be cleared in software)	0 = No timer register compare match occurred					
	PWM mode: Unused in this mode.						
bit 1	TMR2IF: TMR2 to PR2 Match Interrupt Flag bit						
	1 = A timer register match occurred (must be cleared in software)	0 = No timer to PR2 match occurred					
bit 0	TMR1IF: TMR1 Overflow Interrupt Flag bit						
	1 = TMR1 register overflowed (must be cleared in software)	0 = TMR1 register did not overflow					

REGISTER 9-5: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPIPE(R1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit 7							bit 0
Legend:							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared					x = Bit is unknown
bit 7	SPIPE: Streaming Parallel Port Read/Write Interrupt Enable bit ¹						
	1 = Enables the SPIP read/write interrupt	0 = Disables the SPIP read/write interrupt					
bit 6	ADIE: A/D Converter Interrupt Enable bit						
	1 = Enables the A/D interrupt	0 = Disables the A/D interrupt					
bit 5	RCIE: USART Receive Interrupt Enable bit						
	1 = Enables the USART receive interrupt	0 = Disables the USART receive interrupt					
bit 4	TXIE: USART Transmit Interrupt Enable bit						
	1 = Enables the USART transmit interrupt	0 = Disables the USART transmit interrupt					
bit 3	SPIE: Master Synchronous Serial Port Interrupt Enable bit						
	1 = Enables the MSSP interrupt	0 = Disables the MSSP interrupt					
bit 2	CCP1IE: CCP1 Interrupt Enable bit						
	1 = Enables the CCP1 interrupt	0 = Disables the CCP1 interrupt					
bit 1	TMR2IE: TMR2 to PR2 Match Interrupt Enable bit						
	1 = Enables the TMR2 to PR2 match interrupt	0 = Disables the TMR2 to PR2 match interrupt					
bit 0	TMR1IE: TMR1 Overflow Interrupt Enable bit						
	1 = Enables the TMR1 overflow interrupt	0 = Disables the TMR1 overflow interrupt					

REGISTER 9-6: INCON: INTERRUPT CONTROL REGISTER							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GIE/GIEH	PEIE/PEIEL	TMR0IE	INTOE	RBIE	TMR0IF	INT0IF	RBFI
bit 7							bit 0
Legend:							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared					x = Bit is unknown
bit 7	GIE/GIEH: Global Interrupt Enable bit When IPEN = 0: 1 = Enables all unmasked interrupts 0 = Disables all interrupts						
	When IPEN = 1: 1 = Enables all high-priority interrupts 0 = Disables all interrupts						
bit 6	PEIE/PEIEL: Peripheral Interrupt Enable bit When IPEN = 0: 1 = Enables all peripheral interrupts 0 = Disables all peripheral interrupts						
	When IPEN = 1: 1 = Enables all low-priority peripheral interrupts (if GIE/GIEH = 1) 0 = Disables all low-priority peripheral interrupts						
bit 5	TMR0IE: TMR0 Overflow Interrupt Enable bit 1 = Enables the TMR0 overflow interrupt 0 = Disables the TMR0 overflow interrupt						
bit 4	INTOE: INT0 External Interrupt Enable bit 1 = Enables the INT0 external interrupt 0 = Disables the INT0 external interrupt						
bit 3	RBIE: RB Change Interrupt Enable bit 1 = Enables the RB change interrupt 0 = Disables the RB port change interrupt						
bit 2	TMR0IF: TMR0 Overflow Interrupt Flag bit 1 = TMR0 register has overflowed (must be cleared in software) 0 = TMR0 register did not overflow						
bit 1	INT0F: INT0 External Interrupt Flag bit 1 = The INT0 external interrupt occurred (must be cleared in software) 0 = The INT0 external interrupt did not occur						
bit 0	RBIF: RB Port Change Interrupt Flag bit 1 = At least one of the RB7/RB4 pins changed state (must be cleared in software) 0 = None of the RB7/RB4 pins have changed state						

50

(cont...)

- Código en MPASM

```

1 ;Este es un comentario, se le antecede un punto y coma
2 list p=18f4550      ;Modelo del microcontrolador
3 #include <p18f4550.inc> ;Llamada a la librería de nombre de los r
4
5 ;Directivas de preprocesador o bits de configuración
6 CONFIG PLLDIV = 1      ; PLL Prescaler Selection bits (No pres
7 CONFIG CPUDIV = OSC1_PLL2 ; System Clock Postscaler Selection bit
8 CONFIG FOSC = XT_XT    ; Oscillator Selection bits (XT oscillator
9 CONFIG PWRT = ON        ; Power-up Timer Enable bit (PWRT enable
10 CONFIG BOR = OFF       ; Brown-out Reset Enable bits (Brown-out
11 CONFIG WDT = OFF       ; Watchdog Timer Enable bit (WDT disable
12 CONFIG CCP2MX = ON     ; CCP2 MUX bit (CCP2 input/output is multi
13 CONFIG PBADEN = OFF    ; PORTB A/D Enable bit (PORTB<4:0> pins a
14 CONFIG MCLEN = ON      ; MCLR Pin Enable bit (MCLR pin enabled
15 CONFIG LVP = OFF       ; Single-Supply ICSP Enable bit (Single-suppl
16
17 cuenta_reg EQU 0x000
18
19 org 0x0500
20 tabla_7s db 0x3F, 0x06, 0x5B, 0x4F, 0x66, 0x6D, 0x7D, 0x07, 0x7F, 0x67

```

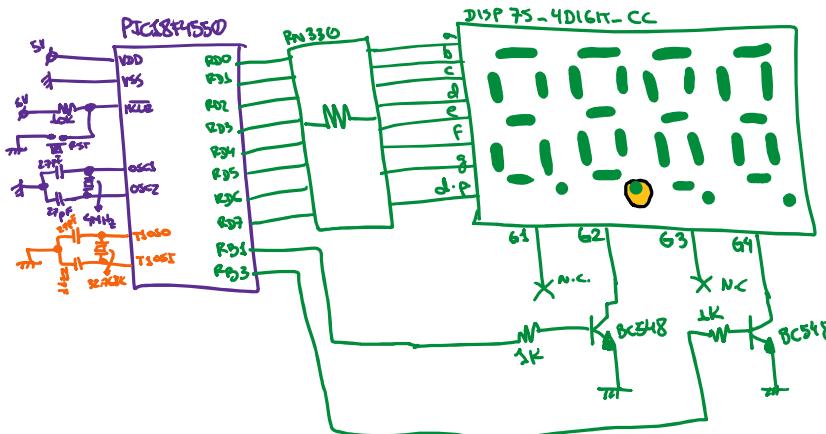
```

22          org 0x0000      ;vector de reset
23          goto init_conf
24
25          org 0x0008      ;vector de interrupcion
26          goto TMR1_ISR
27
28 init_conf: movlw 0x80
29           movwf TRISE      ;RD(6:0) como salidas
30           movlw 0x0F
31           movwf TICON      ;TMR1 on, PSC 1:1, tloscen =1, asynch
32           movlw 0x80
33           movwf TMRIH
34           clrf TMRL         ;carga de cuenta inicial a TMRI
35           bsf PIE1, TMRIIE   ;interrupcion de TMRI habilitada
36           bsf INTCON, PEIE   ;interruptor de interrupciones des
37           bsf INTCON, GIE    ;interruptor global de interrupc
38           clrf cuenta_reg   ;limpiamos cuenta_reg
39           movlw 0x05
40           movwf TBLPTRH
41           movlw 0x00
42           movwf TBLPTRL      ;TBLPTR apuntando a 0x0500
43
44 loop:    movff cuenta_reg, TBLPTRL
45           TBLRD*
46           movff TABLAT, LATD
47           goto loop
48
49 TMR1_ISR: movlw 0x80
50           movwf TMRIH
51           clrf TMRL         ;carga de cuenta inicial a TMRI
52           movlw .9
53           cpfseq cuenta_reg ;pregunto si cuenta_reg=9
54           goto falso
55           clrf cuenta_reg   ;verdadero, limpia cuenta_reg
56           goto otro
57           incf cuenta_reg, f ;falso, incrementa cuenta_reg
58           bcf PIR1, TMRIIF   ;abajamos bandera TMRIIF
59           retfie             ;retorno
60

```

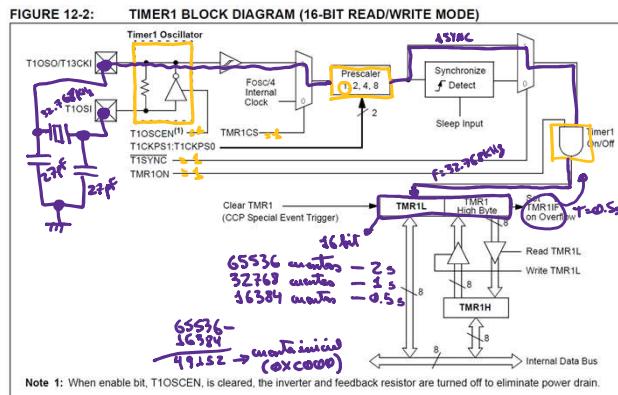
51

Ejemplo 9: Desarrollar un basculador de LED con periodo de 0.5s y una cuenta 0-9 con periodo de 1s empleando el Timer1 en RTC



52

(cont...)



REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER							
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	T1RUN	T1CKPS1	T1CP10	T1OSCEN	T1SYNC	TMR1CS	TMR1ON
bit 7							
Legend:							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR		'1' = Bit is set	'0' = Bit is cleared				x = Bit is unknown
bit 7	RD16: 16-Bit Read/Write Mode Enable bit						
	1 = Enables register read/write of Timer1 in one 16-bit operation						
	0 = Enables register read/write of Timer1 in two 8-bit operations						
bit 6	T1RUN: Timer1 System Clock Status bit						
	1 = Device clock is derived from Timer1 oscillator						
	0 = Device clock is derived from another source						
bit 5-4	T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits						
	11 = 1:8 Prescale value						
	10 = 1:4 Prescale value						
	01 = 1:2 Prescale value						
	00 = 1:1 Prescale value						
bit 3	T1OSCEN: Timer1 Oscillator Enable bit						
	1 = Timer1 oscillator is enabled						
	0 = Timer1 oscillator is shut off						
	The oscillator inverter and feedback resistor are turned off to eliminate power drain.						
bit 2	T1SYNC: Timer1 External Clock Input Synchronization Select bit						
	When TMR1CS = 1:						
	1 = Do not synchronize external clock input						
	0 = Synchronize external clock input						
bit 1	When TMR1CS = 0:						
	This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.						
bit 0	TMR1CS: Timer1 Clock Source Select bit						
	1 = External clock from RCO/T1OSO/T13CKI pin (on the rising edge)						
	0 = Internal clock (Fosc/4)						
	TMR1ON: Timer1 On bit						
	1 = Enables Timer1						
	0 = Stops Timer1						

53

(cont...)

- Configuración de las interrupciones con el Timer1

REGISTER 9-4: PIR1: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1							
R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPIE1 ⁽¹⁾	ADIF	RCIF	TXIF	SSMIF	CCP1IF	TMR2IF	TMR1IF ⁽²⁾
bit 7							bit 0
Legend:							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR		'1' = Bit is set	'0' = Bit is cleared				x = Bit is unknown
bit 7	SPIE1: Streaming Parallel Port Read/Write Interrupt Flag bit ⁽¹⁾						
	1 = A read or a write operation has taken place (must be cleared in software)						
	0 = No read or write has occurred						
bit 6	ADIF: A/D Conversion Interrupt bit						
	1 = The A/D conversion complete (must be cleared in software)						
	0 = The A/D conversion is not complete						
bit 5	RCIF: USART Receive Interrupt Flag bit						
	1 = The USART receive buffer, RCREG8, is full (cleared when RXREG8 is read)						
	0 = The USART receive buffer, TXREG8, is empty (cleared when TXREG8 is written)						
bit 4	TXF1: USART Transmit Interrupt Flag bit						
	1 = The USART transmit buffer, TXREG8, is full						
	0 = The USART transmit buffer is empty						
bit 3	SSMIF: Master Synchronous Serial Port Interrupt Flag bit						
	1 = The master synchronous serial port reception is complete (must be cleared in software)						
	0 = Waiting to transmit/receive a frame						
bit 2	CCP1IF: CCP1 Interrupt Flag bit						
	Capture mode:						
	1 = The CCP1 register capture occurred (must be cleared in software)						
	0 = No CCP1 register capture occurred						
	Compare mode:						
	1 = A TMR1 register compare match occurred (must be cleared in software)						
	0 = No TMR1 register compare match occurred						
	PWM mode:						
	Unused in this mode.						
bit 1	TMR2IF: TMR2 to PR2 Match Interrupt Flag bit						
	1 = TMR2 register match occurred (must be cleared in software)						
	0 = No TMR2 to PR2 match occurred						
bit 0	TMR1IF: TMR1 Overflow Interrupt Flag bit						
	1 = TMR1 register overflowed (must be cleared in software)						
	0 = TMR1 register did not overflow						

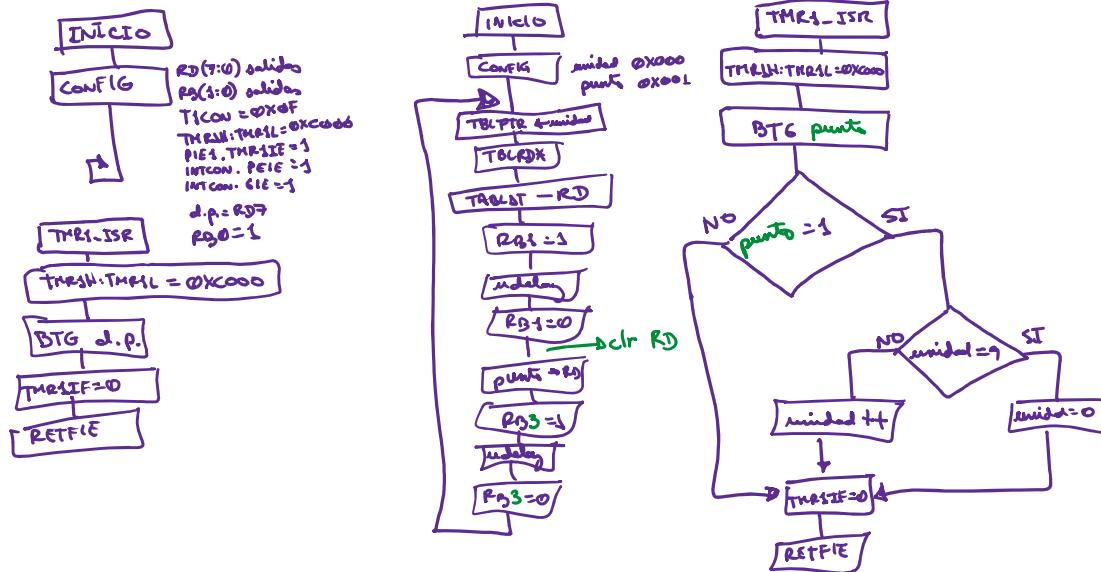
REGISTER 9-5: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE ⁽²⁾
bit 7							bit 0
Legend:							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR		'1' = Bit is set	'0' = Bit is cleared				x = Bit is unknown
bit 7	SPIE: Streaming Parallel Port Read/Write Interrupt Enable bit ⁽¹⁾						
	1 = Enables the SPIP read/write interrupt						
	0 = Disables the SPIP read/write interrupt						
bit 6	ADIE: A/D Converter Interrupt Enable bit						
	1 = Enables the A/D converter						
	0 = Disables the A/D converter						
bit 5	RCIE: USART Receive Interrupt Enable bit						
	1 = Enables the USART receive interrupt						
	0 = Disables the USART receive interrupt						
bit 4	TXIE: USART Transmit Interrupt Enable bit						
	1 = Enables the USART transmit interrupt						
	0 = Disables the USART transmit interrupt						
bit 3	SSPIE: Master Synchronous Serial Port Interrupt Enable bit						
	1 = Enables the MSSP interrupt						
	0 = Disables the MSSP interrupt						
bit 2	CCP1IE: CCP1 Interrupt Enable bit						
	1 = Enables the CCP1 interrupt						
	0 = Disables the CCP1 interrupt						
bit 1	TMR2IE: TMR2 to PR2 Match Interrupt Enable bit						
	1 = Enables the TMR2 to PR2 match interrupt						
	0 = Disables the TMR2 to PR2 match interrupt						
bit 0	TMR1IE: TMR1 Overflow Interrupt Enable bit						
	1 = Enables the TMR1 overflow interrupt						
	0 = Disables the TMR1 overflow interrupt						

REGISTER 9-6: INTC1: INTERRUPT CONTROL REGISTER							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GIE/GIEH	PEIE/PEIEL	RN10	RN10	RN10	RN10	RN10	RN10
bit 7							bit 0
Legend:							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR		'1' = Bit is set	'0' = Bit is cleared				x = Bit is unknown
bit 7	GIE/GIEH: Global Interrupt Enable bit When IPEN = 0:						
	1 = Enables all unmasked interrupts						
	0 = Disables all interrupts						
bit 6	WIE: Watchdog Interrupt Enable bit						
	1 = Enables the watchdog interrupt						
	0 = Disables the watchdog interrupt						
bit 5	PEIE/PEIEL: Peripheral Interrupt Enable bit When IPEN = 1:						
	1 = Enables all low-priority peripheral interrupts						
	0 = Disables all low-priority peripheral interrupts						
bit 4	TMR0IE: TMR0 Overflow Interrupt Enable bit						
	1 = Enables the TMR0 overflow interrupt						
	0 = Disables the TMR0 overflow interrupt						
bit 3	INTOE: INT0 External Interrupt Enable bit						
	1 = Enables the INT0 external interrupt						
	0 = Disables the INT0 external interrupt						
bit 2	RBE/RB4IE: RB Change Interrupt Enable bit						
	1 = Enables the RB change interrupt						
	0 = Disables the RB port change interrupt						
bit 1	TMR0IF: TMR0 Overflow Interrupt Flag bit						
	1 = TMR0 register has overflowed (must be cleared in software)						
	0 = TMR0 register did not overflow						
bit 0	INTOF: INT0 External Interrupt Flag bit						
	1 = The INT0 external interrupt occurred (must be cleared in software)						
	0 = The INT0 external interrupt did not occur						
	RBIF: RB Port Change Interrupt Flag bit ⁽¹⁾						
	1 = At least one of the RB7/RB4 pins changed state (must be cleared in software)						
	0 = None of the RB7/RB4 pins have changed state						

54

(cont...)

- Algoritmo en diagrama de flujo



55

(cont...)

- Código en MPASM

```

1      list p=18f4550           ;Modelo del microcontrolador
2      #include <18f4550.inc>     ;Llamada a la librería de nombre de lo
3
4
5      ;Directivas de preprocesador o bits de configuración
6      CONFIG PLLDIV = 1          ; PLL Prescaler Selection bits (No p
7      CONFIG CPUDIV = OSC1_PLL2   ; System Clock Postscaler Selection
8
9      CONFIG FOSC = XT_XT        ; Oscillator Selection bits (XT osci
10     CONFIG PWRT = ON          ; Power-up Timer Enable bit (PWRT en
11     CONFIG BOR = OFF           ; Brown-out Reset Enable bits (Brown
12     CONFIG WDT = OFF           ; Watchdog Timer Enable bit (WDT dis
13     CONFIG CCP2MX = ON          ; CCP2 MUX bit (CCP2 input/output is
14     CONFIG PBADEN = OFF         ; PORTB A/D Enable bit (PORTB<4:0> p
15     CONFIG MCLRE = ON           ; MCLR Pin Enable bit (MCLR pin enab
16
17     CONFIG LVP = OFF            ; Single-Supply ICSP Enable bit (Sin
18
19
20
21
22      ;Valores de la tabla de búsqueda para el siete segmentos
23      org 0x0400
24      tabla_7s db 0x3F, 0x06, 0x5B, 0x4F, 0x66, 0x6D, 0x7D, 0x07, 0x7F, 0x67
25
26
27      org 0x0000                ;vector de reset
28      goto init_conf
29
30
31      org 0x0008                ;vector de interrupcion
32      goto TMR1_ISR

```

```

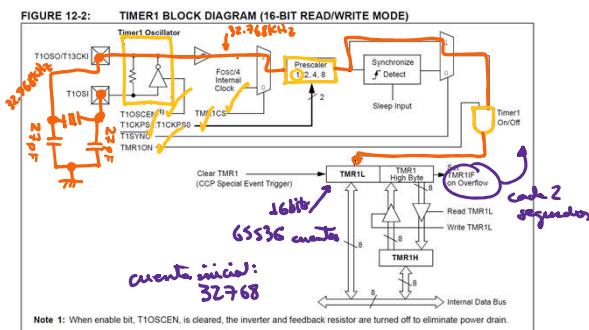
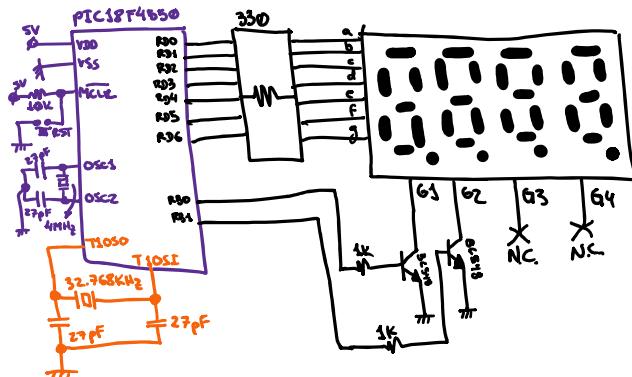
32      org 0x0020 ;zona de programación
33      init_conf: clrf TRISD ;RD col
34          movlw 0xF0
35          movwf TRISB ;RB(1:0)
36          movlw 0x0F
37          movwf TICON ;config
38          movlw 0xC0
39          movwf TMR1H
40          clrf TMRL ;cuenta
41          bsf PIEL, TMR1L ;:i1
42          bsf INTCON, PEIE ;:i1
43          bsf INTCON, GIE ;:i1
44          bcf LATB, 1
45          bcf LATB, 3 ;:a1
46          movlw 0x04
47          movwf TBLPTRH
48          clrf TBLPTRL ;TBLPTR
49          clrf unidad ;:u1
50
51      loop:   movff unidad, TBLPTRL
52          TBLRD+
53          movff TABLAT, LATD
54          bcf LATB, 3
55          call udelay
56          bcf LATB, 3
57          clrf LATD
58          btfs punto, 0
59          goto apaga
60          bsf LATD, 7
61          goto otro
62      apaga: bcf LATD, 7
63      otro:  bcf LATD, 1
64          call udelay
65          bcf LATD, 1
66          goto loop

67      udelay:  nop
68          nop
69          nop
70          nop
71          nop
72          nop
73          nop
74          nop
75          nop
76          nop
77          nop
78          nop
79          return
80
81      TMR1_ISR: movlw 0xC0
82          movwf TMR1H
83          clrf TMRL
84          btfss punto, 0
85          goto final
86          movlw $9
87          cpfseq unidad
88          goto noescierto
89          clrf unidad
90          goto final
91      noescierto: incf unidad, f
92      final:   bcf PIEL, TMR1L
93          retfie
94          end

```

56

Ejemplo 10: Desarrollar un Contador 00-59 con periodo de cuenta 1Hz exacto empleando el Timer1 en RTC y usando el display de cuatro dígitos de siete segmentos de cátodo común multiplexados



57

(cont...)

- Configuración del Timer1

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER							
R/W	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-	R/W-0
bit 6	T1RUN	T1CKPS	T1CKPS0	T1OSCEN	T1OSCNC	TMR1CS	TMR1ON
bit 7	RD16: 16-Bit Read/Write Mode Enable bit 1 = Enables register read/write of Timer1 in one 16-bit operation 0 = Enables register read/write of Timer1 in two 8-bit operations ✓						
bit 6	T1RUN: Timer1 System Clock Status bit 1 = Device clock is derived from Timer1 oscillator 0 = Device clock is derived from another source						
bit 5-4	T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits 11 = 1:8 Prescale value 10 = 1:4 Prescale value 01 = 1:2 Prescale value 00 = 1:1 Prescale value ✓						
bit 3	T1OSCEN: Timer1 Oscillator Enable bit 1 = Timer1 oscillator is enabled 0 = Timer1 oscillator is shut off The oscillator inverter and feedback resistor are turned off to eliminate power drain.						
bit 2	T1SYNCS: Timer1 External Clock Input Synchronization Select bit When TMR1CS = 1: 1 = Do not synchronize external clock input 0 = Synchronize external clock input When TMR1CS = 0: This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.						
bit 1	TMR1CS: Timer1 Clock Source Select bit 1 = External clock from RC0/T1OSO/T13CKI pin (on the rising edge) ✓ 0 = Internal clock (Fosc/4)						
bit 0	TMR1ON: Timer1 On bit 1 = Enables Timer1 0 = Stops Timer1						

58

(cont...)

- Configuración de las interrupciones con el Timer1

REGISTER 9-4: PIR1: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1

R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	SPIPIE ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	bit 0
-------	-------	-----	-------	-------	-------	-------	-----------------------	------	------	------	-------	--------	--------	--------	-------

Legend:
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
-n = Value at POR
'1' = Bit is set
'0' = Bit is cleared
x = Bit is unknown

bit 7
SPIPIF: Streaming Parallel Port Read/Write Interrupt Flag bit⁽¹⁾
1 = A read or a write operation has taken place (must be cleared in software)
0 = No read or write has occurred

bit 6
ADIF: A/D Converter interrupt Flag bit
1 = An A/D conversion completed (must be cleared in software)
0 = No A/D conversion completed

bit 5
RCIF: USART Receive interrupt Flag bit
1 = The USART receive buffer, RCREG, is full (cleared when RCREG is read)
0 = The USART receive buffer is empty

bit 4
TXIF: USART Transmit interrupt Flag bit
1 = The USART transmit buffer, TXREG, is empty (cleared when TXREG is written)
0 = The USART transmit buffer is full

bit 3
SPIIF: Master Synchronous Serial Port interrupt Flag bit
1 = The transmission/reception is complete (must be cleared in software)
0 = Waiting to transmit/receive

bit 2
CAPTURE: Capture interrupt Flag bit
Capture mode:
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred

Compare:
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred

Overflow:
Unused in this mode.

TMRIIF: TMR2 to PR2 Match interrupt Flag bit
1 = TMRI to PR2 match occurred (must be cleared in software)
0 = TMRI register overflowed (must be cleared in software)

TMRIHF: TMRI Overflow interrupt Flag bit
1 = TMRI register overflowed (must be cleared in software)
0 = TMRI register did not overflow

REGISTER 9-6: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

R/W-0	SPIPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	bit 0						
-------	-------	-------	-------	-------	-------	-------	-----------------------	------	------	------	-------	--------	--------	--------	-------

Legend:
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
-n = Value at POR
'1' = Bit is set
'0' = Bit is cleared
x = Bit is unknown

bit 7
SPIPIE: Streaming Parallel Port Read/Write Interrupt Enable bit⁽¹⁾
1 = Enables the SPIP read/write interrupt
0 = Disables the SPIP read/write interrupt

bit 6
ADIE: A/D Converter Interrupt Enable bit
1 = Enables the A/D converter interrupt
0 = Disables the A/D interrupt

bit 5
RCIE: USART Receive Interrupt Enable bit
1 = Enables the USART receive interrupt
0 = Disables the USART receive interrupt

bit 4
TXIE: USART Transmit Interrupt Enable bit
1 = Enables the USART transmit interrupt
0 = Disables the USART transmit interrupt

bit 3
SSPIE: Master Synchronous Serial Port Interrupt Enable bit
1 = Enables the MSSP interrupt
0 = Disables the MSSP interrupt

bit 2
CPIE: CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 1
TMR2IE: TMR2 to PR2 Match interrupt Enable bit
1 = Enables the TMR2 to PR2 match interrupt
0 = Disables the TMR2 to PR2 match interrupt

bit 0
TMRIIE: TMRI Overflow interrupt Enable bit
1 = Enables the TMRI overflow interrupt
0 = Disables the TMRI overflow interrupt

REGISTER 9-1: ICR: INTERRUPT CONTROL REGISTER

R/W-0	GIE/GIEH	PIE1/GIEL	TMR0IE	INT0IE	RBIIE	TMR0IF	INT0IF	RBIIF ⁽¹⁾	bit 0						
-------	-------	-------	-------	-------	-------	-------	----------	-----------	--------	--------	-------	--------	--------	----------------------	-------

Legend:
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
-n = Value at POR
'1' = Bit is set
'0' = Bit is cleared
x = Bit is unknown

bit 7
GIE/GIEH: Global interrupt enable bit
When IEP=1:
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6
When IEP=0:
1 = Enables all priority peripheral interrupts
0 = Disables all peripheral interrupts

bit 5
When IEP=1:
1 = Enables all priority peripheral interrupts (if GIE/GIEH = 1)
0 = Disables all low-priority peripheral interrupts

bit 4
TMR0IE: TMR0 Overflow interrupt Enable bit
1 = Enables the TMR0 overflow interrupt
0 = Disables the TMR0 overflow interrupt

bit 3
INT0IE: INT0 External interrupt enable bit
1 = Enables the INT0 external interrupt
0 = Disables the INT0 external interrupt

bit 2
TMRIIE: TMRI Overflow interrupt Flag bit
1 = TMRI register has overflowed (must be cleared in software)
0 = TMRI register did not overflow

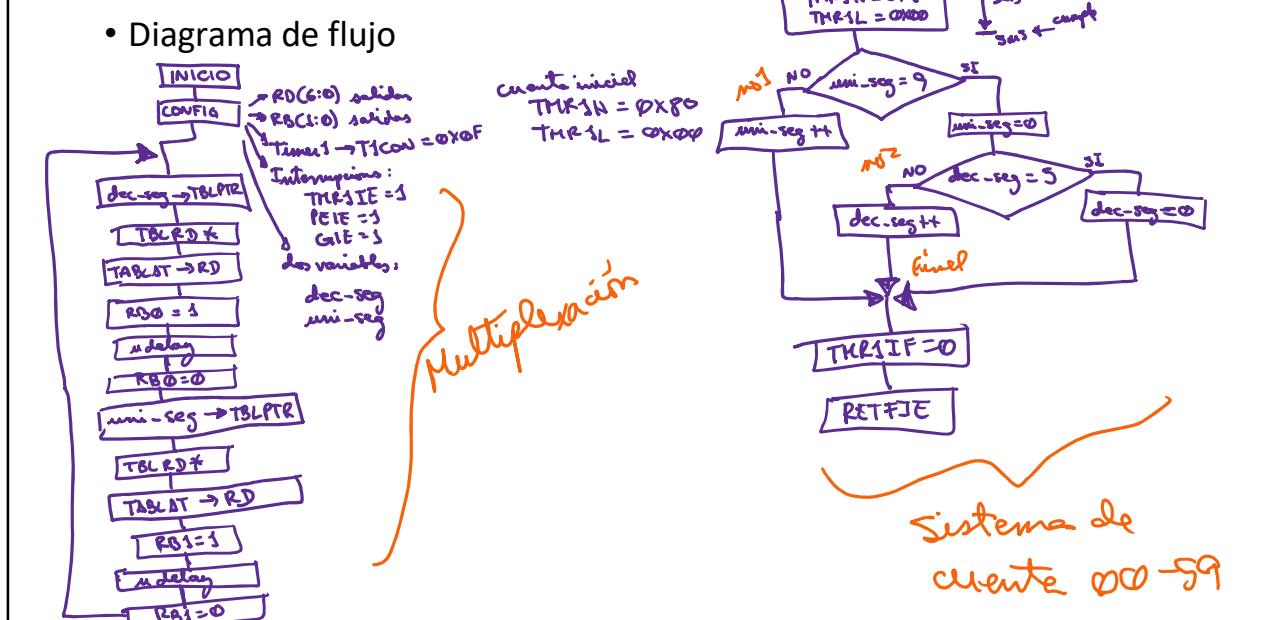
bit 1
INT0IF: INT0 External interrupt Flag bit
1 = The INT0 external interrupt is pending (must be cleared in software)
0 = The INT0 external interrupt did not occur

bit 0
RBIIF: RB Port Change interrupt Flag bit⁽¹⁾
1 = At least one of the RB7/RB4 pins changed state (must be cleared in software)
0 = None of the RB7/RB4 pins have changed state

59

(cont...)

- Diagrama de flujo



Ejercicios:

- Desarrollar un cronómetro mm:ss de 00 minutos 00 segundos hasta 59 minutos 59 segundos empleando la configuración de Timer1 visto en esta sesión de clase, la visualización será en cuatro displays de siete segmentos de cátodo común multiplexados, se deberá usar el Timer1 como RTC. Se tendrá dos entradas de interrupción externa: una para el inicio de la cuenta y otra para la parada. Para colocar la cuenta del cronómetro en 00:00 se usará el botón de RESET.

61

Fin de la sesión!

62