

Microcontroladores Laboratorio

Semana 3

1

Agenda

- Usos del Timer0 e interrupciones

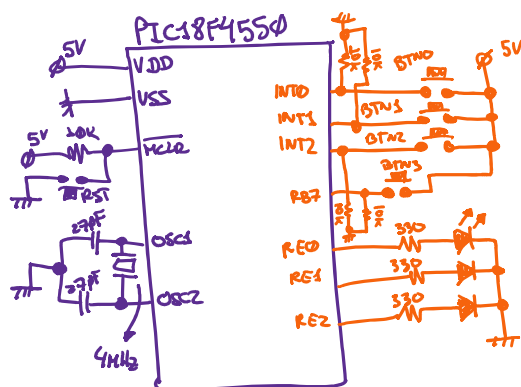
2

Preguntas previas:

- ¿Por qué hay dos diagramas de flujo en el ejemplo del día lunes?
 - Porque hay evento de interrupción y cada evento de esa naturaleza debe de tener su diagrama de flujo.
- ¿Qué significa que hay que configurar el Timer0?
 - Significa que debes de seguir el procedimiento visto en clase para poder configurar el Timer0 para obtener las temporizaciones solicitadas.

3

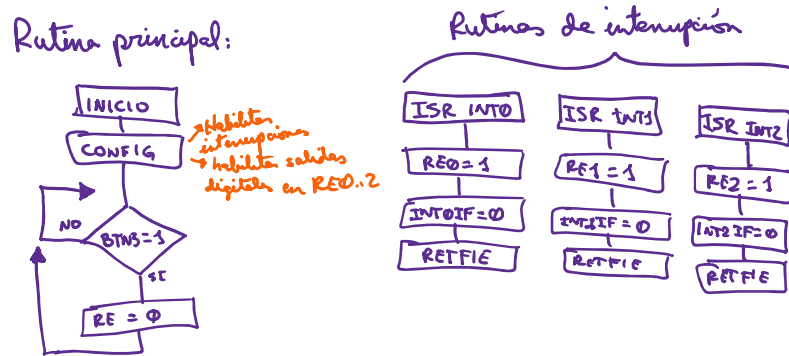
Desarrollar el siguiente circuito:



- El circuito deberá detectar los eventos de pulsación de los botones y encenderá su LED respectivo (INT0 activará RE0, INT1 activará RE1 e INT2 activará RE2), el botón ubicado en RB7 apagará cualquier LED encendido.

4

Diagramas de flujo:



5

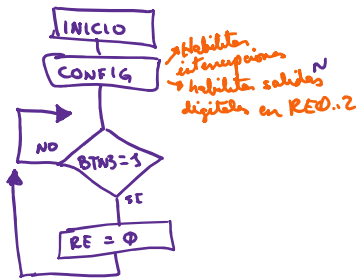
Análisis de lo anterior

- El CPU del microcontrolador no puede hacer procedimientos en paralelo, es un sistema secuencial!
- La atención de los eventos de interrupción también serán de manera secuencial, independientemente si vinieron de la alta prioridad o de la baja prioridad.

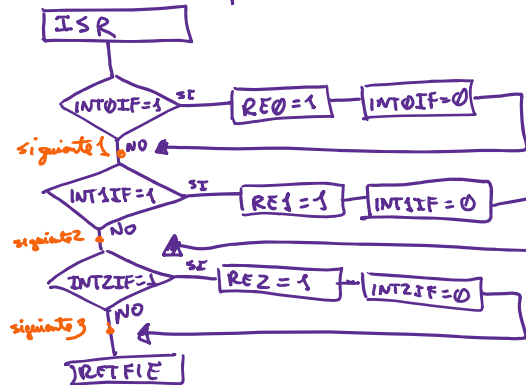
6

Opción 1: Todas las fuentes de interrupción se van al vector 0x0008 (High Priority)

Rutina principal:



Rutina de interrupción:



7

Búsqueda de los habilitadores de INT0, INT1 e INT2

- Debemos de buscar en qué registros están los bits habilitadores de las fuentes de interrupción externa (INT0IE, INT1IE, INT2IE) y los habilitadores globales (GIE ~~y si es el caso PEIE~~).

REGISTER 9-1: INTCON: INTERRUPT CONTROL REGISTER

RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0
GIE/GIEH	PEIE/GIEL	TMR1IE	INT0IE	RBIF	TMR0IF	INT0IF	RBIF
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 7 **GIIE/GIEH**: Global Interrupt Enable bit

When **IPEN** = 0:

- 1 = Enables all unmasked interrupts
- 0 = Disables all interrupts

When **IPEN** = 1:

- 1 = Enables all high-priority interrupts
- 0 = Disables all interrupts

bit 6 **PEIE/GPIH**: Peripheral Interrupt Enable bit

When **IPEN** = 0:

- 1 = Enables all unmasked peripheral interrupts
- 0 = Disables all peripheral interrupts

When **IPEN** = 1:

- 1 = Enables all low-priority peripheral interrupts (if **GIEH** = 1)
- 0 = Disables all low-priority peripheral interrupts

bit 5	TMROIE: TMRO overflow Interrupt Enable bit = Enables the TMRO overflow interrupt = Disables the TMRO overflow interrupt
bit 4	INTIE: INT0 External Interrupt Enable bit = Enables the INT0 external interrupt = Disables the INT0 external interrupt
bit 3	RBIF: RB Port Change Interrupt Enable bit = Enables the RB port change interrupt = Disables the RB port change interrupt
bit 2	TMROIF: TMRO overflow Interrupt Flag bit = TMRO register has overflowed (must be cleared in software) = TMRO register did not overflow
bit 1	INT0IF: INT0 External Interrupt Flag bit = The INT0 external interrupt occurred (must be cleared in software) = The INT0 external interrupt did not occur
bit 0	RBIF: RB Port Change Interrupt Flag bit ¹⁾ = At least one of the RB7-RB4 pins changed state (must be cleared in software) = None of the RB7-RB4 pins have changed state

REGISTER 9-3: INTCON3: INTERRUPT CONTROL REGISTER 3

R/W1	R/W-1	U-0	R/W0	R/W-0	U-0	R/W0	R/W0
INT2P	INT1P	-	INT2E	INT1E	-	INT2F	INT1F
bit 7							bit

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 7 **INT2IP:** INT2 External Interrupt Priority bit
 1 = High priority
 0 = Low priority

bit 6 **INT1IP**: INT1 External Interrupt Priority bit
1 = High priority
0 = Low priority

bit 5 **Unimplemented:** Read as '0'

INT2IE: INT2 External Interrupt Enable bit
1 = Enables the INT2 external interrupt
0 = Disables the INT2 external interrupt

bit 3 **INT1IE:** INT1 External Interrupt Enable bit

1 = Enables the INT1 external interrupt

0 = Disables the INT1 external interrupt

bit 2 **Unimplemented: Read as '0'**

bit 1 **INT2IF: INT2 External Interrupt Flag bit**
 1 = The INT2 external interrupt occurred (must be cleared in software)
 0 = The INT2 external interrupt did not occur

bit 0 **INT1IF:** INT1 External Interrupt Flag bit
 1 = The INT1 external interrupt occurred (must be cleared in software)
 0 = The INT1 external interrupt did not occur

8

Código en MPASM

```

1  ;Este es un comentario, se le da
2  list p=18f4550 ;Modelo
3  #include <pl8f4550.inc>
4
5  ;Directivas de preprocesador
6  CONFIG PLLDIV = 1
7  CONFIG CPUDIV = OSC1_PLL2
8  CONFIG FOSC = XT_XT
9  CONFIG FWRT = ON
10 CONFIG BOR = OFF
11 CONFIG WDT = OFF
12 CONFIG CCP2MX = ON
13 CONFIG PBADEN = OFF
14 CONFIG MCLRRE = ON
15 CONFIG LVP = OFF
16
17 ;Aquí va el cblock o declaración
18 cblock 0x000
19 endc
20
21 org 0x0000
22 goto init_conf
23
24 org 0x0008
25 goto isr_ints
26 ;Aquí se pueden declarar las constantes
27
28 org 0x0020
29 init_conf:
30 movlw 0x0F
31 movwf ADCON1 ;Todos
32 movlw 0x08
33 movwf TRISE ;RE0-RE
34 movlw 0xD8
35 movwf INTCON3 ;INT1 e
36 movlw 0x90
37 movwf INTCON ;INT0 e

```

```

39 loop:
40 btfss PORTB, 7
41 goto loop
42 clrf LATE
43 goto loop
44
45 isr_ints:
46 btfss INTCON, INT0IF
47 goto siguiente1
48 bsf LATE, 0
49 bcf INTCON, INT0IF
50 siguiente1:
51 btfss INTCON3, INT1IF
52 goto siguiente2
53 bsf LATE, 1
54 bcf INTCON3, INT1IF
55 siguiente2:
56 btfss INTCON3, INT2IF
57 goto siguiente3
58 bsf LATE, 2
59 bcf INTCON3, INT2IF
60 siguiente3:
61 retfie
62 end

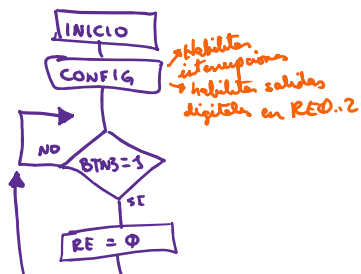
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9

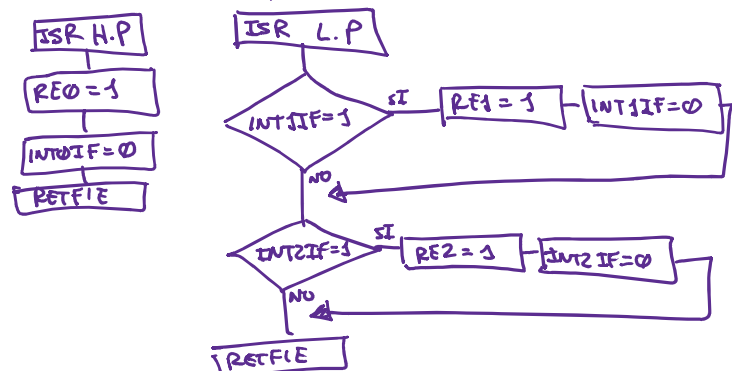
Opción 2: Empleando prioridad en las interrupciones

- Definimos INT0 en alta prioridad, INT1 e INT2 en baja prioridad

Rutina principal:



Rutina de interrupción:



10

Habilitación de las prioridades en interrupción

REGISTER 9-10: RCON: RESET CONTROL REGISTER

R/W-0	R/W-1 ⁽¹⁾	U-0	R/W-1	R-1	R-1	R/W-0 ⁽²⁾	R/W-0
IPEN	SBOREN		RI	TO	PD	POR	BOR
bit 7							bit 0

Legend:

R = Readable bit
-n = Value at POR
W = Writable bit
'1' = Bit is set
U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

- bit 7 **IPEN:** Interrupt Priority Enable bit
1 = Enable priority levels on interrupts
0 = Disable priority levels on interrupts (PIC16CXXX Compatibility mode)
- bit 6 **SBOREN:** BOR Software Enable bit⁽¹⁾
For details of bit operation, see Register 4-1.
- bit 5 **Unimplemented:** Read as '0'
- bit 4 **RI:** RESET Instruction Flag bit
For details of bit operation, see Register 4-1.
- bit 3 **TO:** Watchdog Time-out Flag bit
For details of bit operation, see Register 4-1.
- bit 2 **PD:** Power-Down Detection Flag bit
For details of bit operation, see Register 4-1.
- bit 1 **POR:** Power-on Reset Status bit⁽²⁾
For details of bit operation, see Register 4-1.
- bit 0 **BOR:** Brown-out Reset Status bit
For details of bit operation, see Register 4-1.

11

Búsqueda de los habilitadores de INT0, INT1 e INT2

- Debemos de buscar en qué registros están los bits habilitadores de las fuentes de interrupción externa (INT0IE, INT1IE, INT2IE) y los habilitadores globales (GIE y si es el caso PEIE)

REGISTER 9-1: INTCON: INTERRUPT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GIE/PEIE	PEIE/SEL	INT0IE	INT1IE	INT2IE	INT0IF	INT1IF	INT2IF
bit 7							bit 0

Legend:
R = Readable bit
-n = Value at POR
W = Writable bit
'1' = Bit is set
U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

- bit 7 **GIE/PEIE:** Global Interrupt Enable bit
When IPEN = 1:
1 = Enables all unmasked interrupts
0 = Disables all interrupts
When IPEN = 0:
1 = Enables all high-priority interrupts
0 = Disables all high-priority interrupts
When IPEN = 1:
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts
When IPEN = 0:
1 = Enables all low-priority peripheral interrupts (if GIE/PEIE = 1)
0 = Disables all low-priority peripheral interrupts
- bit 6 **TMROIE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 overflow interrupt
0 = Disables the TMR0 overflow interrupt
- bit 5 **INT0IE:** INT0 External Interrupt Enable bit
1 = Enables the INT0 external interrupt
0 = Disables the INT0 external interrupt
- bit 4 **INT1IE:** INT1 External Interrupt Enable bit
1 = Enables the INT1 external interrupt
0 = Disables the INT1 external interrupt
- bit 3 **INT2IE:** INT2 External Interrupt Enable bit
1 = Enables the INT2 external interrupt
0 = Disables the INT2 external interrupt
- bit 2 **INT0IF:** INT0 External Interrupt Flag bit
1 = The INT0 external interrupt occurred (must be cleared in software)
0 = The INT0 external interrupt did not occur
- bit 1 **INT1IF:** INT1 External Interrupt Flag bit
1 = The INT1 external interrupt occurred (must be cleared in software)
0 = The INT1 external interrupt did not occur
- bit 0 **INT2IF:** INT2 External Interrupt Flag bit
1 = The INT2 external interrupt occurred (must be cleared in software)
0 = The INT2 external interrupt did not occur

REGISTER 9-3: INTCON3: INTERRUPT CONTROL REGISTER 3

R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
INT2IP	INT1IP		INT1IE	INT2IE		INT2IF	INT1IF
bit 7							bit 0

Legend:
R = Readable bit
-n = Value at POR
W = Writable bit
'1' = Bit is set
U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

- bit 7 **INT2IP:** INT2 External Interrupt Priority bit
1 = High priority
0 = Low priority
- bit 6 **INT1IP:** INT1 External Interrupt Priority bit
1 = High priority
0 = Low priority
- bit 5 **Unimplemented:** Read as '0'
- bit 4 **INT2IE:** INT2 External Interrupt Enable bit
1 = Enables the INT2 external interrupt
0 = Disables the INT2 external interrupt
- bit 3 **INT1IE:** INT1 External Interrupt Enable bit
1 = Enables the INT1 external interrupt
0 = Disables the INT1 external interrupt
- bit 2 **Unimplemented:** Read as '0'
- bit 1 **INT2IF:** INT2 External Interrupt Flag bit
1 = The INT2 external interrupt occurred (must be cleared in software)
0 = The INT2 external interrupt did not occur
- bit 0 **INT1IF:** INT1 External Interrupt Flag bit
1 = The INT1 external interrupt occurred (must be cleared in software)
0 = The INT1 external interrupt did not occur

12

Código en MPASM

```

2      list p=18f4550      ;Modelo
3
4      #include <18f4550.inc>
5
6      ;Directivas de preprocesador
7      CONFIG PLLDIV = 1
8      CONFIG CPUDIV = OSC1_PLL2
9      CONFIG FOSC = XT_XT
10     CONFIG FWRT = ON
11     CONFIG BOR = OFF
12     CONFIG WDT = OFF
13     CONFIG CCP2MX = ON
14     CONFIG PBADEN = OFF
15     CONFIG MCLRE = ON
16     CONFIG LVP = OFF
17
18     org 0x0000
19     goto init_conf
20
21     org 0x0008
22     goto isr_hp
23
24     org 0x0018
25     goto isr_lp
26
27     org 0x0020
28     init_conf:
29     movlw 0x0F
30     movwf ADCON1      ;Todos
31     movlw 0x08
32     movwf TRISE      ;REQ-REQ
33     bsf RCON, IPEN    ;Habilita
34     movlw 0x18
35     movwf INTCON3     ;INT1 e
36     movlw 0xD0
37     movwf INTCON      ;INT0 a

```

```

38     loop:
39     btfss PORTE, 7
40     goto loop
41     clrf LATE
42     goto loop
43
44     isr_hp:
45     bsf LATE, 0
46     bcf INTCON, INTOIF
47     retfie
48
49     isr_lp:
50     btfss INTCON3, INT1IF
51     goto siguiente1
52     bsf LATE, 1
53     bcf INTCON3, INT1IF
54     siguiente1:
55     btfss INTCON3, INT2IF
56     goto siguiente2
57     bsf LATE, 2
58     bcf INTCON3, INT2IF
59     siguiente2:
60     retfie
61     end

```