Microcontroladores Laboratorio

Semana 4

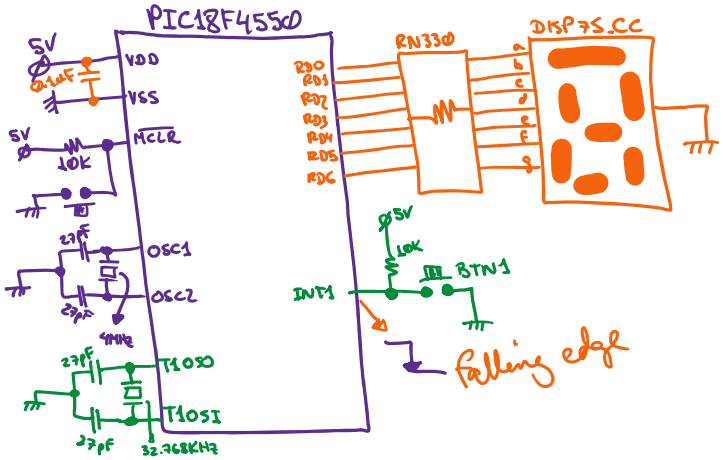
Preguntas previas:

- Para qué sirven los condensadores de 0.1uF que se ven al costado de todos los IC's de un PCB?
  - Se les conoce como "decoupling capacitors" o condensadores de desacople, sirve para estabilizar el nivel de alimentación que recibe el IC.
- Los cristales tienen cuerpo metálico. ¿Sirve para alguna función en particular?
  - Sirve para proteger de interferencias electromagnéticas externas si es que conectas el cuerpo metálico a tierra (jaula de Faraday)

Agenda:

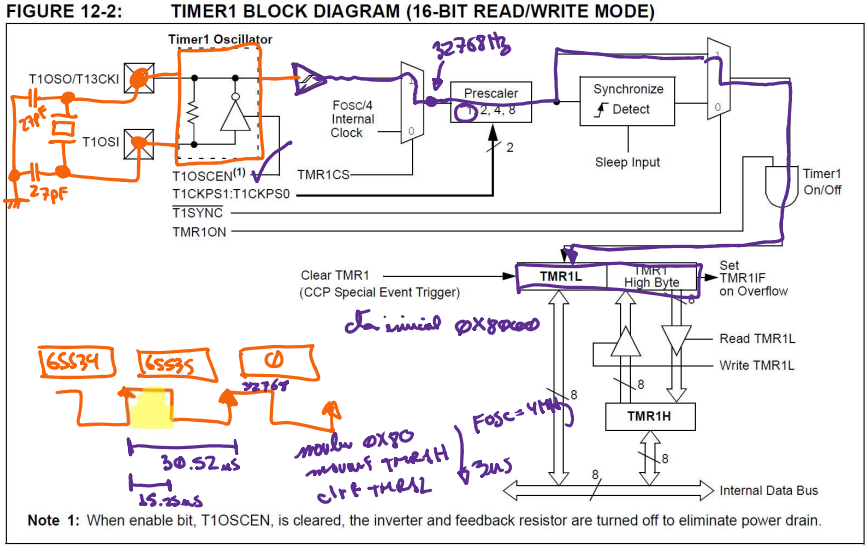
- Aplicaciones con RTC
- PWM con CCP

Ejemplo: Circuito con dos cristales



Trabajando el Timer1 y cristal de 32.768KHz

FIGURE 12-2: TIMER1 BLOCK DIAGRAM (16-BIT READ/WRITE MODE)



Note 1: When enable bit, T1OSCEN, is cleared, the inverter and feedback resistor are turned off to eliminate power drain.

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Configuración del registro T1CON

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	T1RUN	T1CKPS	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **RD16:** 16-Bit Read/Write Mode Enable bit
1 = Enables register read/write of Timer1 in one 16-bit operation
0 = Enables register read/write of Timer1 in two 8-bit operations

bit 6 **T1RUN:** Timer1 System Clock Status bit
1 = Device clock is derived from Timer1 oscillator
0 = Device clock is derived from another source

bit 5-4 **T1CKPS1:T1CKPS0:** Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3 **T1OSCEN:** Timer1 Oscillator Enable bit
1 = Timer1 oscillator is enabled
0 = Timer1 oscillator is shut off
The oscillator inverter and feedback resistor are turned off to eliminate power drain.

bit 2 **T1SYNC:** Timer1 External Clock Input Synchronization Select bit
When TMR1CS = 1:
1 = Do not synchronize external clock input
0 = Synchronize external clock input
When TMR1CS = 0:
This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1 **TMR1CS:** Timer1 Clock Source Select bit
1 = External clock from RC0/T1OSO/T13CKI pin (on the rising edge)
0 = Internal clock (Fosc/4)

bit 0 **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

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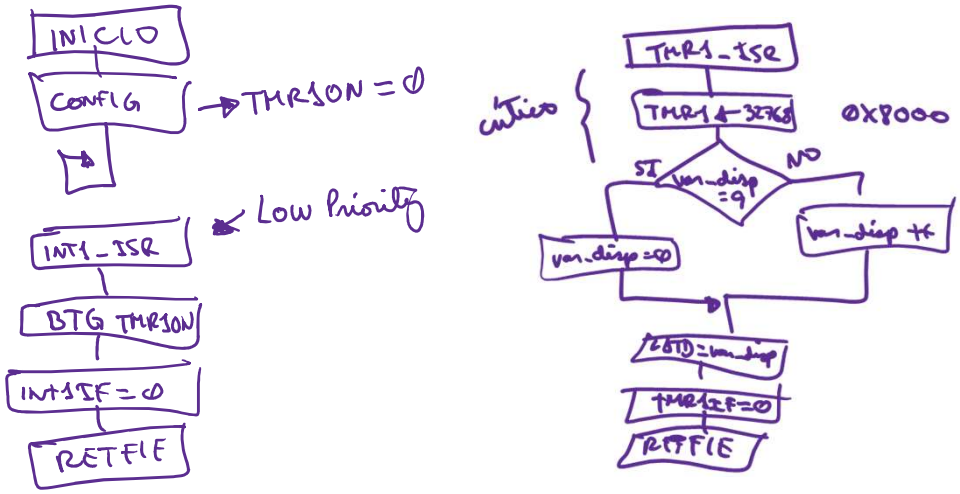
Diagrama de flujo



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Configuración de interrupciones

REGISTER 9-10: RCON: RESET CONTROL REGISTER

R/W-0	R/W-1(1)	U-0	R/W-1	R-1	R-1	R/W-0(2)	R/W-0
IPEN	SBOREN	—	RI	TO	PD	POR	BOR
bit 7							bit 0

Legend:
R = Readable bit — W = Writable bit — U = Unimplemented bit, read as '0'
-n = Value at POR — '1' = Bit is set — '0' = Bit is cleared — x = Bit is unknown

bit 7 **IPEN:** Interrupt Priority Enable bit
1 = Enable priority levels on interrupts
0 = Disable priority levels on interrupts (PIC16CXXX Compatibility mode)
bit 6 **SBOREN:** BOR Software Enable bit(1)
For details of bit operation, see Register 4-1.
bit 5 **Unimplemented:** Read as '0'
bit 4 **RI:** RESET Instruction Flag bit
For details of bit operation, see Register 4-1.
bit 3 **TO:** Watchdog Time-out Flag bit
For details of bit operation, see Register 4-1.
bit 2 **PD:** Power-Down Detection Flag bit
For details of bit operation, see Register 4-1.
bit 1 **POR:** Power-on Reset Status bit(2)
For details of bit operation, see Register 4-1.
bit 0 **BOR:** Brown-out Reset Status bit
For details of bit operation, see Register 4-1.

bsf RCON, IPEN

REGISTER 9-3: INTCON3: INTERRUPT CONTROL REGISTER 3

R/W-1	R/W-1	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
INT2IP	INT1IP	—	INT2IE	INT1IE	—	INT2IF	INT1IF
bit 7							bit 0

Legend:
R = Readable bit — W = Writable bit — U = Unimplemented bit, read as '0'
-n = Value at POR — '1' = Bit is set — '0' = Bit is cleared — x = Bit is unknown

bit 7 **INT2IP:** INT2 External Interrupt Priority bit
1 = High priority
0 = Low priority
bit 6 **INT1IP:** INT1 External Interrupt Priority bit
1 = High priority
0 = Low priority
bit 5 **Unimplemented:** Read as '0'
bit 4 **INT2IE:** INT2 External Interrupt Enable bit
1 = Enables the INT2 external interrupt
0 = Disables the INT2 external interrupt
bit 3 **INT1IE:** INT1 External Interrupt Enable bit
1 = Enables the INT1 external interrupt
0 = Disables the INT1 external interrupt
bit 2 **Unimplemented:** Read as '0'
bit 1 **INT2IF:** INT2 External Interrupt Flag bit
1 = The INT2 external interrupt occurred (must be cleared in software)
0 = The INT2 external interrupt did not occur
bit 0 **INT1IF:** INT1 External Interrupt Flag bit
1 = The INT1 external interrupt occurred (must be cleared in software)
0 = The INT1 external interrupt did not occur

bcf INTCON3, INT1IP
bsf INTCON3, INT1IE

REGISTER 9-1: INTCON: INTERRUPT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
bit 7							bit 0

Legend:
R = Readable bit — W = Writable bit — U = Unimplemented bit, read as '0'
-n = Value at POR — '1' = Bit is set — '0' = Bit is cleared — x = Bit is unknown

bit 7 **GIE/GIEH:** Global Interrupt Enable bit
When IPEN = 0:
1 = Enables all unmasked interrupts
0 = Disables all interrupts
When IPEN = 1:
1 = Enables all high-priority interrupts
0 = Disables all interrupts
bit 6 **PEIE/GIEL:** Peripheral Interrupt Enable bit
When IPEN = 0:
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts
When IPEN = 1:
1 = Enables all low-priority peripheral interrupts (if GIE/GIEH = 1)
0 = Disables all low-priority peripheral interrupts
bit 5 **TMR0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 overflow interrupt
0 = Disables the TMR0 overflow interrupt
bit 4 **INT0IE:** INT0 External Interrupt Enable bit
1 = Enables the INT0 external interrupt
0 = Disables the INT0 external interrupt
bit 3 **RBIE:** RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt
bit 2 **TMR0IF:** TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow
bit 1 **INT0IF:** INT0 External Interrupt Flag bit
1 = The INT0 external interrupt occurred (must be cleared in software)
0 = The INT0 external interrupt did not occur
bit 0 **RBIF:** RB Port Change Interrupt Flag bit(1)
1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

INTCON = 0XC0

REGISTER 9-6: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit 7							bit 0

Legend:
R = Readable bit — W = Writable bit — U = Unimplemented bit, read as '0'
-n = Value at POR — '1' = Bit is set — '0' = Bit is cleared — x = Bit is unknown

bit 7 **SPPIE:** Streaming Parallel Port Read/Write Interrupt Enable bit(1)
1 = Enables the SPP read/write interrupt
0 = Disables the SPP read/write interrupt
bit 6 **ADIE:** A/D Converter Interrupt Enable bit
1 = Enables the A/D interrupt
0 = Disables the A/D interrupt
bit 5 **RCIE:** EUSART Receive Interrupt Enable bit
1 = Enables the EUSART receive interrupt
0 = Disables the EUSART receive interrupt
bit 4 **TXIE:** EUSART Transmit Interrupt Enable bit
1 = Enables the EUSART transmit interrupt
0 = Disables the EUSART transmit interrupt
bit 3 **SSPIE:** Master Synchronous Serial Port Interrupt Enable bit
1 = Enables the MSSP interrupt
0 = Disables the MSSP interrupt
bit 2 **CCP1IE:** CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt
bit 1 **TMR2IE:** TMR2 to PR2 Match Interrupt Enable bit
1 = Enables the TMR2 to PR2 match interrupt
0 = Disables the TMR2 to PR2 match interrupt
bit 0 **TMR1IE:** TMR1 Overflow Interrupt Enable bit
1 = Enables the TMR1 overflow interrupt
0 = Disables the TMR1 overflow interrupt

PIE1 = 0X01

- TMR1 en alta prioridad
- INT1 en baja prioridad

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Código en MPASM

```
;Este es un comentario, se le antecede un
    list p=18f4550      ;Modelo del micro
    #include <p18f4550.inc>     ;Llamada

    ;Directivas de preprocesador o bits d
    CONFIG  PLLDIV = 1          ; PLL P
    CONFIG  CPUDIV = OSC1_PLL2  ; Syste
    CONFIG  FOSC = XT_XT        ; Oscil
    CONFIG  PWRT = ON           ; Power
    CONFIG  BOR = OFF           ; Brown
    CONFIG  WDT = OFF           ; Watch
    CONFIG  CCP2MX = ON         ; CCP2
    CONFIG  PBADEN = OFF        ; PORTB
    CONFIG  MCLRE = ON          ; MCLR
    CONFIG  LVP = OFF           ; Singl

;Aquí va el cblock o declaaración de nomb
    cblock 0x000
    var_disp
    endc

    org 0x0000
    goto init_conf

    org 0x0008
    goto TMR1_ISR

    org 0x0018
    goto INT1_ISR

;Aquí se pueden declarar las constantes en la memoria de programa
    org 0x0600
tabla_7s db 0x3F, 0x06, 0x5B, 0x4F, 0x66, 0x6D, 0x7D, 0x07, 0x7F, 0x67, 0x79, 0x79, 0x79, 0x79, 0x79, 0x79
```

```
    org 0x0020
init_conf:
    movlw 0x80
    movwf TRISD
    movlw HIGH tabla_7s
    movwf TBLPTRH
    clrf TBLPTRL        ;TBL
    movlw 0x0E
    movwf T1CON         ;TMR
    movlw 0x80
    movwf TMR1H
    clrf TMR1L          ;Ca
    bsf RCON, IPEN      ;Hab
    bcf INTCON3, INT1IP ;INT
    bcf INTCON2, INTEDG1;INT
    bsf INTCON3, INT1IE ;Hab
    movlw 0x01
    movwf PIE1          ;TMR
    movlw 0xC0
    movwf INTCON        ;Int
    clrf var_disp
    movff var_disp, TBLPTRL
    TBLRD*
    movff TABLAT, LATD
```

```
loop:
    goto loop

TMR1_ISR:
    movlw 0x80
    movwf TMR1H
    movlw 0x00
    movwf TMR1L     ;tejec = 6us
;    clrf TMR1L     ;tejec = 7us
    movlw .9
    cpfseq var_disp
    goto aunno
    clrf var_disp
    goto final
aunno:
    incf var_disp, f
final:
    movff var_disp, TBLPTRL
    TBLRD*
    movff TABLAT, LATD
    bcf PIR1, TMR1IF
    retfie

INT1_ISR:
    btg T1CON, TMR1ON
    bcf INTCON3, INT1IF
    retfie
    end
```

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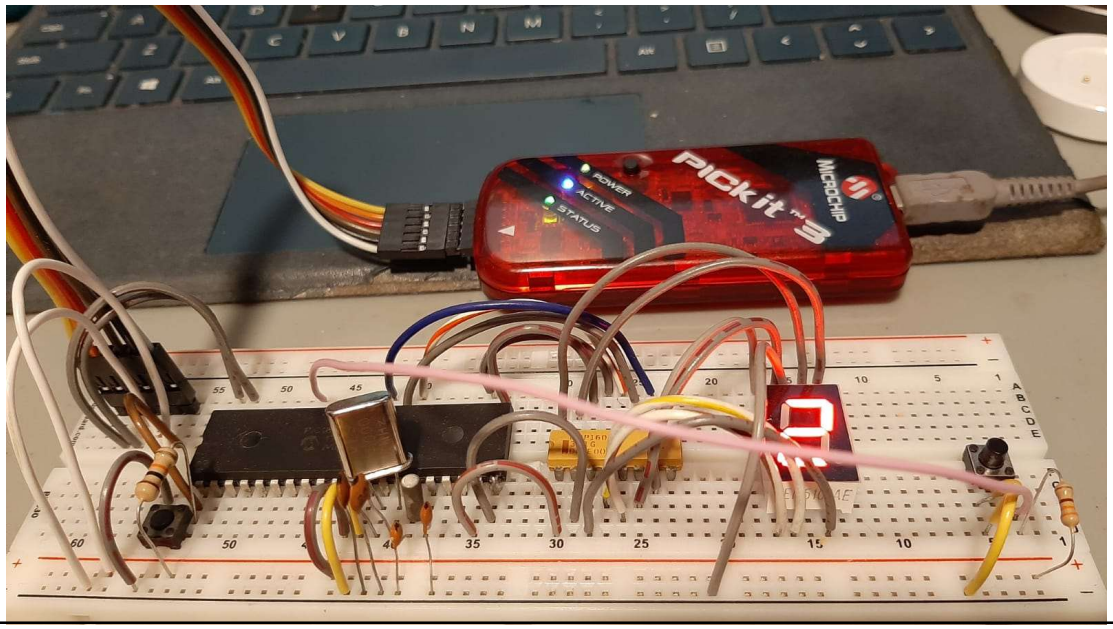
Circuito implementado



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