

Memory Hierarchy

Primary memory / physical / main mem : (original)

RAM → constant power supply voltage
 ROM → X, non-volatile } chip memory, expensive, fast

Secondary Memory : (to increase storage capacity)

HD →
 FD (floppy disk) } magnetic disk
 CD →
 DVD → } optional disk
 portable }

writable,
 non-volatile
 cheap
 need larger power

HD, FD, CD, DVD, pendrive (chip memory)

data acquiring rate =

rate of disk rotation (rpm)

(fast + cheap) → secondary memory need for more storage as it's cheaper than primary

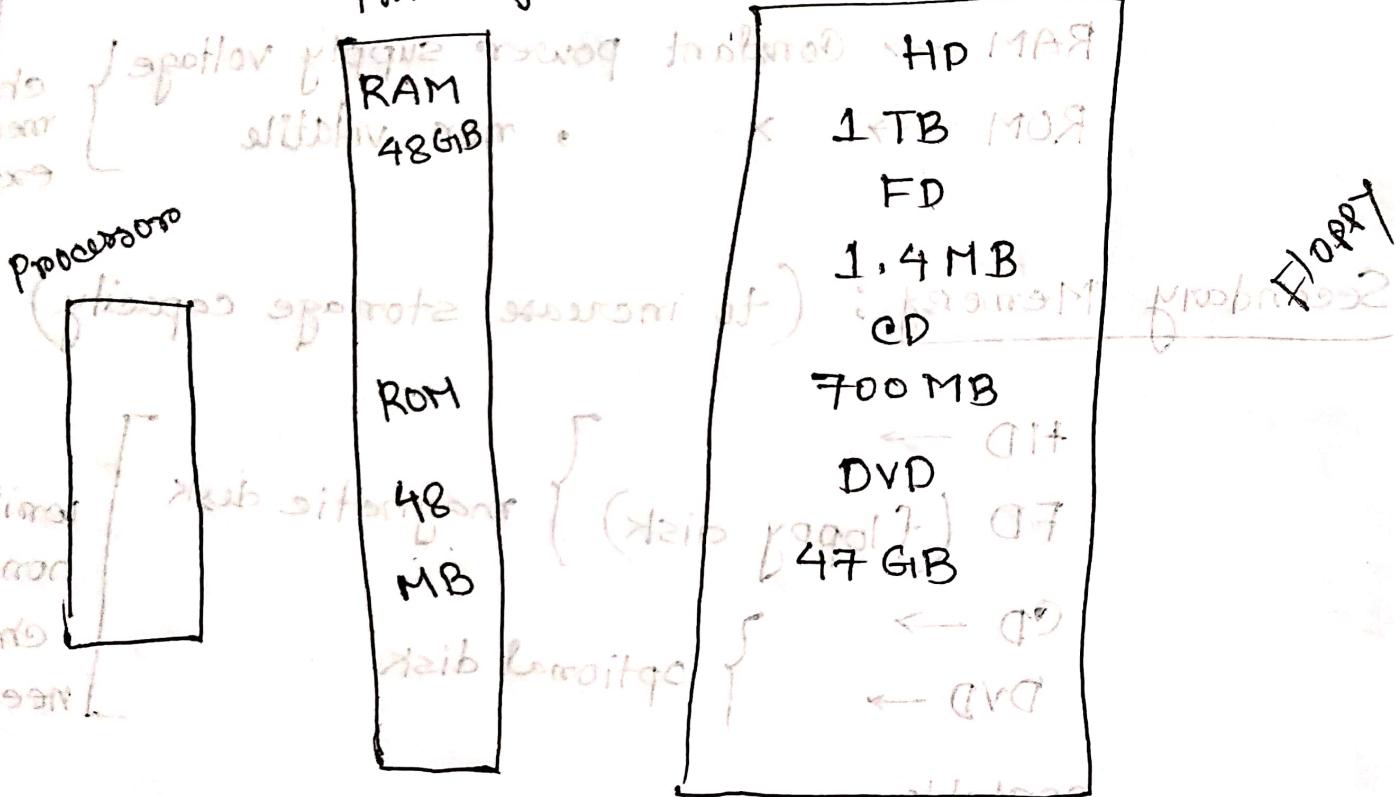
↓ ↓
 for operation for storage

Q: How speed increase of computer by increasing RAM size?

→ full RAM occupied रुक्ति गति, speed कम होती है। RAM पाल्पाल्क स्पेस बाकी, so speed बढ़ती है।

Memory Hierarchy

(Primary) : main memory / registers → Secondary



(Memory hierarchy) → G4, G3, G2, G1

= faster processing speed

(more) information available to user

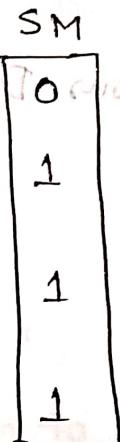
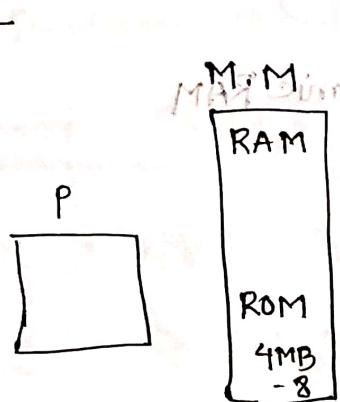
Not been
reported
before

Memory Hierarchy

pen-drive (flash ROM) → writable & non-volatile

SSD → Solid state disk → NO Rotation

ROM:



Viva

BIOS এর কাজ কী?

* BIOS প্রাক্তে ROM এ।

BIOS → Basic Input Output System → Booting Program

* OP Run → load in RAM → a program fetch OP in RAM
→ Booting Program (BIOS) → ROM (Primary)

SRAM	DRAM
Static RAM	Dynamic RAM
Speed fast	slow
cost high	low
used in cache	M.M
power consumption low	high
use flip flop	use capacitors

BDOM with Garments

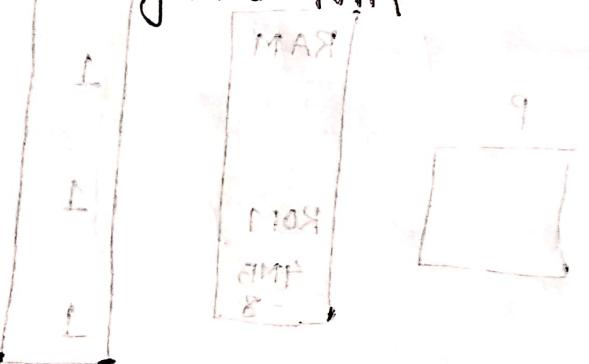
~~SRAM~~ ~~DRAM~~

modification → old state → new state bits → CPU

SDRAM

AVIV

Synchronous Dynamic RAM



Processor

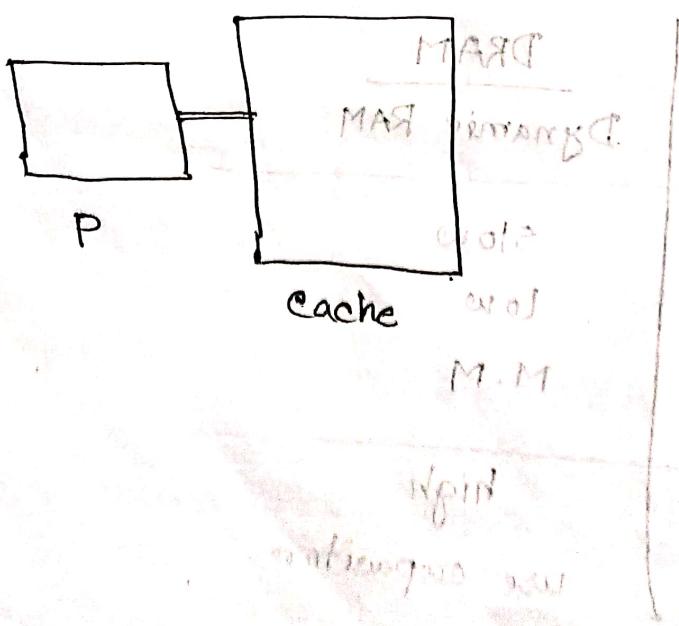
Cache

Main Memory

2nd Memory

MAU Not found in memory → MAR in bus → Bus slow তাই দ্রুত

(Garment) ROM → (e.g.) information আদর পদার্থ possible না।



Pentium
1993

→ এই prob solve কৃতি
পেটি আন্ত হয়,
পেটি fast কৈন??

Virtual Memory Management through Paging

Paging: It is a virtual memory management system. It

tells how information come from hard disk into RAM.

virtual memory তে RAM এ আরি-

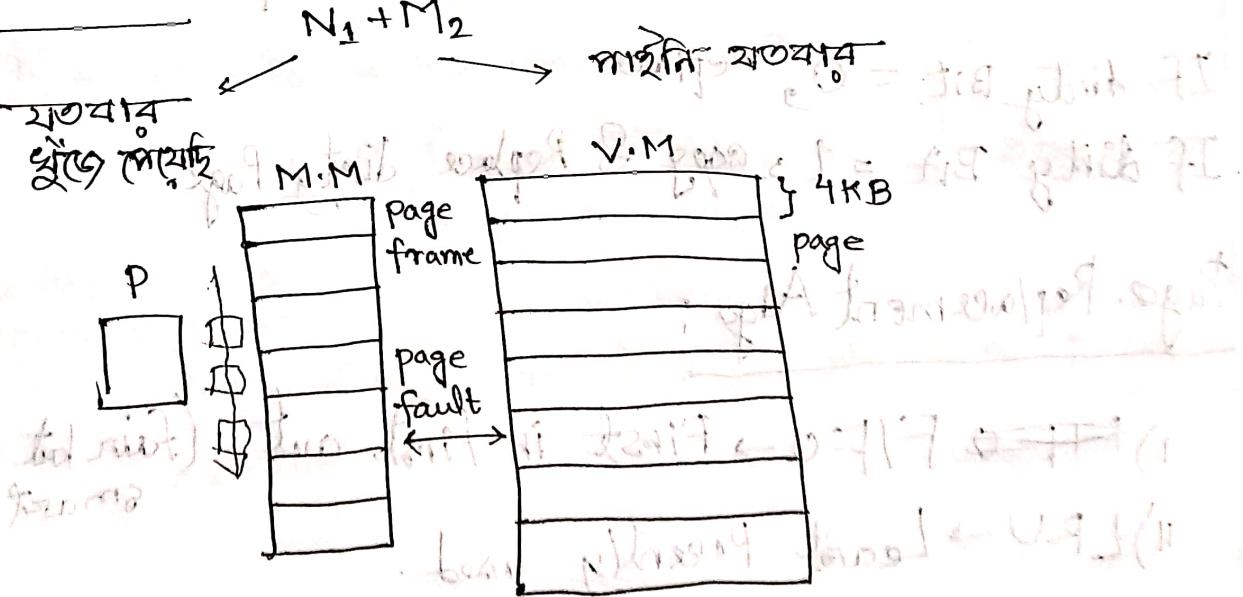
Page: Division of virtual memory

Page frame: Division of main memory

Hit: If processor find something in MM

Page fault: If processor don't find something in MM, go to V.M.

Hit Ratio: $\frac{N_1}{N_1 + M_2}$ number of hit upon total attempt.



প্রতিটি page এর size 4 KB.

* RAM full হয়ে গেলে, extra part রাখার জন্য RAM এর বিশুদ্ধ অঞ্চল Replace করবে।

Page Replacement:

Ques. What are the conditions for replacement?

Ans. 1. Page Fault अवकाश इसके बाद एक पैज़े का नियन्त्रण होता है।

2. Page should be empty यह जारी रखना लोड करने के लिए आवश्यक है।

Whenever there is page fault and there is no empty page available in main memory, page from the main memory is replaced by the page from virtual memory.

Dirty Bit: By default 0, when write operation.

If dirty Bit = 0, replace

If dirty Bit = 1, copy & Replace dirty Page

Page Replacement Algo:

i) ~~FIFO~~ → First in first out. (fair but not smart)

ii) LRU → Least Recently used.

iii) LFU → " Frequently "

Thrashing → When too many page faults.

frame no	1
10	1
2	2
1	3
3	4
5	5

LFU

* LRU — page that haven't used for the longest time will be replaced.

* LFU — Page with the lowest count will be replaced.

* Thrashing: Hit ratio drastically changes.

→ How to solve thrashing?

→ Replacement Algo change

Address translation:

Converting virtual Address into P/A Physical address.

frame	loc
10	1

location no change নাম্বা রই।

To know which page is in which frame, there is a table called page table.

frame & location are compare area.

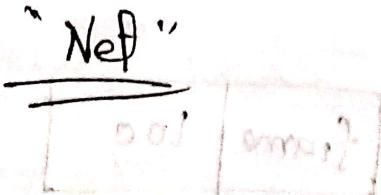
Frame	Address
1	0000 - 0111

* * Translation look ahead Buffer : (TLB)

TLB : Keep the most recently used entry/page

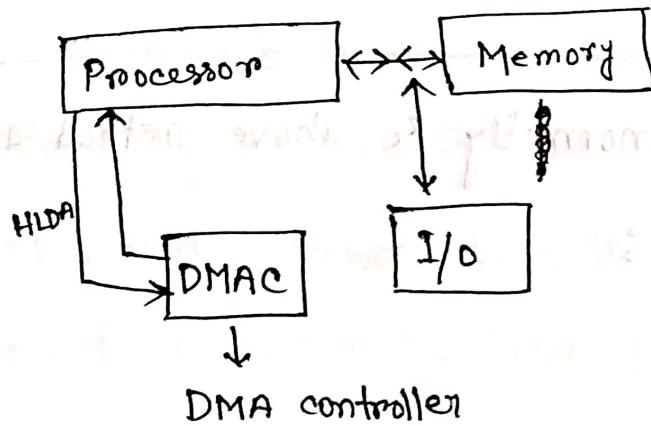
{ 1st search, TLB → then page table (slow) }

{ simultaneously search TLB & page table
TLB : 32 most recently page. }



DMA : Direct Memory Access

→ Transferring data between memory and I/O without utilizing processor.



- to do data transfer control signal is needed. that's why memory and I/O unit transfer data.
- DMA used for Bulk amount of data transfer.

Bus master → control bus করে

processor → control signal generate করে

Read → a control signal যা মুদ্রণ করবে।
 → Data memory দ্বারা processor এ

Q: কেন অন্যান্য memory & I/O এর মাধ্যমে data transfer
 করতে পারি না?

Q: What is DMA concept? কাকেন মে করি?

2টি byte এর জন্য total 4টি step. Small amount.

- যখন শুধু heavy amount of data transfer প্রয়োগ
- তখন DMA controller. Hardware based.

* এই instruction এর ক্ষেত্রে normally & above method এ
বিশেষ কার্য করা। example :

instruction:

take data → MOV AX, 2000 H

Send (to I/O)

INC address

DEC count of byte

check loop

এখানে, একটি byte এর জন্য processor এ 5টি fetch হবে,

5টি decode হবে,

1 byte এর জন্য একে loop 1 বাবু হুবে

1 KB

1000 & 1 KB transfer হবে

Q: How/Why DMA efficient?

1. এমনি- data transfer directly & Oz, processor কে আজে না so cycle করে যায়।
2. As it's hardware based তাই এমনি- fetching and decoding এর দ্বা অল্পতা instruction দিত হয় না।
(It's not software based, transfer is hardware based so, it required no time for fetching & decoding).

steps

1. DMAC give hold=1
2. P relinquishes system bus
3. P gives HLDA
4. DMAC perform data transfer
5. DMA gives hold=0
6. P again become bus master

→ DMAC এর টুইটা reg,

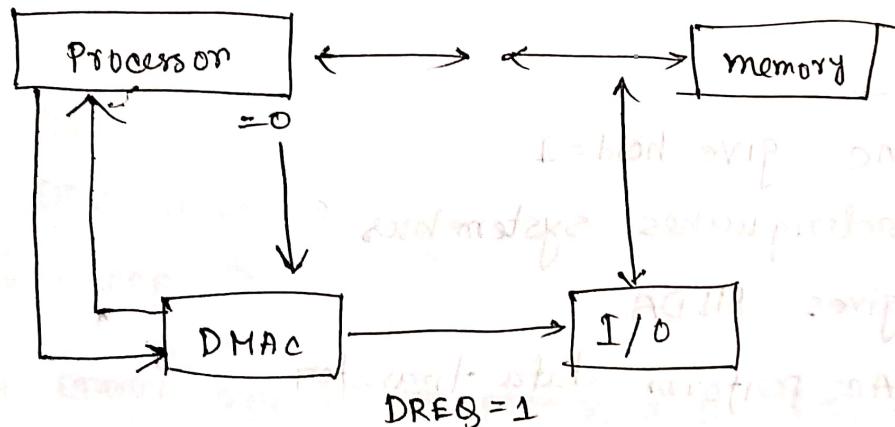
* CAR → current address register

Transfer করার file এর starting address
(দিয়ে দিয়ে)

CWCR → Current Word count Register

(কতো bit / size transfer হবে তা দিব)

$P \rightarrow \text{DMAC} (\text{CAR} \& \text{CWCR}) \rightarrow$ wait for a CP
 confirmation $\rightarrow \text{DMAC } h=1; \Rightarrow \text{HLDA}$
 $\rightarrow \text{ACK to I/O} \rightarrow \text{DMAC starts data transfer}$
 $\rightarrow \text{CAR}++$, $\text{CWCR}...?$
 $+ \text{IR} \& \text{CWR} = 0$ (terminal)
 based on which set information, based on which base address
 (probably 15 greatest) no waiting required for I/O



Wed CT : reference and proceed map 9

pipelining addressing mode

Cache mem mapping

Mapping (state diagram तथा)

Types of DMA :

- 1) Block transfer/Burst Method
- 2) Cycle stealing/1 byte transfer
- 3) Demand Transfer
- 4) Hidden Mode

Processor

কঠোর স্বাক্ষর করে রয়েছে

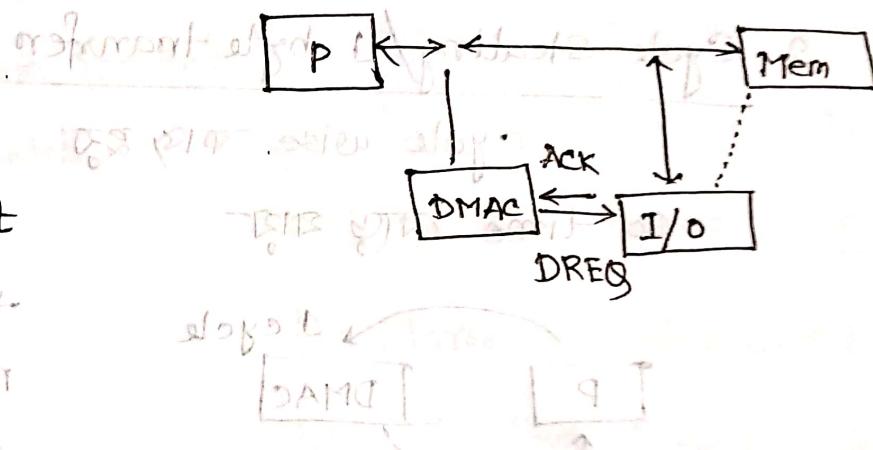
Q: What is DMA?

→ For 4 marks,

DMA concept

Diagram

6 steps



Q: How does DMA work?

DREQ → এই signal দ্বারা output device connected কিনা।

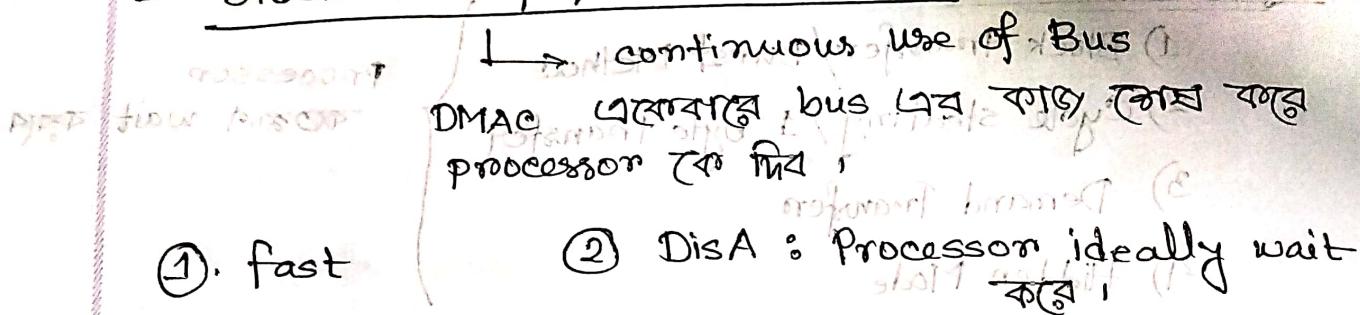
I/O ready হলে DREQ = 1

ACK → acknowledgement signal (যে printer sleep mode এ নাই।)

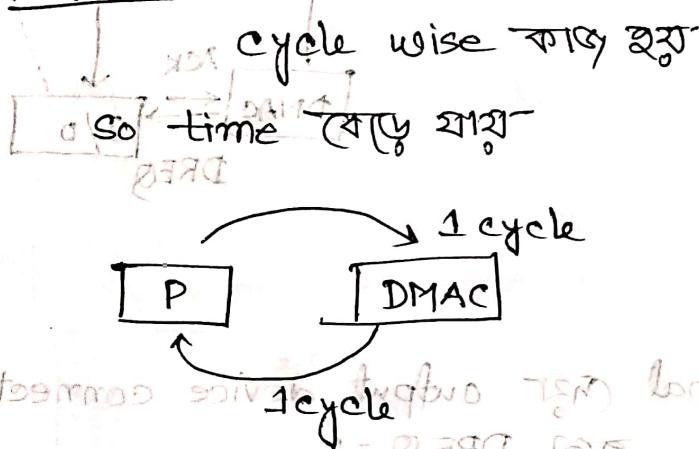
এখানে- সুবিধা, এখানে- fetch বা decode করা জাণেনা just execute হতে।

① WCR = 0 হলে- যাবে।

1. Block transfer / Burst Method



2. Cycle Stealing / 1 byte transfer



time consuming but
not more than the
traditional way.

3. Demand Transfer (Added feature)

DREQ ক্ষমতা, continuous check করে i/o ready
DREQ → 0 or 1 পর্যন্ত printer করে ready
হবে।

4. Hidden Mode :

Processor যখন খেনে কাজ করে না তখনই req পার্শ্ব
Otherwise not.