Department of Computer Science and Engineering

CSE 345 Project Report

Course Name: Digital Logic Design

Course Code: CSE 345

Name of the Project: 7 Segment Display Using K-map

Submitted To:

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Objective:

A seven-segment indicator is a popular digital device for representing numerical values in electronic instruments (e.g. clocks, calculators and counters). In this work a seven segment display is designed by means of Karnaugh Map (K-map) reduction which leads to minimized Boolean expressions for each segment. The implementation is capable to receive as input a 4-bit binary and produce all the necessary output states that can be shown on a seven-segment led display corresponding to decimal digits between 0-9. The simplified logic is implemented and verified through simulation using **Quartus II software**.

Equipment's:

1. bread board - 3pc

2. 9v Battery

3. Bread Board Power Supply

4. Jumper Wires

5. Seven Segment 1 digit Display RED(CC)

6. Gates: 7404 NOT gate - 1pc,

7408 Quad 2 input AND gate - 2pc,

7432 Quad 2-input OR gate – 2pc,

4072 IC Dual 4-Input OR gate – 3pc,

7. Resistance 1k,100k,

9.   4 INPUT switch

10. 9V Battery connector with DC jack

Truth Table:

Let A, B, C, D be the 4-bit binary input.

Decimal	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

K-map:

For a,

AB\CD	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	x	x	x	x
10	1	1	x	x

a $= A + BD + C + B'D'$

For b,

AB\CD	00	01	11	10
00	1	1	1	1

11	x	x	x	x
10	1	1	x	x
01	1	0	1	0

b = B' + C'D' + CD

For c,

AB\CD	00	01	11	10
00	1	1	1	0
01	1	1	1	1
11	x	x	x	x
10	1	1	x	x

c = C' + D + B

For d,

AB\CD	00	01	11	10
00	1	0	1	1
01	0	1	0	1
11	x	x	x	x
10	1	1	x	x

d = A + B'C + CD'

    +B'D' + BC'D

For e,

AB\CD	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	x	x	x	x
10	1	0	x	x

e   = B'D' + CD'

For f,

AB\CD	00	01	11	10
00	1	0	0	0
01	1	1	0	1
11	x	x	x	x
10	1	1	x	x

f   = A + C'D' + BC' +BD'

For g,

AB\CD	00	01	11	10
00	0	0	1	1
01	1	1	0	1
11	x	x	x	x
10	1	1	x	x

g   = A + B'C + BC' + CD'

Boolean Function:

a= A+BD+C+B'D'

b= B'+ C'D'+ CD

c=C'+D+B
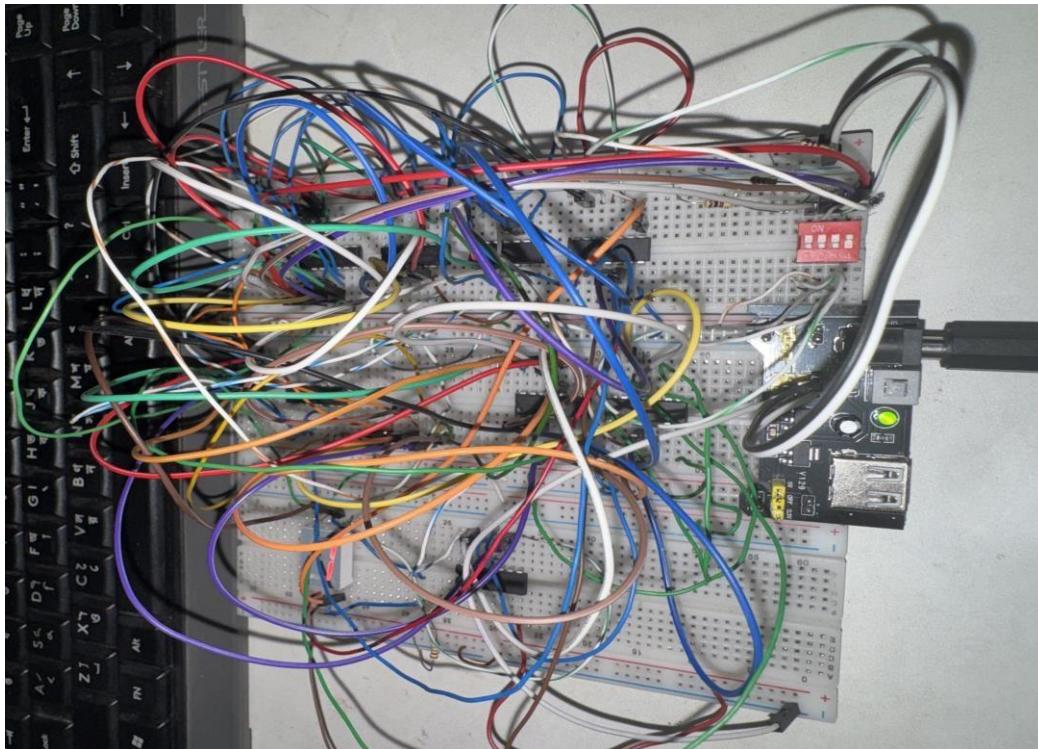
d= A+B'C+CD'+B'D'+BC'D

e=B'D'+CD'

f=A+C'D'+BC'+BD'

g=A+B'C+BC'+CD'

BCD to Seven Segment Circuit From K-map Functions:

Implementation:

Attached 3 Bread Board together . The ground and 5V rails were evenly spaced throughout each board, and a regulated 5V supply from an adjustable breadboard power module was utilized. Pin 7 was connected to ground and pin 14 to VCC, and the integrated circuit was oriented correctly. The K-map simplifications were used to create the segment-control functions a, b, c, d, e, f, and g, which were then implemented and routed to the proper output lines.
Switches positioned appropriately on the breadboard for the input section.
One terminal on each switch was linked to the input line, and the other terminal got 5V. To reduce noise and guarantee steady logic levels, a 100 kΩ pull-down resistor was employed for every input.

Place Seven Segment Display (CC) in bread board. A 1 kΩ current-limiting resistor was used to link the display's pins 3 and 8 to the ground rail. The respective segment pins of the display were then linked to the outputs of the K-map-based logic functions:

- **Pins 1 and 2 → segments e and d • Pin 4 → segment c**
- **Pins 6 and 7 → segments a and b**
- **Pins 9 and 10 → segments g and f**

Used valid truth table for checking the final Output.
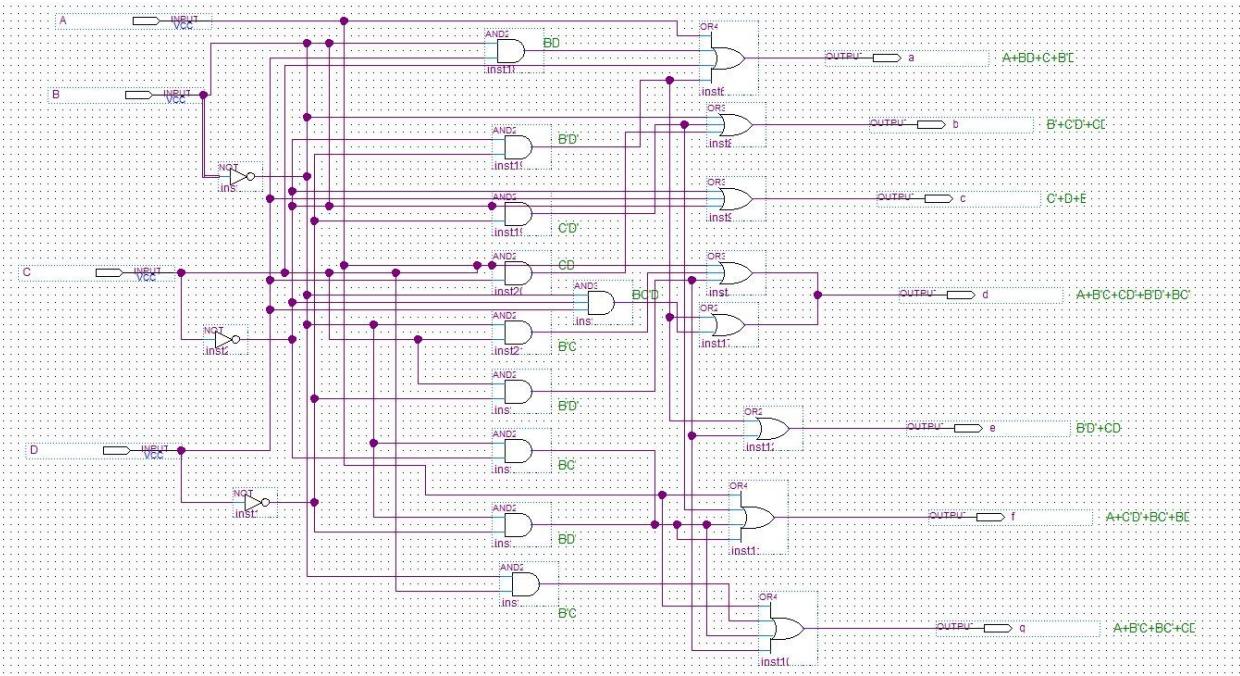
Verilog Code:

```
module seven_segment(
    input A, B, C, D,
    output a, b, c, d, e, f, g
);

assign a = A | (B & D) | C | (~B & ~D);
assign b = (~B) | (~C & ~D) | (C & D);
assign c = (~C) | D | B;
assign d = A | (~B & C) | (C & ~D) | (~B & ~D) | (B & ~C & D);
assign e = (~B & ~D) | (C & ~D);
assign f = A | (~C & ~D) | (B & ~C) | (~B & ~D);
assign g = A | (~B & C) | (B & ~C) | (C & ~D);

endmodule
```
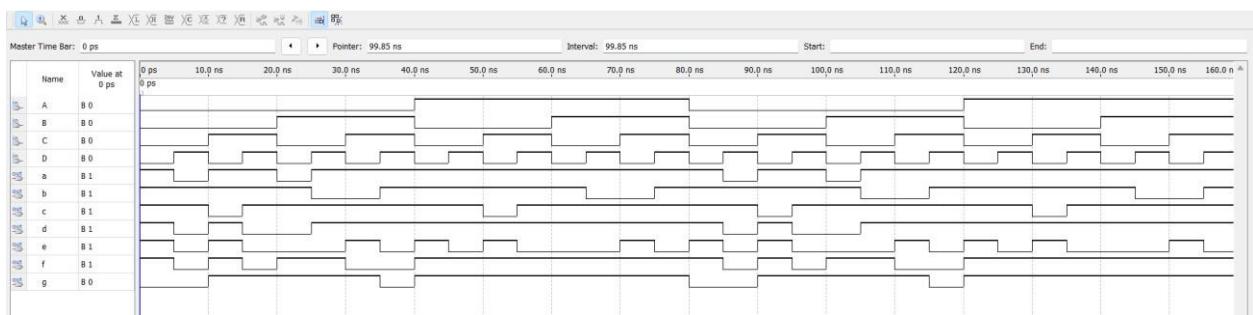
Schematic Circuit:

Waveform:

Discussion about this project:

In this report a seven segment display is designed successfully with the help of K-map techniques. The use of K-maps also facilitated reduction of complex Boolean expressions to simpler forms that in turn reduced the number of required logic gates to implement. By this reduction, the circuit became more optimized and simple to devise.

Quartus II simulation results indicated that the output segments reacted positively by each of 4bit input as decimal values from 0 to 9. Any early mistake on the segment activation was addressed by checking the truth table and grouping of K-map. In general, the project offered a hands-on experience with logic minimization, combinational circuit design and digital simulation.

Conclusion:

This project demonstrated the design and implementation of a seven-segment display using Kmap simplification. Using Karnaugh Maps allowed us to simplify complex Boolean expressions, which reduced the number of logic gates needed in the final circuit. This made the overall design more efficient, cost-effective, and easier to understand. The simulation conducted in Quartus II confirmed that the circuit accurately displays decimal digits from 0 to 9 for all valid input combinations. This project also improved skills in creating truth tables, simplifying logic with Kmaps, and implementing combinational circuits in simulation software. Overall, the project lays a solid foundation for understanding digital display systems and can be expanded in future work to include real hardware implementation or additional display features.