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29.04.2024
EE102-1 Lab 7 Report

LAB 7: FSM DESIGN
Realistic Traffic Light Simulation

Purpose

The purpose of this lab is to design a Finite State Machine (FSM) on the breadboard. On this design logic IC's are used.

Design

On this lab, I designed a traffic light simulation with fsm logic. Output of circuit depends onlythe present state, which means it is a Moore Machine. It has 4 states: ready, pass, stop, don't pass. It simulates usual traffic lightning. Initially, when it is not in reset state, it lights don't pass state. Without the reset condition,the lights change state with every clock cycle. I used 5 different leds, 2 red and 1 green for traffic simulation and 2 leds for flip flop datas. R2: Yellow, R1: Red

STATES:
Don't pass: S0 : Y-R2
Pass: S1: Y
Ready: S2 : R1-R2
Stop: S3: R1

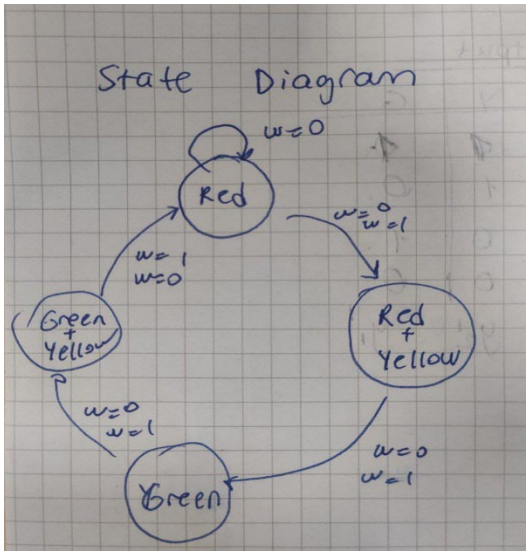

Figure 1: State Diagram

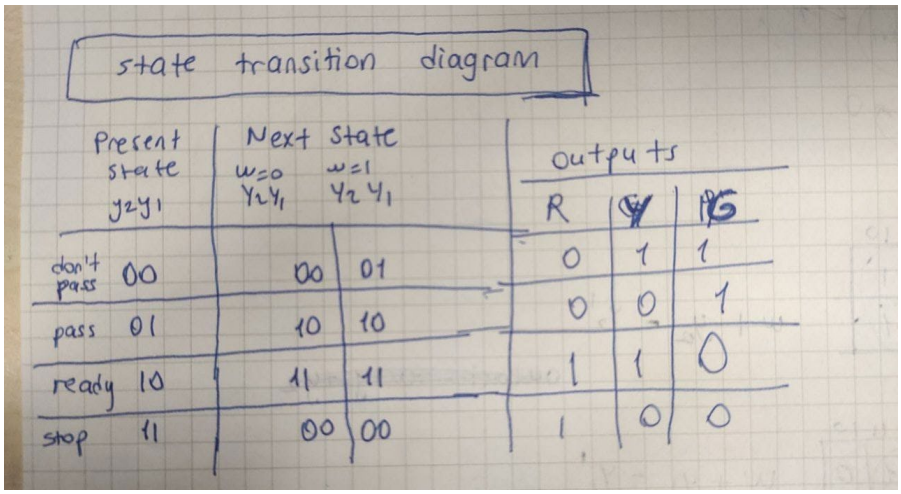

Figure 2: State Transition Diagram

The red(R1) led was high when Q' output of initial flip flop arrives. As long as clock is low, it remains on. No pulses makes the yellow(R2) on. When high clock arrives, output becomes inverse and output Q of FF1(LSB Flip Flop) AND output Q' of FF2(MSB Flip Flop) makes green led on. The green led is on only when both are high.

Methodology

On my design, I implement 1 74HCx74 D Flip Flop and 1 2 input 74HCx08 And Gate. 1 component of flip flop was enough to use for two flip flops. Additionally, I connect the inputs and outputs, datas, preset, clear, Vcc, ground pins to correct places. After the implementation, I get correct results when I connect +, - , provide 5V voltage and 0.5Hz frequency 2.5Vpp amplitude signal generator cables.

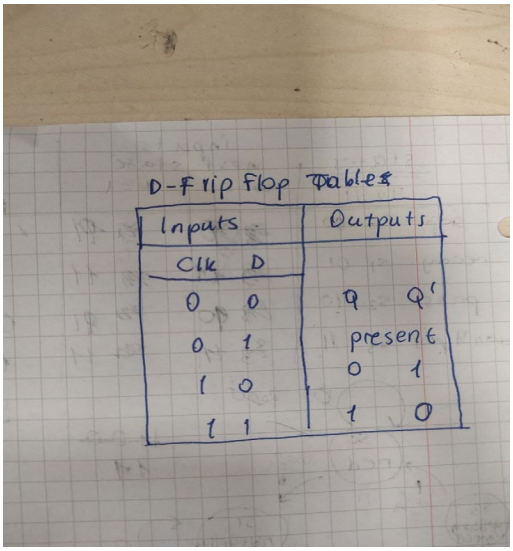

Figure-3: D Flip Flop Table

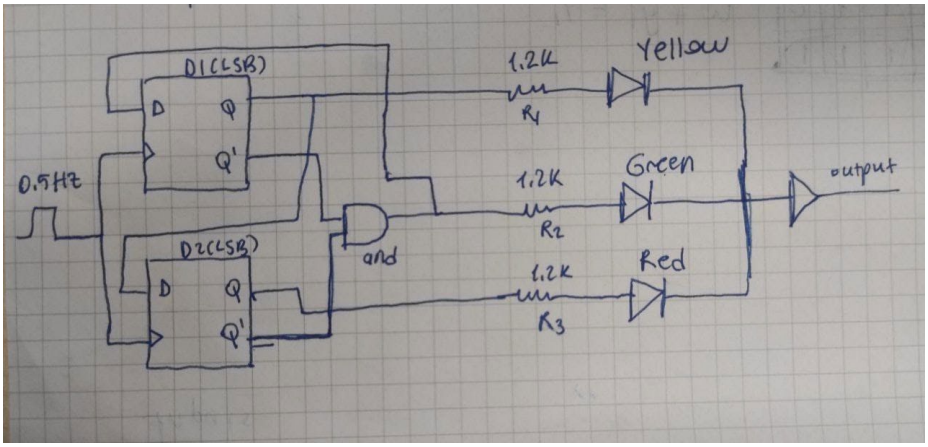

Figure-4: Schematic Design

Results

On this lab, after implementation, my results matched with state transition diagram (figure-2). The experiment was succesfull. However, due to my design, I did not show the reset condition, and it allowed me to have a realistic traffic light simulation.

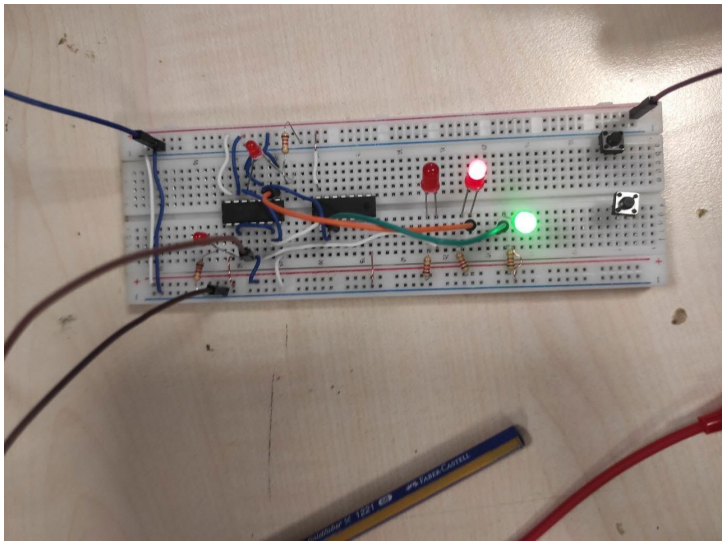
Figure-5: Don’t pass: S0 : Y-R2

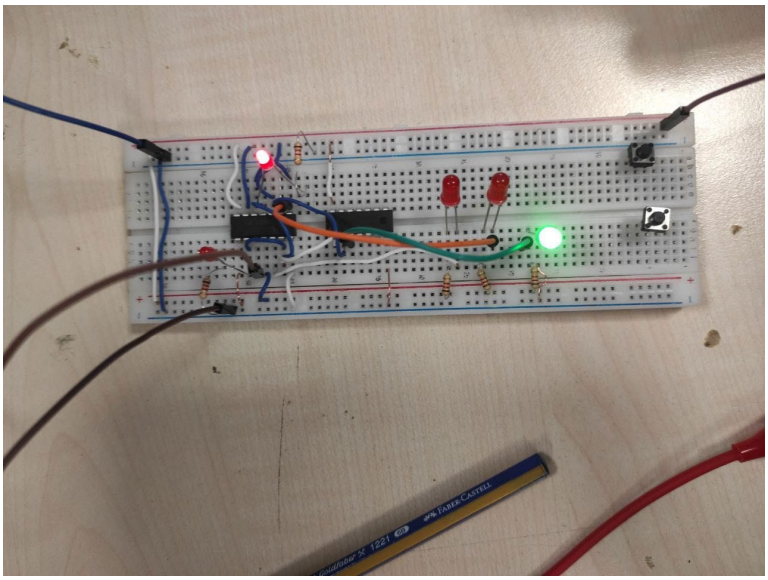

Figure-6: Pass: S1: Y

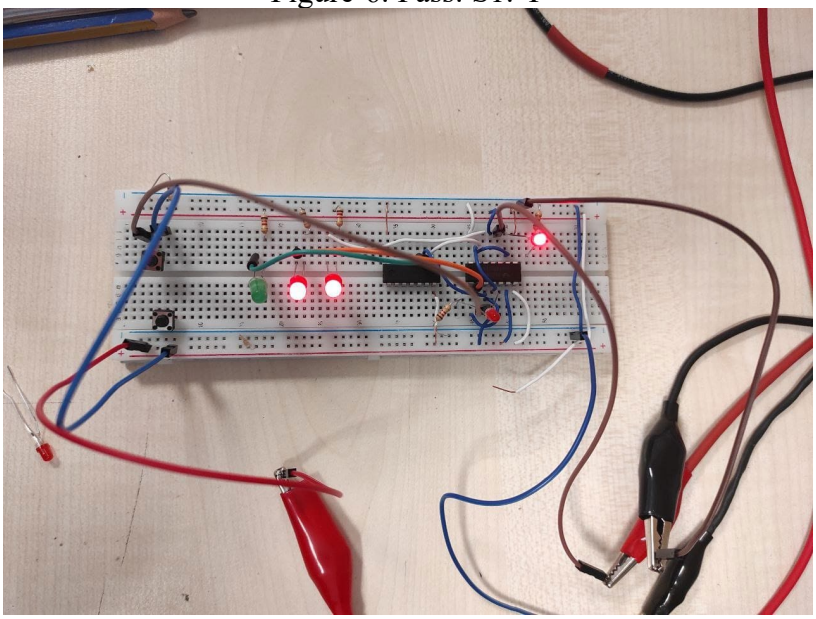

Figure-7: Ready: S2 : R1-R2

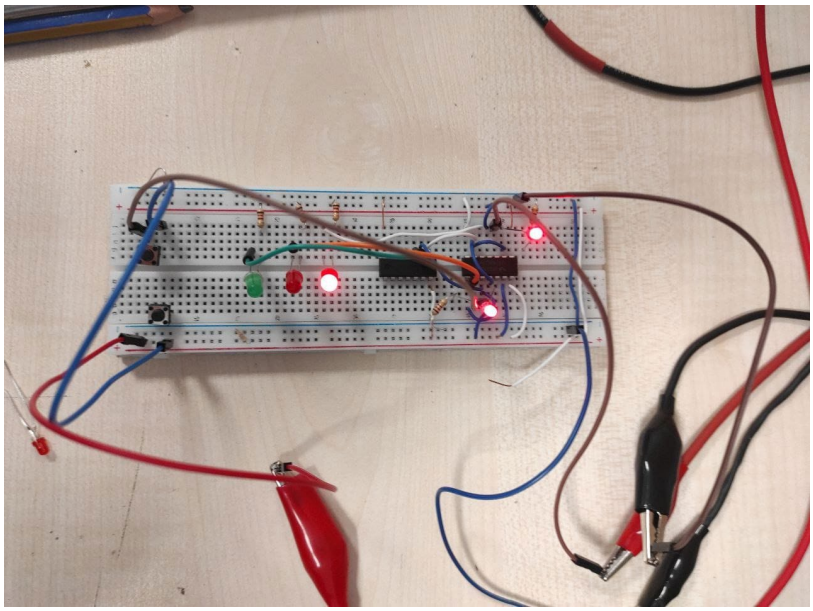

Figure-8: Stop: S3: R1

Conclusion

In conclusion, on this lab, I gained knowledge about finite state machine design and implementation. I learned differences between moore and mealy machines. I learned how to assign a state diagram, write its transition diagram, and from inputs writing karnough maps and drawing circuit schematic. Errors on this lab was generally related with inconnections between jumper cables.

References

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