Specification Document

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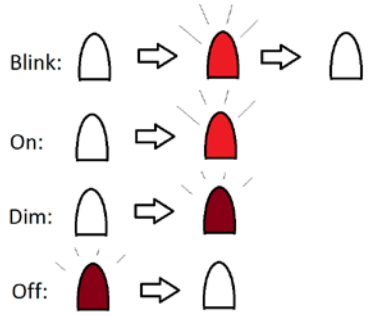
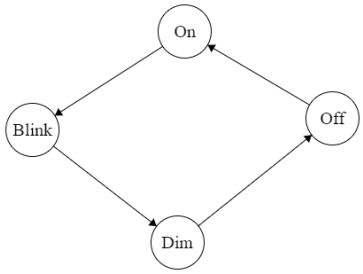
The purpose of this circuit is to run a bike light, with one input and one output. The only input for this circuit is the button, which is responsible for changing the state of the bike light. The only output is the LED, which will be in one of four possible states at any given time: off, on, blinking, or dim. The clock has a frequency of 32,768 Hz. The blink has a delay of 16,384 clock cycles or 0.5 seconds. The dim has a delay of 256 clock cycles, or .007 seconds.

Operational Modes:



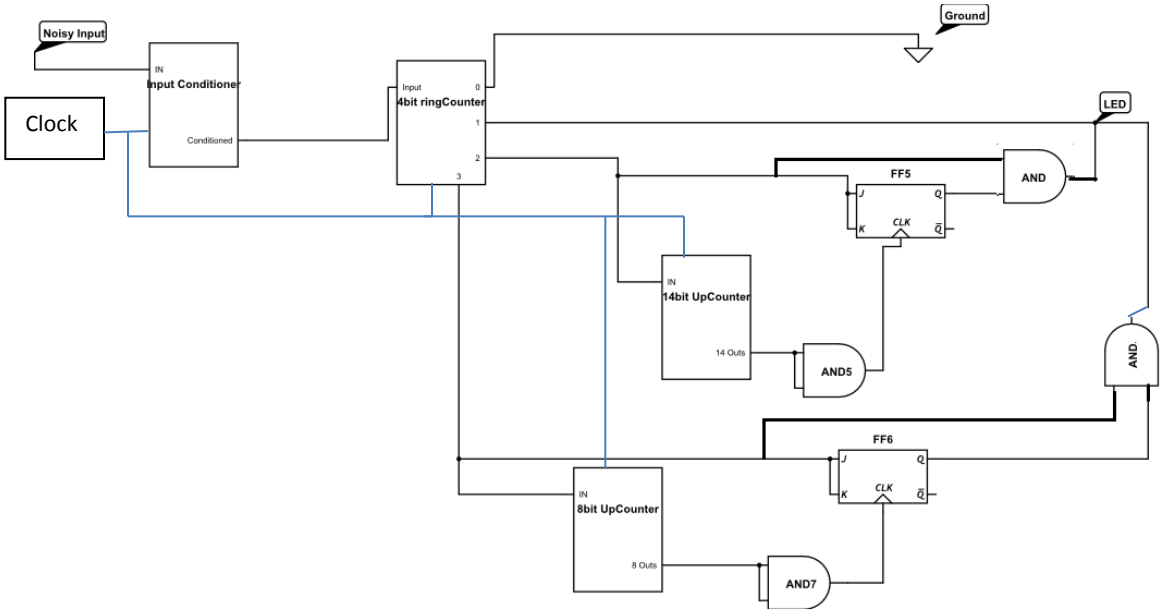
(Blink Patterns)



(FSM Diagram)

Current State	Input	Next State	Output
Off	Press	On	LED is unpowered
On	Press	Blink	LED is powered steadily
Blink	Press	Dim	LED is alternates between powered and unpowered
Dim	Press	Off	LED is partially powered

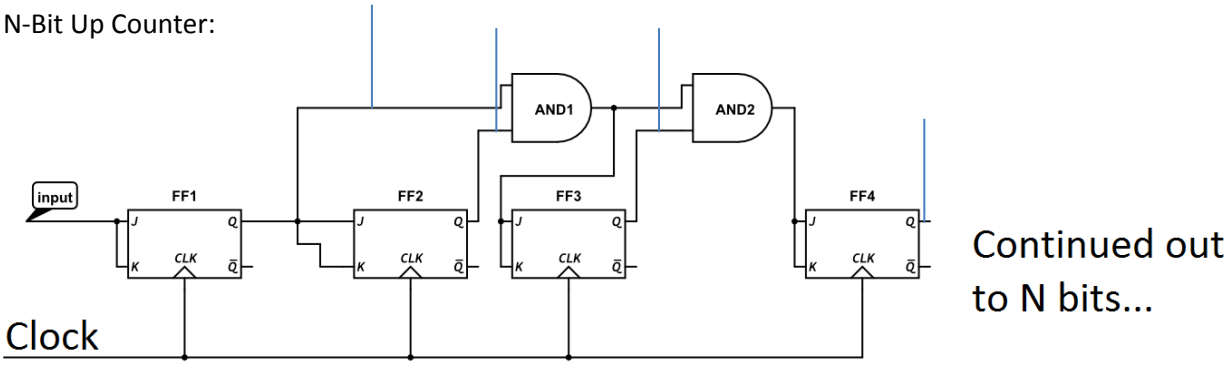
Block Diagram



The system works by using an input conditioner to make the button press useful, which increments the 4 bit counter, cycling through the four possible states. The 0 position is off, 1 is on, 2 is blinking, and 3 is dim.

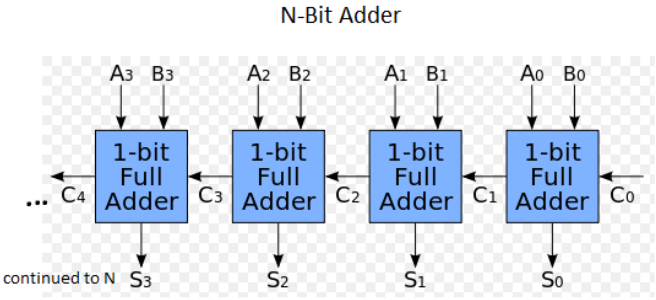
Total cost: 547

N-Bit Up Counter:



This circuit is responsible for slowly propagating a signal through it, allowing for things like dimming and blinking lights. For the purpose of this circuit, it is 14 or 8 bits for the blinker in order to give it a 0.5 seconds of on and off and the dimmer respectively. The inputs are the signal to be delayed and the clock. The output is the number of bits of the up counter in wires, which will be go to an and gate to be sure it only fires when all the JK flip flops are toggled on. The size of this is 166 inputs for 14-bit, the size is 94 for 8-bit. The cost is 179 for 14-bit, the size is 101 for 8-bit.

N-Bit Adder:

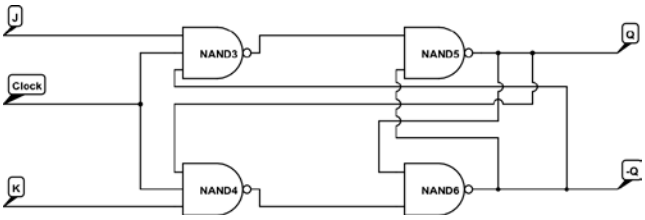


https://commons.wikimedia.org/wiki/File:4-bit_ripple_carry_adder.svg

The n bit adder is responsible for adding up an n bit binary number to another n bit binary number. This is used in this circuit to help the input conditioner to count to the appropriate number of clock cycles for

the input to stabilize. The inputs are Carryin0, all A's, and all B's. The outputs are all the Sums. The size of this component is n*10, or 60 for its use in this circuit. The cost is 25*n or 150 for this circuit.

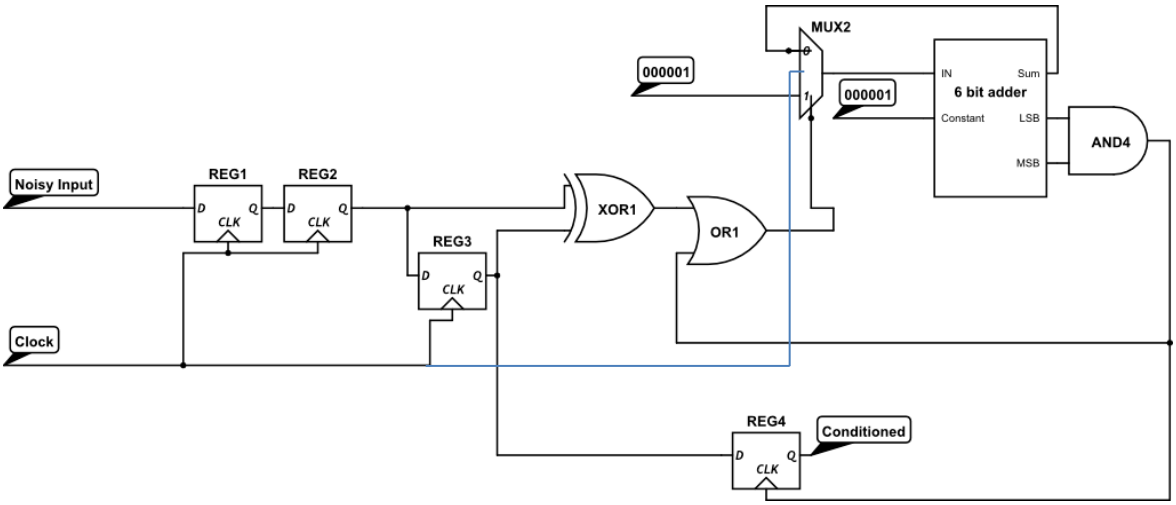
JK Flip Flop:



The JK Flip Flop is responsible for holding a state and toggling when necessary between propagating an on or off state. This part is used in the up counter in order to economize on space and allow for large amounts of counting with only a few flip flops. The inputs are the clock, the J data, and the K data. The outputs are Q and –Q.

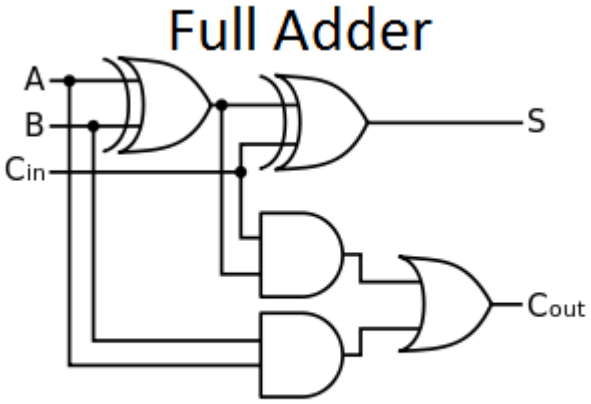
The size of this component is 10 inputs. The cost is 10.

Input Conditioner:



The Input Conditioner is responsible for debouncing the input from the button. It works by first synchronizing the input using two D-Flip Flops, then compares the current value of the input with the last value of the input, and continues to do so until the 6 bit adder adds to the appropriate number of clock cycles, being 33, when the debouncing is complete. The signal is then propagated through. If at any point the input changes, the adder will reset and begin counting again. The inputs are the clock and the noisy input. The output is the conditioned signal. The size is 125 inputs. The cost is 228.

Full Adder:



https://en.wikibooks.org/wiki/Microprocessor_Design/Add_and_Subtract_Blocks

The full adder takes in two binary values and adds them together. This is a one bit full adder, so it is only capable of taking in two one bit binary numbers and adding them. It has three inputs: A input, B input, and carryin. It has two outputs: Sum and carryout. The size of this system is 22 inputs. The cost is 25.

Sources:

http://madebyevan.com/fsm/