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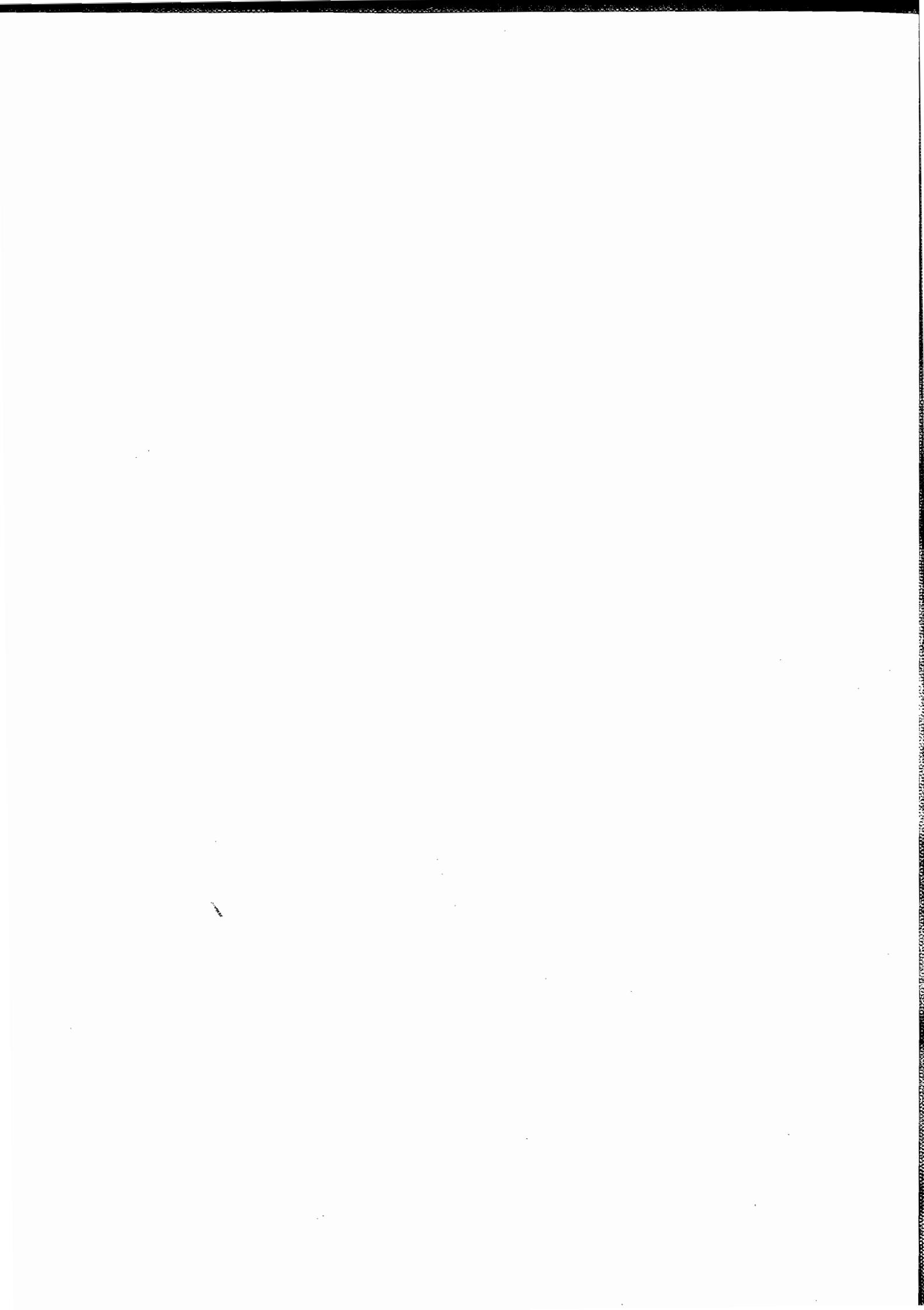
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SUBJECT:-.....

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- SPIRAL BINDING, HARD BINDING
- TEST PAPER FOR PSU, GATE, IES
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Lecture - I

Temperature (in K) :-(i) Absolute temperature :-

$0\text{K} = -273^\circ\text{C}$ → Reference temperature

→ Below it no temperature exist and no device work at this temperature.

(ii) Room temperature :-

$300\text{K} = 27^\circ\text{C}$ (Never constant).

But if in problem temperature is not given take it 300K .

(iii) Ambient Temperature (T_A°) :-

$290\text{K} = 17^\circ\text{C}$ → Surrounding temperature

→ All common system deals with T_A

e.g:- SNR,

Temperature Conversion :-

Temperature in $^\circ\text{C}$ = Temperature in Kelvin
 - 273

⇒ Temperature in Kelvin = Temperature in $^\circ\text{C}$ + 273

$$0\text{K} = \text{K}$$

→ Latest notation.

Old notation

$$f \rightarrow \text{Hz or cycles/sec}$$

↓
Latest

Notation

↓
Old notation.

Thermal Voltage:-

- denoted by V_T or V_t or V_{th}
- voltage equivalent of temperature

$$V_T = \frac{kT}{q} \text{ volts}$$

T = Temperature in kelvin

q = charge = $1.6 \times 10^{-19} C$

k = Boltzmann's constant

Boltzmann's Constant:-

$$k = 1.381 \times 10^{-23} J/\text{K}$$

$$k = 8.62 \times 10^{-5} \text{ eV}/\text{K}$$

$$V_T = \frac{T}{11600} \text{ volts}$$

$$V_T \propto T$$

$$\text{At } T = 0 \text{ K}, V_T = 0$$

$$\text{At } T = 300 \text{ K}, V_T = \frac{300}{11600} = 0.02568 \text{ volts}$$

$$\Rightarrow V_T = 26 \text{ mV} \quad \text{at room temperature}$$

- For large variation in temperature (0-300 K) there will be small variation in thermal voltage (0-26 mV)
- The standard room temperature corresponds to a voltage of 26 mV
- Semiconductor devices are sensitive to temperature very much.

Electron Volt (eV) :-

- It is the practical unit for energy in electronics.
- Very small compare to Joule.
- 1eV is defined as the energy gained by the electron in moving through a potential difference of 1V.
- Air is perfect insulator.
- Vacuum is a conductor.
eg:- vacuum tube, picture tube, CRT
- Relative permittivity ϵ_r (air) ≈ 1 (slightly > 1)

$$\epsilon_r (\text{vacuum}) = 1$$

$$\begin{aligned} \rightarrow 1\text{eV} &= 1\text{J} \times 1 \\ &= 1.6 \times 10^{-19} \text{C} \times 1 \text{ Volts} \\ &= 1.6 \times 10^{-19} \text{ C.Volt} \end{aligned}$$

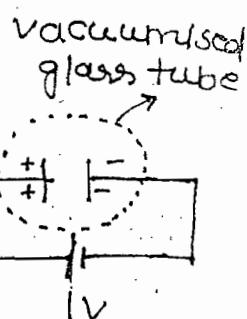
$$\Leftrightarrow 1\text{eV} = 1.6 \times 10^{-19} \text{ J}$$

- 1J energy can't applied to e's bcz. of very less capacity

$$K.E = \frac{1}{2} m v^2 \text{ J}$$

$$P.E = q \cdot V \text{ J}$$

- eV indicates the amount of kinetic energy gained by the electron or potential energy lost by the electron.



K.E Gained = P.E lost by \vec{e}

$$\Rightarrow \frac{1}{2}mv^2 = qV$$

$$\Rightarrow \text{Velocity of } \vec{e}, \boxed{v = \sqrt{\frac{2qV}{m}}} \text{ m/s}$$

→ It is the equation for the velocity of \vec{e} in terms of applied voltage (V)

Electric field Intensity :-

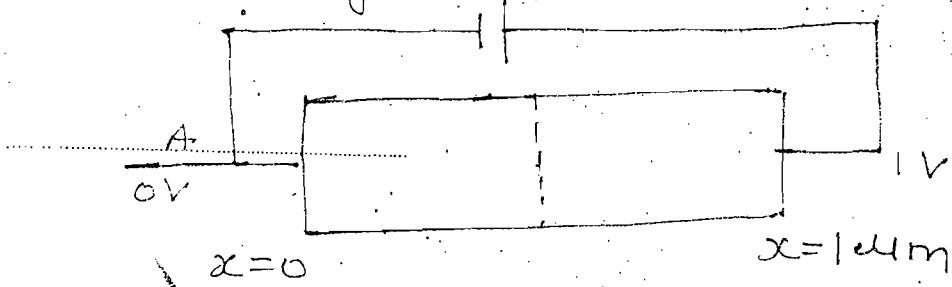
→ Also known as field gradient or field intensity or field

→ denoted by E or \mathcal{E}

$$\rightarrow \boxed{E = -\frac{dv}{dx} \text{ V/m}}$$

$$\rightarrow |\mathcal{E}| = \frac{1 \text{ voltage existing or applied}}{\text{distance or spacing}}$$

ques:- considering a uniform semiconductor bar



Find field intensity at the centre of bar and at the end of B.

SOLN:- (i) Field intensity at the centre of bar

$$|\mathcal{E}_c| = \frac{|V_c|}{x_c} = \frac{0.5V}{0.5 \times 10^{-6}} = 10^6 \text{ V/m}$$

(ii) Field intensity at the end of B

$$|\mathcal{E}_B| = \frac{|V_B|}{x_B} = \frac{1V}{1 \times 10^{-6}} = 10^6 \text{ V/m}$$

$$(iii) |\mathcal{E}_A| = \frac{|V_A|}{x_A} = \frac{0}{0} = ???$$

Mobility of charge carriers:-

→ Mobility is defined as

$$\mu = \frac{\text{drift velocity}}{\text{field intensity}}$$

$$\frac{m_e}{m_h}$$

⇒ scattering time

$$\mu = \frac{v_d}{E_0}$$

→ Unit for $\mu = \text{m}^2/\text{sec} \text{ or } \text{cm}^2/\text{vsec}$

→ Drift velocity always greater than normal velocity.

→ Mobility indicates how fast is the E's or the hole is moving from one place to another.

Gie Si

→ E mobility $\mu_n = 3800 \text{ cm}^2/\text{vsec}, 1300 \text{ cm}^2/\text{vsec}$

Hole mobility $\mu_p = 1800 \text{ " } 500 \text{ " }$

$$\Rightarrow \frac{\mu_n}{\mu_p} = 2.1 : 1 \quad 2.6 : 1$$

→ E mobility is always greater than μ_p & therefore E's can travel faster and will contribute more current when compared to the hole.

Gie → Higher conductivity
(Due to larger mobility)

→ Relatively more suitable for high frequency application

→ In Gie & Si switching times are very small & both are suitable for high frequency application. But Gie has larger BW & Gie is best for high frequency application.

→ Switching time in both Ge & Si are very small so can work on high frequency but Ge is better bcz its BW is high.

$$f \uparrow = \frac{1}{T},$$

Si

→ Relatively more suitable for switch application

[bcz in Si switching there is no false triggering]

→ suitable for high power application

→ Always mobility dec with temp for all devices. It is a universal statement

→ Mobility of charge carriers always dec with temperature

→ As temperature inc, the atoms in the material will vibrate and due to thermal vibrations the mobility of charge carriers dec.

$$\mu \propto T^{-m}$$

m is a constant and its value is equal to For Si For Ge

$$m = 2.5 \text{ for } e^-$$

$$m = 1.66 \text{ for } e^-$$

$$= 2.7 \text{ for hole}$$

$$= 2.33 \text{ for hole}$$

→ Mobility decreases with temperature as a non-linear variation

μ Vs E for a semiconductor :-

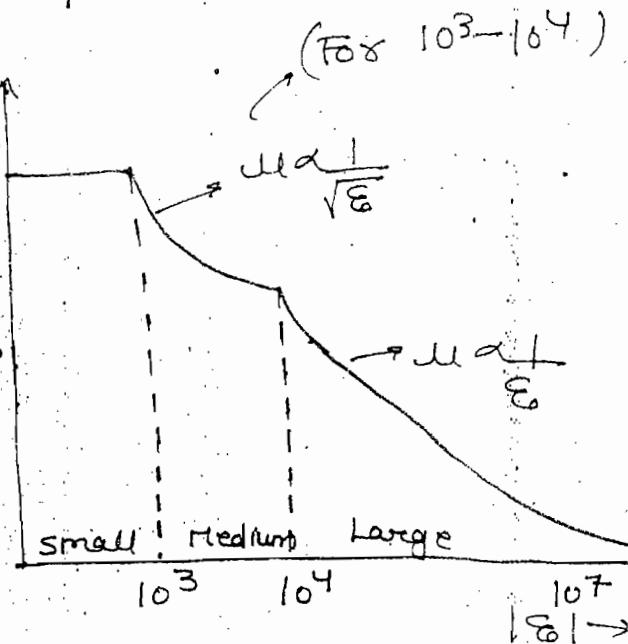
→ It is a experimental graph

$$\rightarrow v_d = \mu E$$

→ For smaller field intensity is applied to the semiconductor then

(i) Mobility of charge carriers will remain constant

(ii) drift velocity linearly increases with the field (E)



→ For larger field intensity is applied to the semiconductor then

(i) Mobility of charge carriers dec. with the field.

$$(ii) \text{ As } v_d = \mu \sqrt{E} \uparrow$$

↓ enter into saturation

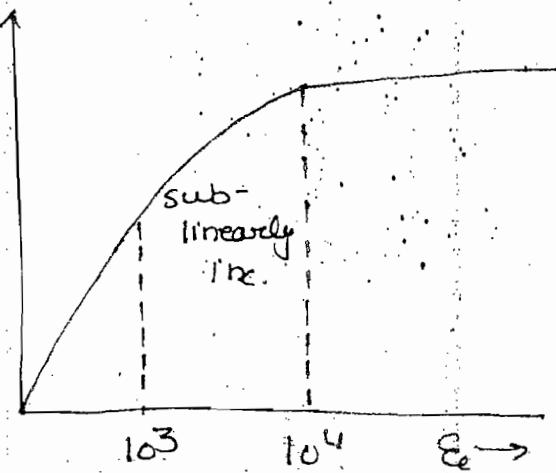
drift velocity will enter into saturation for larger fields applied.

v_d Vs E curve for a semiconductor :-

If a semiconductor

subjected to field intensity, $v_d \uparrow$
the drift velocity

(i) linearly inc., then sub-linearly inc and then enters into saturation with larger fields applied



Current:-

- current is defined as rate of change of charge. $i = \frac{dq}{dt} \text{ A}$
- In a semiconductor, there is a bipolar current i.e. current is carried by both e's and holes.

Drift Current:-

It is the flow of current through the material or device under the influence of field intensity or applied voltage.

Voltage → driving force → drift current
Without applying force or voltage → diffusion current.

Operating temperature:-

(i) For Ge :-

-60°C to 75°C

→ Max. operating temperature is 75°C

(ii) For Si :-

-60°C to 175°C

→ Max. operating temperature is 175°C

→ Si is more suitable for high temperature application

Normal Working temperature:-

- For semiconductor devices, the normal working temperature will less than or equal to. 400K ; $\leq 400K$
- Above 400K, property changes & come into material science.

Ques:- Why carbon is not considered as a semiconductor element?

Soln:- In periodic table :-

Because:-

Gp-IV

(I) Energy gap is very large

C

(II) C has very - 2 unstable properties

Si
Ge

Semiconductor

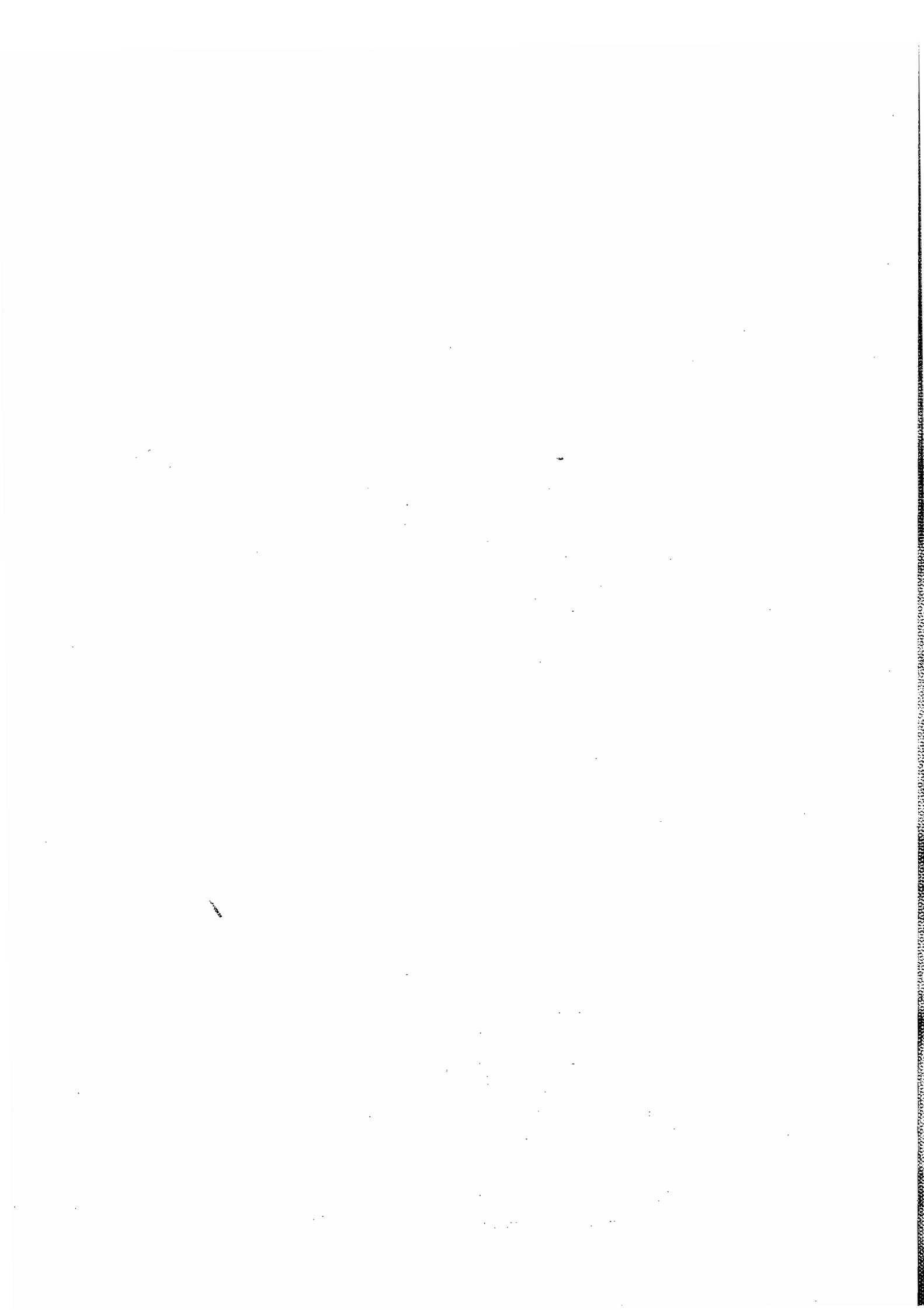
(III) C having unreliable properties

(IV) C having unpredictable properties.

NOTE:-

Sometimes, C → Conductor → Graphite

" " → Insulator → Diamond



Lecture - 2

Leakage Current (I_o):

- Also called minority carrier current or thermally generated current or reverse saturation current
- I_o depends on minority carriers and minority carrier conc. depends on temperature & therefore this current is generated because of temperature. Therefore it is thermally generated current.
- If leakage current are small, the temperature effect on material or device will be less and this indicates better thermal stability

$$I_o = \mu A \text{ nA}$$

(Ge) Si)

I_o of Ge $>$ I_o of Si

- Silicon is having better thermal stability than germanium. This is due to smaller leakage current.
- I_o is independent of applied voltage i.e. this current is saturated w.r.t. applied voltage. Hence the name saturation current.
- I_o is highly sensitive to temp
- For 1°C , I_o approximately \uparrow by 7% in both Ge & Si
- I_o doubles for every 10°C

$$I_o(T_2) = I_o(T_1) \left[2^{\frac{T_2 - T_1}{10}} \right]$$

where $T_2 > T_1$

Resistivity (ρ) :-

- specific resistance of the material
- Unit:- $\Omega \text{ cm}$ or $\Omega \text{ m}$
- For metals :-
+ve temperature coefficient of Resistance

i.e. $R \uparrow$ with $\uparrow T$

$$R = \rho \frac{l}{A}$$

In metals $\rho \uparrow$ with inc. in temperature

For semiconductors :-

- ve temperature coefficient of resistance
- i.e. $R \downarrow$ with inc. in temperature

In a sc, $\rho \downarrow$ with \uparrow in temperature

Conductivity (σ) :-

- It is the reciprocal of resistivity
- Unit:- $\frac{1}{\Omega \text{ cm}} \rightarrow \text{S/cm}$ or S/m
- conductivity denotes current carrying capacity of the material or device

$$\text{Conductivity} = \text{carrier conc.} \times \text{charge} \times \text{mobility}$$

- conductivity depends on
 - carrier conc.
 - charge
 - mobility

Variation in conductivity due to temperature depends on :-

- Variation in mobility of charge carriers
- Variation in carrier concentration.

For Metals :- \rightarrow unipolar

$$\sigma = nq\mu_n$$

- In metal $\rightarrow \downarrow$ with inc. in temperature
- In metal free e^- concentration is independent of temperature
- In metals as temperature inc., mobility of charge carriers dec. and therefore conductivity decreases.

For semiconductor :- \rightarrow Bipolar

$$\sigma = nq\mu_n + p\eta\mu_p$$

- In a semiconductor, conductivity increases with inc. in temperature.
- Increase in carrier conc. $>$ dec in mobility with inc. in temperature.
- In a semiconductor as temp. inc. mobility of charge carriers dec and it will reduce the conductivity slightly and at the same time because of temperature a large no. of covalent bond will be broken and large no. of e^- , $\&$ hole are created and this will \uparrow the conductivity. But larger value and the net result conductivity inc. with the temperature.
- In a semiconductor conductivity mainly depends on carrier concentration
- Semiconductor means by default it is intrinsic semiconductor.

NOTE :-

In intrinsic semiconductor, conductivity increases with inc. in temperature.

Current density (J) :-

→ It is the current passing per unit area

$$J = \frac{I}{\text{Area}} \quad \text{Amp/m}^2$$

$$J = \sigma |E| \quad \text{A/m}^2$$

Electric field intensity

$$= \frac{\sigma}{m} \cdot \frac{V}{m}$$

$$J = \text{mho} \cdot \text{volt}$$

For metals :-

$$J = nq \mu n E \quad \text{A/cm}^2$$

For semiconductor :-

$$J = [nq \mu_n + pq \mu_p] E \quad \text{A/cm}^2$$

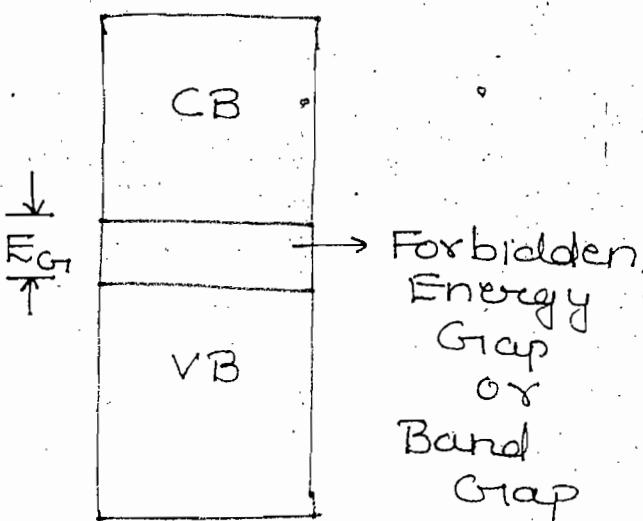
Conductivity sensitivity :-

- In intrinsic semiconductor, conductivity increases with inc. in temperature
- For 1°C ↑ of Ge ↑ by 6%
- For 1°C ↑ of Si ↑ by 8%
- When compare to Ge, conductivity of Si is more sensitive to temperature. But Si is more suitable for high temp. application. This is due to small leakage current.

Energy Gap :- E_g or E_{G1} :-

E_{G10} = Energy Gap at 0K

E_{G1300} = Energy Gap at 300K



Gte	Si
$E_{G10} = 0.785 \text{ eV}$	1.21 eV
$E_{G1300} = 0.72 \text{ eV}$	1.1 eV

Energy Band Diagram

of an Element

→ Energy Gap decreases with increase in the temperature i.e.

$$E_g \propto \frac{1}{\text{Temp}}$$

$$E_{G(T)} = E_{G10} - \beta_0 T \text{ eV}$$

where β_0 = Material constant

$$\beta_0 = \text{eV}/\text{OK}$$

For Si :-

$$E_{G(T)} = 1.21 - 3.6 \times 10^{-4} T$$

Temp. should be in Kelvin

For Gte :-

$$E_{G(T)} = 0.785 - 2.23 \times 10^{-4} T$$

Energy Band Diagram of Metals / Conductors :-

- All metals are very good conductors of current i.e. they allow large flow of current through them
- All metals are unipolar i.e. current is carrying in metals only by e's
- In metal e. conc. is very high i.e. $n = 10^{28}/m^3$
- In metals free e. conc. is independent of temperature

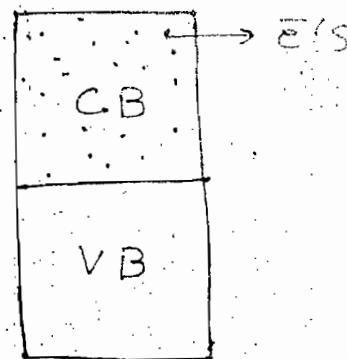
→

$$E_G = 0$$

At 0K

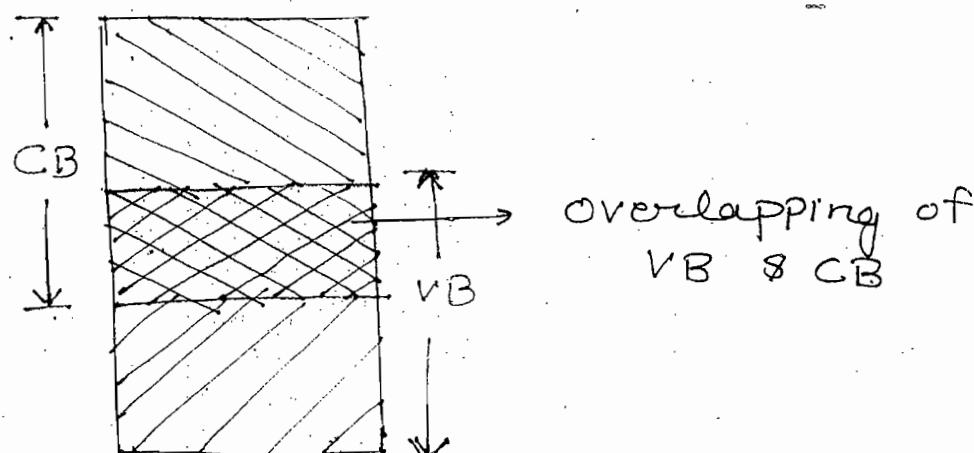
→

At 0K :-



- In metals free e's are available even at 0K

At 300K :-

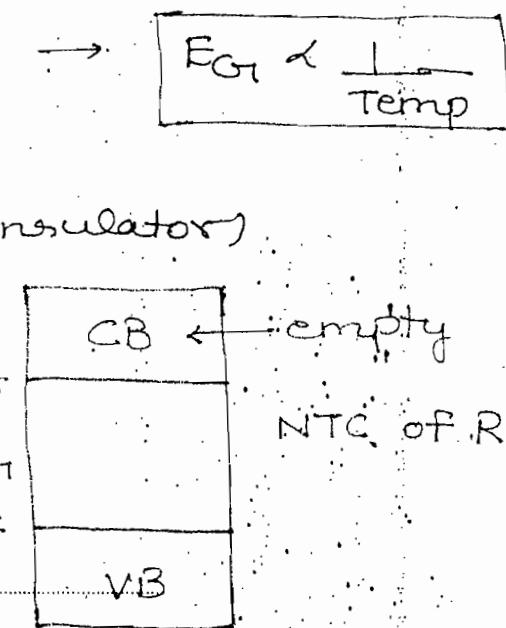


- Overlap ↑ with ↑ temperature

- Due to the overlapping of valence band & conduction band, metals having +ve temperature coefficient of resistance (PTC)
- In metals there will be only drift current
eg:- Gold, Silver, Platinum, Cu, Al etc

Energy Band Diagram of an insulator:-

- Insulator are bad conductor of current i.e. they don't allow any flow of current through them
- Ionic bonding
- $\sigma = 0$ (Ideal insulator)
= negligible (Practical insulator)
- $E_G = \text{Large}$
 $\geq 5\text{eV}$
- Negative temperature coefficient i.e. $R \downarrow$ with $T \uparrow$

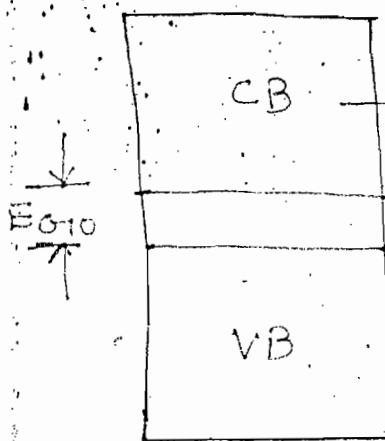


eg:- Diamond, SiO_2 , Air, paper, glass etc

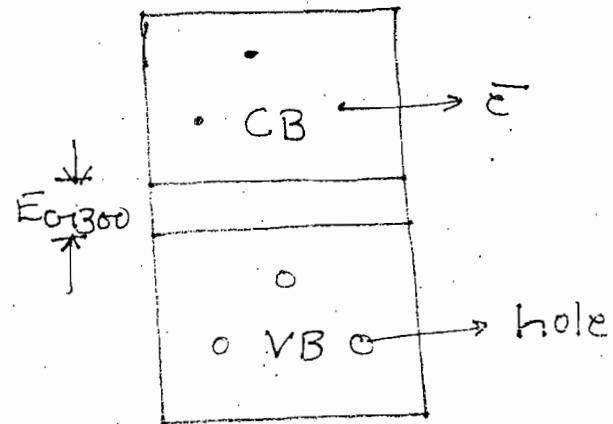
Energy Band Diagram of a semiconductor:-

- Semiconductor belongs to IV th group of periodic table
- The nature of bonding is covalent bonding
- Bipolar i.e. having two different types of charge carriers.
- For a semiconductor, the energy gap is small i.e. $E_G \rightarrow$ around 1 eV
0.7 eV to 1.5 eV

AT 0K



At T=300K :-



→ At T=0K carrier conc. are zero thereby conduction band is empty. Hence conductivity is zero.

→ All semiconductors are insulators at 0K.

→ At room temperature, because of thermal energy, a large no. of covalent bonds will be broken and equal no. of e's and holes are created and there will be a overall conductivity in the semiconductor.

$$\rightarrow E_{0,T} \propto \frac{1}{\text{temp}}$$

→ Semiconductor possess negative temperature coefficient of resistance

→ In a semiconductor there is a diffusion current.

→ Semiconductor elements are Si, Ge

Definition of Semiconductor:-

Semiconductor are the elements whose conductivity lies b/w the conductivity of insulator and conductivity of a conductor.

Einstein's Equation :-

→ It is named as Einstein equation to give the respect to great scientist Einstein.

In a semiconductor

$$\frac{\partial n}{\mu_n} = \frac{\partial p}{\mu_p} = V_T$$

or

$$\frac{\mu_n}{\partial n} = \frac{\mu_p}{\partial p} = \frac{1}{V_T}$$

→ It gives the relationship b/w diffusion constant mobility and thermal voltage

→

$$\frac{\partial}{\mu} \propto \text{Temperature}$$

→

$$\frac{\mu}{\partial} \propto \frac{1}{\text{Temperature}}$$

→ The unit for mobility to diffusion constant is A^{-1}

→ The unit for $\frac{\partial}{\mu}$ is volt

Diffusion constant of charge carriers (∂) :-

Diffusion constant $\partial_n = \mu_n V_T$

Hole " " " " $\partial_p = \mu_p V_T$

Unit for ∂ :- cm^2/sec or m^2/sec

- It is a material constant related with the property diffusion.
- Diffusion constant of the charge carriers decreases with the temperature

$$D = \mu V_T \uparrow$$

it is more sensitive with temp. as compare to V_T

For Ge at 300K :-

$$D_n = 99 \text{ cm}^2/\text{sec}$$

$$D_p = 47 \text{ cm}^2/\text{sec}$$

For Si at 300K :-

$$D_n = 34 \text{ cm}^2/\text{sec}$$

$$D_p = 13 \text{ cm}^2/\text{sec}$$

NOTE :-

$$\frac{D_n}{D_p} = \frac{\mu_n V_T}{\mu_p V_T}$$

⇒

$$\boxed{\frac{D_n}{D_p} = \frac{\mu_n}{\mu_p}}$$

or $\boxed{D_n \mu_p = D_p \mu_n}$

NOTE :-

→ Diffusion constant can't be negative & it can't be represented in fraction.

For Ge at 300K :-

$$\boxed{\frac{D_n}{D_p} = 2.1}$$

Mass Action Law :-

$$\boxed{n_p = n_i^2}$$

It states that, "In a semiconductor (intrinsic or extrinsic) under thermal equilibrium the product of electrons and holes will be always a constant and is given by square of intrinsic concentration."

→ The law is mainly used for extrinsic semi-conductor to calculate minority carrier conc.

For n-type semiconductor :-

Majority carriers are \bar{e} 's = n_n

Minority " " holes = p_n

$$p_n = \frac{n_i^2}{n_n}$$

For p-type semiconductor :-

Majority carriers are holes = p_p

Minority " " " " \bar{e} 's = n_p

$$n_p = \frac{n_i^2}{p_p}$$

NOTE :-

$$n_n p_n = n_p p_p = n_i^2$$

$$\rightarrow \text{Minority carrier conc} = \frac{n_i^2}{\text{Majority carrier conc}}$$

$$\rightarrow \text{Majority carrier conc} \propto \text{Doping}$$

$$\rightarrow \text{Minority carrier conc} = \frac{n_i^2}{\text{Doping conc}}$$

→ In an intrinsic semiconductor, \bar{e} 's and holes conc. are n & p respectively. By adding impurity atoms, the \bar{e} & hole conc. are n_i & p_i respectively then the following relation is acceptable

Before Doping

$$n_p = n_i^2$$

Hence

$$n_p = n_i p_i$$

After Doping

$$n_i p_i = n_i^2$$

or

$$n_p = n_i p_i = n_i^2$$

Intrinsic Concentration (n_i) :-

Intrinsic = Pure

→ It is the conc. available in the pure semiconductor at a given temperature

$$n = p = n_i$$

$$n_i^2 = A_0 T^3 e^{-E_G / kT}$$

where

A_0 = material constant

or

$$n_i = \sqrt{A_0} T^{3/2} e^{-E_G / 2kT}$$

→ Intrinsic concentration in a semiconductor depends on (i) Temperature

(ii) Energy Gap.

$$\begin{aligned} n_i &\propto T^{3/2} \\ n_i &\propto e^{-E_G / kT} \\ n_i &\propto e^{-E_G / y} \end{aligned}$$

dominating factor

→ Intrinsic concentration n_i^2 is \propto (a) T^3 (b) $T^{3/2}$

→ Intrinsic concentration n_i is \propto (a) T^3

(b) $T^{3/2}$

- Intrinsic concentration increases with the temperature as a non-linear variation.
- When compare to Si, Ge is having larger value of n_i and it is due to smaller value of energy gap.

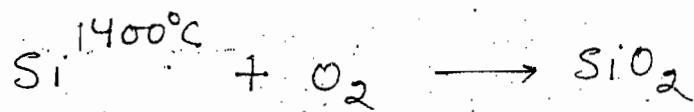
At 300K:-

$$\text{For Ge} \rightarrow n_i = 2.5 \times 10^{13} \text{ atoms/cm}^3$$

$$\text{For Si} \rightarrow n_i = 1.5 \times 10^{10} \text{ atoms/cm}^3$$

Electrical Properties of Germanium & Silicon :-

	<u>Properties</u>	Ge	Si
1. Atomic No.		32	14
2. Total No. of atoms or	/cm ³	4.421×10^{22}	5×10^{22}
Density of atoms			
3. Intrinsic conc. n_i at 300K (atoms/cm ³)		2.5×10^{13}	1.5×10^{10}
4. Intrinsic resistivity ρ_i at 300K (Ω) cm		45	230,000
5. Leakage current (I_0)	mA		nA
6. Max. operating Temperature	75°C		175°C
7. Power handling Capability	low		high
8. E_{G10}			
9. E_{G1300}			
10. M_n			
11. M_p			
12. Φ_n			
13. Φ_p			



Cheapest insulating material

→ Silicon is more fancy when compare to Ge due to

- (i) Smaller leakage current
- (ii) High temperature application
- (iii) Suitable for low power & high power handling
- (iv) Plenty available on the surface of earth

→ This is the primary reason why Si is fancy by semiconductor device manufacturer

(v) Cheapest Material

(vi) Favourable properties to form SiO_2

This is the main reason why Si is fancy by IC manufacturers

NOTE:-

1. Si when exposed to 1400°C we get liquid Si which reacted with O_2 to give SiO_2
2. SiO_2 is used to provide isolation in between the components inside the IC.

Disadvantage of Si:-

The main disadvantage of Si is smaller conductivity.

Lecture - 3

Diffusion & Diffusion current :-

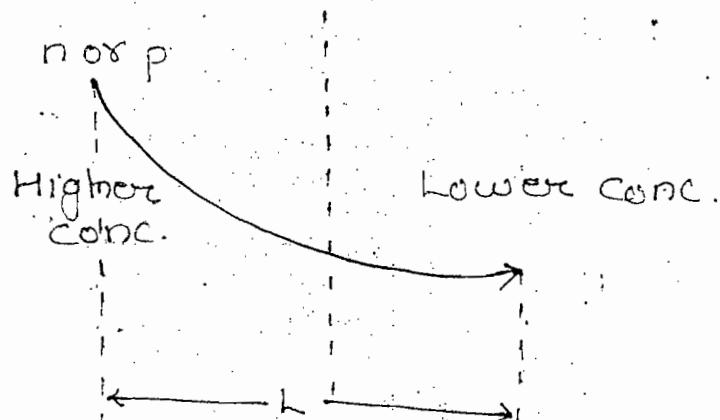
- Diffusion is a natural phenomenon.
- The migration of charge carriers from higher conc. to lower conc. or from higher density to lower density is called diffusion.
- Diffusion is mainly due to conc. gradient

$\frac{dc}{dx}$ → Slope → Gradient

$\frac{dn}{dx}$ → \bar{n} conc. gradient

$\frac{dp}{dx}$ → hole " "

Semiconductor



- Diffusion current flows only in semiconductors.
- In a semiconductor, diffusion is due to unequal distribution of charge carriers

NOTE:-

- In metal, \bar{n} conc. is very high ($n = 10^{28}/m^3$) and therefore \bar{n} are arranged with equal distribution. Hence diffusion can't takes place.
- Diffusion is also associated with random motion of charge carriers due to thermal vibrations.

Length of Diffusion:-

$$L = \sqrt{\theta \cdot \tau} \text{ cm}$$

where $\theta \rightarrow$ diffusion constant of charge carrier

$\tau \rightarrow$ carrier lifetime / Average lifetime

→ Length of diffusion is, average length

Since $\theta = \mu V_T$

$$L = \sqrt{\mu V_T \tau} \text{ cm}$$

→ Length of diffusion depends on

- (I) Diffusion constant of charge carriers
- (II) Mobility of charge carrier
- (III) carrier life-time
- (IV) Temperature.

→ Electron diffusion length, $L_n = \sqrt{\theta_n \tau_n} \text{ cm}$

→ Hole diffusion length, $L_p = \sqrt{\theta_p \tau_p} \text{ cm}$

→ Diffusion current density, Junction

$$J_n = +q \theta_n \frac{dn}{dx} \text{ A/cm}^2$$

(Diff.)

→ Hole diffusion current density,

$$J_p (\text{Diff.}) = -q \theta_p \frac{dp}{dx} \text{ A/cm}^2$$

→ Electron diffusion current :-

$$I_n (\text{Diff.}) = J_n (\text{Diff.}) \times \text{Area}$$

→ Hole diffusion current

$$I_p(\text{Diff.}) = J_p(\text{Diff.}) \times \text{Area}$$

Note:-

By default always consider unit cross sectional area

Total current density in a semiconductor:-

→ The total current density in a semiconductor

$$J = J_n + J_p \text{ A/cm}^2$$

where $J_n = J_n(\text{Diff.}) + J_n(\text{Drift})$

$$J_n = q \mu_n \frac{dn}{dx} + n q \mu_n \epsilon \text{ A/cm}^2$$

$$J_p = J_p(\text{Drift}) + J_p(\text{Diff.})$$

$$J_p = p q \mu_p \epsilon - q \mu_p \frac{dp}{dx} \text{ A/cm}^2$$

NOTE:-

- Drift current depends on (i) carrier conc.
(ii) charge
(iii) Mobility of charge carriers
(iv) Field intensity
- Drift current mainly depends on field intensity
- Diffusion current mainly depends on concentration gradient
- In a semiconductor total diffusion current density is given by

$$\begin{aligned} J(\text{Diff.}) &= J_n(\text{Drift}) + J_p(\text{Diff.}) \\ &= +q \mu_n \frac{dn}{dx} - q \mu_p \frac{dp}{dx} \text{ A/cm}^2 \end{aligned}$$

Ques:- If drift velocity of holes under the field gradient of 100 V/m . Find its mobility

Ans:- $E = 100 \text{ V/m}$

$$V_d = 5 \text{ m/sec}$$

$$\mu = \frac{V_d}{E}$$

$$= \frac{5}{100} = 0.05 \text{ m}^2/\text{Vsec}, \text{ Ans}$$

Ques:- The carrier mobility in a semiconductor is $0.4 \text{ m}^2/\text{Vsec}$. Find diffusion constant?

Ans:- $\mu = 0.4 \text{ m}^2/\text{Vsec}$

$$D = ?$$

$$\text{At } T = 300\text{K} \quad V_T = 26 \text{ mV}$$

$$D = \mu V_T$$

$$= 0.4 (26 \times 10^{-3})$$

$$= 0.0104 \text{ m}^2/\text{sec}, \text{ Ans.}$$

Ques:- The minority carrier lifetime and the diffusion constant in a semiconductor are $100 \mu\text{sec}$ and $100 \text{ cm}^2/\text{sec}$ respectively. Find the diffusion length of charge carrier.

Ans:- $\tau = 100 \mu\text{sec}$

$$D = 100 \text{ cm}^2/\text{sec}$$

$$L = \sqrt{D\tau}$$

$$= \sqrt{100 \times 100 \times 10^{-6}}$$

$$= 0.1 \text{ cm}, \text{ Ans}$$

Ques:- A sample of n-type semiconductor has carrier density of $6.25 \times 10^{18}/\text{cm}^3$ at 300K. If the intrinsic conc. of charge carriers in the sample is $2.5 \times 10^{13}/\text{cm}^3$. Find the hole conc.

Ans:- N-type SC

$$n = 6.25 \times 10^{18}/\text{cm}^3$$

$$n_i = 2.5 \times 10^{13}/\text{cm}^3$$

$$P = ?$$

By Mass action law

$$P = \frac{n^2}{n_i} = \frac{(2.5 \times 10^{13})^2}{6.25 \times 10^{18}} = 10^{18}/\text{cm}^3$$

Ques:- A flat Al strip with a resistivity of $3.44 \times 10^{-8} \Omega \text{m}$ and a length of 5mm with a cross-sectional area is $2 \times 10^{-4} \text{ mm}^2$ is subjected to a current flow of 50mA. Find Voltage drop across it.

Ans:- $\rho = 3.44 \times 10^{-8} \Omega$

$$l = 5\text{mm}$$

$$a = 2 \times 10^{-4} \text{ mm}^2$$

$$I = 50\text{mA}$$

$$R = \frac{\rho l}{A} = 0.86 \Omega$$

$$V = IR = 43\text{ mV, Ans}$$

Ques:- A semiconductor wafer is 0.5mm thick. A potential of 100mV is applied across the thickness.

(i) What is the carrier drift velocity if the mobility is $0.2 \text{ m}^2/\text{Vs}\text{er}$.

(ii) How much time is required for an e⁻ to move across this thickness?

Ans:- (1) $x = 0.5 \text{ mm}$
 $= 0.05 \text{ cm} = 0.5 \times 10^{-3} \text{ m}$
 $V = 100 \text{ volt} = 10^4 \text{ V}$
 $E = \frac{10^{-4} \times 10}{0.5 \times 10^{-3}} = 0.2 \text{ volt/m}$
 $v_d = \mu E$
 $= 0.2 \times 0.2 = 0.04 \text{ m/sec.}$

(II) $t = \frac{x}{v_d}$
 $= \frac{0.5 \times 10^{-3} \times 10^2}{0.04 \times 10} = \frac{5}{4} \times 10^{-2}$
 $= 1.25 \times 10^{-2} \text{ sec.}$

Ques:- A small conc. of minority carriers are injected into a homogeneous semiconductor crystal at one point and having electric field of 10 V/cm is applied across the crystal shows so that minority carriers in the crystal will be moving a distance of 1cm in $20 \mu\text{sec}$. calculate the mobility in cm^2/sec .

Soln:- $E = 10 \text{ V/cm} = \frac{10}{100} \text{ V/cm}^2 = 0.1 \text{ V/cm}$

$t = 20 \mu\text{sec} = 20 \times 10^{-6} \text{ sec.}$

$x = 1 \text{ cm}$

$v_d = \frac{x}{t} = \frac{1}{20 \times 10^{-6}} = 50,000 \text{ cm/sec}$

$\mu = \frac{v_d}{E} = \frac{50,000}{10} = 5000 \text{ cm}^2/\text{Vsec.}$

ques:- In Gie, leakage current are 5 μA at 10°C . Find its value when the temperature is 25°C .

Soln:-

$$I_0(T_1) = 5 \mu\text{A} \quad T_1 = 10^{\circ}\text{C} = 283\text{K}$$

$$I_0(T_2) = ? \quad T_2 = 25^{\circ}\text{C} = 298\text{K}$$

$$I_0(T_2) = I_0 \left[2^{\frac{(T_2 - T_1)}{10}} \right]$$

$$I_{02} = 5 \left[2^{\frac{25 - 10}{10}} \right] = 14.14 \mu\text{A}, \text{ Ans}$$

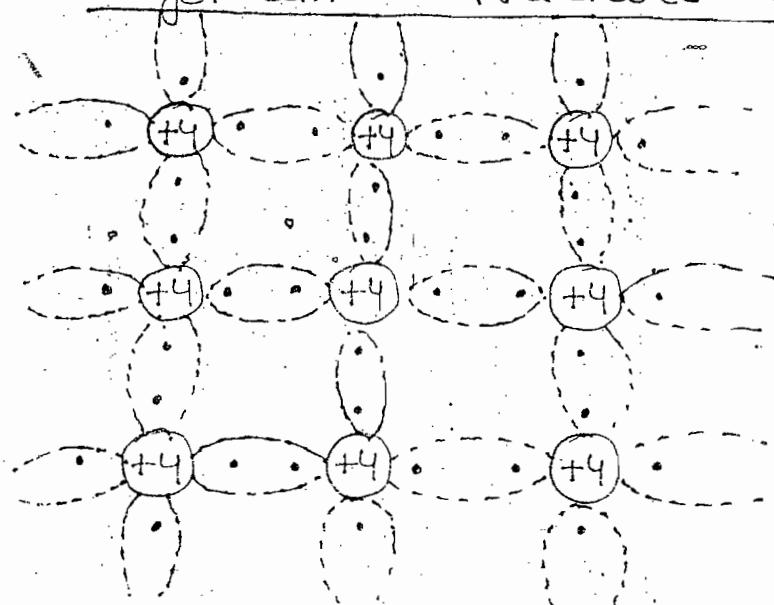
NOTE:-

Semiconductor is non-linear element. Hence we can't applied ohm's law.

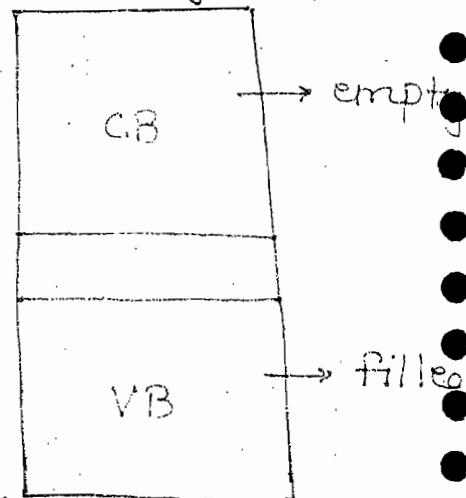
Intrinsic Semiconductor

- also known as pure semiconductor or natural semiconductor or non-degenerate semiconductor.
- The outermost orbit in an atom is known as valency band.
- The max. no. of valency e's are 8.

Crystalline structure at OK !-

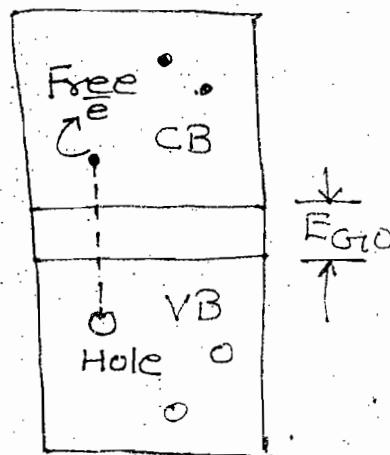
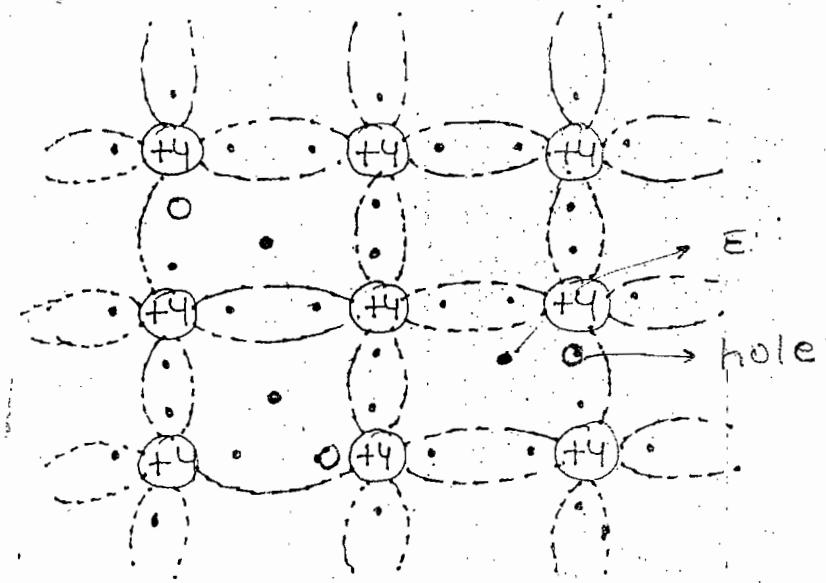


- The sharing of \bar{e} with neighbouring atom is known as covalent bonding
- In one covalent bond there will be two valency electron
- At 0K all valency \bar{e} 's are imperfect covalent bonding
- Intrinsic semiconductor at 0K will be working as a insulator.



Energy band diagram
at 0K

Crystalline structure at 300K

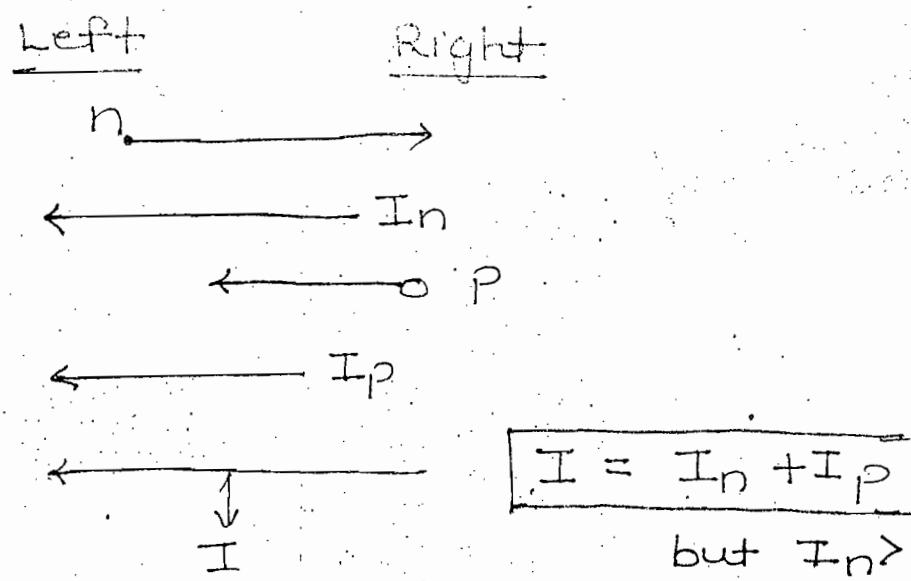


For intrinsic semiconductor $n = p = n_i$

- When a covalent bond is broken, it will give one \bar{e} & hole (\bar{e} will be jumping from VB to CB and becomes a free \bar{e} , and hole will remain in the valency band)
- Charge on the hole is tre
- Hole is created because of the \bar{e}
- Hole is defined as deficiency of \bar{e} in the broken covalent bond
- Intrinsic semiconductor is always $n = p$

- The condition for intrinsic semiconductor
 $n = p = n_i$
- Because of opposite charges electron & hole always move in the opposite direction.
- Current direction is opposite to the flow of e's
- Current direction is in the direction of holes

In a semiconductor:



- In a semiconductor, e and holes always moves in opposite direction but they contribute the current in the same direction.
- The free e's will be moving in the conductive band and will contribute same current and at the same time hole will be moving in the valence band and will contribute the same current and the total current is electron current + hole current.

(I) Conductivity of intrinsic semiconductor :-

$$\sigma_i = n_i \mu_n + p_i \mu_p$$

but $n_i = p_i = n_i$

$$\boxed{\sigma_i = n_i \nu [\mu_n + \mu_p]}$$

$$\sigma_i \propto n_i$$

$$\text{but } n_i \propto T^{3/2}$$

Hence $\sigma_i \uparrow$ with \uparrow in T , i.e. a non-linear variation.

(II) Intrinsic Resistivity :-

$$\rho_i = \frac{1}{\sigma_i}$$

$$\boxed{\rho_i = \frac{1}{n_i \nu [\mu_n + \mu_p]}}$$

Disadvantage of intrinsic semiconductor :-

→ The major disadvantage is ~~weakness~~ of intrinsic semiconductor is smaller conductivity.

NOTE :-

The only electronic device fabricated with intrinsic semiconductor is PIN diode.

(III) Generation of e-hole pairs :-

→ When covalent bonds are broken, large no. of e's and holes are created. This process is called as generation of e-hole pair.

(IV) Recombination:-

A free \bar{e} pairing with a hole is known as recombination.

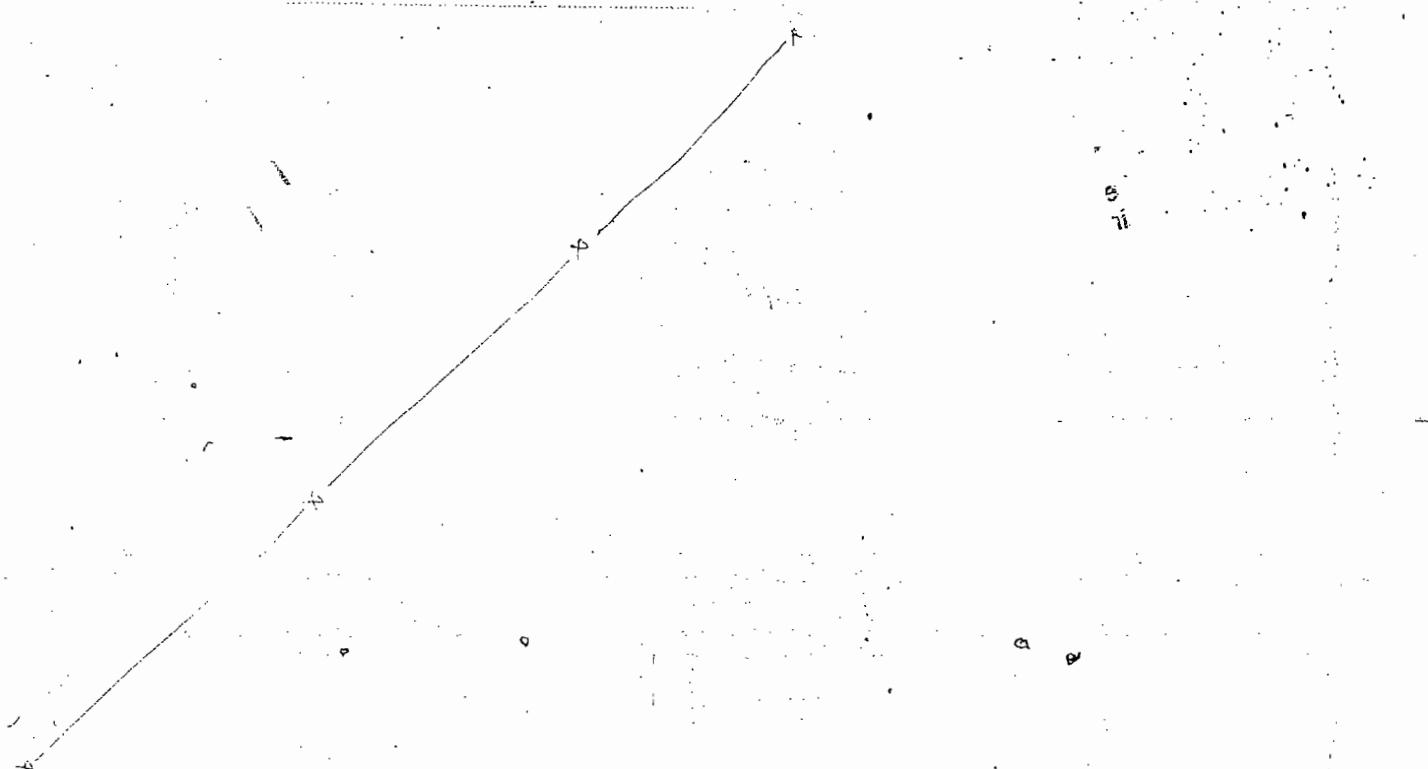
- During recombination, free \bar{e} and hole both will disappear and a covalent bond is created
- During the recombination, the free \bar{e} will be falling from conduction band to valency band to recombine with the hole.

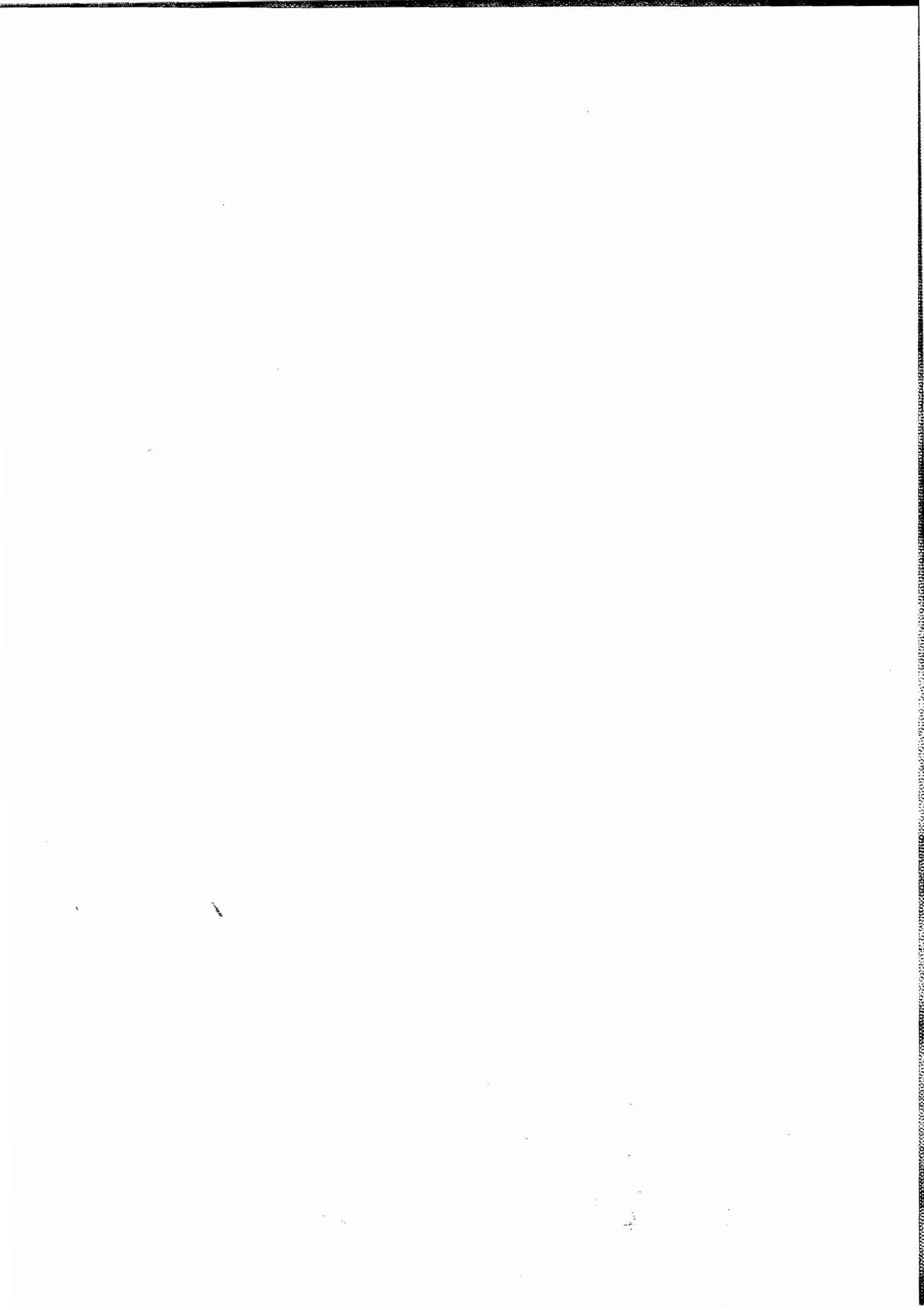
(V) Carrier lifetime (τ):-

- It is the interval of time from breaking of covalent bond until its recombination.
- τ is average lifetime.
- τ is in the range of usec to nsec.

NOTE:-

- Hole is basically a valency electron, for assumed with a tre charge
- Hole is considered with a tre mass.





Lecture - 4

Doping:-

- The process of adding the impurities to the semiconductor is called doping.
- Doping increases the carrier concentration and thereby increases the conductivity.

Trivalent / Acceptor impurities :-

B, Al, Ga & In

Pentavalent / Donor impurities :- P, As, Sb & Bi

impurity atom More affinity towards Si

Doping is based on $1: 10^6$ or $1 \text{ in } 10^6$ or $\frac{1}{10^6}$

Standard Doping Concentration :-

- Moderate Doping $\rightarrow 1: [10^6 \text{ to } 10^8]$ $\rightarrow P^- N^+$
- Lightly Doped $\rightarrow 1: 10^{11}$ $\rightarrow P^+ N^+$
- Highly / Heavily doped $\rightarrow 1: 10^3$ $\rightarrow P^+ N^+$

→ The minimum doping required to convert intrinsic semiconductor to extrinsic semiconductor is $1: 10^8$.

→ When intrinsic semiconductor is lightly doped, it will remain intrinsic.

→ * With $1: 10^8$ doping in Ge, $\rightarrow \uparrow$ by 12 times

→ * With $1: 10^7$ " " " " " \rightarrow " " approx 120 fm

→ In a natural semiconductor / intrinsic semiconductor because of unequal distribution of charge carrier there will be always a diffusion current.

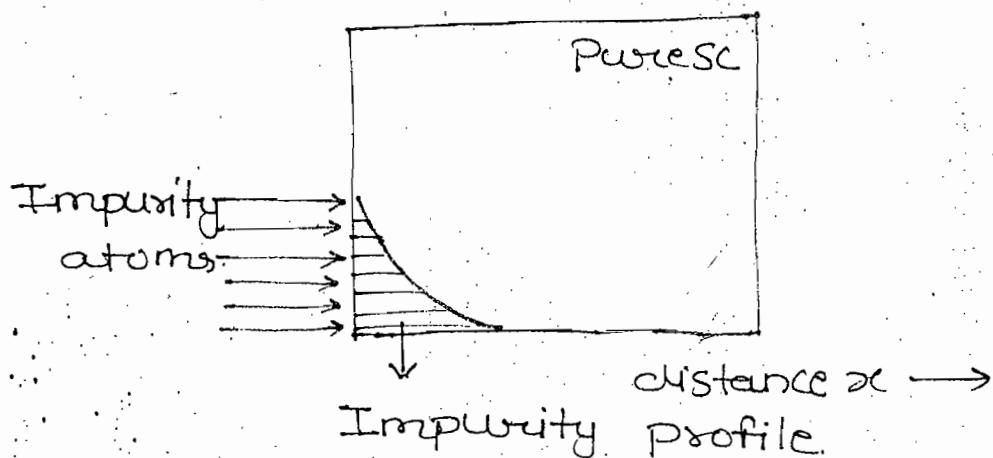
→ Even when a voltage is applied there will be no drift current.

→ The impurities atom or doping or impurities profile can be homogeneous or non-homogeneous.

→ The impurities profile must be introduced, 'built in electric field' or internal electric field in the semiconductor so that semiconductor

will not be having a drift current along with the diffusion current.

→ The intrinsic semiconductor is lightly doped. It will remain intrinsic. But due to the impurity profile there will be drift current along with a diffusion current.



→ The impurity profile will be maximum on the surface of a semiconductor where it is introduced and the profile gradually decreases as an exponentially decaying function with the distance into the semiconductor.

NOTE:-

→ Trivalent and pentavalent impurities when added to the semiconductor will introduce built-in electric field.

Ge-Si Crystal:-

→ When Ge is added to the Silicon or Si is added to the Ge as impurities, we get Ge-Si crystal.

→ The nature of the bonding is covalent bonding.

→ At 0K there will be working as a insulator.

→ At 300K they will be working as intrinsic semiconductor.

Extrinsic Semiconductor / Doped Semiconductor :-

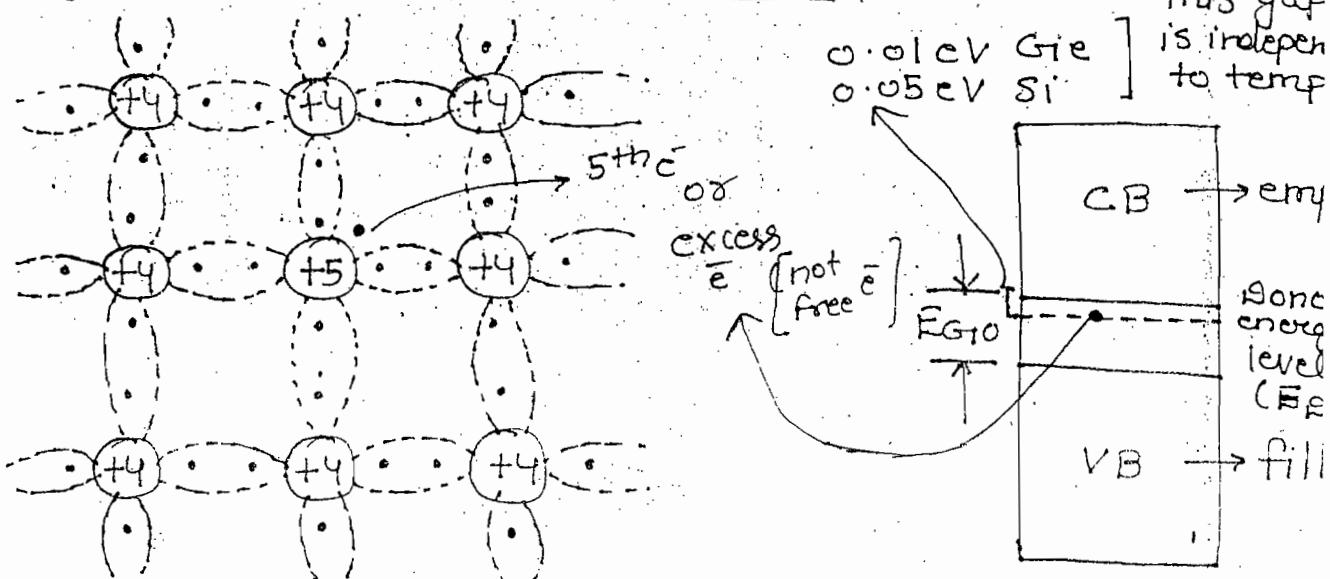
→ also known as impurity SC or artificial SC or degenerate SC or compensated SC.

Types of Extrinsic Semiconductor :-

(1) N-type Semiconductor or DONAR :-

→ The impurity is pentavalent.

Crystalline structure at 0K :-

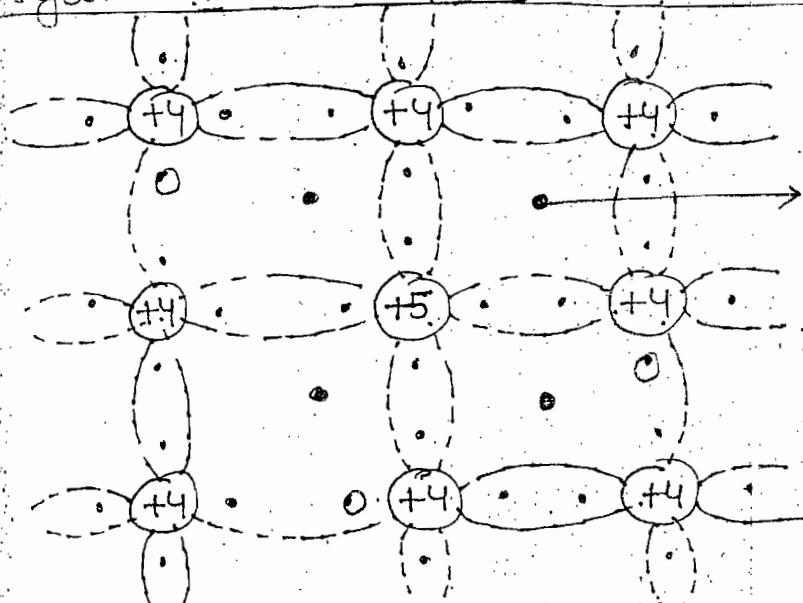


NOTE :-

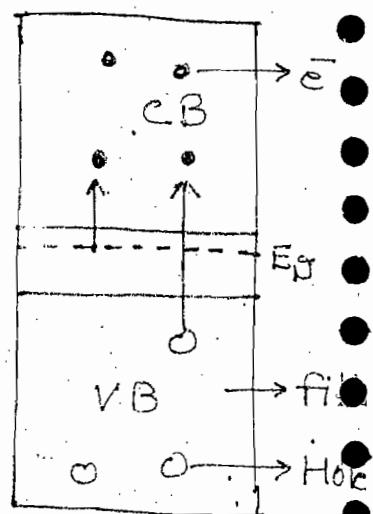
- Donor energy level is a discrete energy level created just below the conduction band.
- Donor energy level indicates the energy level of pentavalent atoms added to the semiconductor.
- At 0K, the fifth e^- of all the impurity atom will be existing in the donor energy level.
- The additional energy required to detach the fifth e^- from its orbit = 0.01 eV for Ge
= 0.05 eV for Si.
- n-type semiconductor at 0K will be working as a insulator.

$$\begin{aligned} \rightarrow \text{No. of } 5^{\text{th }} e^- &= \frac{\text{Si}}{5 \times 10^{22} \frac{\text{atoms}}{\text{cm}^3} \times \frac{1}{10^8}} \\ &= 5 \times 10^{14} \text{ atoms/cm}^3 \end{aligned}$$

Crystalline Structure at 300K :-



fifth
 \bar{e}
or
free
 \bar{e}
 $E_{G,300}$



$$n-p = 5 \times 10^{14}$$

Hence $n \gg p$ & \bar{e} are majority carriers & holes are minority carriers.

- In n-type semiconductor, every impurity atom will be donating one \bar{e} into the conduction band and therefore it is also called as a donor.
- Donor level ionisation indicates the fifth \bar{e} 's moving from donor energy level into the conduction band.
- Donor level ionisation increases with the temperature (i.e. as temp is increasing from 0K to 300K, the fifth \bar{e} will be moving from donor energy level to conduction band).
- At room temperature donor level ionization is completed (i.e. the fifth \bar{e} of all the impurity atoms is shifted from donor energy level into the conduction band).
- Above 300K there is no donor level ionization.
- In n-type semiconductor as temp inc from 0K to 300K, due to donor level ionization, the fifth \bar{e} will be moving from donor to

energy level to conduction band and at the same time because of thermal energy a large no. of covalent bond are broken and equal no. of \bar{e} 's & holes are created and all these \bar{e} 's will be moving from valence band to conduction band.

The \bar{e} concentration in the conduction band, is more greater than the hole concentration in the valence band. The \bar{e} are majority and holes are minority carriers.

- Majority carriers will contribute more current with less noise.
- Minority carriers will contribute less current and more noise.
- Minority carrier noise is thermal noise / white noise / Johnson noise. It increases with the temperature.
- As temp increases, because of smaller conc; minority carriers will vibrate and due to thermal vibration they produce more noise.
- The condition for n-type semiconductor is

$$\boxed{n > n_i \\ P < n_i}$$

- In n-type semiconductor, as \bar{e} conc. increase above n_i , the hole conc. will be falling below n_i and this is due to a large no. of recombination.
- According to law of electrical neutrality

$$\boxed{N_d + P = N_A + n}$$

where

N_d = Donor conc
or

density of
donor atom

In n-type semiconductor

$$N_A \approx 0$$

$$\boxed{* \\ n = N_d + P}$$

$$n \approx N_d$$

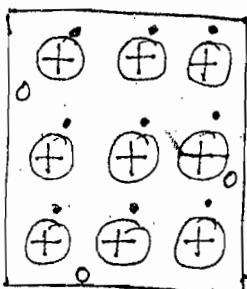
- N_d denotes total no. of pentavalent atoms added to the semiconductor
- In n-type semiconductor, current is predominated dominated by electrons.
- In n-type semiconductors, the free e⁻ conc. is approximately = density of donor atoms (i.e. approximately equal to N_d)
- The conductivity due to minority carriers is almost negligible.
- The conductivity of n-type semiconductors is

$$\sigma_N = n \nu_m n + P \nu_m p$$

$$\Rightarrow \sigma_N \approx n \nu_m n \quad \text{S/cm}$$

$$\Rightarrow \sigma_N \approx N_d \nu_m n \quad \text{S/cm}$$

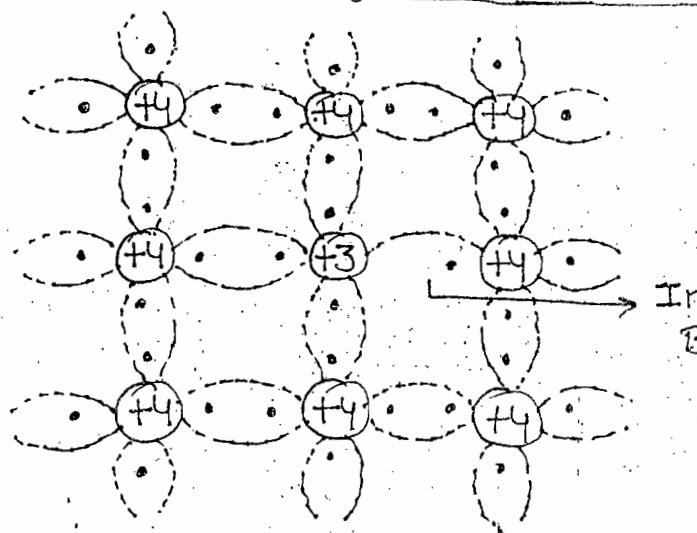
- Representation of n-type semiconductor is
- ⇒ In n-type semiconductor, after donating the e⁻ will be gaining the +ve charge and will become +ve ion



P-type semiconductor or Acceptor :-

→ The impurity is trivalent

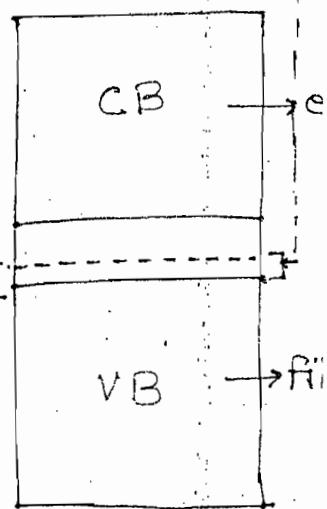
Crystalline structure at 0K :-



Incomplete Bond

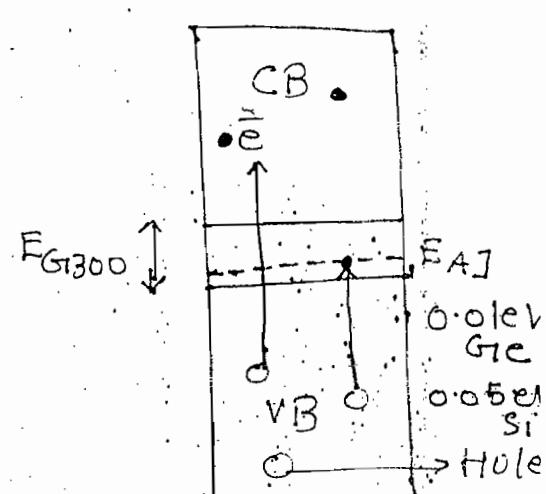
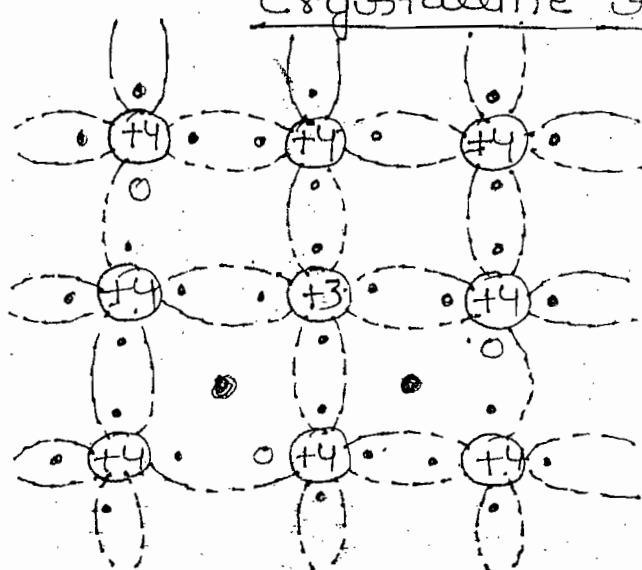
Acceptor energy level
[E_A]

0.01eV Ge
0.05eV Si



- Acceptor energy level is a discrete energy level created just above the valency band.
- Acceptor energy level denotes energy level of all the trivalent atoms added to the pure semiconductor
- p-type semiconductor at 0K will be working as a insulator.

Crystalline structure at 300K :-



→ In p-type semiconductor, every impurity atom will be receiving one e⁻ to complete its covalent bond. Hence it is acceptor.

→ Since $P \gg n$

In p-type semiconductor at room temp, because of thermal energy a large no. of covalent bonds will be broken and equal no. of e⁻'s & holes are created and most of these e⁻ will be moving from valency band to acceptor energy level to complete the bonding and a very few e⁻ will be moving from valency band to conduction band and therefore holes are majority carriers.

The hole conc. in valency band is far greater than hole conc. in conduction band. Hence holes are majority carrier and e⁻ are minority carriers.

→ In p-type semiconductor, current is dominated by holes.

→ Positive type semiconductor \leftrightarrow P-type

→ The condition for p-type semiconductor is

$$\boxed{\begin{array}{l} P > n_i \\ n < n_i \end{array}}$$

→ In p-type semiconductor as hole conc. is increasing above n_i , the hole conc. will fall below n_i . This is due to large no. of bonding.

→ According to law of electrical neutrality:-

$$\boxed{N_D + P = N_A + n}$$

In p-type semiconductor

$$*\boxed{N_D = 0}$$

$$\boxed{P = N_A + n} \quad \text{and}$$

$$\boxed{P \approx N_A}$$

where N_A = acceptor concentration.

→ N_A indicates the no. of trivalent atoms added to a semiconductor.

$$N_A = \text{Total no of atoms/cm}^3 \times \text{impurity ratio}$$

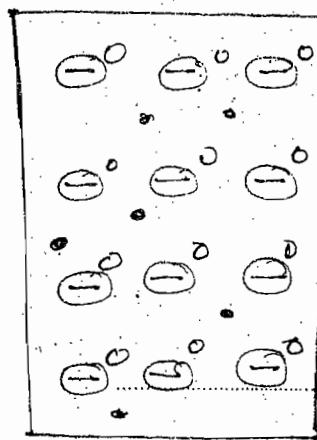
→ The conductivity of p-type semiconductor is

$$\sigma_p = n \nu u_n + P \nu u_p \text{ } \Omega^{-1}/\text{cm}$$

$$\Rightarrow \sigma_p \approx P \nu u_p \text{ } \Omega^{-1}/\text{cm}$$

$$\Rightarrow \sigma_p \approx N_A \nu u_p \text{ } \Omega^{-1}/\text{cm}$$

Representation of p-type semiconductor :-



→ The impurity atom after receiving the e⁻ and will become a -ve ion

→ -ve ion indicates a neutral atom with excess e⁻

Law of Electrical Neutrality :-

→ It is based on law of conservation of charge

→ i.e. total +ve charges = total -ve charges

$$P/F/N$$

$$N_D + P = N_A + n$$

N_D = Donor conc. & is associated with the charge

N_A = Acceptor conc. & is associated with -ve charge

$$\Rightarrow N_D - N_A = n - p$$

→ Any semiconductor accepting law of electrical neutrality will be always electrically neutral.

→ For intrinsic semiconductor :-

$$N_A = 0$$

$$N_D = 0$$

$$P = n$$

$$\Rightarrow P - n = 0 \quad \text{It is electrically neutral.}$$

→ For n-type semiconductor :-

$$N_A = 0$$

$$n = N_D + P$$

$$n \approx N_D$$

→ For p-type semiconductor :-

$$N_D = 0$$

$$P = N_A + n$$

$$P \approx N_A$$

→ All semiconductors are electrically neutral

Ques:- N-Type semiconductor is —

- (a) — very charged
- (b) truly charged
- (c) No charge at all
- (d) electrically neutral

Lecture - 5

Note:-

All semiconductors are electrically neutral
intrinsic as well as p-type & n-type.

Ques:- Calculate intrinsic conductivity and intrinsic resistivity of Ge at 300K. Assume $n_i = 2.5 \times 10^{13}$ atoms/cm³, $\mu_n = 3800 \text{ cm}^2/\text{Vsec}$, $\mu_p = 1800 \text{ cm}^2/\text{Vsec}$.

Soln:-

$$\begin{aligned}\sigma_i &= n_i e [\mu_n + \mu_p] \\ &= 2.5 \times 10^{13} \times 1.6 \times 10^{-19} [3800 + 1800] \\ &= 0.0224 \Omega^{-1}/\text{cm}\end{aligned}$$

$$\rho_i = \frac{1}{\sigma_i} = \frac{1}{0.0224} = 44.6 \Omega \text{ cm}$$

Ques:- Calculate conductivity and resistivity of pure Si at 800K temperature. $n_i = 1.5 \times 10^{16}$ atoms/cm³, $\mu_n = 1300 \text{ cm}^2/\text{Vsec}$, $\mu_p = 500 \text{ cm}^2/\text{Vsec}$.

Soln:-

$$\begin{aligned}\sigma_i &= n_i e [\mu_n + \mu_p] \\ &= 1.5 \times 10^{16} \times 1.6 \times 10^{-19} [1300 + 500] \\ &= 4.32 \times 10^{-6} \Omega^{-1}/\text{cm}\end{aligned}$$

$$\rho_i = \frac{1}{\sigma_i} = \frac{1}{4.32 \times 10^{-6}} = 231481 \Omega \text{ cm}$$

Ques:- A pure semiconductor (Ge) is doped with donor impurities to the extent of 1 impurity atom for every 10^7 atom. Calculate

(i) Donor conc.

(ii) Electron & hole conc.

(iii) Conductivity & resistivity of doped semiconductor.

(IV) How many times conductivity is increased in the semiconductor due to doping?

$$\text{Assume total no. of atoms} = 4.421 \times 10^{22} / \text{cm}^3$$

$$n_i = 2.5 \times 10^{13} \text{ atoms/cm}^3$$

$$m_n = 3800 \text{ cm}^2/\text{Vsec}$$

$$m_p = 1800 \text{ "}$$

Soln:- (i) $N_d = \text{total no. of atoms/cm}^3 \times \text{Impurity ratio}$

$$= 4.421 \times 10^{22} \times \frac{1}{10^7}$$

$$= 4.421 \times 10^{15} \text{ atoms/cm}^3$$

(ii) In n-type semiconductor

$$n \approx N_d = 4.421 \times 10^{15} / \text{cm}^3$$

$$P = \frac{n_i^2}{n} = \frac{(2.5 \times 10^{13})^2}{4.421 \times 10^{15}}$$

$$P = 1.41 \times 10^{11} / \text{cm}^3$$

$$\sigma_N = N_d \cdot m_n$$

$$\approx 4.421 \times 10^{15} \times 1.6 \times 10^{-19} \times 3800$$

$$\approx 2.68 \Omega^{-1}/\text{cm}$$

$$R_N = \frac{1}{\sigma_N} = 0.373 \Omega \text{ cm}$$

(iv) Before doping the semiconductor is intrinsic.

$$\sigma_i = n_i \cdot [m_n + m_p]$$

$$= 2.5 \times 10^{13} \times 1.6 \times 10^{-19} [3800 + 1800]$$

$$= 0.0224 \Omega^{-1}/\text{cm}$$

By adding donor impurities $1:10^7$ the conductivity of semiconductor is increased from $0.0224 \Omega^{-1}/\text{cm}$ to $2.68 \Omega^{-1}/\text{cm}$. Increased conductivity due to doping

$$\therefore \frac{2.68}{0.0224} = 119 \approx 120 \text{ times}$$

ques:- A pure semiconductor is doped with acceptor impurities to extent of 4 impurity atom for every million of atoms (10^6). Calculate its conductivity.

Soln:- Acceptor impurities = $4: 10^6$

$$\text{Total no. of atoms} = 5 \times 10^{22} / \text{cm}^3$$

$$n_i = 1.5 \times 10^{10} \text{ atoms/cm}^3$$

$$u_n = 1300 \text{ cm}^2 \text{ V/sec}$$

$$u_p = 500 \text{ " " " }$$

$$N_A = 5 \times 10^{22} \times \frac{4}{10^6}$$

$$= 2 \times 10^{17} \text{ atoms/cm}^3$$

$$n_p = N_A \nu u_p$$

$$= 2 \times 10^{17} \times 1.6 \times 10^{-19} \times 500$$

$$\approx 16 \text{ A/cm}^2$$

ques:- A pure semiconductor (Si) is doped with donor impurities to a extent $1: 10^6$. Calculate

(1) Conductivity due to majority carriers

(II) " " " minority "

Assume

$$\text{total no. of atoms} = 5 \times 10^{22} / \text{cm}^3$$

$$n_i = 1.5 \times 10^{10} \text{ atoms/cm}^3$$

$$u_n = 1300 \text{ cm}^2 / \text{Vsec}$$

$$u_p = 500 \text{ " " " }$$

Soln:- In N-type semiconductor

(1) Conductivity due to majority carriers :-

$$N = N_d u_n \nu$$

$$= 5 \times 10^{16} \times 1.6 \times 10^{-19} \times 1300 = 10.4 \text{ A/cm}^2$$

$$N_S = \text{total no. of atoms/cm}^3 \times I \cdot R$$

$$= 5 \times 10^{22} \times \frac{1}{10^6} = 5 \times 10^{16}$$

(II) Minority $\approx \left[\frac{n_i^2}{N_S} \right] q \mu p$

$$\approx \frac{(1.5 \times 10^{10})^2}{5 \times 10^{16}} \times 1.6 \times 10^{-19} \times 500$$

$$\approx 3.6 \times 10^{-13} \text{ A/cm, Ans}$$

Ques: In a semiconductor at room temperature the intrinsic conc. & intrinsic resistivity are $1.5 \times 10^{16}/\text{cm}^3$ & $2 \times 10^3 \Omega \cdot \text{m}$ respectively. It is converted into extrinsic semiconductor with a doping concentration of $10^{20}/\text{cm}^3$. For the extrinsic semiconductor calculate

- (I) Minority carrier concentration
- (II) Resistivity
- (III) Electron mobility
- (IV) Minority carrier conc. when its temperature is increased to a value at which the intrinsic carrier conc. is doubled.

Assume ~~up to~~ the mobility of majority carriers is equal to the mobility of minority carriers.

Soln: — $\overset{\text{Intrinsic}}{=} \frac{1}{2 \times 10^3} \Rightarrow \rho_i = 2 \times 10^3$

$$\begin{aligned} \text{Minority carrier conc} &= \frac{n_i^2}{\text{Doping conc}} \\ &= \frac{(1.5 \times 10^{16})^2}{10^{20}} \\ &= 2.25 \times 10^{12}/\text{m}^3 \end{aligned}$$

$$(III) \quad \mu_n = \mu_p = \mu$$

$$P_i = \frac{1}{n_i q [\mu_n + \mu_p]}$$

$$= \frac{1}{n_i q \cdot 2\mu}$$

$$\mu = \frac{1}{P_i n_i q}$$

$$= \frac{1}{2 \times 10^3 \times 1.5 \times 10^{16} \times 2 \times 1.6 \times 10^{-19}}$$

$$\Rightarrow \mu = 0.1042 \text{ m}^2/\text{Vsec} = \mu_n = \mu_p$$

$$(III) \quad \varphi = \frac{1}{\text{carrier conc.} \times q \times \mu} = \frac{1}{\text{Doping conc.} \times q \times \mu}$$

$$= \frac{1}{10^{20} \times 1.6 \times 10^{-19} \times 0.1042} = 0.5998 \Omega \cdot \text{m}$$

(IV) As $T \uparrow$, n_i is doubled

$$\text{New } n_i = 2 \times 1.5 \times 10^{16} / \text{m}^3$$

Min. carrier conc. due to \uparrow in temperature

$$= \frac{(\text{New } n_i)^2}{\text{Doping conc.}} = \frac{(2 \times 1.5 \times 10^{16})^2}{10^{20}}$$

$$= 9 \times 10^{12} / \text{m}^3$$

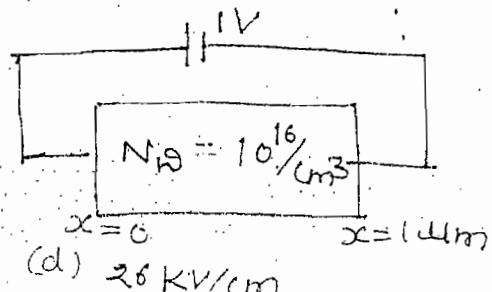
Ques:- The Silicon sample with unit cross-sectional area given below is under thermal equilibrium. The following information is given

$$T = 300 \text{ K} \quad q = 1.6 \times 10^{-19} \text{ C}$$

$$V_T = 26 \text{ mV} \quad \mu_n = 1350 \text{ cm}^2/\text{Vsec}$$

(i) The magnitude of electric field at $x = 0.5 \mu\text{m}$

- (a) 1kV/cm (b) 5kV/cm (c) 10kV/cm



(ii) The magnitude of drift current density at $x = 0.5 \mu\text{m}$

- (a) $4.32 \times 10^3 \text{ A/cm}^2$ (b) $6.48 \times 10^2 \text{ A/cm}^2$

- (c) $2.16 \times 10^4 \text{ A/cm}^2$ (d) $1.08 \times 10^4 \text{ A/cm}^2$

Soln: - (i) $|\mathcal{E}_d|_{x=0.5\mu\text{m}} = ?$

$$|\mathcal{E}_d|_{x=0.5\mu\text{m}} = \frac{|V_{x=0.5\mu\text{m}}|}{x=0.5\mu\text{m}} = \frac{0.5}{0.5 \times 10^{-6} \text{ m}}$$

$$|\mathcal{E}_d| = 10^6 \text{ V/m} = 10^4 \text{ V/cm} = 10 \text{ kV/cm}$$

(ii) $|\mathcal{J}_n(\text{drift})| = nq\mu_n |\mathcal{E}_d|_{x=0.5\mu\text{m}}$

$$n = N_D = 10^{16} / \text{cm}^3$$

$$= 10^{16} \times 1.6 \times 10^{-19} \times 1350 \times 10^4$$

$$= 2.16 \times 10^4 \text{ A/cm}^2$$

Minimum conductivity in the semiconductor :-

→ The conductivity of a semiconductor is

$$\sigma = nq\mu_n + p\mu_p \quad \text{---(i)}$$

→ By mass action law

$$P = \frac{n_i^2}{n} \quad \text{---(ii)}$$

Substitute eq-(ii) in eq-(i), we get

$$\sigma = nq\mu_n + \frac{n_i^2}{n} q\mu_p$$

Differentiate above eqn w.r.t. n

$$\frac{d\sigma}{dn} = q\mu_n + \left(-\frac{1}{n^2}\right) n_i^2 q\mu_p$$

$$\Rightarrow \frac{d^2\sigma}{dn^2} = 0 + \left(+ \frac{2}{n^2} \right) n_i^2 q \mu_p$$

Since second derivative is +ve, we get condition of minimum conductivity in a semiconductor.

The ~~plus~~ equation of min. conductivity can be obtained by $\frac{d\sigma}{dn} = 0$

$$\Rightarrow 0 = q \mu_n - \frac{n_i^2}{n^2} q \mu_p$$

$$\Rightarrow \mu_n = \frac{n_i^2}{n^2} \mu_p \Rightarrow n^2 = n_i^2 \frac{\mu_p}{\mu_n}$$

$$\Rightarrow n = n_i \sqrt{\frac{\mu_p}{\mu_n}} \quad \text{--- (A)}$$

The above equation indicates the conc. of e's in the semiconductor when conductivity is minimum

Substitute eq-(A) in eq-(II).

$$P = \frac{n_i^2}{n_i \sqrt{\frac{\mu_p}{\mu_n}}} \Rightarrow P = n_i \sqrt{\frac{\mu_n}{\mu_p}}$$

Equation -B denotes conc. of hole in the semiconductor when conductivity is minimum

Substitute eq-(A) & (B) in eq-(I), we get the equation for minimum conductivity

$$\sigma_{\min} = n_i \sqrt{\frac{\mu_p}{\mu_n}} q \mu_n + n_i \sqrt{\frac{\mu_n}{\mu_p}} q \mu_p$$

$$\Rightarrow \min \sigma = n_i q [\sqrt{\mu_n \mu_p} + \sqrt{\mu_n \mu_p}]$$

$$\Rightarrow \min \sigma = 2 q n_i \sqrt{\mu_n \mu_p}$$

Ques:- A semiconductor has the following parameters
 $\mu_n = 7500 \text{ cm}^2/\text{vsec}$
 $\mu_p = 300 \text{ "}$
 $n_i = 3.6 \times 10^{12}/\text{cm}^3$

Find (a) min. σ

(b) Hole conc. in the semiconductor when σ is min.

(c) e conc. in the semiconductor when σ is minimum.

Soln:- (I) $\min \sigma = 2q n_i \sqrt{\mu_n \mu_p}$

$$= 1.7 \times 10^{-3} \text{ A/cm}^2$$

(II) $P = n_i \sqrt{\mu_n / \mu_p} = 1.8 \times 10^{13} / \text{cm}^3$

(III) $n = n_i \sqrt{\mu_p / \mu_n} = 7.2 \times 10^{11} / \text{cm}^3$

Ques:- The diffusion constant for hole in Si is $13 \text{ cm}^2/\text{sec}$. What is the diffusion current if the gradient of hole conc. is $-2 \times 10^{14} \text{ holes/cm}^3/\text{cm}$

(a) -0.416 mA (b) $-3.2 \times 10^{-5} \text{ A}$ (c) $+32 \text{ mA}$

Ans: $+0.416 \text{ mA}$

Soln:- $I_{P(\text{diff.})} = J_{P(\text{diff.})} \times \text{Area}$

$$= -q \mu_p \frac{dP}{dx} \times \text{Area}$$

By default, Area = 1 cm^2

$$I_{P(\text{diff.})} = -1.6 \times 10^{-19} (13) [-2 \times 10^{14}] \times 1$$

$$= +0.416 \text{ mA, Ans}$$

Gallium-Arsenide (GaAs) :-

- It is a compound obtained with Ga from 3rd group & As from 5th group.
- It is the best example of direct band gap semiconductor material.
- During the recombination mostly of the energy released in the form of light.
- GaAs emits Infrared radiation.
- Cutting Voltage = 1.3 V
- $E_{G0} = 1.43 \text{ eV}$
- $\mu_n = 5600 \text{ cm}^2/\text{Vsec} + 8500 \text{ cm}^2/\text{Vsec}$
- $\mu_p = 400 \text{ cm}^2/\text{Vsec}$
- Higher conductivity.
- Switching times are very small.
- Suitable for microwave switching application
- fastest semiconductor material.
- Low noise microwave material.
- f noise is very small.
- GaAs is used in the fabrication of laser, LED, PIN diode, IMPATT diode, Tunnel diode, Varactor diode and microwave IC's
- An alternative for GaAs is InP
- GaAs exhibits -ve differential mobility & due to this property it is more suitable for higher frequency or microwave application.

- The nature of bonding in GaAs is mixed bonding.
For objective type → it is covalent bonding.
- GaAs can be converted into n-type GaAs or p-type GaAs by adding amphoteric material.
- When Ge, Be, Zn, Cd are added to gallium arsenide they will be working as acceptor in GaAs and they ~~will~~ replace the As so we get p-type GaAs.
- When Si, Se & Te are added to GaAs they will be working as donors in GaAs and replace the As. ~~and~~ and we get n-type GaAs.
- When Si is added to GaAs, we get n-type GaAs.

CARRIER CONCENTRATION :-

- They are charge carriers which are contributing current or conductivity.

CARRIER CONC. IN INTRINSIC SEMICONDUCTOR :-

$$n_i = n_e u_n + P_h u_p$$

In intrinsic semiconductor carrier conc means \bar{e} & hole conc.

EFFECT OF TEMPERATURE ON CARRIER CONC. IN INTRINSIC SEMICONDUCTOR :-

$$n = p = n_i$$

$$\text{But } n_i \propto T^{3/2}$$

Hence $n \uparrow$ with $T \uparrow$ & $P \uparrow$ with $T \uparrow$

In intrinsic semiconductor carrier conc increases with the temperature.

Effect of temperature on the conductivity of intrinsic semiconductor :-

$$\sigma_i = n_i q [m_n + m_p]$$

$$\sigma_i \propto n_i$$

$$\text{but } n_i \propto T^{3/2}$$

$$\sigma_i \uparrow \text{ with } T$$

In intrinsic semiconductor, conductivity increases with the temperature.

Effect of temperature on the mobility of charge carriers:-

$$m \propto T^{-m}$$

Mobility of charge carriers is always dec. with the temperature.

Carrier conc. in extrinsic semiconductor :-

In extrinsic semiconductor, conductivity is mainly due to majority carriers and therefore in extrinsic SC carrier conc. means majority carrier conc.

Effect of doping on carrier conc.:-

N-type SC

Majority carriers are e's

$$n \approx N_A$$

P-type SC

Majority carriers are holes

$$P \approx N_D$$

Carrier concentration increases with doping.

Effect of doping on majority & minority carriers:-

N-Type SC

Majority carriers are \bar{e} 's

$$n \approx N_D$$

Minority carriers are holes

$$P = \frac{n_i^2}{n} = \frac{n_i^2}{N_D}$$

For P-Type SC

Majority carriers are holes

$$P \approx N_A$$

Minority carriers are \bar{e} 's

$$n = \frac{n_i^2}{P} = \frac{n_i^2}{N_A}$$

Majority carrier conc. \propto Doping

Minority carrier conc. $\propto \frac{1}{\text{Doping Conc.}}$

Doping inc. majority carriers and simultaneously dec. minority carriers.

Effect of doping on the conductivity of extrinsic semiconductor

For N-type SC

$$\tau_n \approx N_D^{-1} u_n$$

$$\tau_n \propto N_D$$

For P-type SC

$$\tau_p \approx N_A^{-1} u_p$$

$$\tau_p \propto N_A$$

In extrinsic semiconductor, conductivity inc. with the doping.

- A highly doped semiconductor exhibits metallic properties i.e.
 - (i) very larger conductivity
 - (ii) NTC of resistance in the semiconductor will become PTC of resistance.
 - (iii) Bipolar nature of semiconductor will ~~work as~~ become unipolar.
- A highly doped semiconductor will work as a conductor.

Effect of doping on the mobility of charge carriers:-

As doping increases, the conc. of atoms in the semiconductor inc. and thereby mobility of charge carriers decreases.

Mobility of charge carriers will always decrease with doping.

NOTE :-

In the absence of any derived equation for mobility we always consider mobility of charge carriers will remain same before and after the doping for solving the problem.

Effect of temperature on majority & minority carriers :-

Considering a bar of Si material when it is pure, $n = p = n_i$

$$= 1.5 \times 10^{10} \text{ atoms/cm}^3$$

By adding pentavalent impurities of $1:10^6$, semiconductor becomes n-type.

$$N_D = 5 \times 10^{22} \times \frac{1}{10^6} = 5 \times 10^{16} \text{ atoms/cm}^3$$

In n-type semiconductor at 300K

Majority carriers are e's

$$n \approx N_D \Rightarrow 5 \times 10^{16} / \text{cm}^3$$

Minority carriers are holes

$$P = \frac{n_i^2}{n} = \frac{(1.5 \times 10^{10})^2}{5 \times 10^{16}}$$

$$P = 4500 / \text{cm}^3$$

Let Temp \uparrow i.e. $T > 300\text{K}$

Let 10^6 covalent bonds are broken

Thermally generated e's $\Rightarrow 10^6 / \text{cm}^3$

" " holes $\Rightarrow 10^6 / \text{cm}^3$

10^6 e's will be moving from VB to CB

Total no. of e's in the CB:

$$n = 5 \times 10^{16} / \text{cm}^3 + 10^6 / \text{cm}^3$$

$$(n = N_D + P)$$

$$n = 5 \times 10^{16} / \text{cm}^3$$

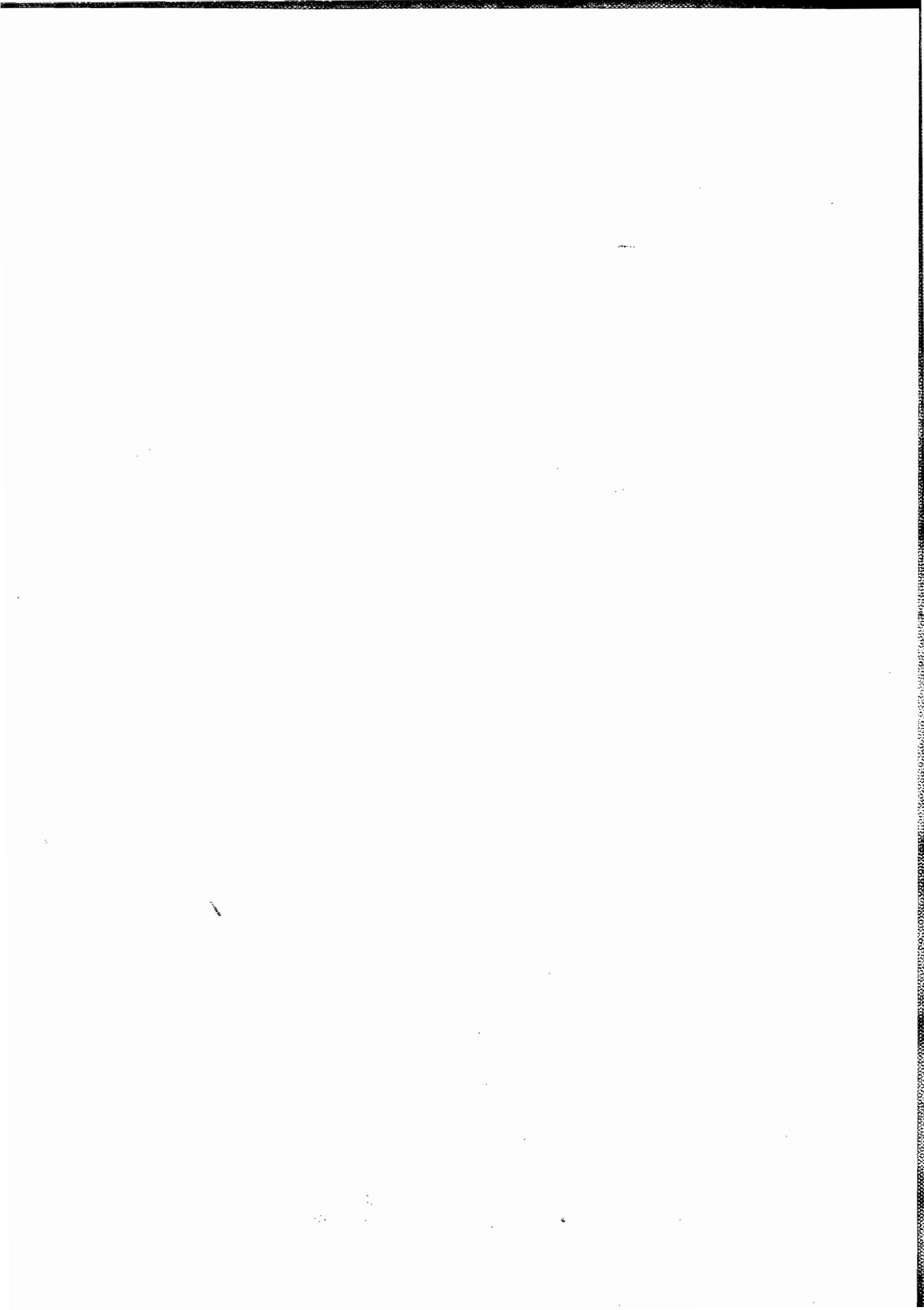
\uparrow in majority carrier conc. due to temp
is negligible

Total no. of holes in the VB

$$P = 4500 / \text{cm}^3 + 10^6 / \text{cm}^3$$

$$\Rightarrow P = 10^6 / \text{cm}^3$$

- ↑ in minority carrier conc is very large
- Majority carrier conc. is almost independent of temperature.
- Minority carrier conc. will be increasing with the temperature.



Lecture - 6

Effect of temperature on the conductivity of extrinsic semiconductor :-

→ Vs temperature curve →

for extrinsic semiconductor

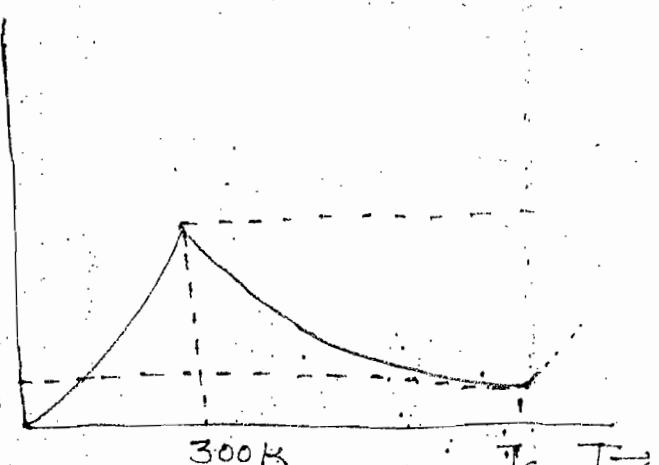
max →

→ At 0K carrier conc.

is zero. Hence,

conductivity is zero

min →



- Semiconductor curves are always non-linear
- Below room temperature in extrinsic semiconductor the conductivity increases and at room temperature conductivity is maximum and after room temperature the conductivity decreases with temperature (due to mobility)
- At curve temperature (T_c) minority carrier conc. = majority carrier conc. then the extrinsic semiconductor became intrinsic
- At curve temperature conductivity of semiconductor is minimum and min. is slightly greater than σ_i (intrinsic conductivity)

At $T=0K$:

Carrier conc. are zero and therefore conductivity is zero and extrinsic semiconductor at 0K will be working as an insulator.

At $0K < T < 300K$:

As temperature is increases because of thermal energy, a large no. of covalent bonds will be broken and equal no. of electrons and holes are created and due to the doping majority and minority carriers are created and the conductivity of the extrinsic semiconductor will be increases with the temperature.

At $T = 300K$:-

The conductivity of extrinsic semiconductor is maximum.

At $300K < T < T_c$:-

- Majority carrier conc. will remain almost independent of temperature.
- Minority carrier conc. will be increases with the temperature.
- As temperature increases, mobility of charge carriers decreases and therefore the conductivity of extrinsic semiconductor will be decreases with the temperature.

At $T = T_c$:-

At curie temperature minority carrier conc. approaches majority carrier conc. and extrinsic semiconductor will become intrinsic semiconductor and conductivity will become minimum.

$T > T_c$:-

Above the curie temperature, since the semiconductor is intrinsic, its conductivity will be increases with the temperature.

→ At very high temperature the extrinsic semiconductor will work as intrinsic semiconductor.

→ $T_c \ggg 400K$:-

(I) At very high temperature extrinsic semiconductor will become intrinsic semiconductor.

(II) At low temperature, the conductivity of extrinsic semiconductor will be increases with the temperature.

(III) In extrinsic semiconductor as temperature increases, its conductivity decreases
(Consider above $300K$)

NOTE:-

For intrinsic semiconductor

$\rightarrow \uparrow$ with $T \uparrow$

so $p \downarrow$ with $T \downarrow$

NTC of R

For extrinsic semiconductor

$\rightarrow \downarrow$ with $T \uparrow$

so \uparrow^* with $T \uparrow$

PTC of R

(Because of doping)

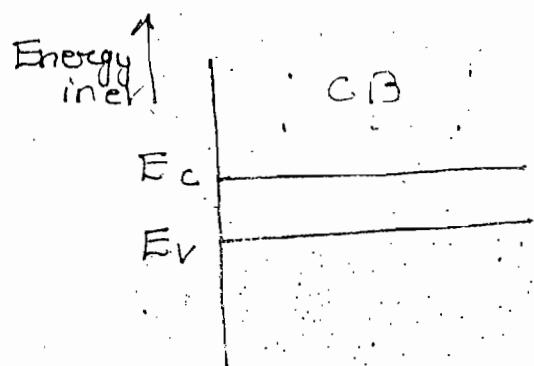
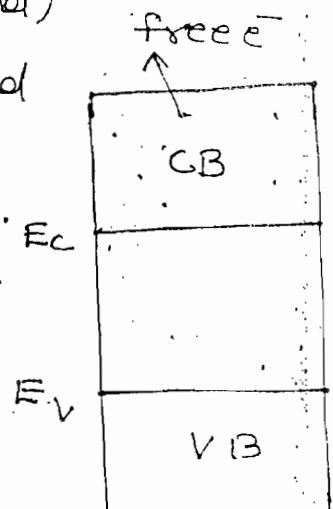
Conc. of free \bar{e} in the conduction band :-

E_c (min. energy of conduction band)

E_v = max. energy of valence band

Approx Energy Band Diagram :-

$$n = \int_{E_c}^{+\infty} \dots [\bar{e} \text{ energy from } E_c \text{ to } \infty]$$



(hole energy $-\infty$ to E_v)

Exact Energy Band Diagram :-

- E_c min. energy of the conduction band or energy at the edge of the conduction band.
- E_v max. energy of the valence band or energy at the edge of valence band.
- The energy possessed by free \bar{e} will be in the range of (E_c to ∞)

The conc. of \bar{e} in the conduction band is given by

$$n = N_c e^{-(E_c - E_F)/kT}$$

or

$$n = N_c e^{-(E_c - E_F)/kT}$$

where E_F = Fermi energy in eV

N_c = material constant and is a function of temperature

$$N_c = 2 \left(\frac{2\pi k T m_n}{h^2} \right)^{3/2}$$

$$N_c = 2 \left(\frac{2\pi k m_n}{h^2} \right)^{3/2} T^{3/2}$$

where h = Planck's constant

$$= 6.64 \times 10^{-34} \text{ J sec.}$$

If $T = 300$, then

$$N_c =$$

N_c is approximately equal of states in the conduction band

m_n = effective mass of \bar{e}

Effective mass of the \bar{e} is the mass of \bar{e} in the given material when \bar{e} is revolving in its orbit

For Si $\frac{m_n}{m} = 1.08 \Rightarrow m_n = 1.08 m$

$$\Rightarrow m_n = 1.08 \times 9.1 \times 10^{-31} \text{ kg}$$

rest mass of \bar{e}
 $(9.1 \times 10^{-31} \text{ kg})$

NOTE:- Effective mass of \bar{e} is greater than the rest mass of \bar{e} . i.e. $m_n > m$ i.e. 8% greater

Concentration of hole in valence band :-

The energy possessed by holes in valence band is in the range of $(-\infty \text{ to } +E_V)$

→ The conc. of hole in the valence band is

$$P = N_V e^{-\frac{(E_F - E_V)}{KT}}$$

where N_V is a material constant and it is a function of temperature

$$\begin{aligned} N_V &= 2 \left(\frac{2\pi k T m_p}{h^2} \right)^{3/2} \\ &= 2 \left(\frac{2\pi k m_p}{h^2} \right)^{3/2} T^{3/2} \\ \Rightarrow N_V &= T^{3/2} \end{aligned}$$

NOTE :-

N_V is approximately equal to density of states in Valency band

If $T = 300K$, then

$$\Rightarrow N_V =$$

m_p = effective mass of hole

For Si:

$$\left(\frac{m_p}{m} \right) = 0.56 \Rightarrow m_p = 0.56 \underline{m} \quad \begin{matrix} \rightarrow \text{IES} \\ \text{mass of proton} \\ (1.6 \times 10^{-27} \text{ kg}) \end{matrix}$$

$$\begin{aligned} m_p &= 0.56 \times 1.6 \times 10^{-27} \\ &= 0.896 \times 10^{-27} \text{ kg} \end{aligned}$$

NOTE:-

1. Effective mass of electron is greater than the rest mass of electron i.e. $m_n > m$
2. If $m_n = m_p$ then $N_c = N_V$
3. Effective mass of hole is greater than effective mass of \bar{e} .

Derive an equation for intrinsic concentration n_i :

In a semiconductor

$$n = N_c \cdot e^{-\frac{(E_c - E_F)}{kT}} \quad \text{--- (I)}$$

$$p = N_v \cdot e^{-\frac{(E_F - E_v)}{kT}} \quad \text{--- (II)}$$

Multiply eq-(I) & (II)

$$\begin{aligned} np &= N_c N_v e^{-\frac{E_c + E_F - E_F + E_v}{kT}} \\ \Rightarrow np &= N_c N_v e^{-\frac{[E_c - E_v]}{kT}} \end{aligned}$$

$$\text{Since } np = n_i^2 \quad \& \quad E_c - E_v = E_G$$

$$\Rightarrow \boxed{n_i^2 = N_c N_v e^{-\frac{E_G}{kT}}} \quad \text{--- (III)}$$

$$\text{but } N_c = 2 \left(\frac{2\pi k T m_n}{h^2} \right)^{3/2}$$

$$N_v = 2 \left(\frac{2\pi k T m_p}{h^2} \right)^{3/2}$$

$$\Rightarrow N_c \times N_v = 4 \left(\frac{2\pi k}{h^2} \right)^3 (m_n m_p)^{3/2} T^3$$

$$\text{Let } 4 \left(\frac{2\pi k}{h^2} \right)^3 (m_n m_p)^{3/2} = A_0 \text{ then}$$

$$\Rightarrow N_c N_v = A_0 T^3 \quad \text{--- (IV)}$$

Substitute eq-(IV) in eq-(III)

$$\boxed{n_i^2 = A_0 T^3 e^{-\frac{E_G}{kT}}}$$

or

$$\boxed{n_i = \sqrt{A_0} T^{3/2} e^{-\frac{E_G}{2kT}}}$$

Fermi Energy (E_F): -

Fermi energy is defined as the maximum energy possessed by the \bar{e} at 0K

OR

Fermi energy is defined as the maximum kinetic energy possessed by \bar{e} at 0K

$$\text{Fermi Energy} = \text{Max KE}$$

$$\Rightarrow E_F = \frac{1}{2} m v_{\max}^2$$

where m = rest mass of \bar{e}

$$= 9.1 \times 10^{-31} \text{ kg}$$

$$\Rightarrow v_{\max} = \sqrt{\frac{2 E_F}{m}} \text{ m/s}$$

It is the equation for velocity of \bar{e} terms of fermi energy

OR

Fermi energy is also defined as the energy possessed by fastest moving \bar{e} at 0K.

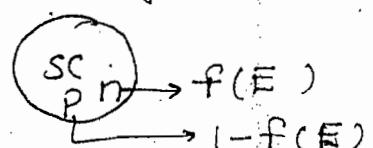
Fermi-Dirac Function: - $f(E)$

→ It is also called as Fermi-Dirac probability function.

→ $f(E)$ indicate the probability \bar{e} existing as a function of E .

For metal or semiconductor

$$f(E) = \frac{1}{1 + e^{[E - E_F]/kT}}$$



where E = Energy possessed by the \bar{e} in eV

At $T=0K$, we get two possible conditions

$$(i) E > E_F, f(E) = \frac{1}{1 + e^{+\infty}} = \frac{1}{1 + \infty} = 0$$

This indicates no \bar{e} 's available in the semiconductor with energies $E > E_F$ since the probability answer is 0.

$$(ii) E < E_F, f(E) = \frac{1}{1 + e^{-\infty}} = \frac{1}{1 + 0} = 1$$

or
100%

Since probability is 1 it indicates at $T=0K$, \bar{e} 's are available in the semiconductor with energies $E < E_F$.

At $T \neq 0K$ $T > 0K$:

$$\text{If } E = E_F, f(E) = \frac{1}{1 + e^0} = \frac{1}{2} \text{ or } 0.5 \text{ or } 50\%$$

→ Fermi level is the characteristic level with 50% probability of being filled, if no forbidden band exists.

- In metal probability of \bar{e} existing is 1 or 100%
- In a semiconductor if the probability of \bar{e} existing is $f(E)$ then probability of hole existing in the semiconductor is $[1 - f(E)]$

Fermi Level in intrinsic semiconductor:

In intrinsic semiconductor

$$n = p$$

$$\Rightarrow N_c \epsilon^{-(E_c - E_F)/kT} = N_v \epsilon^{-(E_F - E_v)/kT}$$

$$\Rightarrow \frac{N_c}{N_v} = \epsilon^{-\frac{E_F + E_v + E_c - 2E_F}{kT}}$$

$$\Rightarrow \log \frac{N_c}{N_v} = \frac{E_c + E_v - 2E_F}{kT}$$

$$E_c + E_v - 2E_F = kT \log_e \frac{N_c}{N_v}$$

$$\Rightarrow E_F = \frac{E_c + E_v}{2} - \frac{kT}{2} \log_e \frac{N_c}{N_v}$$

In intrinsic semiconductor, fermi level depends only on temperature.

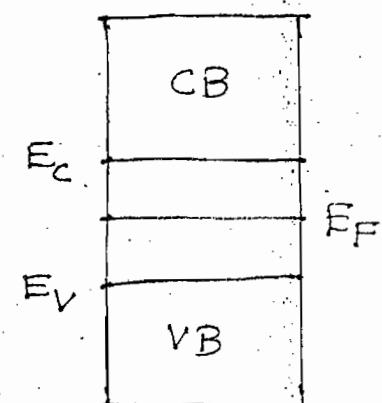
Case-(I) :-

$$\text{Let } m_n = m_p$$

$$\text{then } N_c = N_v$$

$$\Rightarrow \log_e \frac{N_c}{N_v} = 0$$

$$\Rightarrow E_F = \frac{E_c + E_v}{2}$$



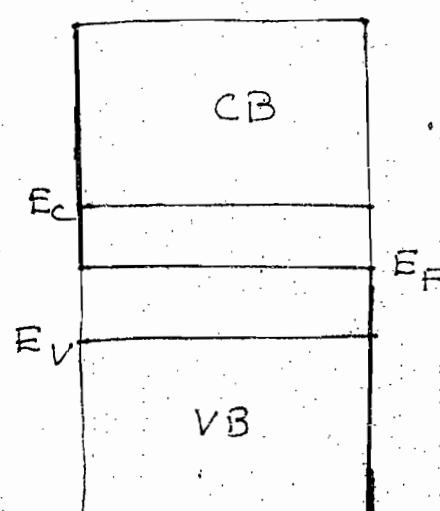
The fermi level now existing exactly at the centre of energy gap

Case-(II) :-

$$At \quad T=0K$$

$$E_F = \frac{E_c + E_v}{2}$$

In intrinsic semiconductor at 0K, fermi level is existing exactly at the centre of energy gap.



NOTE :-

In intrinsic semiconductor, fermi level will be existing exactly at the centre of the energy gap under the following conditions:-

$$(I) \quad m_n = m_p$$

$$(II) \quad N_c = N_v$$

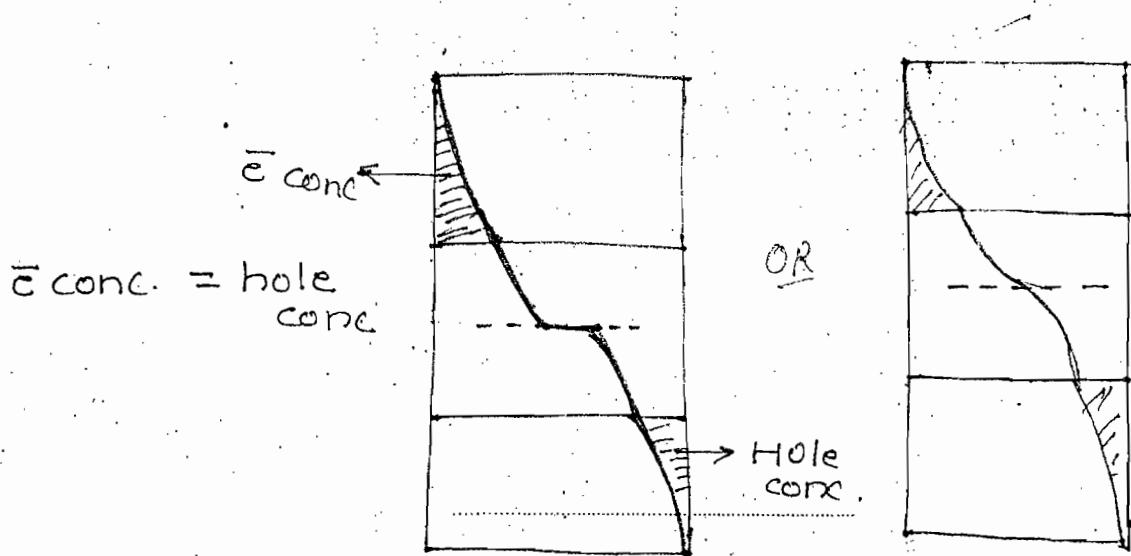
$$(III) \quad T = 0K$$

Case-(III) :-

Let $T = 300K$

$$E_F = \frac{E_c + E_v}{2} - \frac{KT}{2} \log_e \frac{N_c}{N_v}$$

where $T = 300K$



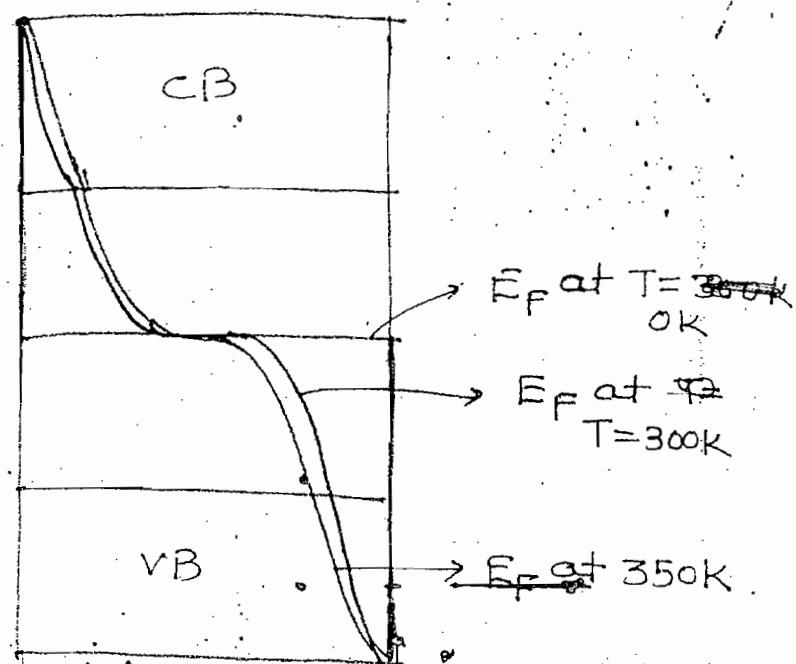
In intrinsic semiconductor at room temperature, the fermi level will be passing through the centre of the energy gap.

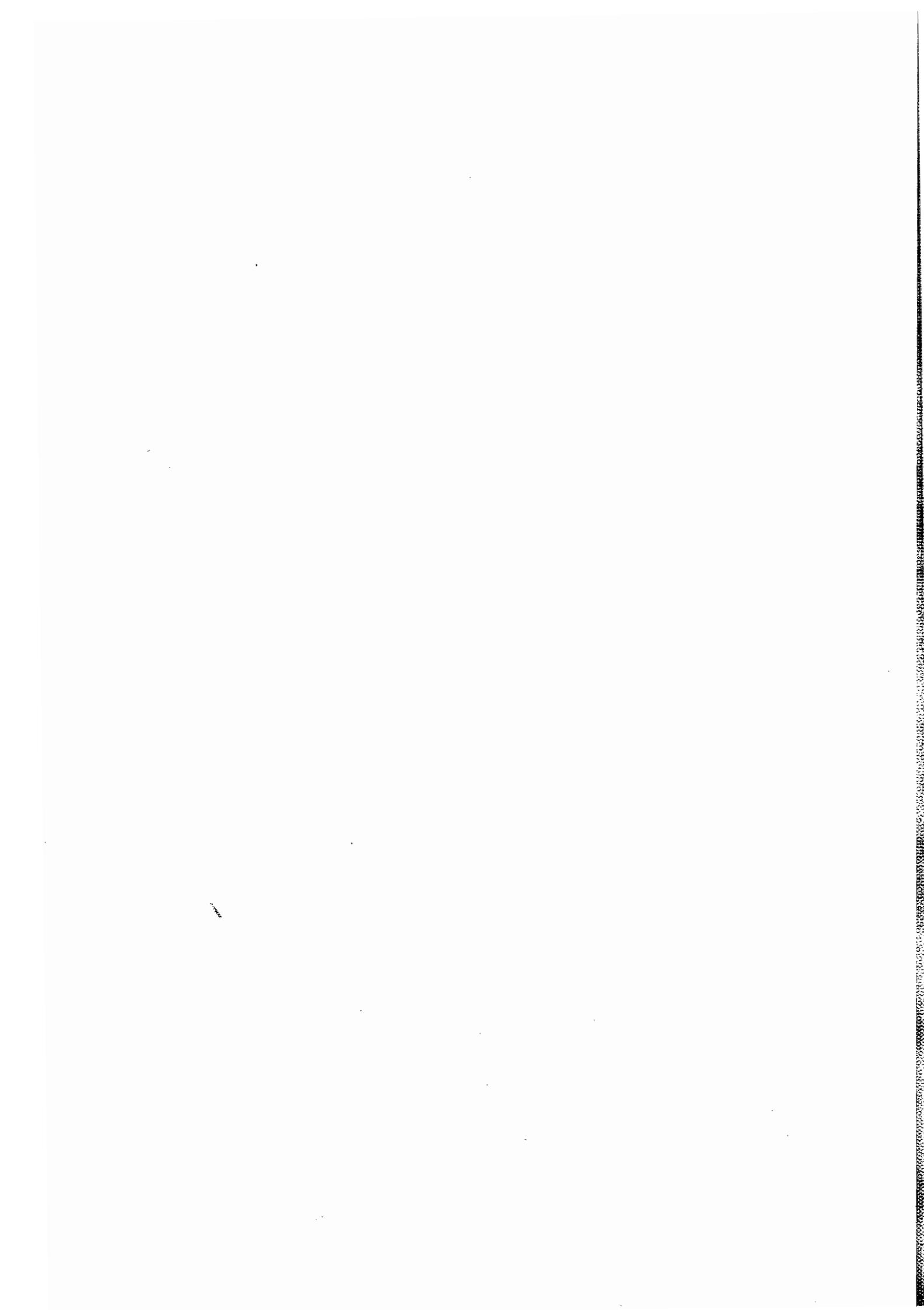
[Slightly above the centre of the energy gap]

At room temperature because of thermal energy a no. of covalent bond will be broken and equal no. of e^- & holes are created and there will be a small conductivity in the semiconductor.

Case - (IV) :-

Position of Fermi level in intrinsic semi-conductor at different temperature :-





Lecture - 4

Fermi level in n-type semiconductor

$$n \approx N_D$$

$$\Rightarrow N_C e^{-(E_C - E_F)/kT} = N_D$$

$$\Rightarrow \frac{N_C}{N_D} = e^{(E_C - E_F)/kT}$$

$$\Rightarrow \log_e \frac{N_C}{N_D} = \frac{E_C - E_F}{kT}$$

$$\Rightarrow E_C - E_F = kT \log_e \frac{N_C}{N_D}$$

It indicates the position of fermi level below the conduction band

$$E_F = E_C - kT \log_e \frac{N_C}{N_D}$$

In n-type semiconductor, fermi level is a function of temperature and doping conc.

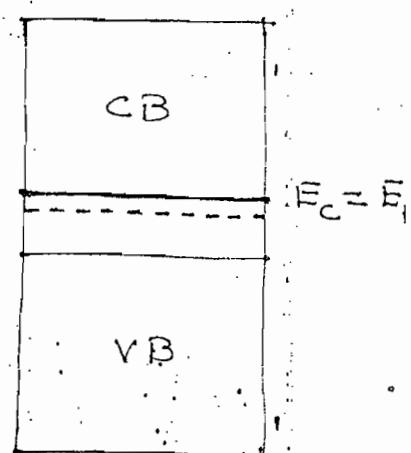
Case - (I) :-

Let $T = 0K$

$$\Rightarrow E_F = E_C$$

E_F coincides with the edge E_C of conduction band

→ Donor energy level is always nearer to conduction band as compare to centre.



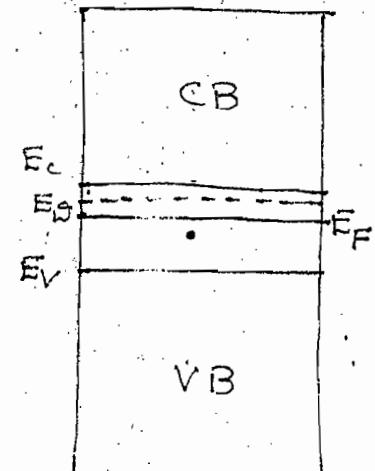
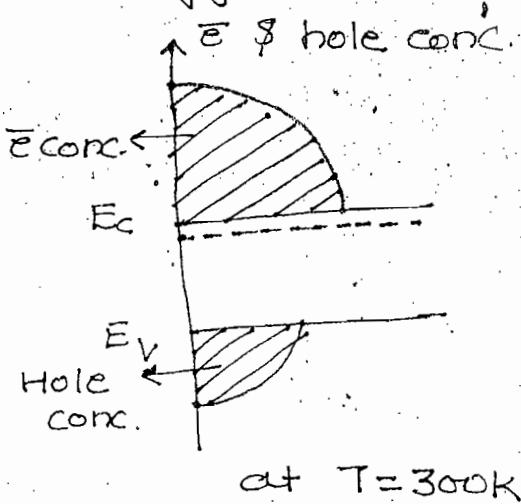
Case - (II) :-

Let $T = 300K$

$$E_F = E_C - kT \log_e \frac{N_C}{N_D}$$

where $T = 300K$.

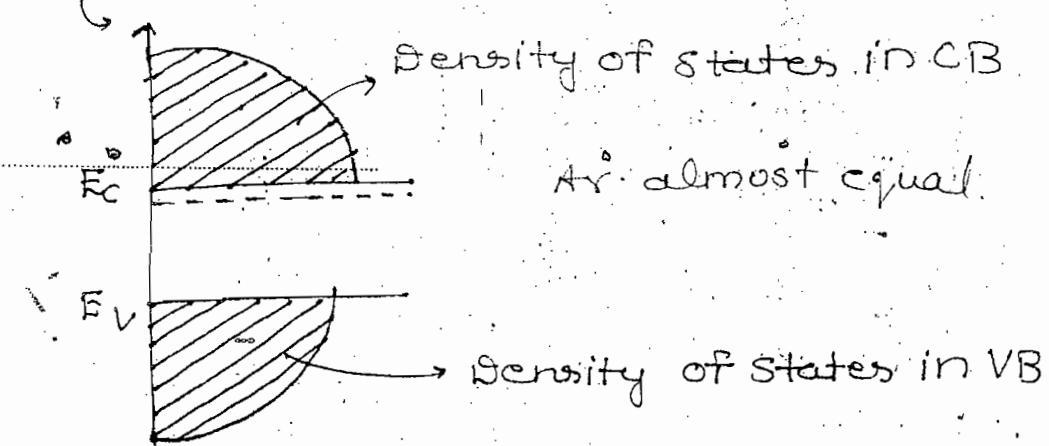
- At room temperature, in n-type semiconductor, fermi level exist just below the donor energy level
- In n-type semiconductor as temperature increases from 0K to 300K at some intermediate temperature, the fermi-level will be coinciding with the donor energy level.



$\bar{e} \text{ conc.} \gg \text{Hole conc.}$

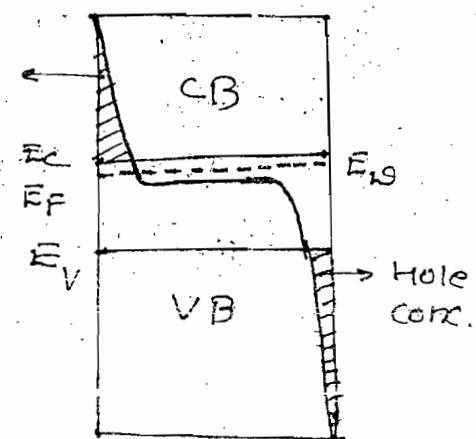
Different
→ Shape of $\bar{e} \text{ & conc.}$
are possible acc.
to your choice

Sensity of states



$\bar{e} \text{ conc.}$

Diagrammatic Representation
of both \bar{e} , hole conc. &
Fermi level



Case - (III) :-

Mathematical Analysis :-

$$E_C - E_F = kT \log_c \frac{N_c}{N_D}$$

→ Fermi level depends on temperature & Doping conc.

(1) Effect of temperature :-

As temp ↑ , $N_c \uparrow$ & let $N_c > N_D$ ($T > 300$)

$$E_C - E_F > 0$$

$$\Rightarrow \boxed{E_C > E_F}$$

→ In N-type, as temperature inc, E_F moves away from conduction band or E_F moves towards the center of energy gap. Hence ↓ with the temperature.

→ Temperature denotes the fermi level of intrinsic semiconductor.

→ The position of fermi level at different temp in the N-type semiconductor as given below.

→ At critic temperature, in N-type semiconductor, the fermi level will be at the centre of energy gap and the conductivity will be minimum and n-type ~~semiconductor~~ semiconductor will become intrinsic semiconductor.

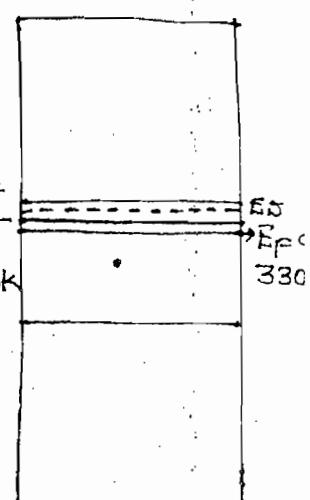
(II) Effect of Doping :-

As doping (N_D) ↑

Let $N_D > N_c$

$$E_C - E_F < 0, \Rightarrow$$

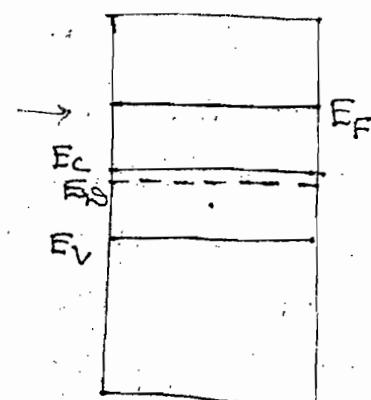
$$\boxed{E_C < E_F}$$



- In N-Type semiconductor, as doping (N_D) ↑ E_F moves towards conduction band or E_F moves away from the center of energy gap. Hence ↑ with doping.
- In N-type semiconductor as doping increases, fermi level takes upward shift
- In a highly doped semiconductor or highly degenerate n-type semiconductor, fermi level will be in the conduction band

N^+ semiconductor at 300K

"BHARAT PHOTOSTAT"



Cause - (IV) :-

Shift in the position of fermi level due to doping :-

OR

Shift in the position of E_F w.r.t E_F of intrinsic semiconductor :-

OR

Shift in the position of E_F w.r.t center of energy gap :-

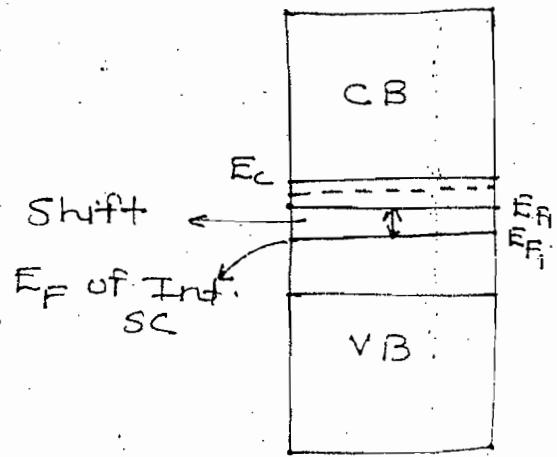
**

$$\text{Shift} = KT \log_e \frac{N_D}{N_i} \text{ eV}$$

**

OR

$$\text{Shift} = KT \log_e \frac{n}{n_i} \text{ eV}$$



Case-(v) :-

Derivation for Shift :-

$$\text{Shift} = E_{FN} - E_{Fi}$$

$$\text{But } E_{FN} = E_c - KT \log_e \frac{N_c}{N_D}$$

$$\therefore E_{Fi} = \frac{E_c + E_v}{2} - \frac{KT}{2} \log_e \frac{N_c}{N_v}$$

Fermi Level in P-Type semiconductor :-

$$P \approx N_A$$

$$\Rightarrow N_V e^{-(E_F - E_V)/kT} = N_A$$

$$\Rightarrow \frac{N_V}{N_A} = e^{(E_F - E_V)/kT}$$

$$\Rightarrow \log_e \frac{N_V}{N_A} = \frac{E_F - E_V}{kT}$$

$$\Rightarrow E_F - E_V = kT \log_e \frac{N_V}{N_A}$$

It indicates the position of fermi level above the valence band in the p-type semiconductor.

$$E_F = E_V + kT \log_e \frac{N_V}{N_A}$$

In p-type semiconductors, fermi level is a function of temperature and doping conc.

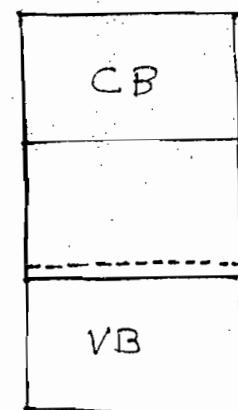
Case-(I) :-

At T=0K

$$E_F = E_V$$

→ E_F coincides with the edge of VB

→ At 0K, carrier conc. are zero and therefore $\tau = 0$: Hence p-type semiconductor at 0K will be working as insulator.

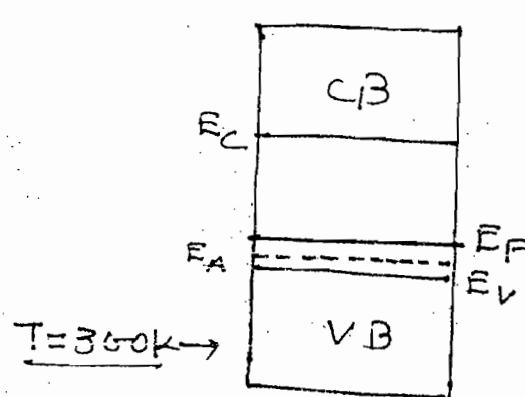


Case-(II) :-

At T=300K

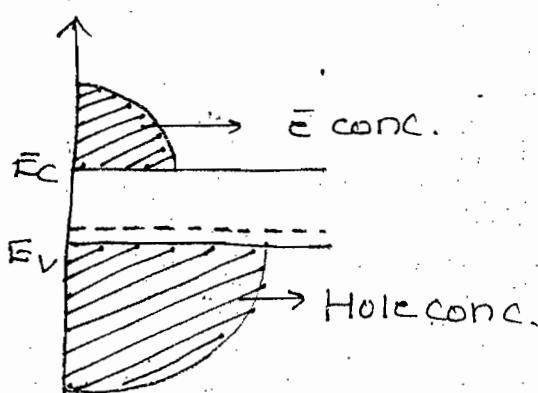
$$E_F = E_V + kT \log_e \frac{N_V}{N_A}$$

where $T = 300K$.



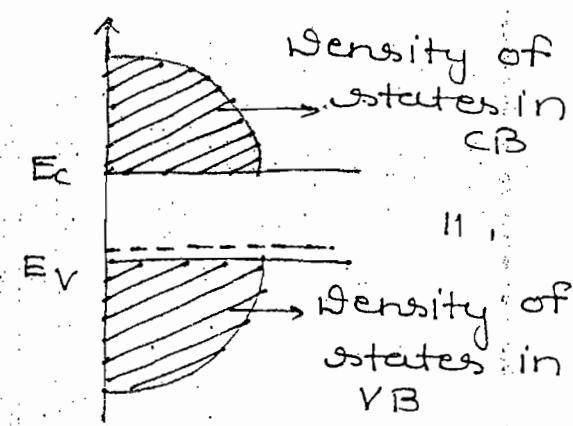
→ In p-type semiconductor at room temperature fermi level exist just above the acceptor energy level.

\bar{e} & hole conc.



Hole conc. $\gg \bar{e}$ conc.

Sensity of states



Cause-(III) :-

Mathematical Analysis:-

$$E_F - E_V = kT \log_e \frac{N_V}{N_A}$$

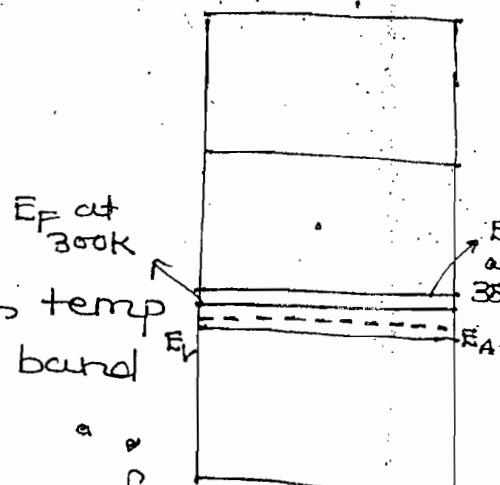
(1) Effect of temperature :-

As temp \uparrow , $N_V \uparrow$ ($T > 300\text{K}$)

Let $N_V > N_A$

$$E_F - E_V > 0$$

$$\Rightarrow \boxed{E_F > E_V}$$



In p-type semiconductor, as temp

↑ E_F moves away from valence band
or

E_F moves towards the center of energy gap. Hence \downarrow with temperature

→ In p-type semiconductor, the position of fermi level for different temperature is given above

(II) Effect of doping :-

As doping (N_A) \uparrow & Let $N_A > N_V$

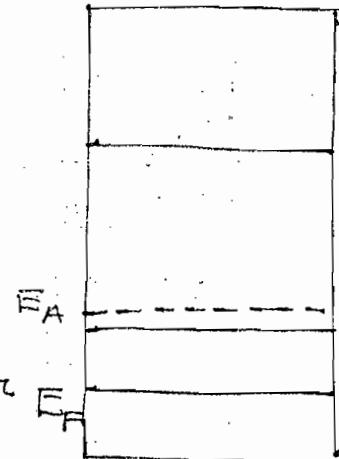
$$E_F - E_V < 0$$

$$\Rightarrow E_F < E_V$$

→ In p-type semiconductor, as doping (N_A) \uparrow , E_F moves towards the valence band.

OR

E_F moves away from the center of energy gap. Hence $\rightarrow \uparrow$ with doping



→ In p-type semiconductor, as doping inc, fermi level takes downward shift.

Downward shift is denoted with -ve sign

→ In a highly doped p-type semiconductor or highly degenerate p-type semiconductor, fermi level exist in the valence band.

Cause-(IV) :-

Shift in the position of E_F due to doping

OR

Shift in the position of E_F w.r.t. E_F of intrinsic semiconductor

OR

Shift in the position of E_F w.r.t center of energy gap :-

$$\text{Shift} = -KT \log_e \frac{N_A}{N_i} \text{ eV}$$

OR

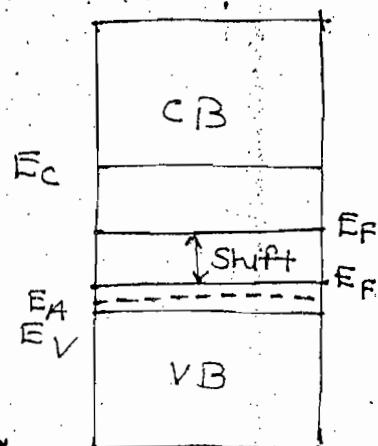
$$\text{Shift} = -KT \log_e \frac{P}{n_i} \text{ eV}$$

case-cr :-

$$\text{Shift} = E_{FP} - E_{FI}$$

$$\text{But } E_{FP} = E_V + kT \log_e \frac{N_V}{N_A}$$

$$\therefore E_{FI} = \frac{E_C + E_V}{2} - \frac{kT}{2} \log_e \frac{N_C}{N_V}$$



NOTE :-

→ In the p-type semiconductor, at cubic temperature, the fermi level will be at the center of energy gap and the conductivity will become minimum and also the p-type semiconductor will become intrinsic semiconductor.

ques:- In an n-type semiconductor, the fermi level lies 0.3 eV below conduction band at 300K, if the temp is increased to 330. Find the approx. new position of fermi level.

Soln:- N-Type SC

$$E_c - E_F = kT \log_e \frac{N_c}{N_B}$$

Since N_c value is not given and cannot be found the variation of N_c with the temperature is neglected and therefore

$$E_c \propto E_F \propto T$$

$$\Rightarrow 0.3 \text{ eV} \propto 300 \quad (I)$$

$$E_c - E_F \propto 330 \quad (II)$$

$$\Rightarrow E_c - E_F = \frac{330 \times 0.3 \text{ eV}}{300} = 0.33 \text{ eV}$$

ques:- In the n-type sc, the fermi level lies 0.4eV below the conduction band if the conc. of donor atoms is doubled find the new position of fermi level.

Assume $kT = 0.03 \text{ eV}$

$$N_B \approx N_c e^{-(E_c - E_F)/kT}$$

$$N_B = N_c e^{-0.4/0.03} \quad (I)$$

$$2N_B = N_c e^{-\frac{(E_c - E_F)}{0.03}} \quad (II)$$

$$(I) \div (II)$$

$$\frac{1}{2} = \frac{e^{-0.4/0.03}}{e^{-\frac{(E_c - E_F)}{0.03}}}$$

$$\frac{1}{2} = e^{\frac{-0.4}{0.03}} + \left(\frac{E_c - E_{F_2}}{0.03} \right)$$

$$\Rightarrow \log \frac{1}{2} = \frac{-0.4}{0.03} + \frac{E_c - E_{F_2}}{0.03}$$

$$\Rightarrow E_c - E_{F_2} = 0.4 + 0.03 \log \frac{1}{2}$$

$$= 0.4$$

$$= 0.379 \text{ eV, Ans}$$

Ques:— In a p-type SC, the fermi level lies 0.4eV above the valence band, if the conc. of acceptor atoms is increased by 3 times. Find the new position of fermi level. Assume $kT = 0.03 \text{ eV}$

$$\text{Ans} = 0.367 \text{ eV}$$

Ques:- In a SC at room temperature, the intrinsic carrier conc. and intrinsic resistivity are $1.5 \times 10^{16} / \text{cm}^3$ and $2 \times 10^{13} \Omega \text{m}$ respectively. It is converted into an extrinsic semiconductor with a doping conc. of $10^{20} / \text{m}^3$. Find the shift in Fermi-level due to doping.

Soln:- Shift = $KT \log_e \frac{\text{Doping conc.}}{n_i} \text{ eV}$

$$= 8.62 \times 10^{-5} (300) \log_e \frac{10^{20}}{1.5 \times 10^{16}} \text{ eV}$$

$$= 0.227 \text{ eV, Ans}$$

Ques:- Si is doped with Boron conc. of 4×10^{17} atoms / cm^3 . Assume $n_i = 1.5 \times 10^{10} / \text{cm}^3$, $T = 27^\circ\text{C}$ compare to undoped Si, the Fermi level of doped Si.

Soln:- Shift = $-KT \log_e \frac{N_A}{n_i} \text{ eV}$

$$= -8.62 \times 10^{-5} \times 300 \times \log_e \frac{4 \times 10^{17}}{1.5 \times 10^{10}} \text{ eV}$$

$$= -0.442 \text{ eV, Ans.}$$

Downward shift = -0.442 eV } Ans.
or
Down shift of 0.442 eV

Ques:- A Si SC is doped with donor impurities with resultant doping profile $n = G_1 x$ & $n \gg n_i$, sample is spaced isolated. Find the built-in electric field as a function of x .

→ Also calculate field at $x = 1 \mu\text{m}$ at room temp.

Soln:- The semiconductor is n-type and current density

$$J_n = J_n(\text{diff.}) + J_n(\text{shift})$$

$$= q D_n \frac{dn}{dx} + n q u_n \mathcal{E}$$

Sample is isolated $\therefore J_n = 0$

$$n = G_1 x$$

$$\frac{dn}{dx} = G_1$$

$$0 = G_1 x \gamma \mu_n \epsilon_0 + \gamma \beta n G_1$$

$$\Rightarrow x \mu_n \epsilon_0 = -\beta n$$

$$\Rightarrow \epsilon_0 = -\frac{\beta n}{\mu_n x} \quad \text{but } \frac{\beta n}{\mu_n} = V_T$$

$$\Rightarrow \boxed{\epsilon_0 = -\frac{V_T}{x}}$$

Equation for built in electric field as a function of x

$$(11) \quad x = 1 \text{ mm}$$

$$\text{At room temp., } V_T = 26 \text{ mV}$$

$$\epsilon_0 = -\frac{V_T}{x}$$

$$= -\frac{26 \times 10^{-3} \text{ V}}{1 \times 10^{-6} \text{ m}} = -26 \text{ KV/m, Ans}$$

WORKBOOK - I

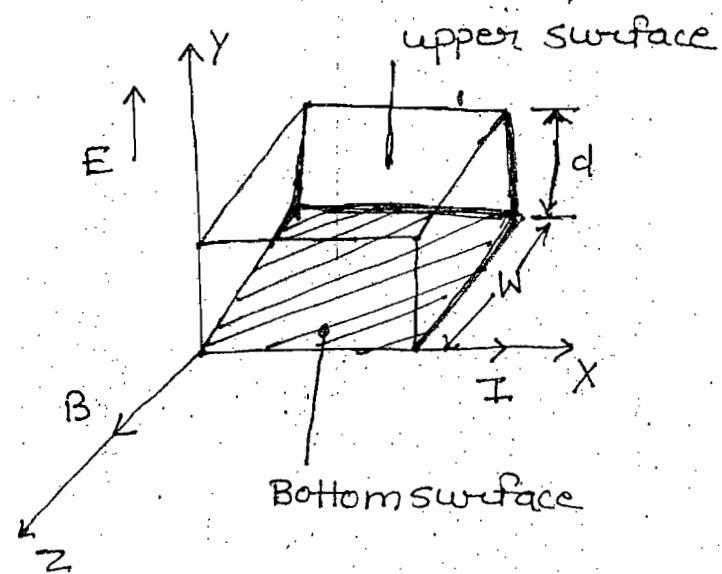
1	B	13	B	24
2	B	14	A, C \rightarrow Best	25
3	B	15	A	26
4	B	16	B	27
5	B	17	B	28
6		18	B	29
7	B	19	C	30
8		20	B	
9	C	21	B	
10		22		
11		23		
12	B			



Lecture - 8

Hall Effect:-

It states that if a specimen (metal or sc.) carrying the current I is placed in transverse field magnetic field B , an electric field intensity E is induced in a direction perpendicular to both ' B ' and ' I '.



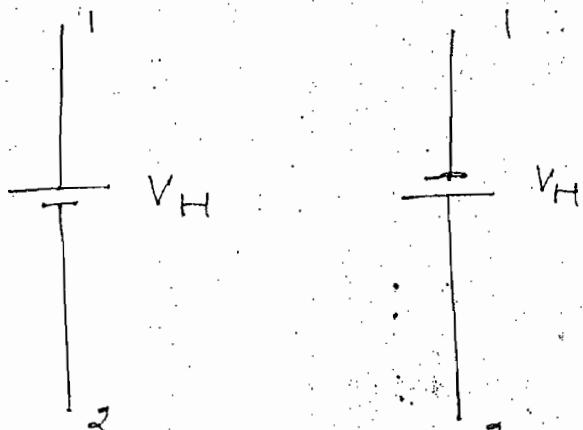
- The specimen must be either equal or square or rectangular in shape
- 'W' is the width of specimen
- 'd' is height or thickness of specimen or spacing b/w the bottom surface and upper surface of the specimen
- The current is taken on X -direction and magnetic field in the Z -direction and field intensity will be in Y -direction

In the above diagram, the direction of the force is downward and direction ^{of force} will be same for e and hole because hole is physically not existing and hole is basically a valence e⁻.

- From the above experiment we can determine
 - (i) Whether the given specimen is metal or semiconductor
 - (ii) To measure the carrier conc.
 - (iii) mobility of charge carriers
 - (iv) Magnetic flux density

(v) In designing hall effect transducer

(vi) To measure the signal power in the electromagnetic wave



Metal or n-type
semiconductor

p-type
semiconductor

→ Hall voltage is induced voltage

→ The polarity and magnitude of the induced Hall voltage will indicate whether the given specimen a metal or semiconductor

→ Electric field intensity

$$|E| = \frac{|V_H|}{d} \text{ V/m}$$

→ Hall voltage V_H :-

$$V_H = E d \text{ Volt}$$

$$V_H = \frac{BI}{\rho W} \text{ Volt}$$

where ρ = charge density

$$\frac{1}{\rho} = R_H \text{ = Hall coefficient}$$

[Material constant related with experiment]

$$V_H = \frac{BIR_H}{W} \text{ Volt}$$

$$V_H \propto R_H$$

→ From Hall experiment

$$U = \frac{8}{3\pi} \sigma R_H$$

where σ = conductivity of specimen

**

$$U \approx \sigma R_H$$

Application :-

- (i) Magnet-o-field meter or magnetic field meter
- (ii) Hall effect multiplier

NOTE :-

- (i) Magnetic field meter is an instrument working on the principle of Hall effect and is used in the measurement of magnetic flux density B .
- (ii) From the hall experiment we can measure magnet flux density and magnetic field intensity ($H \propto B$)
- (iii) Hall effect multiplier is instrument which has two i/p i.e. (i) current (ii) magnetic flux density and induced Hall voltage is the product of I & B .

Hall effect multiplier is an instrument in which one i/p signal is applied in the form of current and another i/p signal is applied in the form of magnetic flux density and Hall voltage is the product of the two i/p signal and hence the name multiplier.

- (iv) In Hall effect multiplier, the two i/p signal are multiplied.
- (v) If the polarity of Hall voltage is +ve for the bottom surface, the given specimen is p-type.
- (vi) Hall voltage is measured w.r.t to upper surface of specimen.

In metal $V_H = -ve$

In n-type semiconductor, $V_H = -ve$

In p-type " " , $V_H = +ve$

For intrinsic semiconductor, $V_H = 0$

Charge density (ρ) = charge \times carrier conc. c/m^3

Hall coefficient (R_H):-

$$R_H = \frac{1}{\rho} = \frac{1}{\text{charge} \times \text{carrier conc.}} \frac{m^3}{c}$$

In metal & n-type semiconductor $R_H = -ve$

In p-type semiconductor, $R_H = +ve$

In intrinsic semiconductor R_H is very large

In intrinsic semiconductor carrier conc. are very large & small and therefore Hall coefficient will be very large.

$$\mu \approx -R_H$$

$$\Rightarrow R_H \approx \frac{\mu}{e}$$

Since $V_H \propto R_H$

$$V_H \propto \frac{1}{\rho}$$

→ In metal ρ is very large, V_H is small (μV)

→ In semiconductor ρ is small, V_H is large (mV or around 1 Volt)

→ Hall voltage weak in metal & strong in semiconductor

NOTE :-

(i) In extrinsic semiconductor, R_H is independent of temperature.

(i) $R_H = \frac{1}{\eta \times \text{carrier conc.}}$

In extrinsic semiconductor carrier conc. mean majority carrier conc and it is independent of temperature. Hence R_H is independent of temperature.

(ii) $R_H = \frac{V_H W}{BI}$

Since all parameters are constant. Hence Hall coefficient is independent of temperature.

(iii) $R_H \propto \frac{1}{\sigma} \quad T \uparrow \sigma \downarrow$

$$\downarrow R_H \uparrow = \frac{\sigma \downarrow}{\sigma \uparrow}$$

In intrinsic semiconductor, Hall coefficient decreases with temperature.

(iv) $\downarrow R_H = \frac{1}{\eta \times \text{carrier conc.} \uparrow}$

In intrinsic semiconductor carrier conc. increase with temperature and hence R_H decrease with temperature.

(v) $\downarrow R_H \downarrow = \frac{\sigma \downarrow}{\sigma \uparrow}$

Hence R_H is decrease with temperature.

NOTE :-

1. The mobility of charge carrier can be experimentally found by using Hall effect.
2. The mobility of charge carrier can be found by using Haynes - Shockley experiment.
3. By using Haynes - Shockley experiment we can measure
 - (a) mobility of minority carriers
 - (b) diffusion constant of the minority carriers

$$\Rightarrow \sigma = \mu V_T$$

Cues:- A doped semiconductor specimen $R_H = 3.6 \times 10^{-4}$ m³/C and resistivity $9 \times 10^{-3} \Omega \text{m}$ achieving single carrier conduction the mobility and density of charge carrier in specimen approximately are given by —

SOL:- (i) $R_H = 3.6 \times 10^{-4}$

$$\rho = 9 \times 10^{-3} \Omega \text{m}$$

$$\mu = ?$$

$$\mu = \sigma R_H$$

$$= \frac{1}{9 \times 10^{-3}} \times 3.6 \times 10^{-4} = 0.04.$$

$$(ii) R_H = \frac{1}{\rho \times \text{carrier conc.}}$$

$$\Rightarrow \rho = \frac{1}{R_H}$$

Carrier conc. = carrier density

$$\Rightarrow \text{carrier density} = \frac{1}{\rho R_H}$$

$$= \frac{1}{1.6 \times 10^{-19} \times 3.6 \times 10^{-4}}$$

$$= 1.73611 \times 10^{22} / \text{m}^3$$

Assuming single carrier conduction

$$\sigma = \text{carrier conc.} \times q \times u$$

$$\Rightarrow \text{carrier density} = \frac{\sigma}{q \times u}$$

$$\Rightarrow \text{carrier conc.} = \frac{1}{\text{Resistivity} \times q \times u}$$

Ques:- Find the magnetic field in a rectangular specimen having 4 mm width and 2mm thick with a Hall coefficient $10^{-3} \text{ m}^3/\text{C}$ and current of 1mA is passed through the sample. Hall voltage 2mV is obtained.

Soln:- $V_H = 2 \text{ mV}$ $w = 4 \text{ mm}$ $I = 1 \text{ mA}$ (Firstly all -
 $R_H = 10^{-3}$, $I = 1 \text{ A}$ they convert in m.)

$$R_H = \frac{V_H w}{B \times I} = 8 \text{ Wb/m}^2, \text{ Ans}$$

Ques:- Find the magnitude of Hall coefficient in n-type germanium bar of width 3mm and height 2mm

Assume $B = 0.9 \text{ Wb/m}^2$ & $I = 1.5 \text{ mA}$

Soln:- $w = 3 \text{ mm} = 3 \times 10^{-3} \text{ m}$

$$b = 2 \text{ mm} = 2 \times 10^{-3} \text{ m}$$

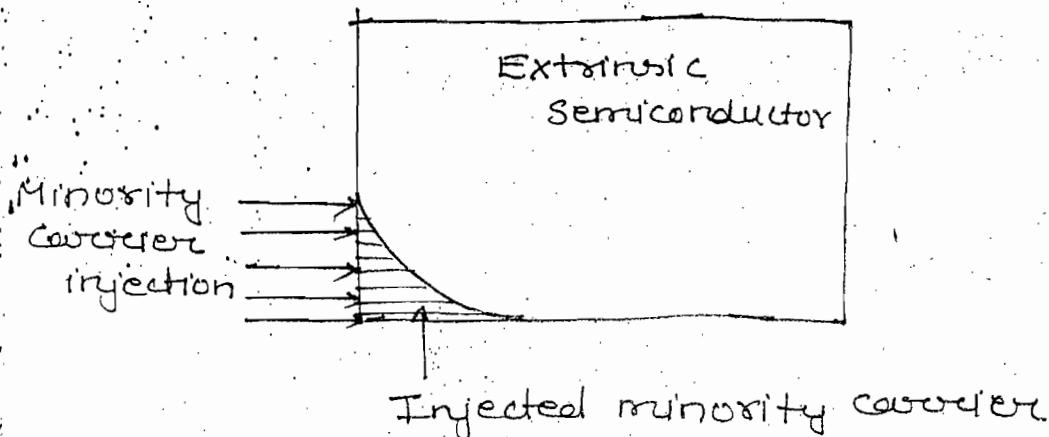
$$V_H = \frac{BI}{\rho w} \Rightarrow V_H = \frac{R_H BI}{w}$$

$$\Rightarrow R_H = \frac{V_H \times w}{BI}$$

$$\Rightarrow R_H = \frac{0.5 \times 3 \times 10^{-3}}{0.9 \times 1.5 \times 10^{-3}}$$

$$= 2.22 \text{ m}^3/\text{C}, \text{ Ans}$$

Minority carrier Injection



- When minority carrier are injected into the semiconductor, the injected minority carrier conc. will be maximum on the surface where they are introduced into the semiconductor and injected minority carrier conc in the semiconductor will be moving from higher conc to lower conc i.e. due to property of diffusion.
- The injected minority carrier conc. will be maximum where they are introduced and conc. will be decreasing into the semiconductor as exponential decaying function with distance.
- When holes are injected into the n-type semiconductor, the injected hole in the semiconductor will be moving from higher conc to lower conc i.e. the property due to diffusion.

Low level Injection

- It means the conc. of majority carriers is far greater than the conc. of minority carriers.
- Light is focussed on the semiconductor only under low level injection.
- When light falls on the semiconductor because of photon energy or larger no. of the surface of the semiconductor gets heated up and due to the thermal energy a large no. of covalent bonds are broken and equal no. of

electrons and holes are created.

Under steady state Analysis :-

Excess e conc. = excess hole conc.

$$\Delta n = \Delta p$$

→ Since majority carrier conc. in semiconductor is almost independent of temperature. When light falls on the semiconductor minority carriers are generated.

→ The generation rate for the generation of minority carriers in the n-type semiconductor is

$$\frac{dp}{dt} = \frac{\text{excess hole generated}}{\text{minority carrier life time}}$$

$$\Rightarrow \boxed{\frac{dp}{dt} = \frac{\Delta p}{\tau_p}}$$

Unit for generation rate $\rightarrow \frac{\text{e-hole pair}/\text{cm}^3}{\text{sec}}$

Cases:- A semiconductor is irradiated with light such that the carriers are uniformly generated through out it volume. The semiconductor is n-type with $N_d = 10^{19}/\text{cm}^3$. Excess e conc. in steady state is $\Delta n = 10^{15}/\text{cm}^3$ & if $\tau_n = 5 \mu\text{sec}$ & $\tau_p = 10 \mu\text{sec}$ the generation rate due to irradiation is

Soln:- $\Delta p = \Delta n = 10^{15}/\text{cm}^3$

$$\frac{dp}{dt} = \frac{\Delta p}{\tau_p}$$

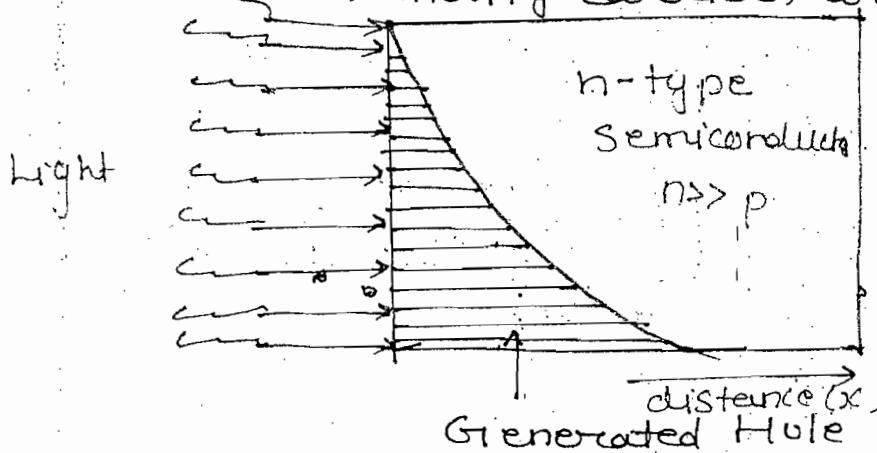
$$= \frac{10^{15}}{10 \times 10^{-16}} = 10^{20} \text{ e hole pair}/\text{cm}^3$$

/sec, Ans.

Ques:- The generation rate due to irradiation in the n-type semiconductor $N_{10} = 10^{17}/\text{cm}^3$ when excess e⁻ conc. in steady state is $10^{15}/\text{cm}^3$ and $\tau_p = 10 \mu\text{sec}$. i.e.

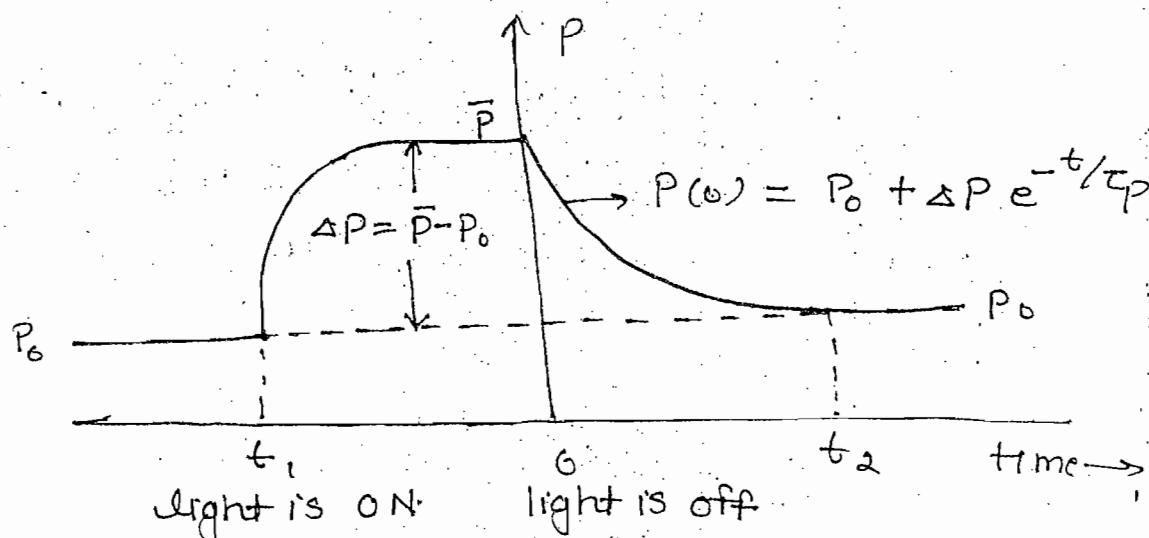
Soln :- $\frac{dP}{dt} = \frac{\Delta P}{\tau_p} = \frac{10^{15}}{10 \times 10^{-6}} = 10^{15+5} = 10^{20}$

→ When light falls on the semiconductor
minority carriers are generated. e^- hole pair $/\text{cm}^3/\text{sec}$



- The generated hole conc. will be maximum on the surface where the light is focussed & the hole conc. exponentially decreases into the depth of the semiconductor
- When the light falls on the n-type semiconductor there will be two current component
 - (i) Hole diffusion current because of light falling on the n-type semiconductor
 - (ii) Hole drift current
 - It is due to pentavalent impurity in the n-type semiconductor which introduces built in electric field.
- Under low level injection in n-type semiconductor, Hole diffusion current (I_p) \gg I_p (drift), i.e. I_p (diff.) \gg I_p (drift)
- When light falls on n-type, the current is mainly due to hole diffusion current.

- Under low level injection in the semiconductor, current is dominated by diffusion current
- When light falls on n-type semiconductor under low level injection.



$$P(t) = P_0 + \Delta P e^{-t/\tau_p}$$

At $t = 0$

$$\Rightarrow P(0) = P_0 + \Delta P e^{-0}$$

$$\Rightarrow P(0) = P_0 + \Delta P \times 1$$

$$\Rightarrow \boxed{P(0) = P_0 + \Delta P}$$

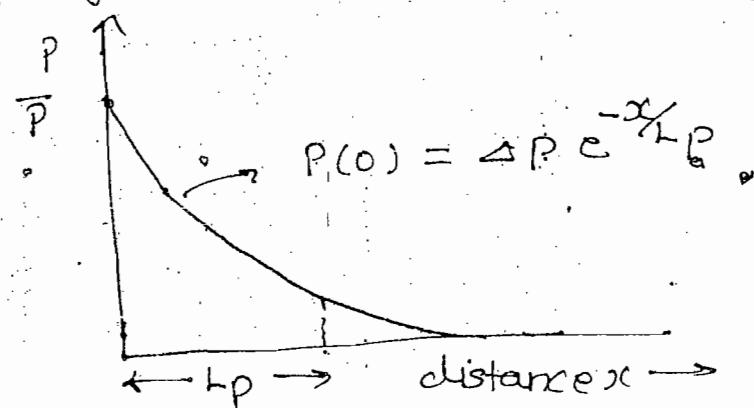
At time $t = t_2$

where $t_2 = 5\tau_p$

$$P(t_2) = P_0 + \Delta P e^{-5\tau_p}$$

$$\Rightarrow \boxed{P(t_2) = P_0}$$

- When light falls on the n-type semiconductor



→ When light falls on the N-type, holes are generated and hole conc. is maximum where the light is focused at $x = 0$.

$$\text{If } x = 0 \text{ then } P(0) = \Delta p e^{-x/L_p}$$

$$\Rightarrow P(0) = \Delta p \rightarrow \text{Excess hole generated}$$

→ Excess hole generated conc. will be decreasing as exponential decrease in function into the semiconductor.

$$\text{At } x = L_p$$

$$P(0) = \Delta p e^{-1}$$

$$\Rightarrow P(0) = \frac{\Delta p}{e}$$

It indicates the length of diffusion is defined as the length into the semiconductor where the excess generated conc. will reduced to $\frac{1}{e}$ of its peak value.

$$\text{If } x = 5L_p,$$

$$\Rightarrow P(0) = \Delta p e^{-5}$$

$$\Rightarrow \Delta p = 0 \quad P(0) = 0$$

Lecture 9e

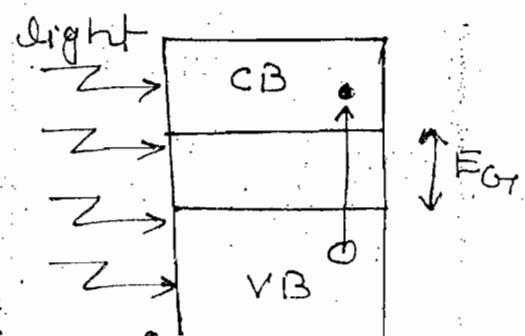
Intrinsic Excitation:-

→ When light falls on the semiconductor, an electron may be exciting from valence band to conduction band and it is called intrinsic excitation

→ For intrinsic excitation

$$\text{Photon energy} \geq E_{G7}$$

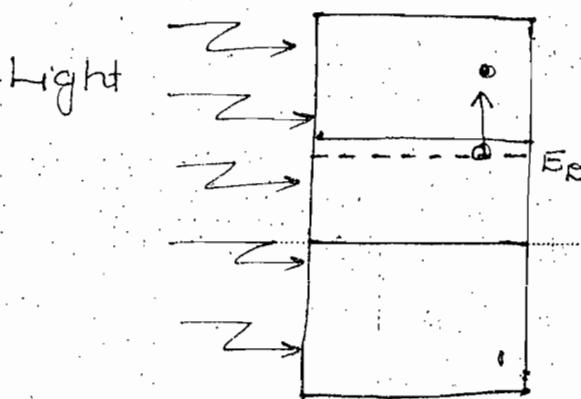
$$\Rightarrow h\nu \geq E_{G7}$$



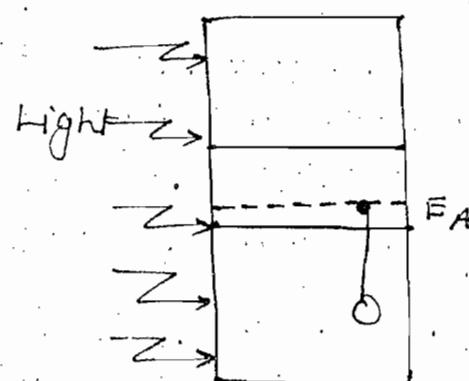
→ For intrinsic excitation, minimum photon energy required must be equal to its energy gap E_{G7}

Extrinsic Excitation:-

N-Type
SC



P-Type
SC



→ When light falls on n-type semiconductor, an electron may be excited from donor energy level into the conduction band and it is called extrinsic excitation

→ When light falls on p-type semiconductor, an electron may be excited from valence band into acceptor energy level (E_A) and it is called extrinsic excitation

→ For extrinsic excitation min. photon energy required is 0.01 eV for Ge, 0.05 eV for Si

Photoconductive Effect :-

- The process where the conductivity of a semi-conductor material or device increases with the light falling on it is called photoconductive effect.
- Photodiode, phototransistor will be working on the principle of photoconductive effect.
- The process where resistivity of a material or device decreases with the light falling on it is called photoresistive effect.
- LDR operates on the principle of photoresistive effect.

Classification of semiconductors :-

- I Direct band gap semiconductor
- II Indirect band gap semiconductor

Direct Band Gap Semiconductor

- During recombination most of energy will be released in the form of light

eg:- GaAs (Best example)

PSU :- GaN, GaAsB, ZnS,
other examples InAs, CdS, InP
InSb, CdSe

↓
Highly unstable
property,
unreliable

- Most of the free e^- will be directly falling from conduction band to valence band & energy is directly released by falling e^- 's in the form of light

Indirect Band Gap Semiconductor

- During recombination most of the energy will be released in the form of heat

eg:- Si & Ge (Best example)

other :- AlP, AlAs, PbS,
example PbSe, GaP

↓
Highly unstable
property

- Most of the free e^- falling from conduction band will go to the intermediate level & then fall into the valence band & energy is dissipated in the form of heat.

Direct Band Gap SC

3. The falling \bar{e} will be directly releasing the energy & hence the name direct bandgap semiconductor

4. During the recombination, most of the falling \bar{e} from conduction band will be directly falling into the valence band and energy is dissipated in the form of light and at the same time very few \bar{e} from the conduction band when falling will be colliding with the crystal and these crystal will absorb the energy from the falling \bar{e} and heated up and they will release some energy in the form of heat.

5. The energy of falling \bar{e} changes, i.e. K.E & P.E changes.

P.E inc & K.E dec.

6. The direction of the falling \bar{e} will not change (direction means from CB to VB)

7. No change in the path of falling \bar{e}

Indirect Band Gap SC

The falling \bar{e} will be indirectly releasing the energy through the crystal in the form of heat & hence the name indirect bandgap semiconductor

During recombination most of free \bar{e} falling from the conduction band will be colliding with the crystal & these crystals will be absorbing the energy from the falling \bar{e} & gets heated up and they released energy in the form of heat but very few falling \bar{e} from conduction band will be escaping the collision & they will fall directly into the valence band and small energy is released in the form of light.

The energy of falling \bar{e} changes i.e. K.E & P.E both changes.

Direction of falling \bar{e} will not change

The path of falling \bar{e} changes (due to intermediate energy level or collision)

Direct Band Gap SC

8. The energy can be released by the falling \bar{e} without a change in momentum or the momentum of the falling \bar{e} does not change

$$\text{Momentum} = \text{mass} \times \text{velocity}$$

Momentum is constant because there is a change in the mass of falling \bar{e} along with the change in the velocity.

9. Relatively smaller carrier lifetime

NOTE :-

InP \rightarrow Direct bandgap semiconductor

GaP \rightarrow Direct bandgap semiconductor

Ques:- Si is never used in the fabrication of LED because it is a indirect band gap semiconductor

Ques:- SC laser are fabricated with direct band gap semiconductor

Indirect Band Gap SC

The momentum of the falling \bar{e} changes or energy cannot be released without a change in the momentum in the falling \bar{e}

The change in momentum is due to a change in the velocity of falling \bar{e} .

Relatively larger carrier lifetime

NOTE :-

InP \rightarrow Indirect band gap semiconductor

Ques:- SC laser are fabricated with
Let IBG SC with large T

(b) " " " smaller T

(c) IIBG " " larger T

(d) " " " smaller T

Ques:- GrAs is an example for

(i) IBG SC

(ii) IIBG SC

(iii) Wide Band gap SC

(iv) Narrow Band Gap SC

out of these correct statement is

(a) Only (i) (b) (i) & (iii) (c) (ii) & (iii) (d) (i) & (ii)

Ques:- A p-type semiconductor follows the equation $P = K \left[1 - \frac{x}{L} \right] / \text{cm}^3$ for $0 \leq x \leq L$

where $K = 10^{15}$, $L = 15 \mu\text{m}$, $\tau_{sp} = 10 \text{ cm}^2/\text{sec}$

J_p (diff.) — ?

Soln:- $P = K \left[1 - \frac{x}{L} \right]$

$$\frac{dP}{dx} = -\frac{K}{L}$$

$$J_p \text{ (diff)} = -\tau_{sp} \frac{dP}{dx}$$

$$= -1.6 \times 10^{-19} \times 10 \left[\frac{-10^{15}}{15 \times 10^{-4}} \right]$$

$$= 1.06 \text{ A/cm}^2$$

Ques:- In the SC sample, if the hole conc.

$$p(x) = 10^{15} e^{-x/L_p} \text{ cm}^{-3} \text{ for } x \geq 0 \text{ and } e \text{ conc.}$$

$$n(x) = 6 \times 10^{14} e^{-x/L_n} \text{ cm}^{-3} \text{ for } x \geq 0$$

$$L_p = 4.8 \times 10^{-4} \text{ cm}, L_n = 9.6 \times 10^{-4} \text{ cm}$$

$\tau_{sp} = 20 \text{ cm}^2/\text{sec}$, $\tau_n = 35 \text{ cm}^2/\text{sec}$. Total current density at $x=0$ is — ?

$$\text{Soln} - J = J_n (\text{diff.}) + J_p (\text{diff.})$$

$$\Rightarrow J = q \theta n \frac{dn}{dx} + q \theta p \frac{dp}{dx}$$

$$= 1.6 \times 10^{-19} \times 35 \left[\frac{6 \times 10^{14} e^{-x/L_n}}{-L_n} \right]$$

$$= 1.6 \times 10^{-19} \times 20 \times \left[\frac{10^{15} e^{-x/L_p}}{-L_p} \right]$$

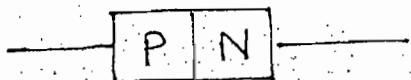
$$\Rightarrow J_{\text{diff.}} \Big|_{x=0} = 1.6 \times 10^{-19} \times 35 \times \frac{(-6 \times 10^{14})}{9.6 \times 10^{-4}}$$

$$= 1.6 \times 10^{-19} \times 20 \times \frac{10^{15}}{(-4.8 \times 10^{-4})}$$

$$= 3.22 \text{ A/cm}^2, \text{ Ans}$$

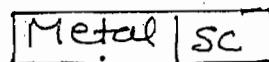
SEMICONDUCTOR DIODE

PN Junction Diode



- Rectification property exist
- can work as a rectifier

Metal SC Junction diode



- No rectification property
- cannot work as a rectifier

eg:- (I) Point contact diode
 (II) Schottky diode

PN Junction diode or Junction Theory :-

- PN Junction can be formed only when a bondir force is created b/w p-type & n-type sc
- Latest diodes are fabricated with any one of the following methods:-

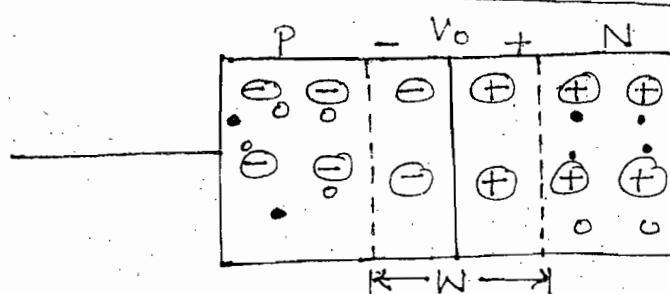
(I) Alloy-junction Technique

(II) Diffusion " " "

(III) Growth " " "

(IV) Epitaxial Method → Latest method

Open circuit PN Junction diode :-



V_0 = contact potential difference

V_0 :- Barrier Voltage
 OR
 Potential Hill
 OR
 Diffusion voltage
 OR
 V_{bi} :- built in voltage

→ For Ge diode, $V_0 = 0.1V$ to $0.5V$

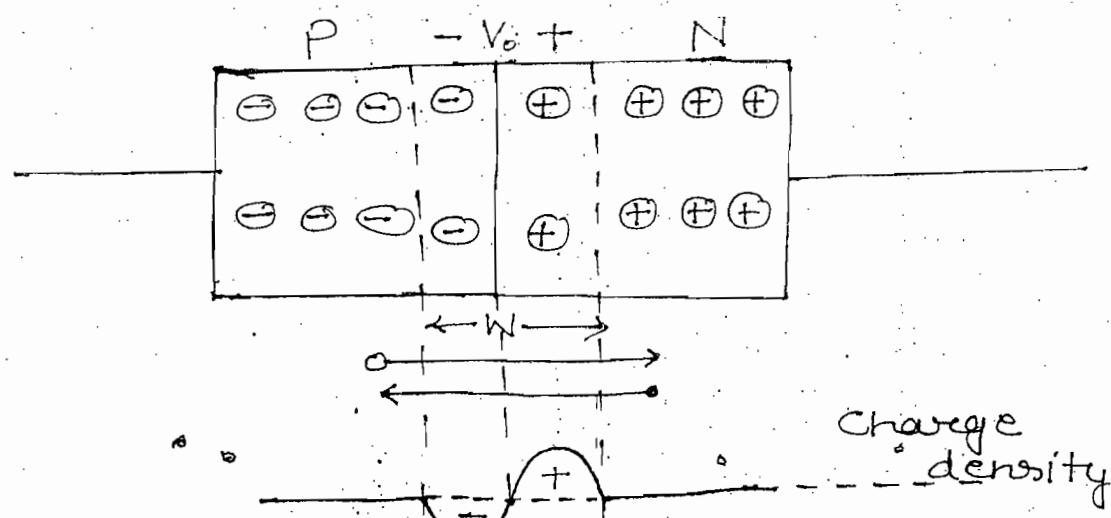
Typical value = $0.2V$

→ For Si diode, $V_0 = 0.6V$ to $0.9V$

Typical value = $0.7V$

Ques:- Why biasing is applied to SC device?

Ans:- As food is available for us, biasing is necessary for semiconductor device. As biasing is applied majority charge carriers cross barrier & contribute to conductivity. Temperature is not sufficient to cross carrier across the barrier.



$$|E_0| \propto \frac{1}{w}$$

Electric field intensity
 $E = -\frac{dV_0}{dw} V/m$

Barrier for the flow of hole

Barrier for the flow of e⁻

- Depletion layer is also called space charge region or transition region
- In the depletion layer, mobile charge carriers are zero
- Depletion layer is created due to diffusion of majority carriers across the junction
- Depletion layer opposes majority carriers in crossing the junction.
- Depletion layer will not oppose in crossing the junction
- Depletion layer will help minority carriers in crossing the junction.
- Depletion layer consists of immobile charges particles (ions).
- Depletion layer consists of large number of ions and covalent bonds
- Depletion layer consists of negative charges and positive charge on either side of junction
- Depletion layer consists of negative ions (acceptor ions) on the p-side and positive ions (donor ions) on the N-side
- The width of the depletion layer $W \propto \frac{1}{\sqrt{\text{Doping}}}$

$$W = 0.1\mu\text{m} \text{ to } 1\mu\text{m} \quad \& \text{ typical value} = 0.5\mu\text{m}$$

V_0 is called contact potential or potential hill or barrier voltage or diffusion voltage or built in voltage [V_{bi}]

For Ge diode

$$V_0 = 0.1\text{V to } 0.5\text{V}$$

$$\text{Typical value} = 0.2\text{V}$$

For Si diode

$$V_0 = 0.6\text{V to } 0.9\text{V}$$

$$\text{Typical value} = 0.7\text{V}$$

- The polarity of diffusion voltage is -ve to the P-side and positive towards N-side.
- Contact potential of the diode cannot be practically measured by using a voltmeter.
- In any type of PN junction, field intensity is always maximum at the junction.
- In a normal diode, field intensity is -ve and it is maximum at the junction and it tapers on either side of junction and will be zero outside the depletion region.
- The majority carriers of P and N region has to climb up the barrier voltage and therefore there will be an opposition for the majority carriers in crossing the junction.
- The minority carriers of P and N region will be falling down the barrier voltage and therefore there is no opposition for the minority carriers in crossing the junction.

Diode symbol :-



The arrow mark denotes the direction of forward current or the direction of conventional current when diode is forward biased.

Equation for width of the depletion layer in open ckt. PN Junction diode :-

$$W = \sqrt{\frac{2\epsilon}{q} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) V_0} \text{ m}$$

ϵ = permittivity in F/m

$\epsilon = \epsilon_0 \epsilon_r$ → Relative permittivity of medium

Absolute permittivity of free space

$$\epsilon_0 = 8.854 \times 10^{-12} \text{ F/m}$$

$$\epsilon_x (\text{Si}) = 11.7$$

$$\epsilon_x (\text{Ge}) = 16$$

In the open circuit PN junction, the width of the depletion region depends on

- (i) doping conc. of P & N - region.
- (ii) contact potential.
- (iii) Permittivity of the medium i.e. on the type of material used for the fabrication.

Let P and N region have equal doping

i.e. $N_A = N_D$

$$W = \sqrt{\frac{2\epsilon}{q}} \left(\frac{2}{N_A \text{ or } N_D} \right) V_0$$

$$W \propto \frac{1}{\sqrt{N_A \text{ or } N_D}}$$

$$W \propto \frac{1}{\sqrt{\text{Doping}}}$$

Equation for contact potential in open circuit PN junction diode :-

$$V_0 = V_{bi}$$

$$V_0 = V_T \log_e \frac{N_A N_D}{n_i^2} \text{ Volts}$$

Contact potential of diode slightly increases with increase in the doping concentration.

Contact potential of diode decreases with temperature

$n_i \rightarrow$ Highly sensitive to Temp.

$V_T \rightarrow$ less

Equation for maximum field intensity in open circuit diode :-

$$E_{\max} = \frac{-V}{\epsilon} W_p N_D$$

OR

$$E_{\max} = \frac{-V}{\epsilon} W_p N_A$$

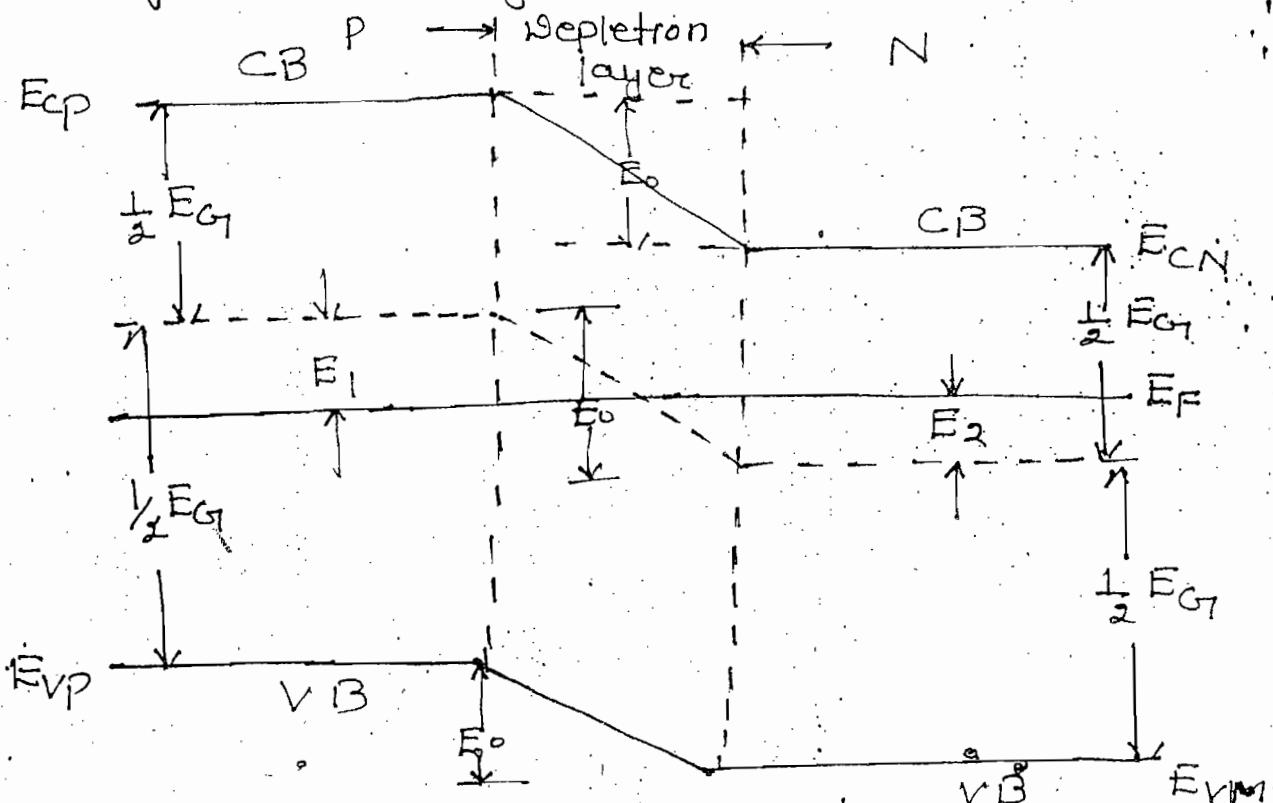
Equation for contact potential in terms of maximum field intensity :-

$$V_0 = -\frac{1}{2} E_{\max} W \text{ Volts}$$

Lecture - 10

Ques:- Draw the energy band diagram of open circuit PN Junction and derive the equation for contact potential for diode.

- In p-type semiconductor, at room temperature fermi level exist just above the acceptor energy level.
- In n-type semiconductor, at room temperature fermi level exist just below the donor energy level.
- When P-N junction is formed, the energy band diagram of P & N type semiconductor will adjust such that the fermi level will now maintained a straight line.
- The energy band diagram of open circuit PN junction is given below :-



E_o is called potential energy of the e⁻ at the junction expressed in eV.

$$E_0 = E_{CP} - E_{CN} = E_{VP} - E_{VN} = E_1 + E_2 \quad \text{--- (I)}$$

$$E_F - E_{VP} = \frac{1}{2} E_G - E_1 \quad \text{--- (II)}$$

$$E_{CN} - E_F = \frac{1}{2} E_G - E_2 \quad \text{--- (III)}$$

Adding (II) & (III)

$$(E_F - E_P) + (E_{CN} - E_F) = E_G - (E_1 + E_2)$$

From eq-(I)

$$(E_F - E_{VP}) + (E_{CN} - E_F) = E_G - E_0$$

$$E_0 = E_G - (E_F - E_{VP}) - (E_{CN} - E_F) \quad \text{--- (IV)}$$

From p-type semiconductor

$$E_F - E_{VP} = KT \log_e \frac{N_V}{N_A} \quad \text{--- (A)}$$

From n-type semiconductor

~~$$E_{CN} - E_F = KT \log_e \frac{N_C}{N_D}$$~~
$$E_{CN} - E_F = KT \log_e \frac{N_C}{N_D} \quad \text{--- (B)}$$

From the derivation of n_i

$$\Rightarrow n_i^2 = N_C N_V e^{-E_G/KT}$$

$$\Rightarrow E_G = KT \log_e \frac{N_C N_V}{n_i^2} \quad \text{--- (C)}$$

Substitute the equation A, B & C in equation-(IV)

$$E_0 = KT \log_e \frac{N_C N_V}{n_i^2} - KT \log_e \frac{N_V}{N_A} - KT \log_e \frac{N_C}{N_D}$$

$$\Rightarrow E_0 = KT \log_e \left[\frac{N_C N_V}{n_i^2} \times \frac{N_A}{N_V} \times \frac{N_D}{N_C} \right]$$

$$\boxed{E_0 = KT \log_e \frac{N_A N_D}{n_i^2}}$$

- It uses the equation to calculate potential energy of the e's at the junction expressed in eV.
- The equation for contact potential can be obtained from equation of E_0 by converting eV into volt.

$$V_0 = V_T \log_e \frac{N_A N_D}{n_i^2} \text{ Volts}$$

$$K_T = 8.62 \times 10^{-5} \frac{\text{eV}}{\text{OK}} \times 300\text{K}$$

$$= 0.02568 \text{ eV}$$

$$\Rightarrow V_T = \frac{I}{11600} = \frac{300}{11600} = 0.02568 \text{ Volts}$$

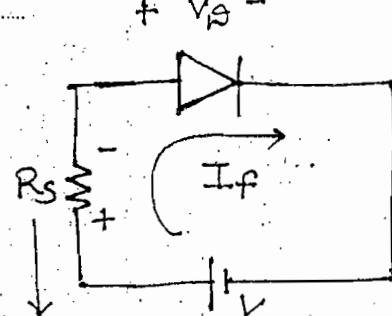
- **
- The contact potential of the p-n junction numerically equal to the difference in the position of fermi level of the p-type and n-type semiconductor.

Forward Bias:-

$$V = V_R + V_S$$

OR

$$V = I_f R_s + I_f R_f$$



current limiting resistance

When p-n junction is forward biased

- The width of depletion layer reduces
- The barrier height reduces

→ In a forward bias diode, current is only due to majority carriers.

→ Forward bias current, $I_f = I_s [e^{\frac{V_f}{nV_T}} - 1]$

$$\Rightarrow I_f \approx I_s \frac{V_f}{nV_T}$$

where V_T = Thermal voltage [26 mV for room temp.]

V_f = forward voltage across the diode
 below 0.5 V for Ge diode
 below 0.9 V for Si

η = utility factor/ Recombination factor

$n = 1 \rightarrow \text{Ge}$] Old representation
 $= 2 \rightarrow \text{Si}$

Modern Representation:-

$n = 1 \rightarrow$ for larger current

$= 2 \rightarrow$ " smaller "

NOTE:-

If Ge or Si are not specified in the problem of diode & BJT then by default take $n=1$.

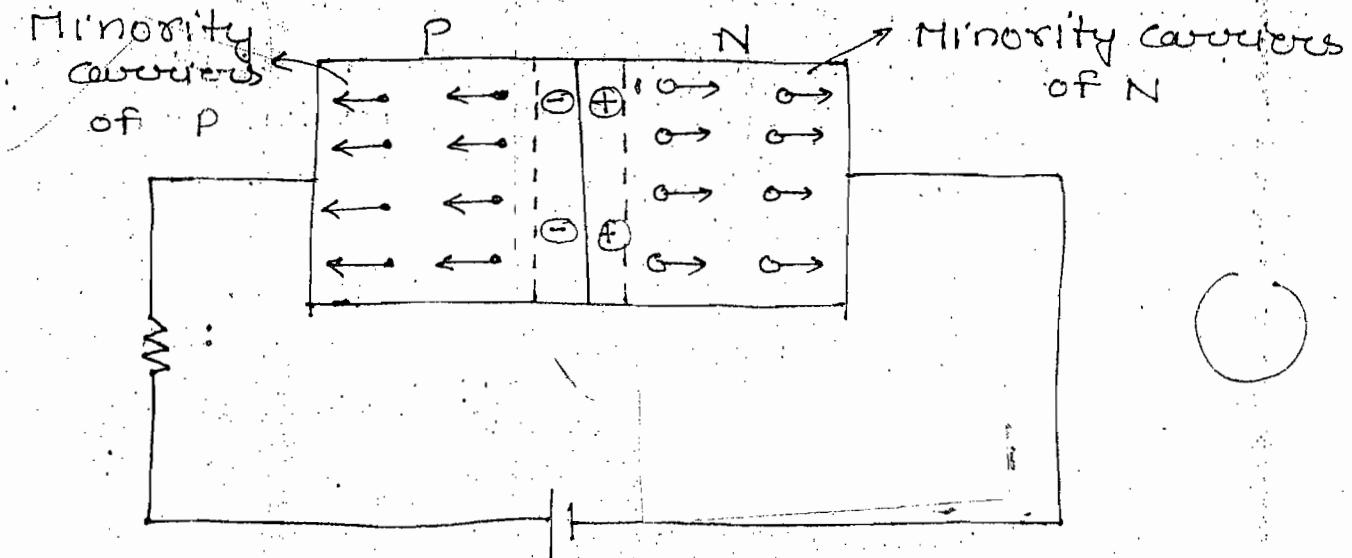
I_s = saturation current and this current is highly sensitive to temperature

→ I_s is in the range 10^{-6} to 10^{-11} A

→ I_s doubled for every 5°C as against the thumb rule which says this current is doubles for every 10°C .

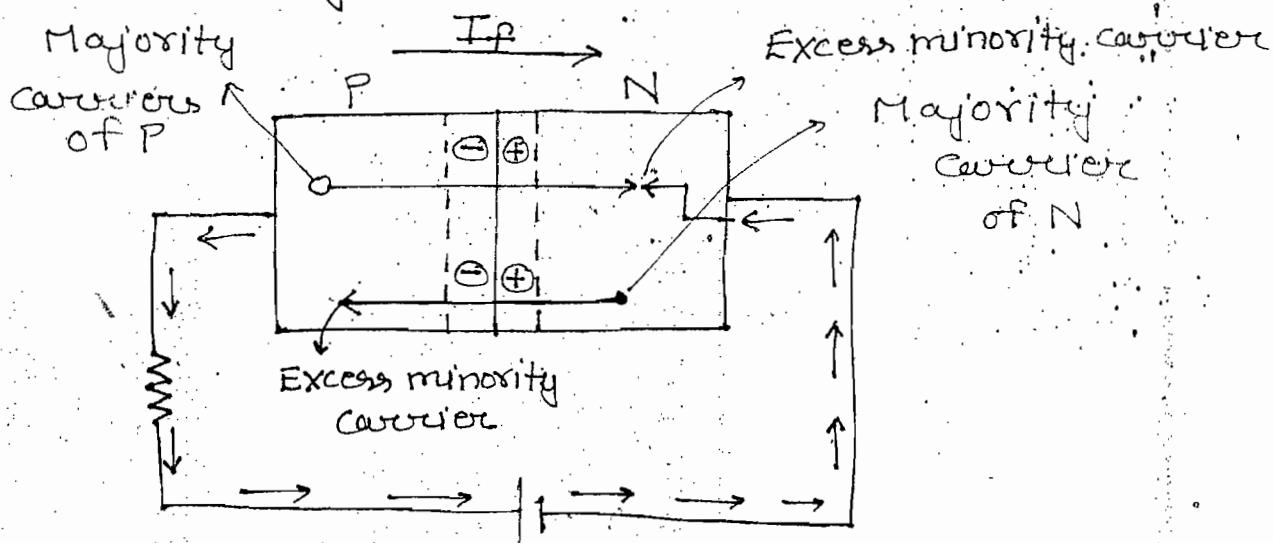
→ Forward current exponentially increases with forward voltage across the diode

→ Forward current flows to p to n and it is in mA.



→ In a forward biased diode, the minority carriers of p and n-region will be moving away from the junction and will accumulate and store in the device and therefore in a forward bias diode the current due to minority carrier is zero.

→ The time taken to store the minority carriers in the forward biased diode is called minority carrier storage time.



→ In a forward biased diode the current at edge of the depletion layer is due to the drift of majority carriers.

- Forward current is a diffusion current.
- Forward current is due to majority

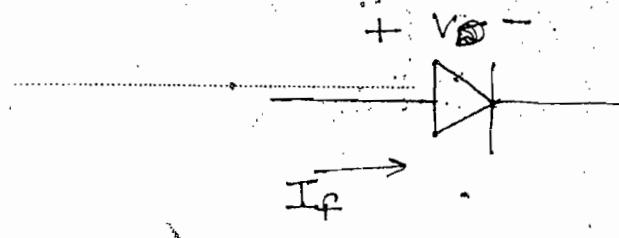
carriers and majority carrier will be crossing the junction from higher conc. to lower conc. i.e. due to property called diffusion and hence forward current is a diffusion current.

- The majority carriers of P and N region on crossing the junction will become minority carriers and they are called as excess minority carriers.
- Forward current is due to flow of excess minority carriers.
- In forward biased diode, the current is controlled by the flow of excess minority carrier crossing the junction.

Cutting Voltage (V_F) / Offset voltage (V) / knee

voltage (V) / Threshold voltage (V) / Breakdown voltage (V) :—

- cutting voltage is defined as the min. forward voltage required so that a current will pass into the diode.



For Ge diode

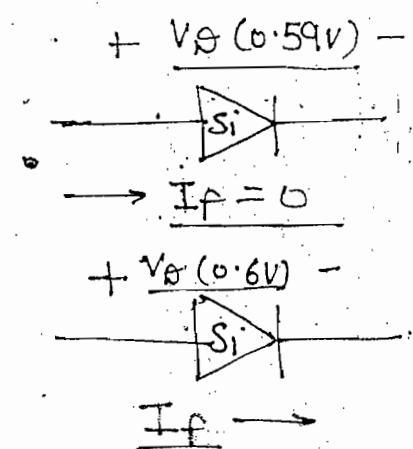
$$0.1 \rightarrow 0.5V$$

Typical value = 0.2V

For Si diode

$$0.6V \text{ to } 0.9V$$

Typ. value = 0.7V



NOTE:-

- cutting voltage is the min. forward voltage required and it is equal to barrier voltage of the diode
- cut-in voltage decreases with the temperature
- For 1°C , $V_T \downarrow$ by 2.3mV for (Latest)
 2.5mV (old)

Effect of temperature on forward current :-

- Forward current is due to majority carriers and majority carrier conc is almost independent to temperature and therefore the forward current is almost independent of temperature

$$I_F = I_S e^{\frac{V_F}{nV_T}} \quad \text{with } T \uparrow$$

- Experimentally found that I_F remains almost independent of temperature.

Forward voltage across the diode :-

$$I_F = I_S e^{\frac{V_F}{nV_T}}$$

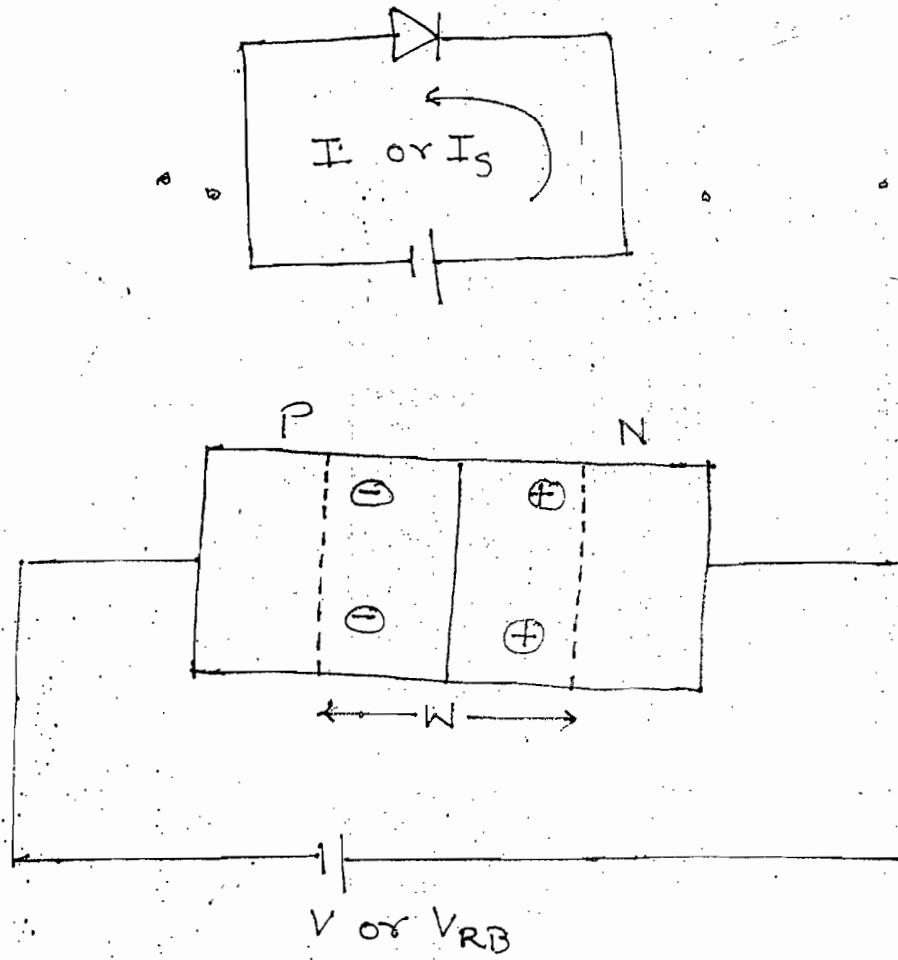
$$\Rightarrow V_F = nV_T \log_e \left(\frac{I_F}{I_S} \right)$$

I_S is more sensitive to temp than compare to V_T

- Forward voltage across the diode decreases with the temperature.

- For 1°C , $V_T \downarrow$ by 2mV → Latest
 2.5mV → Old

Reverse Bias / Blocking Bias / Back Bias :-



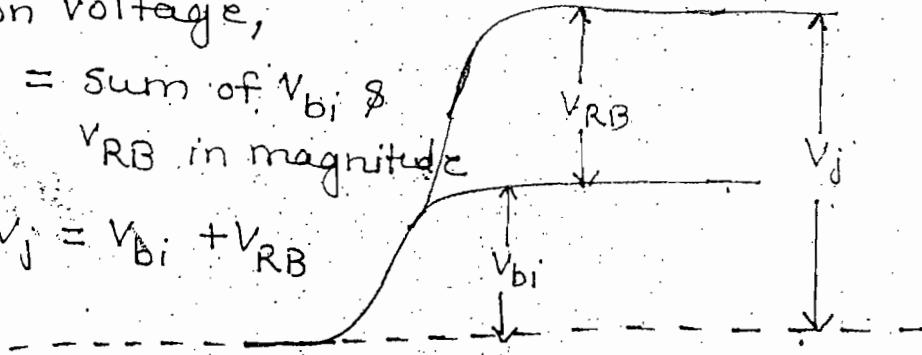
where

Junction voltage,

$$V_J = \text{sum of } V_{bi} \text{ & }$$

V_{RB} in magnitude

$$\Rightarrow V_J = V_{bi} + V_{RB}$$



→ Under Reverse bias

- (a) The width of the depletion layer inc.
- (b) The barrier height inc;

→ Width of depletion layer ,

$$W \propto \sqrt{V_J}$$

$$W \propto \sqrt{V_{bi} + V_{RB}}$$

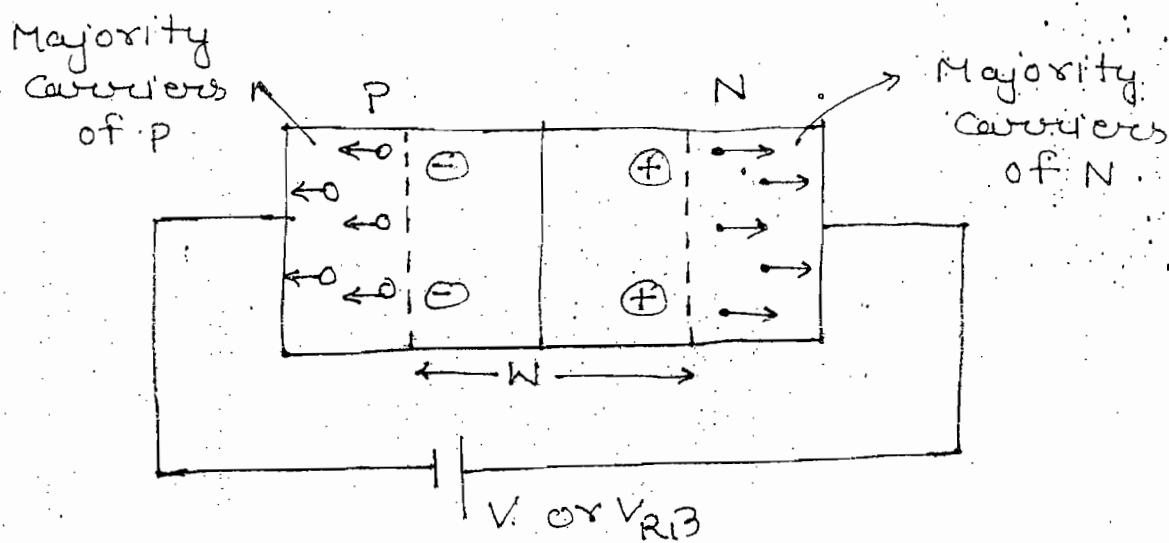
- In a reverse bias diode, current is only due to flow of minority carriers
- The current I_o is known as reverse current and flows from N to P.
- I_o is called leakage current / reverse saturation current / minority carrier current / thermally generated current.

<u>Ge diode</u>	<u>Si diode</u>
I_o	mA
	nA

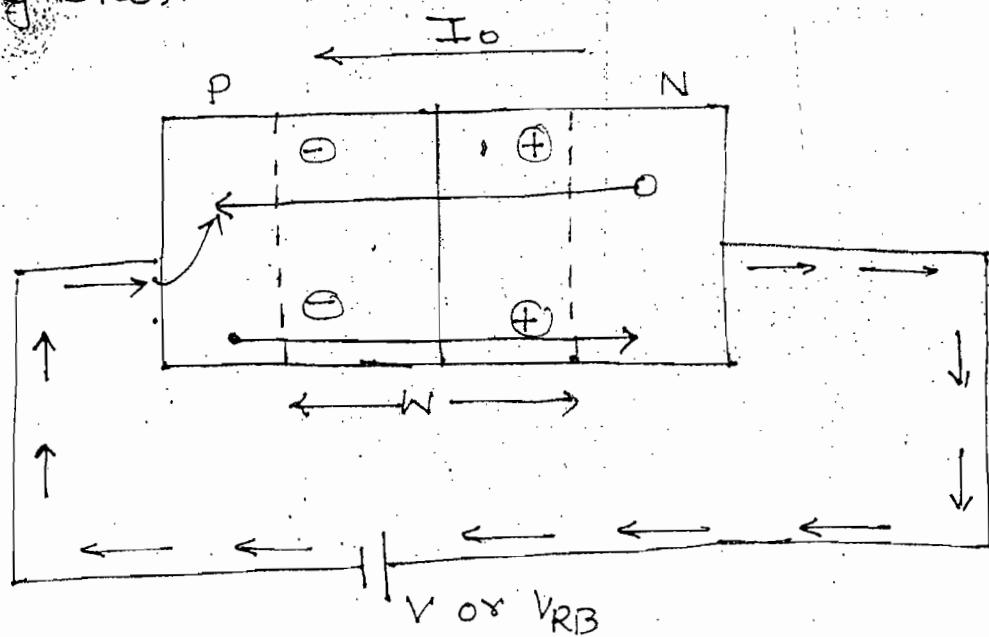
I_o of Ge diode $>$ I_o of Si diode

- I_o is independent of applied reverse voltage i.e. this current is saturated w.r.t applied voltage.
- I_o is highly sensitive to temperature.
- For 1°C , I_o approximately inc. by 7% for both Si & Ge.
- I_o doubles for every 10°C

$$I_o(T_2) = I_o(T_1) \left[2^{\frac{T_2 - T_1}{10}} \right]$$



- In a reverse bias diode, majority carriers of p and n-region will be moving away from the junction and they will accumulate and store in device and therefore in reverse bias diode majority carrier current is zero.
- Since majority carriers are blocked in crossing the junction, reverse bias is also called blocking bias.



- Reverse current is a drift current.
- Reverse current is due to minority carriers and these minority carrier will be crossing the junction from lower conc. to higher conc. and therefore the reverse current is a drift current.

Equation for width of the depletion layer in a Reverse bias diode:-

In a RB P-n junction

$$W = \sqrt{\frac{2\epsilon}{q} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) (V_0 + V_{RB})} \text{ metres}$$

$$W = \sqrt{\frac{2e}{q}} \left(\frac{1}{N_A} + \frac{1}{N_S} \right) V_J \quad \text{metres}$$

Equation for current I in the reverse bias diode :-

$$I = -I_s [e^{\frac{-V}{nV_T}} - 1]$$

$$\Rightarrow I_r = -I_s e^{-\frac{V}{nV_T}} + I_s$$

For Ge diode

$$n=1, V_T = 26 \text{ mV}, I_s = 10^{-6} \text{ A}$$

$$V = 5 \text{ volt}$$

$$I_s e^{-\frac{V}{nV_T}} = 10^{-6} e^{\frac{-5}{1(26 \times 10^{-3})}} \\ = 10^{-6} e^{\frac{-5000}{26}} = 3.6 \times 10^{-90}$$

Hence $-I_s e^{-\frac{V}{nV_T}}$ can be neglected &

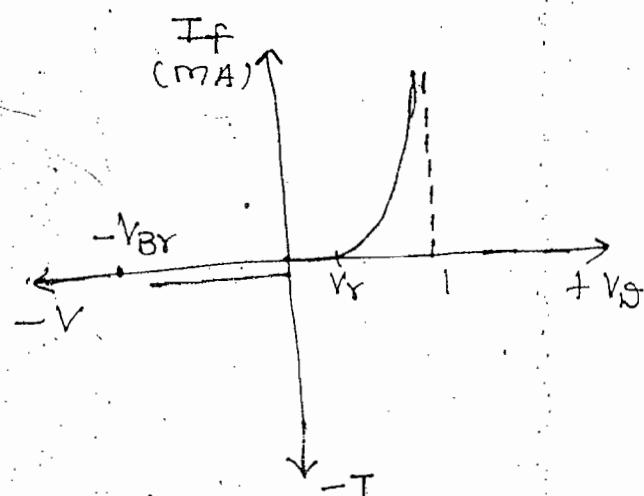
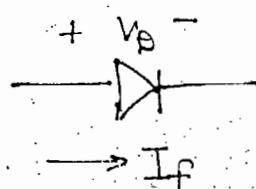
$$I = I_s$$

V-I characteristics of diode :-

OY

Volt - Ampere characteristics of diode :-

$V \rightarrow X\text{-axis}, I \rightarrow Y\text{-Axis}$

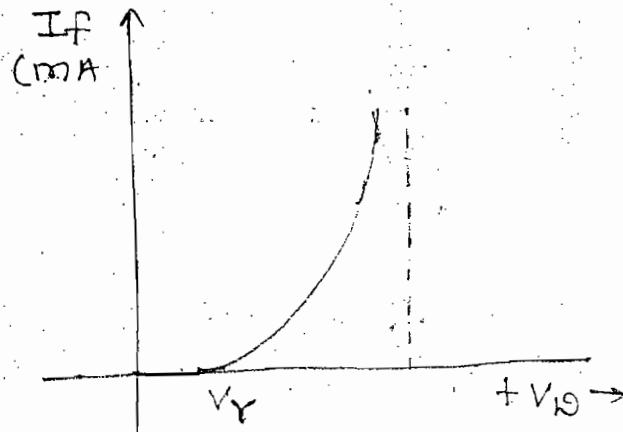


Forward characteristics of diode is plotted with I_f vs V_f .

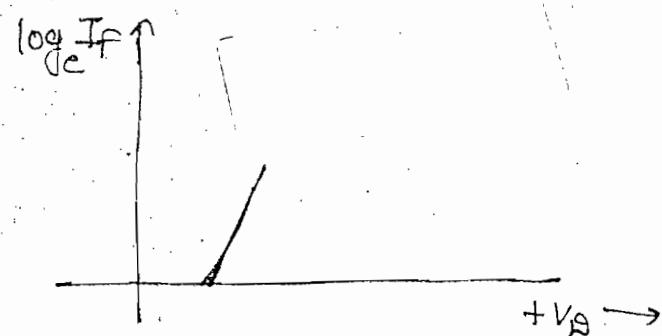
WT \rightarrow Ge diode
NT \rightarrow Si diode.

- When diode is reverse biased, the reverse voltage must be always less than breakdown voltage of diode otherwise diode will be destroyed.

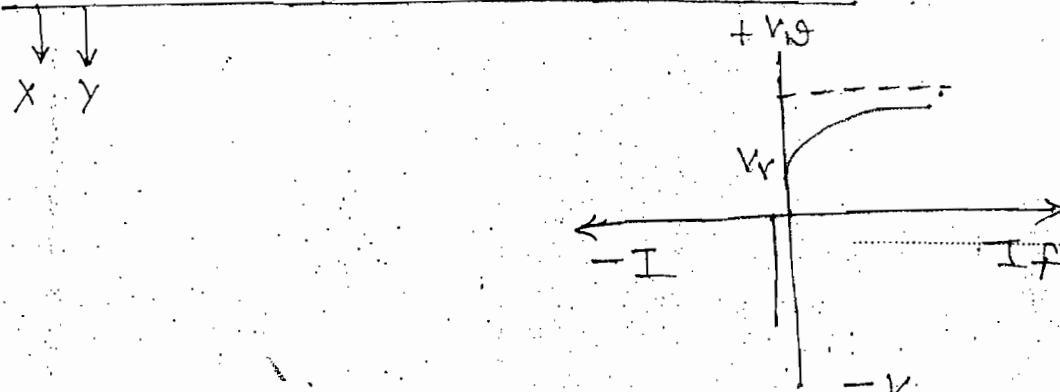
- If exponentially ↑ with V_F



- $\log_e I_F$ Vs V_F Curve represents a straight line.



IV characteristics of diode :-



Breakdown voltage (V_{BR} or B_V): -

- It is manufacturer's specification & it varies from device to device
- In any type of PN junction

$$V_{BR} \propto \frac{1}{\text{Doping}}$$

NOTE :-

→ Diode is a non-linear device, active device & also a unidirectional device.

Diode Resistance :-

Diode Resistance

Forward resistance

10Ω to 100Ω

AC resistance

or

static resistance

Reverse resistance

$R_r \geq 1M\Omega$

$R_r \downarrow$ with $T \uparrow$

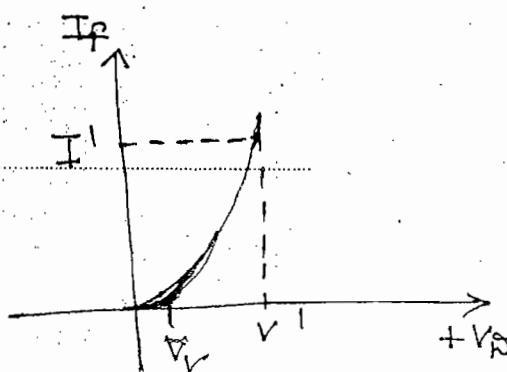
AC resistance

or dynamic resistance

$$r = \frac{\Delta V}{\Delta I} \Omega$$

→ The resistance of diode when signal is not applied is known as DC resistance or static resistance.

$$R_p = \frac{V^1}{I^1} \Omega$$



- The resistance of diode when signal is applied is known as AC or dynamic resistance
- DC resistance is greater than AC resistance
OR
static resistance is greater than dynamic resistance.

Dynamic resistance of diode :-

$$\gamma = \frac{nV_T}{I_f}$$

At room temperature

if $I_f = 26 \text{ mA}$

For Ge diode $\gamma = 1\Omega$

Si $\gamma = 2\Omega$

Hence dynamic resistance is more in Si diode when compare to Ge diode.

$$\boxed{\gamma = \frac{nV_T}{I_f} = \frac{nKT}{VI_f}} \quad \Omega$$

Dynamic conductance (g) :-

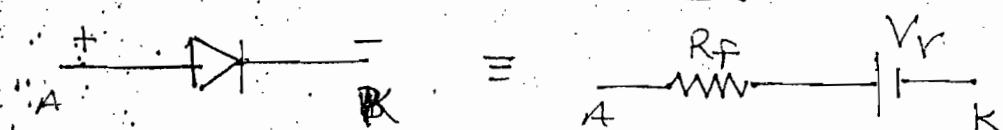
$$\boxed{g = \frac{1}{\gamma}} \quad \text{or } s \text{ or } A/V$$

$$\Rightarrow g = \frac{I_f}{nV_T} \quad \Omega^{-1}$$

$$g \propto I_f$$

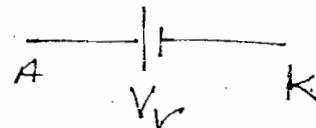
$$\boxed{g = \frac{I_f}{nV_T} = \frac{VI_f}{nKT}} \quad \Omega^{-1}$$

Equivalent circuit of diode :-

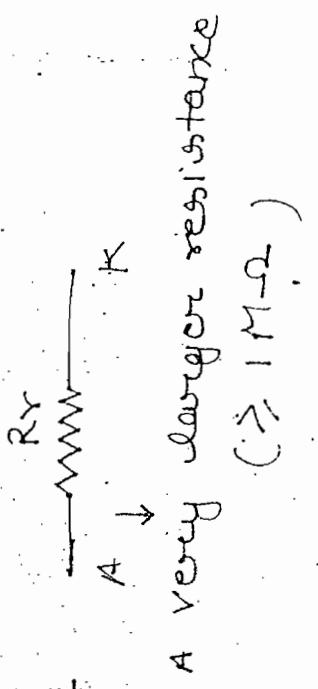
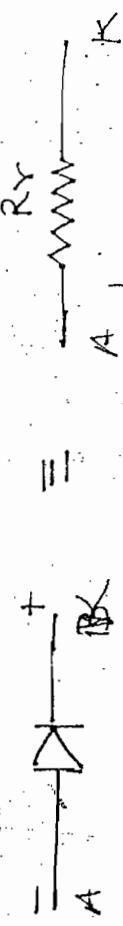


If R_f is not given or neglected then

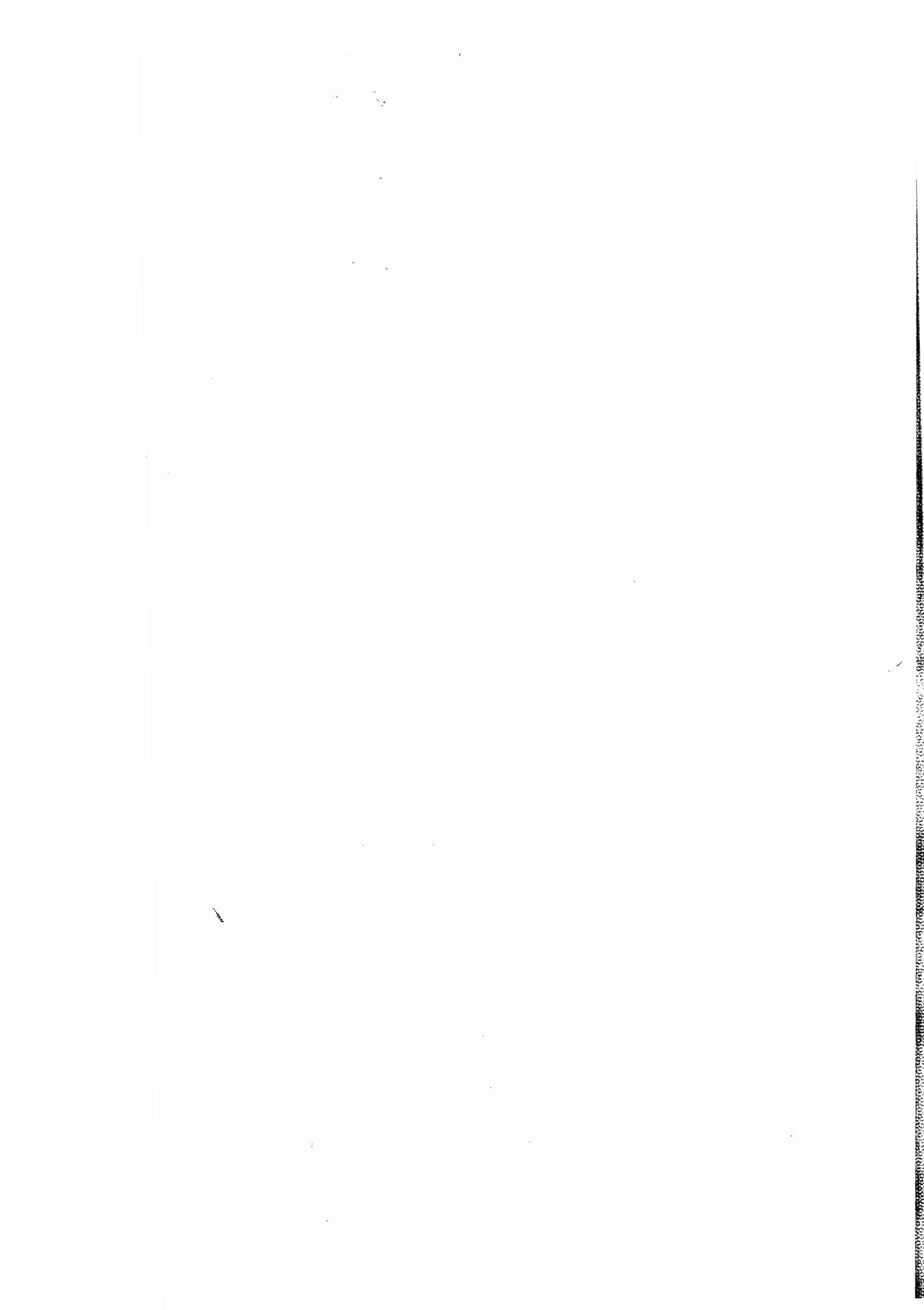
(A) When diode is forward bias



(b) When diode is RB :-



A very large resistance
($\gg 1 M\Omega$)

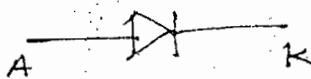


Lecture - 11

Ideal diode :-

→ Perfect diode or imaginary diode i.e. physically not existing.

Symbol :-



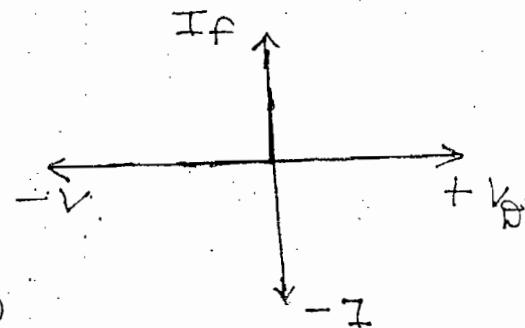
Ideal diode
 $R_f = 0$, $R_g = \infty$, $V_V = 0$

V-I characteristic :-

→ If Ideal diode is FB

then $R_f = 0$ & short circuited

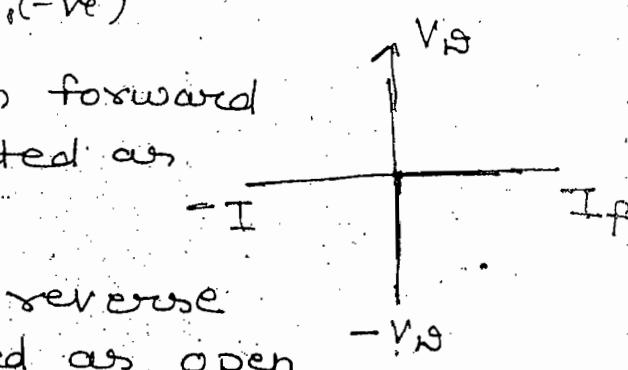
$\Rightarrow I_f$ is maximum



→ If ideal diode is reverse biased then

$R_g = \infty$ & Ideal diode is open circuit

$\Rightarrow I_r = 0$, $V = \text{max}$
 $(-ve)$



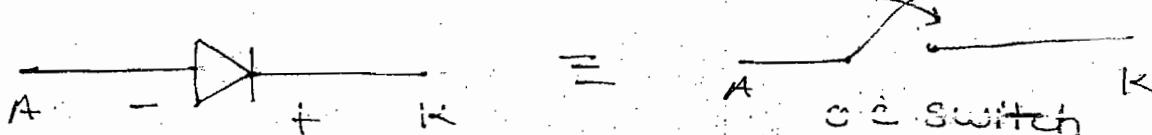
→ Ideal diode when forward biased will be treated as short-circuit

→ Ideal diode when reverse biased will be treated as open circuit.

Equivalent circuit :- (a) When I_D is FB ! -



(b) When I_D is RB ! -

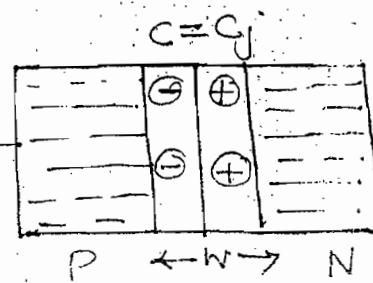


Junction Capacitance (C_J) :-

$$C_J = \frac{\epsilon_0 \epsilon_r A}{W} \text{ Farad}$$

Let $\epsilon_0 \epsilon_r = \epsilon$

$$C_J = \frac{\epsilon A}{W} \text{ Farad}$$



$$C_J \propto A, \quad C_J \propto \frac{1}{W}$$

$$C_J \rightarrow PF$$

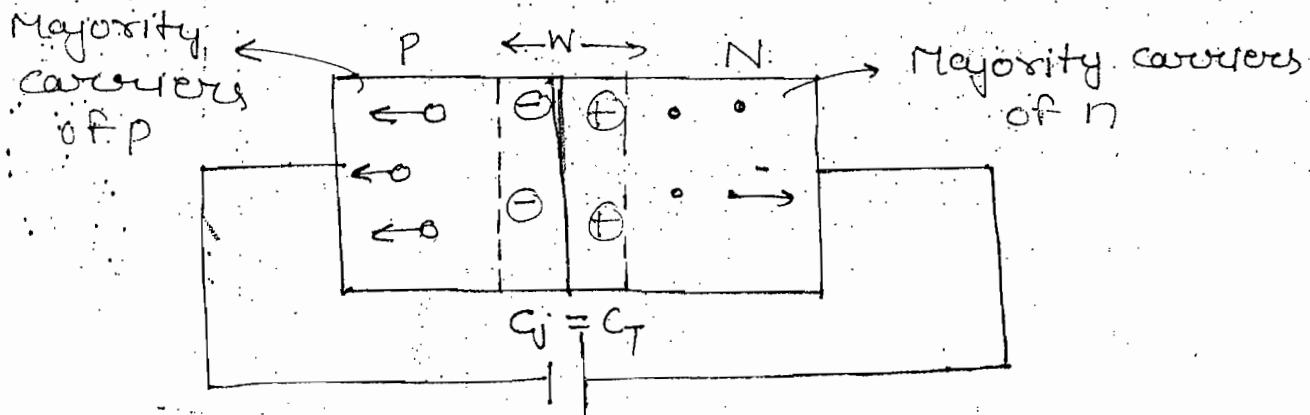
$$C_J \rightarrow C_T \rightarrow RB$$

$$C_J \rightarrow C_D \rightarrow FB$$

→ Depletion layer will be working as a parallel plate capacitor

Transition capacitance (C_T) :-

→ Also known as depletion layer capacitance or space-charge capacitance



- C_T is the junction capacitance in a RB diode.
- C_T is due to the storage of majority carriers in the RB diode

$$C_T = C_J = \frac{\epsilon A}{W} \text{ Farad}$$

$$C_T \propto A$$

$$C_T \propto \frac{1}{W}$$

Since $W \propto \sqrt{\text{Doping}}$

$C_T \propto \sqrt{\text{Doping}}$

$$\Rightarrow C_T \propto \frac{1}{\sqrt{V_J}} \quad (\because W \propto \sqrt{V_J})$$

$$\Rightarrow C_T \propto \frac{1}{\sqrt{V_{bi} + V_{RB}}} \quad (\because V_J = V_{bi} + V_{RB})$$

Since $V_{bi} \ll V_{RB}$

$$C_T \propto \frac{1}{\sqrt{V_{RB} \text{ voltage}}}$$

H- π -Model

→ For better performance of the diode, during high frequency operation, the transition capacitance C_T must be as small as possible.

Typical value $C_T = 3 \mu F \rightarrow \text{BJT}$
 $= 5 \mu F \rightarrow \text{for Diode}$

→ The property of C_T is used in designing of Varactor diode.

→ In a RB diode, the transition capacitance

$$C_T \propto V^{-n}$$

where V is the applied Reverse bias voltage

& n is a constant and is given by

Grading coefficient $\leftarrow n = \frac{1}{2}$ for step graded diode

or

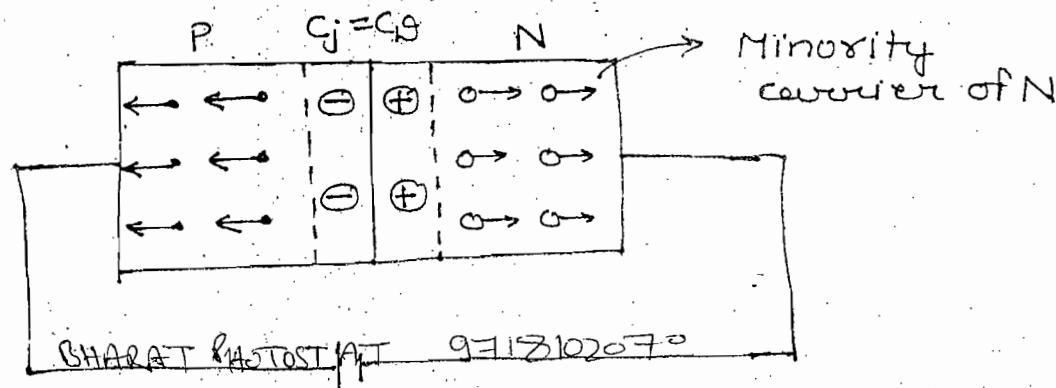
Absrupt junction diode

$= \frac{1}{3}$ for linear graded diode

$= \frac{1}{2.5}$ for diffused P-N junction diode

Diffusion Capacitance (C_D):-

→ also called storage capacitance



→ C_D is the junction capacitance in forward biased diode.

→ C_D is due to the storage of minority carriers in the forward bias diode.

→ Since minority carriers are accumulated and stored in the device, C_D is also called storage capacitance

→ The time taken to store the minority carriers in the device is called minority carrier storage time

→ If minority carrier storage time is small then switching time will be smaller and the device will be faster in operation.

$$C_D = C_j = \frac{\epsilon A}{W} = \text{Farad}$$

$C_D \propto A$

$$\text{and } C_D \propto \frac{1}{W}, \quad C_D \propto \sqrt{\text{Doping}}$$

$$\text{Since } W \propto \frac{1}{\sqrt{\text{Doping}}}$$

NOTE:-

C_D is always greater than C_J
($\because W_S < W_T$)

Typical value $\rightarrow 100 \text{ pF}$

- The high frequency operation of the diode or BJT is limited by C_S
- C_S is a high frequency parameter i.e. it will dominate in the device only during high frequency operation and will reduce the performance of the device.

$$C_S = \tau g \text{ Farad}$$

$g \rightarrow$ dynamic conductance

$$C_S = \frac{\tau}{g} \text{ Farad}$$

$$\text{but } \tau = \frac{nV_T}{I_F}$$

$$C_S = \frac{\tau \times I_F}{nV_T} \text{ Farad}$$

$$C_S \propto I_F$$

- Diffusion capacitance linearly increases with the forward current.

$\tau \rightarrow$ Mean lifetime of excess minority carrier

Ques! - In PN junction diode, the diffusion capacitance is \propto

- Life time of holes in P
- " " " in P
- " " " in N
- " " holes in N

$$I_F \approx I_s e^{\frac{V_S}{nV_T}}$$

$$C_S = \frac{\tau \cdot I_s e^{\frac{V_S}{nV_T}}}{nV_T}$$

→ Diffusion capacitance exponentially increases with forward voltage across the diode.

Carrier lifetime (τ):

→ Average lifetime or mean lifetime of minority carriers or the lifetime of excess minority carriers.

$$\tau_0 = \frac{C_D}{g} = C_D \times \frac{n V_T C_D}{I_f} \text{ sec}$$

→ The mean lifetime of minority carriers in the diode is equal to the time constant of the diode.

Diffusion capacitance:

→ When a sinusoidal signal is applied (C_D')

If a high freq. sine wave is applied

$$C_D' = \left(\frac{\tau}{2\omega} \right)^{1/2} g \text{ Farad}$$

→ Angular freq. of sine wave

→ The diffusion capacitance of the diode dec. as the frequency of the sinusoidal signal is increased.

Derive an equation for Transition capacitance (C_T):

C_T is the junction capacitance in a RB diode.

$$C_T = C_J = \frac{EA}{W} \text{ Farad.}$$

$$\text{where } W = \sqrt{\frac{2e}{V} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) (V_0 + V_{RB})} \text{ m}$$

$$C_T = \frac{EA}{\sqrt{\frac{2e}{V} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) (V_0 + V_{RB})}} \text{ Farad}$$

Dividing numerator & denominator by t

$$C_T = \frac{A}{\sqrt{\frac{2}{\epsilon V} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) (V_0 + V_{RB})}} \text{ Farad}$$

$$C_T = C_j = \frac{A}{\sqrt{\frac{2}{\epsilon V} \left(\frac{N_A + N_D}{N_A N_D} \right) V_0 \left(1 + \frac{V_{RB}}{V_0} \right)}}$$

$$C_T = C_j = \frac{A \sqrt{\frac{\epsilon N_A N_D}{2 V_0 (N_A + N_D)}}}{\sqrt{1 + \frac{V_{RB}}{V_0}}} \text{ Farad}$$

If V_{RB} is kept zero

$$C_j = C_{j0}$$

$$C_{j0} = A \sqrt{\frac{2 \epsilon N_A N_D}{2 V_0 [N_A + N_D]}} \text{ Farad}$$

C_{j0} is the value of C_j when $V_{RB} = 0$

Now

$$C_T = C_j = \frac{C_{j0}}{\left(1 + \frac{V_{RB}}{V_0} \right)^{1/2}} \text{ Farad}$$

The above equation can be generalised

$$C_T = C_j = \frac{C_{j0}}{\left(1 + \frac{V_{RB}}{V_0} \right)^n} \text{ Farad}$$

n = grading coefficient

ques! - A small signal capacitance of abrupt p+N junction is 1nF at 0 bias. If the built in voltage is 1V . The capacitance at RB voltage of 99 V

Soln:- $C_p = 1\text{nF}, V_{RB} = 99\text{V}, V_0 = 1\text{V}$

Step graded $\theta, n = \frac{1}{2}$

$$C_j = \frac{1\text{nF}}{(1 + \frac{99}{1})^{\frac{1}{2}}} , \text{Ans.}$$

ques! - Find the forward current of a Ge diode operating at room temperature with a forward voltage of 150mV and the saturation current is $I_s = 20 \times 10^{-8}\text{A}$.

Soln:- $I_f \approx I_s e^{\frac{V_f}{nV_T}}$

$$\approx 20 \times 10^{-8} e^{\frac{150\text{mV}}{1(26\text{mV})}}$$

$$\approx 20 \times 10^{-6} e^{150/26}$$

$$\approx 0.064\text{mA}, \text{Ans.}$$

ques! - A diode has a leakage current of 10mA at certain temperature. Find this value when the temperature is increased by 25°C .

Soln:- $I_{(T_a)} = 10 (2^{\frac{25}{10}})$

$$= 10 \times 2^{2.5} = 56.56\text{mA}, \text{Ans}$$

ques! - A step graded Ge diode having $N_A = 500\text{ N_A (PN)}$, is designed with acceptor impurities to the extent of 2 impurity atoms for every 10^8 atoms. Find the contact potential at room temperature.

Assume $n_i = 2.5 \times 10^{13}\text{ atoms/cm}^3$

Total no. of atoms in Ge = $4.421 \times 10^{22}/\text{cm}^3$

$$\text{Soln:-- } V_0 = V_T \log_e \frac{N_A N_D}{n_p^2}$$

$$N_A = \frac{2}{10^8} \times 4.421 \times 10^{22}$$

$$= 8.842 \times 10^{14} \text{ atoms/cm}^3$$

$$N_D = 500 \times 2.242 \times 10^{14}$$

$$V_0 = 26 \times 10^{-3} \ln \frac{500 \times (8.842 \times 10^{14})^2}{(2.5 \times 10^{13})^2}$$

$$\Rightarrow V_0 = 0.347 \text{ Volts.}$$

Ques:— A step graded Si diode having $N_D = 500 N_A$ is subjected to acceptor impurities to the extent of 2×10^8 . Find contact potential at room temperature.

$$\text{Assume } n_i \rightarrow 1.5 \times 10^{13} \text{ atoms/cm}^3$$

$$\text{Total atoms} \rightarrow 5 \times 10^{22} / \text{cm}^3$$

(Ans:— 0.739 V)

ques:- A silicon diode indicates forward current of 2mA and 10mA when forward voltages are 0.6V and 0.7V respectively. Estimate the operating temperature of the diode junction.

Soln:- $I_f = 2\text{mA}$

$$I_f \approx I_s e^{\frac{V_D}{nV_T}}$$

$$\Rightarrow I_f \approx I_s e^{\frac{11600 V_D}{nV}}$$

For Si, $n=2$

$$\Rightarrow \frac{2}{10\text{mA}} \approx \frac{e^{\frac{11600(0.6)}{2T}}}{e^{\frac{11600(0.7)}{2T}}}$$

$$\Rightarrow \frac{1}{5} = e^{-\frac{580}{T}}$$

$$\Rightarrow \log_e \frac{1}{5} \approx -\frac{580}{T}$$

$$\Rightarrow T = \frac{-580}{\log_e 1/5}$$

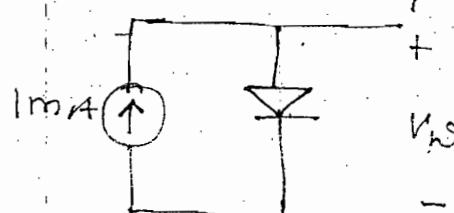
$$\Rightarrow T \approx +360 \text{ Kelvin.}$$

ques:- Two identical diodes when connected in series has a breakdown voltage of 20 Volts. The breakdown voltage of each diode is —

Soln:- In series connection of diodes breakdown voltages are added Ans - 10V .

ques:- In the circuit given below, Si diode is carrying a constant current of 1mA . When the temperature of the diode is 20°C , V_{SD} is found to be 700mV .

If the temperature increases to 40°C , V_{SD} becomes



Soln:- Temp \uparrow from 20°C to 40°C

$$\Delta T = 20^\circ\text{C}$$

For 1°C , $V_D \downarrow$ by 2mV

$$\text{For } 20^\circ\text{C} \downarrow \text{in } V_D = \frac{2\text{mV}}{^\circ\text{C}} \times 20^\circ\text{C}$$
$$= 40\text{mV}$$

$$V_D \text{ at } 40^\circ\text{C} = 700 - 40$$

$$= 660\text{mV}$$

Ques:- A forward biased Si diode, when carrying negligible current have a voltage drop of 0.64V . When current is 1A it dissipates 1W . The ON resistance of the diode is _____

Soln:- ON resistance \rightarrow resistance of diode when large current is passing through it

$$\begin{array}{l} I \rightarrow 0 \\ V_D \neq \dots \end{array} \quad I \rightarrow 1\text{A}$$

$$P = 1\text{W}$$

D is ON

$$P = I^2 R$$

$$\Rightarrow I = 1 \times R \Rightarrow R = 1\Omega, \text{ Ans}$$

Ques:- At 300K , for a diode current of 1mA , a certain Ge diode requires a forward voltage of 0.1435V , whereas a certain Si diode requires a forward voltage 0.718V under the condition given above. Find $\frac{I_0(\text{Ge})}{I_0(\text{Si})}$

Soln:-

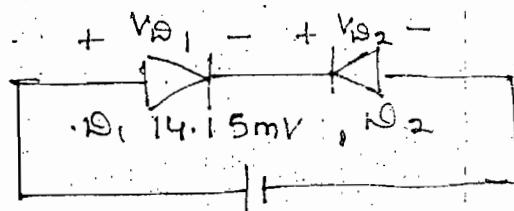
$$(V_D)_{\text{Ge}} = 0.1435, (V_D)_{\text{Si}} = 0.718\text{V}$$

$$I = \frac{I_0 \text{ Ge} e^{V_D / 2V_T}}{I_0 \text{ Si} e^{V_D / V_T}}$$

$$\Rightarrow \frac{I_0 \text{ Ge}}{I_0 \text{ Si}} = \frac{e^{0.718 / 52 \times 10^{-3}}}{e^{0.1435 / 26 \times 10^{-3}}} = \frac{e^{718 / 52}}{e^{143.5 / 26}}$$

$$\frac{I_{D(\text{Ge})}}{I_{D(\text{Si})}} = \frac{\frac{718}{e^{52}} - \frac{143.5}{26}}{e^{52}} = 3977$$

ques:- The circuit diagram below consist of 2 identical diodes each having utility factor of unity. Assume $V_T = 25 \text{ mV}$



Find V_{D_1} & V_{D_2}

Soln:- The two identical Ge diodes are connected back to back and the same current will be passing in both the diodes D_1 is forward biased D_2 is reversed biased.

For D_1 :-

$$I = I_f \\ = I_s [e^{\frac{V_{D_1}}{nV_T}} - 1] \quad \text{(i)}$$

For D_2 :-

$$I = I_s \\ = -I_s [e^{-\frac{V_{D_2}}{nV_T}} - 1] \quad \text{(ii)}$$

Equating (i) & (ii)

$$I_s [e^{\frac{V_{D_1}}{nV_T}} - 1] = -I_s [e^{-\frac{V_{D_2}}{nV_T}} - 1]$$

$$\Rightarrow e^{\frac{V_{D_1}}{nV_T}} - 1 = -e^{-\frac{V_{D_2}}{nV_T}} + 1$$

$$\Rightarrow e^{\frac{V_{D_1}}{nV_T}} + e^{-\frac{V_{D_2}}{nV_T}} = 2$$

$$\text{But. } V_{D_1} + V_{D_2} = 50 \text{ mV}$$

$$\therefore V_{D_2} = 50 \text{ mV} - V_{D_1}$$

$$\begin{aligned}
 e^{\frac{V_{D1}}{nV_T}} + e^{-\left(\frac{50mV - V_{D1}}{nV_T}\right)} &= 2 \\
 \Rightarrow e^{\frac{V_{D1}}{nV_T}} + e^{-2} \cdot e^{\frac{V_{D1}}{nV_T}} &= 2 \\
 \Rightarrow e^{\frac{V_{D1}}{nV_T}} [1 + e^{-2}] &= 2 \\
 \Rightarrow e^{\frac{V_{D1}}{nV_T}} &= \frac{2}{1+e^{-2}} \\
 \Rightarrow V_{D1} &= nV_T \log_e \frac{2}{1+e^{-2}} \\
 \Rightarrow V_{D1} &= 1 [25 \times 10^{-3}] \log_e \frac{2}{1+e^{-2}} \\
 &= 14.15 \text{ mV}
 \end{aligned}$$

$$\begin{aligned}
 \therefore V_{D2} &= 50 - V_{D1} \\
 &= 35.85 \text{ mV}
 \end{aligned}$$

In the above circuit, none of the diode will be conducting but one diode is forward bias below the cut in voltage and therefore will be non-conducting and second diode will be reverse biased & non-conducting.

These circuits are used in designing of power supplies as

- (i) Overload protection circuit.
- (ii) Short circuit protection circuit.

Lecture-12

Ques: - For a p-n junction with $N_A = 10^{17}/\text{cm}^3$ and $N_D = 10^{16}/\text{cm}^3$ and operating at 300 K.

Find

$$(i) C_{j0}$$

$$(ii) C_j$$

If $V_{RB} = 2V$, junction Area = $2500 \mu\text{m}^2$

$$n_i = 1.5 \times 10^{10}/\text{cm}^3, m = 1/2, V_0 = 0.728 \text{ volt}$$

$$E_V(\text{Si}) = 11.7$$

Sol:

$$C_{j0} = A \sqrt{\frac{q\epsilon}{2V_0} \left(\frac{N_A N_D}{N_A + N_D} \right)}$$

$$= A \sqrt{\frac{1.6 \times 10^{-19} \times 8.85 \times 10^{-12} \times 11.7}{2 \times 0.728} \left(\frac{10^{33}}{10 \times 10^{16} + 10^{16}} \right)}$$

$$\Rightarrow C_{j0} = 8.04 \times 10^{-10} \text{ F}$$

$$C_j = \frac{C_{j0}}{\left(1 + \frac{2}{0.728} \right)^{1/2}}$$

$$= 4.153 \times 10^{-13} \text{ F, Ans}$$

Simple diode circuit

(I) Using ideal diode

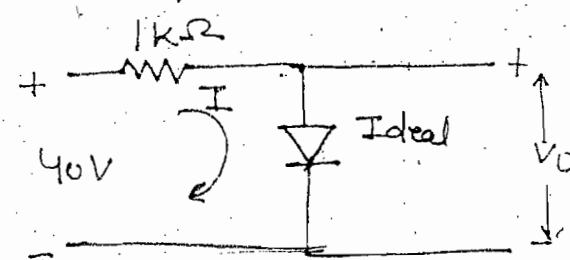
Find I & V_o

Ideal diode is F.B

& short circuit

$$V_o = 0$$

$$I = \frac{V}{1\text{ k}\Omega} = \frac{40}{1\text{ k}\Omega} = 40\text{ mA}$$

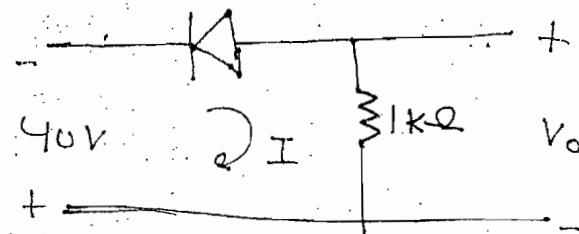


(II) Find I & V_o

$$V_o = -40V$$

$$I = \frac{V_o}{1\text{ k}\Omega}$$

$$= \frac{-40}{1 \times 10^3} = -40\text{ mA}$$



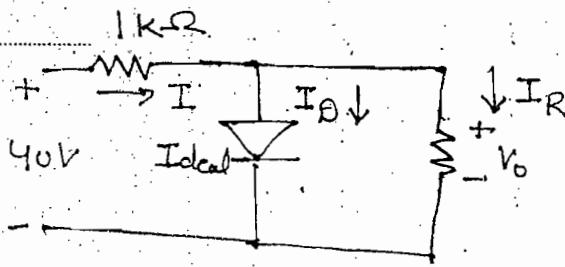
(III) Find V_o , I , I_D & I_R

I_D is F.B & S.C

$$I_R = 0$$

$$V_o = 0$$

$$I_D = I = \frac{40V}{1k} = 40\text{ mA}$$



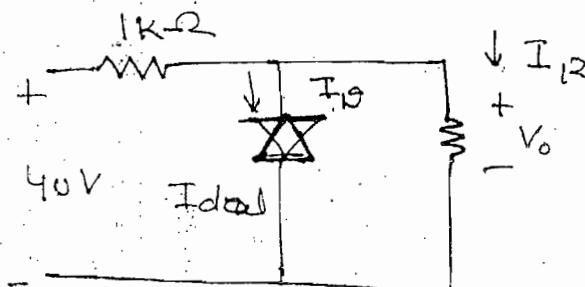
(IV) Find V_o , I , I_D & I_R

I_D is R.B & O.C

$$I_D = 0$$

$$I_R = I = \frac{40}{1k + 1k} = 20\text{ mA}$$

$$V_o = I(1k) = 20V$$

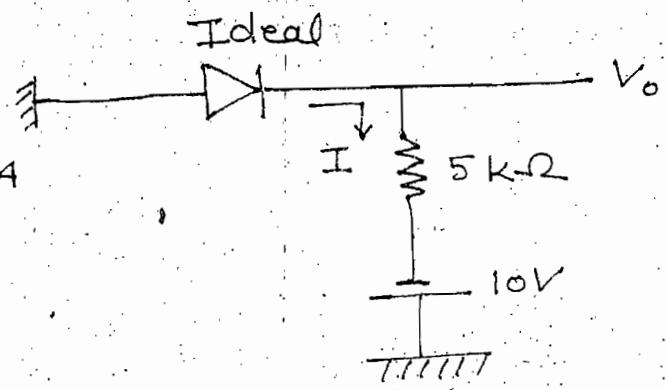


(V) Find I & V_o

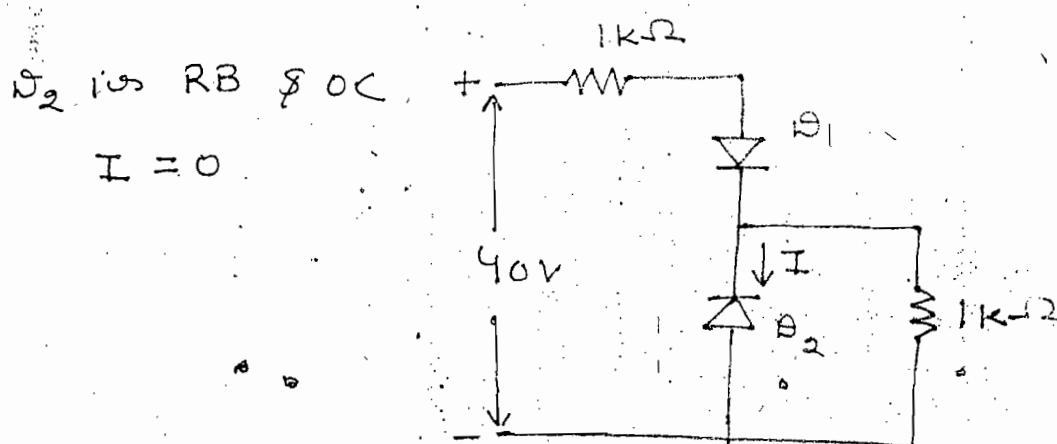
D_1 is FB & SC

$$I = \frac{10V}{5\text{k}\Omega} = 2\text{mA}$$

$$\begin{aligned} V_o &= I(5\text{k}) - 10 \\ &= 10 - 10 \\ &= 0V \end{aligned}$$



(VI) Find I , if D_1 & D_2 are ideal diodes



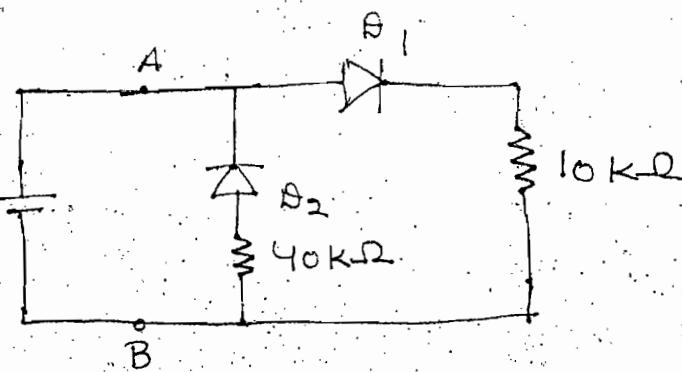
(VII) Find Z_{AB}

A is the w.r.t B

D_1 is FB & SC

D_2 is RB & OC

$$Z_{AB} = 10\text{k}\Omega$$

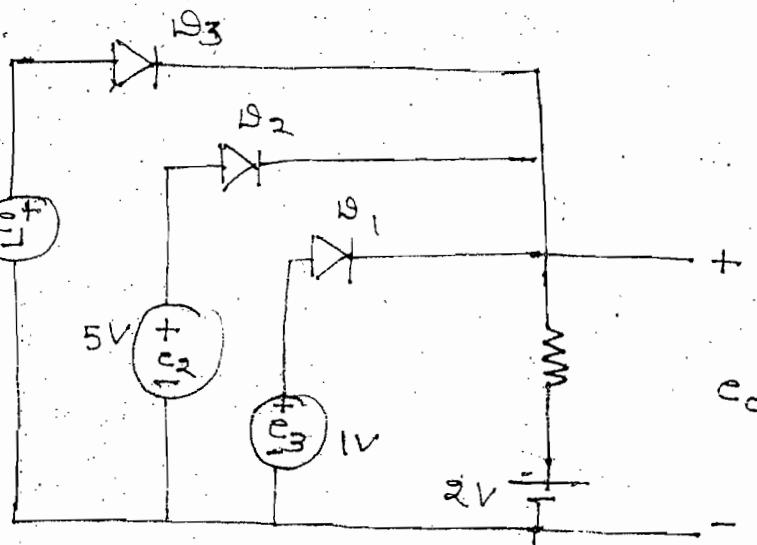


(VIII) Find which diode is conducting in the given ckt? find e_o .

Let the resistance is very small in the given circuit

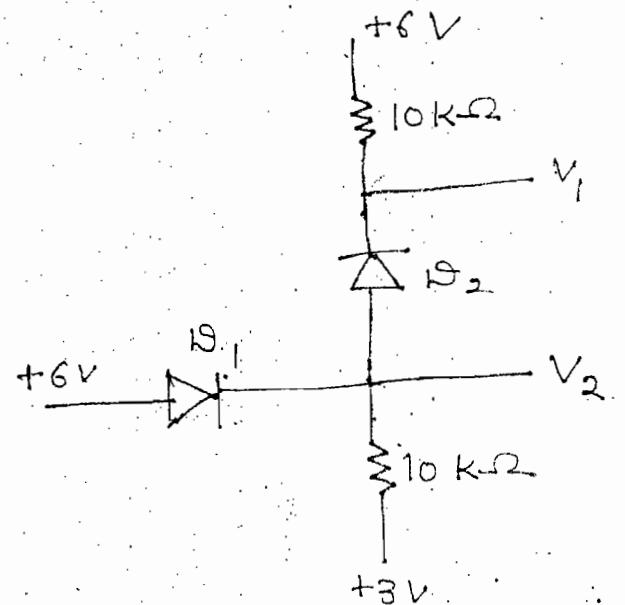
D_2 is conducting 1.5V

$$e_o = 5V$$

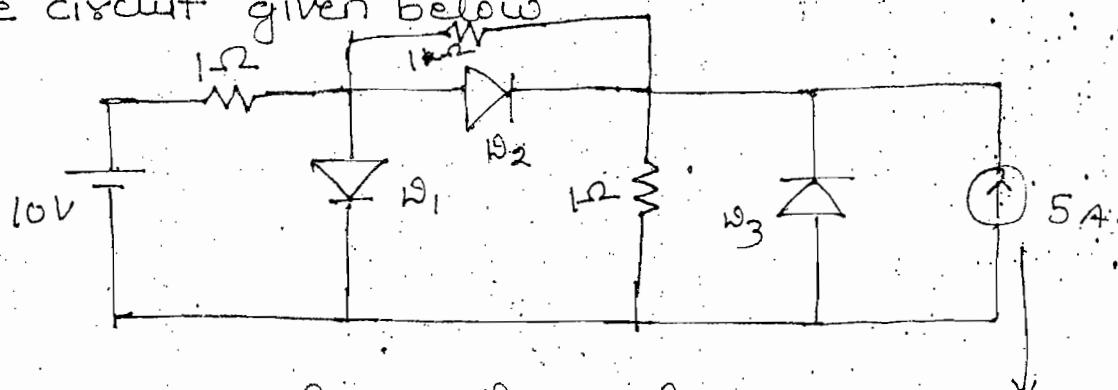


ques! - The voltages at V_1 & V_2 are for the circuit arrangement given will be ____?

- (a) 3V & 6V
- (b) 6V & 3V
- (c) 5.4V & 6V
- (d) 6V & 6V



ques! - What are the states of three ideal diode in the circuit given below



- | | | | |
|-----|-----|-----|-----|
| (a) | OFF | ON | ON |
| (b) | ON | OFF | ON |
| (c) | ON | OFF | OFF |
| (d) | OFF | ON | OFF |

Ideal current source & whole current is passed through them hence D_3 is OFF.

→ D_1 is S.C. Hence all the current passed through them & current through D_2 is 0. Hence D_2 is OFF.

Practical diode circuit:-

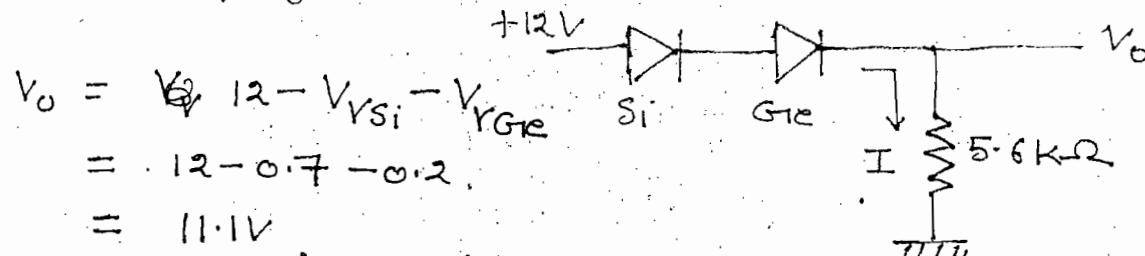
(I) Find $I \& V_o$

Ge diode is FB &
replaced by V_V

$$V_o = V_V Gie \\ = 0.2 V$$

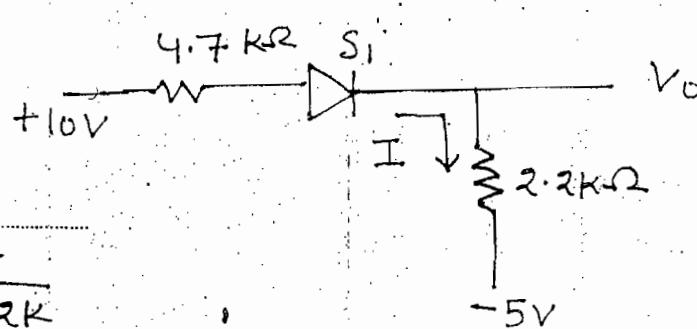
$$I = \frac{20 - V_V Gie}{1k} = 19.8 \text{ mA}$$

(II) Find $I \& V_o$

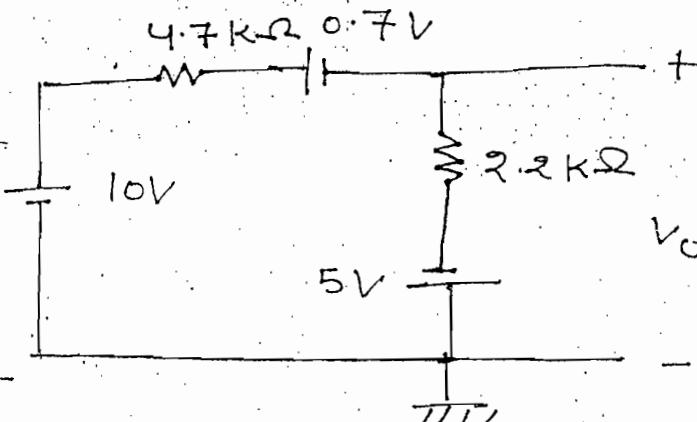


$$I = \frac{V_o}{5.6 k} = \frac{11.1}{5.6 k} = 1.98 \text{ mA}$$

(III) Find $I \& V_o$



$$V_o = I(2.2k) - 5 \\ = 2.07 \text{ mA} \times 2.2k - 5 \\ = -0.45 \text{ Volt}$$



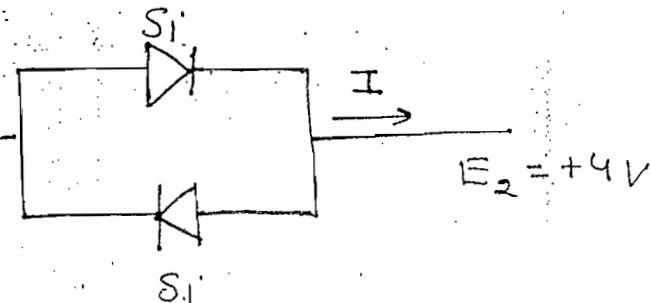
(IV) Find I

since $E_1 > E_2$
 → UF is FB &
 conducting

→ BD is RB & O.C

$$I = \frac{E_1 - E_2 - V_{rSi}}{R}$$

$$= \frac{20 - 4 - 0.7}{2.2 \text{ k}} = 6.95 \text{ mA}$$

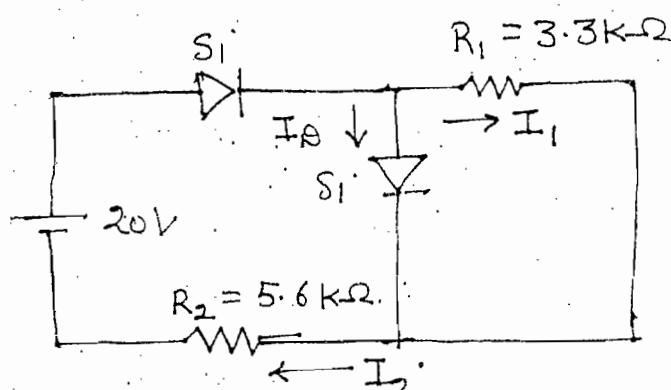


(V) Find I_D

$$V_{R1} = V_{rSi} \Rightarrow 0.7V$$

$$I_1 = \frac{V_{R1}}{R_1} = \frac{0.7}{3.3 \text{ k}}$$

$$= 0.212 \text{ mA}$$

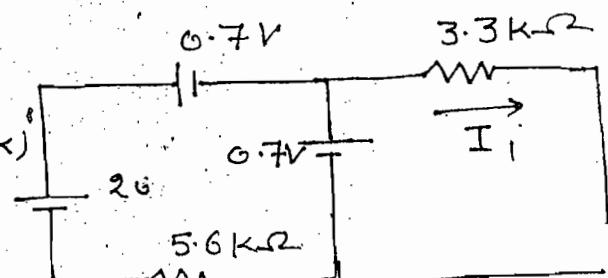


KVL to 1st mesh

$$20 = V_r + V_r + I_2 R_2$$

$$20 = 0.7 + 0.7 + I_2 (5.6 \text{ k})$$

$$\Rightarrow I_2 = 3.32 \text{ mA}$$



$$I_2 = I_1 + I_D$$

$$\Rightarrow I_D = I_2 - I_1$$

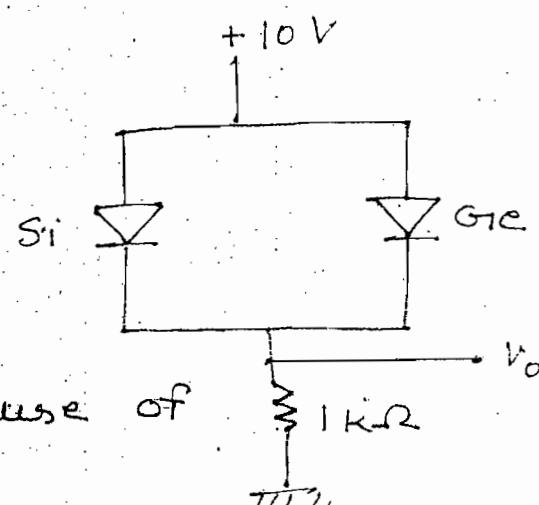
$$= 3.109 \text{ mA}$$

(VI) Find V_o

$$V_o = 10 - V_{rGIE}$$

$$= 10 - 0.2$$

$$= 9.8V$$



GIE is conducting because of smaller cutting voltage.

→ Both Ge & Si diode are simultaneously FB. Due to smaller cutting voltage, Ge diode will enter into conduction & o/p voltage is 9.8V

→ The Si diode is FB below the cutting voltage. Hence it will remain non-conducting.

ques:- Explain the circuit

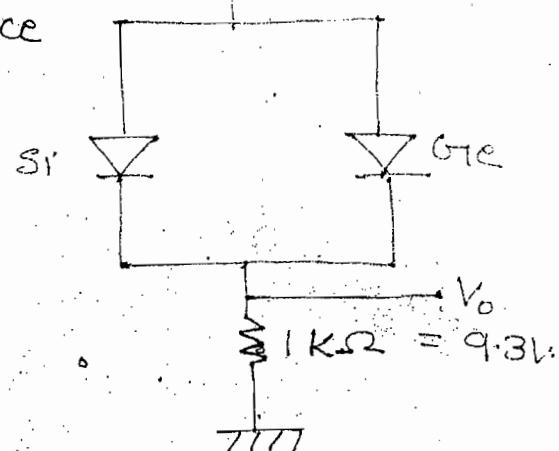
Ans:- o/p voltage is 9.3. Hence

Si diode is conducting &

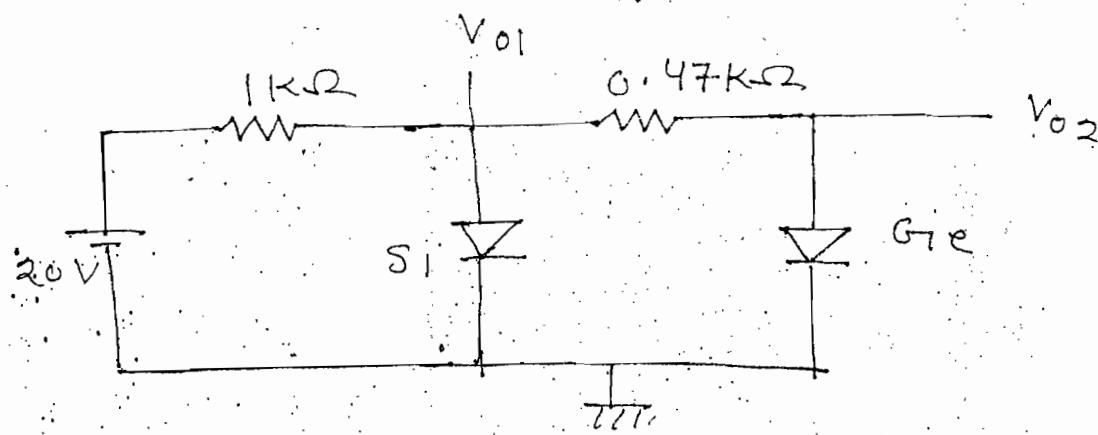
Ge diode has been

destroyed.

16V



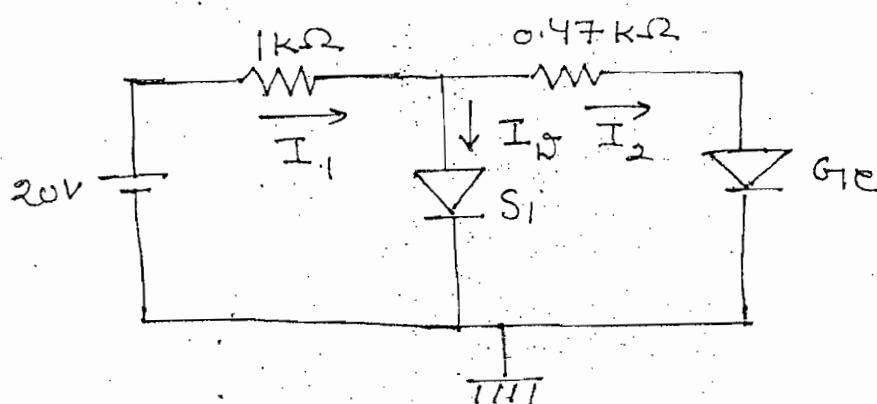
ques:- Find V_{o1} & V_{o2}



$$\text{Ans:- } V_{o1} = 0.7V$$

$$\therefore V_{o2} = 0.2V$$

ques:- Find I_1 , I_2 & I_S



Soln:-

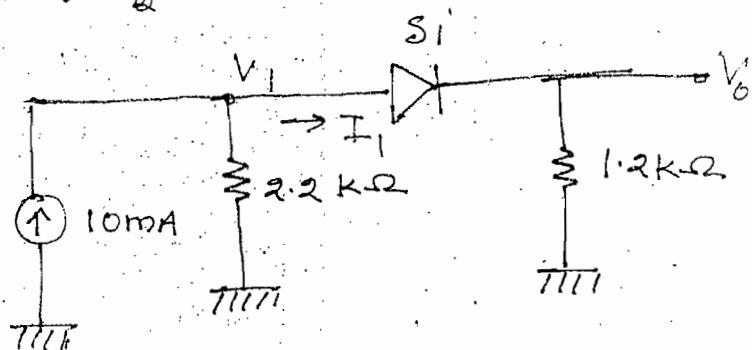
$$I_1 = \frac{20 - V_{YSi}}{1k} = 19.3 \text{ mA}$$

$$I_2 = \frac{V_{YSi} - V_{YGie}}{0.47k} = \frac{0.5V}{0.47k} = 1.06 \text{ mA}$$

$$I_{10} = I_1 - I_2$$

$$= 19.3 - 1.06 = 18.24 \text{ mA, Ans}$$

ques:- Find $I_1, V_1 \& V_o$



Soln:-

$$I = \frac{22 - 0.7}{2.2k + 1.2k} = 6.26 \text{ mA}$$

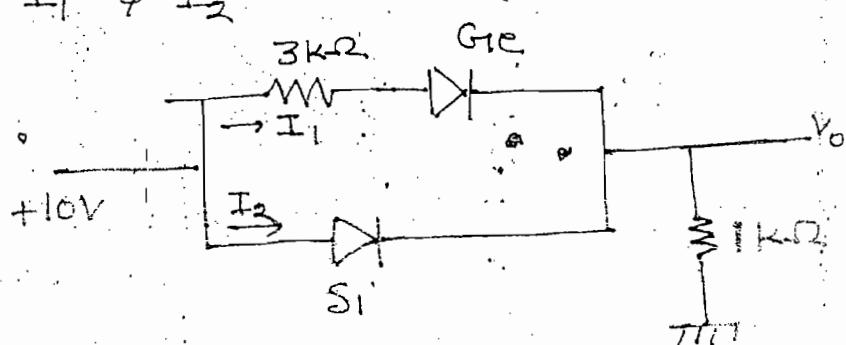
$$V_1 = 22 - I(2.2k) = 22 - 6.26(2.2k) = 8.21V$$

$$V_o = V_1 - V_{YSi} = 8.21 - 0.7 = 7.51V$$

OR

$$V_o = I(1.2k) = 7.51V, \text{ Ans.}$$

ques:- Find $V_o, I_1 \& I_2$



Soln:- $V_o = 10 - V_{rSP}$ Both Ge & Si diode
 $= 10 - 0.7$ will be conducting
 $= 9.3V$ because of resistance

$$I_1 = \frac{0.5V}{8k} = 0.1667 \text{ mA, Ans}$$

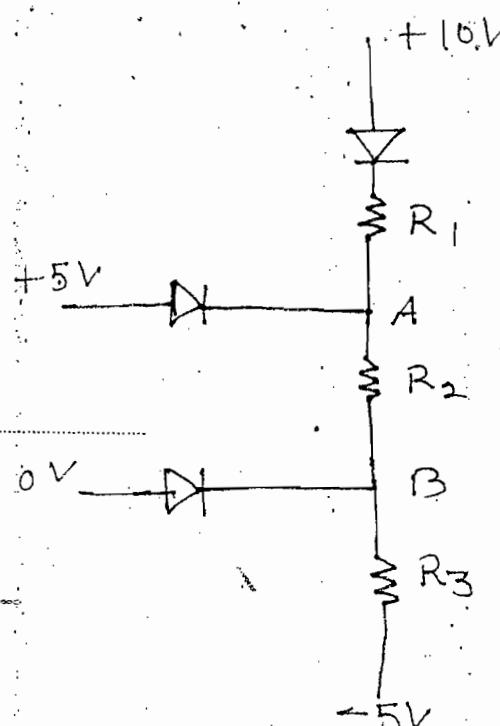
$$I = \frac{V_o}{1k} = \frac{9.3V}{1k\Omega} = 9.3 \text{ mA}$$

$$I = I_1 + I_2 \Rightarrow I_2 = I - I_1$$

$$= 9.3 - 0.1667$$

$$= 9.133 \text{ mA}$$

Ques:- The cut-in voltage for each diode is 0.6V and each diode current is 0.5mA. Find the values of R_1 , R_2 & R_3



Soln:-

$$V_A = 5 - V_r$$

$$= 5 - 0.6$$

$$= 4.4V$$

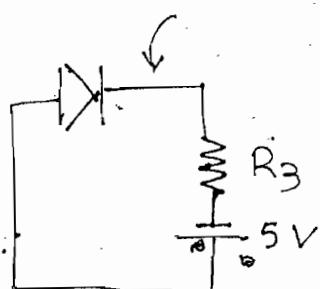
$$V_B = 0 - V_r$$

$$= -0.6V$$

$$R_1 = \frac{10 - V_r - V_A}{0.5 \text{ mA}}$$

$$= \frac{10 - 0.6 - 4.4}{0.5 \times 10^{-3}}$$

$$= 10 k\Omega$$



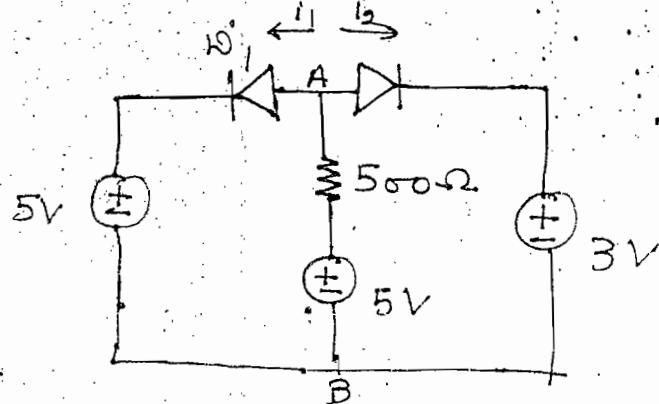
$$R_2 = \frac{V_A - V_B}{1 \text{ mA}} = \frac{4.4V - (-0.6)}{1 \text{ mA}} = 5 k\Omega$$

$$R_3 = \frac{V_B - (-5V)}{1.5 \text{ mA}}$$

$$= \frac{-0.6 + 5}{1.5 \times 10^{-3}} = 2.93 k\Omega$$

ques:- If $\$_1$, $\$_2$ are ideal diode, the current I_1 , I_2 are

- (a) 0, 4mA
- (b) 4mA, 0
- (c) 0, 8mA
- (d) 8mA, 0



The current passing through 500Ω resistor is greater than 0. Hence the voltage V_{AB} is lower than 5V. Diode $\$_1$ is R_B & $i_1 = 0$

$$i_2 = \frac{5-3}{500} = 4\text{mA, Ans}$$

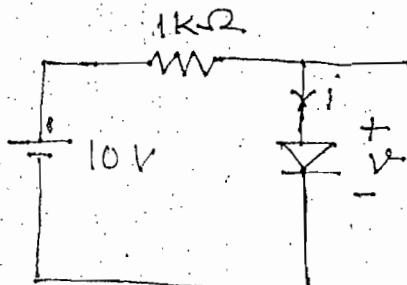
ques:- The IV characteristics of the diode in the circuit given below

$$i = \frac{v-0.7}{500} \text{ A}, v \geq 0.7\text{ volt}$$

$$= 0 \quad v < 0.7\text{ volt}$$

The current is

- (a) 10mA
- (b) 9.3mA
- (c) 6.67mA
- (d) 6.2mA

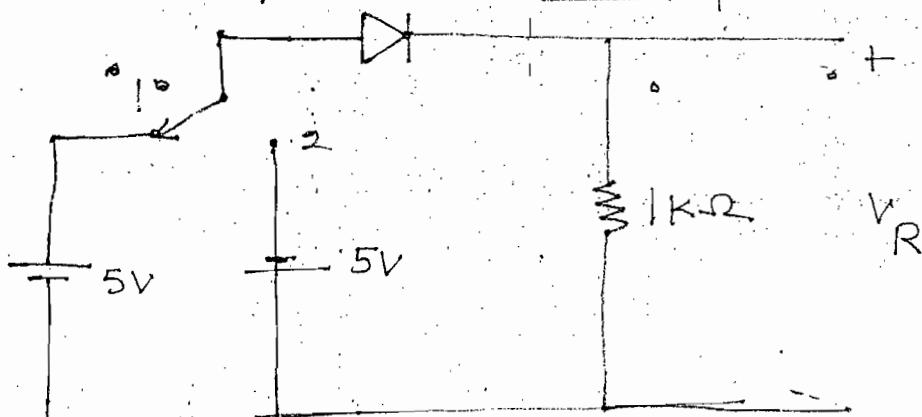


The internal resistance of the diode is 500Ω . Therefore the current $i = \frac{10-v_r}{R_s + R_d}$

$$= \frac{10-0.7}{1000+500}$$

$$= 6.2\text{mA}$$

ques:- In the circuit given below, the switch was connected to position 1 at time $t < 0$. When it is changed to position 2 at time $t = 0$. Assume that the diode has zero voltage drop & a storage time t_s . The O/P voltage V_R for $0 < t < t_s$ is equal to _____?

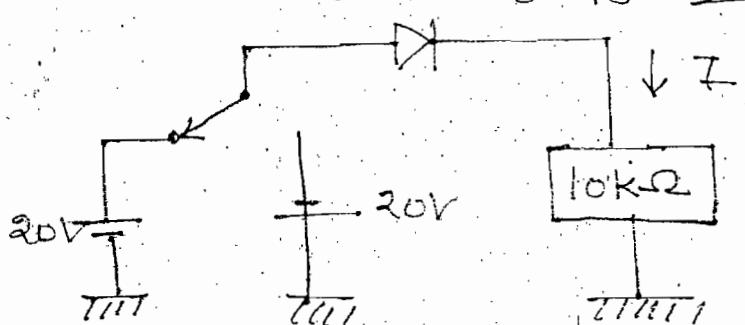


Soln:- At time $t < 0$, the switch is at position 1 and +5V is connected to the diode & FB & short circuited. Therefore $V_R = 5V$

→ At time $t = 0$, the switch is changed to position 2 and -5V is connected to the diode but the diode will continue to remain in FB upto the storage time t_s . After the storage time, the diode will be charged to RB.

→ For the time $0 < t < t_s$, the diode will remain FB & short circuited and -5V will go to the O/p voltage & $V_R = -5V$

ques:- In the figure switch S is in position 1 initially and steady state condition exists from time $t=0$ to $t=t_0$. At time $t=t_0$ the switch is suddenly thrown into the position 2. The current I to the 10kΩ resistor at time $t=t_0$ is _____?



SOLN:- At $t=0$ to $t=t_0$

For time $t=0$ to $t=t_0$, the circuit is under steady state & switch is at position 1 & +20V is connected to the diode. The diode is FB & SC and the current I is equal to $\frac{20V}{10k} = \frac{20}{10k} \text{mA}$

At time $t=t_0$, the switch is thrown to position 2 & -20V is connected to the diode & the current I at time $t=t_0$ is

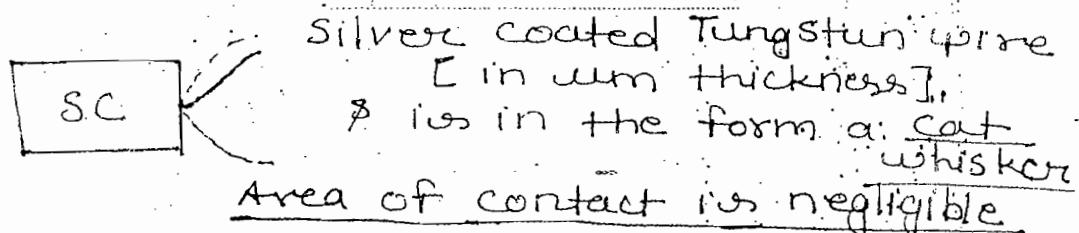
$$I = \frac{-20V}{10k} = -2 \text{mA}, \text{ Ans}$$

Ques:- A PN junction in series with a 100Ω resistor is FB so that a current of 100 mA flows through it. If the voltage across this combination is instantly reversed to 10V at time $t=0$, the reverse current that flows through the diode at time $t=0$ is

- (a) 0 mA (b) 100mA (c) -100mA (d) 200mA

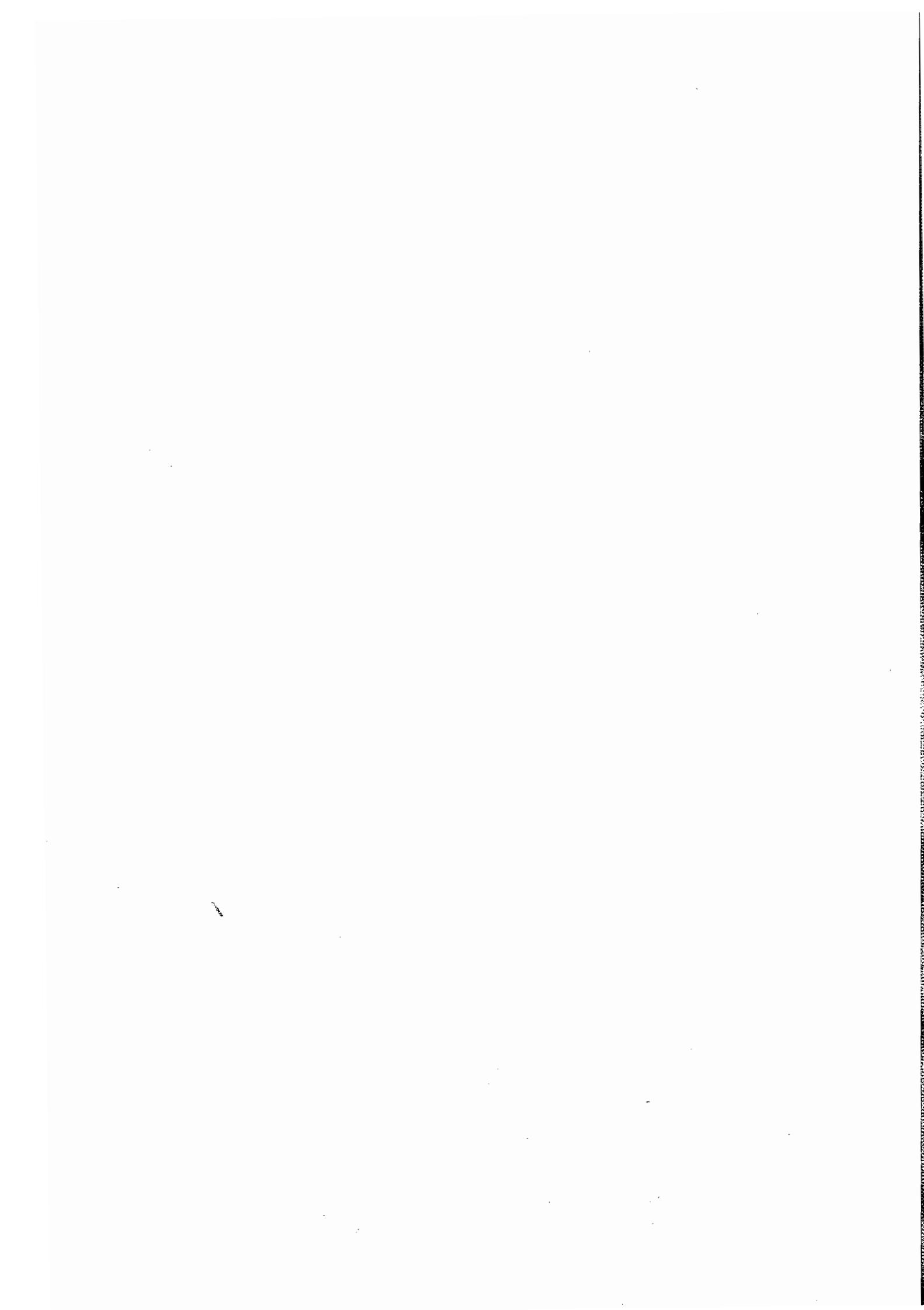
Point Contact Diode

→ Metal - Semiconductor junction diode



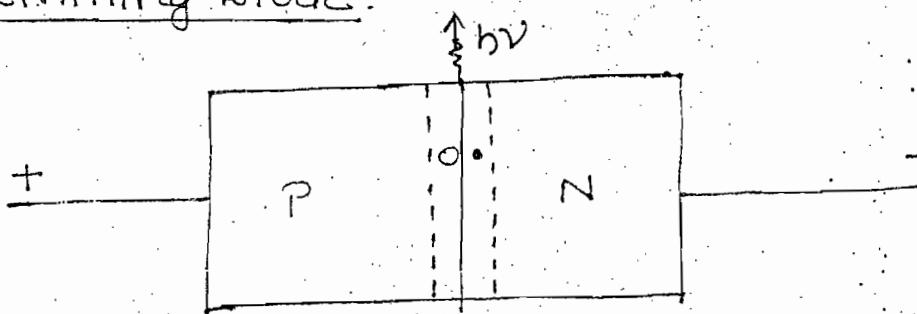
→ The least value of junction capacitance is obtained with point contact diode.

→ It is the first diode or the earliest diode or old diode.

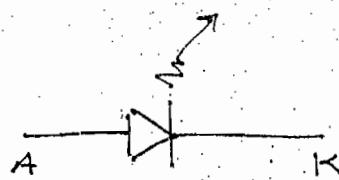


Lecture - 13

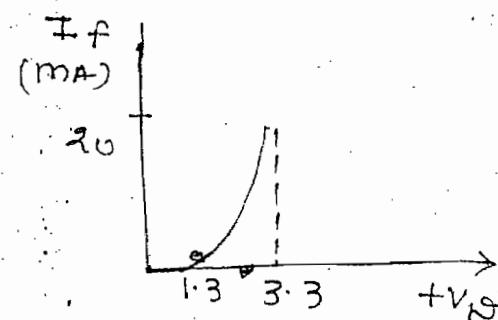
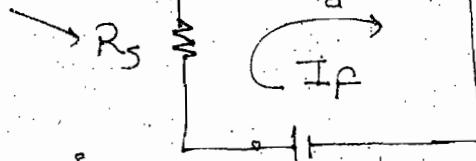
Light Emitting Diode: -



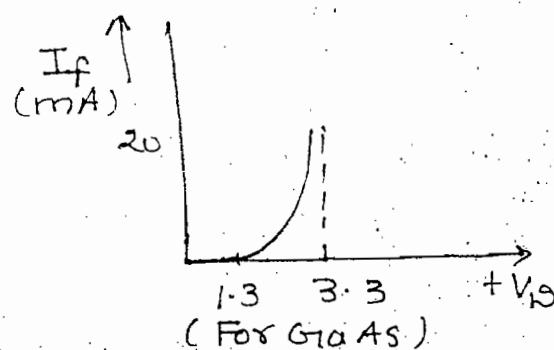
Symbol: -



Lumitine
resistance



LED Characteristics or Forward characteristics of LED or VI: -



→ LED will emit the light when properly biased

Principle: -

Electroluminescence

- The best electroluminescence device is LED
- In LED, light is emitted due to a large no. of recombinations at the junction.
- In LED, most of the light is concentrated near the junction because charge carriers are within the diffusion length (so that e's & holes

will get recombine and energy is released to the junction).

- Generally fabricated with AIGa_As Semiconductors.
- Properly used material is GaAs.
- LED can emit the light either in the visible spectrum or invisible spectrum of light depending on the material used.
- In the invisible spectrum, LED emits infrared light.
- IR LED is used as a remote control transmitter.
- In the visible spectrum of light LED can emit any one of the following colours like Red, Green, Orange, Yellow, white, amber
- The colour of light given by LED depends on
 - (i) The wavelength & frequency of the radiated light

$$\lambda = \frac{1.24}{E_\text{G}} \text{ nm}$$

$$\lambda = \frac{c}{f}$$

(ii) The type and conc. of dopant

- LED fabricated with GaAs which emit IR light
- LED materials are GaAs, GaAsP, GaP
- Modern LED are fabricated with AIGa_As and some of InGa_As semiconductor under control doping
- Always under operated forward bias
- With $20mA$ of forward current LED gives out the max. intensity of light
- When forward current increases from 0 to $20mA$, the efficiency of LED will be increasing i.e. it will emit more brightness of light.

→ Efficiency of LED & forward current (I_f)

→ If forward current is more than 20mA, the junction temperature increases and LED can heat up & the efficiency decreases i.e. it will emit dull colour light.

→ $n \propto \frac{1}{\text{temperature}}$

→ When reverse bias, LED working as a normal diode and therefore it will not emit any light.

→ Power dissipation (I^2R loss) → (internal power consumed is milliwatt).

→ Longer operating life (1,00,000 + hrs)

→ Response time in usec.

→ Cut in voltage → (1.3V - 1.5V) depending on dopant.

→ Longer carrier life time when compare to LC.

→ LED is faster than LCD, because of smaller response time.

→ When compared to LCD, the disadvantage of LED is higher power dissipation.

Applications:-

→ As a remote control transmitter

→ As a display device

→ In designing of opto couplers.

Liquid Crystal Display (LCD) :-

- Power dissipation (μW)
- Response time (msec)
- Operating time (50000 hrs)
- Major application is as a display device

Principle:-

Dynamic scattering of light

- LCD material is liquid crystal material
eg:- Pneumatic liquid

Ques:- A GaAs LED is operated at room temperature. Find the wavelength of the radiated light.

$$\text{Soln:- } \lambda = \frac{1.24}{E_G} \text{ nm}$$

For GaAs, $E_{G,300} = 1.43 \text{ eV}$

$$\lambda = \frac{1.24}{1.43} = 0.867 \text{ nm}$$

Since $\lambda > 0.76 \text{ nm}$

Hence LED fabricated with GaAs emits infrared light.

Ques:- A green colour LED emits light with a wavelength of 5490 Å . Find the energy gap of the material used in eV.

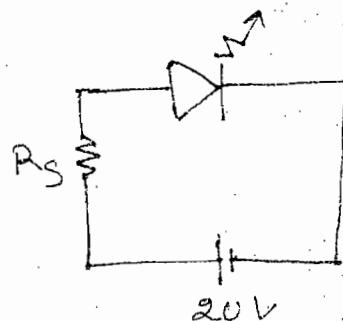
$$\text{Soln:- } \lambda = 5490 \text{ Å}$$

$$\Rightarrow \lambda = \frac{1.24}{(E_G \text{ (eV)})}$$

$$\Rightarrow E_G = \frac{1.24}{5490 \times 10^{-4}}$$

$$= 2.26 \text{ eV}$$

Ques:- Find the value of limiting resistance required for L.E.D ckt given below.



- (a) 735Ω
- (b) 835Ω
- (c) 935Ω
- (d) 1000Ω

Soln:- Let $I_F = 20mA$

$$V_{FD} = 3.3V$$

$$\begin{aligned} 20 &= I_F R_s + V_{FD} \\ \Rightarrow 20 &= 20 \times 10^{-3} R_s + 3.3 \\ \Rightarrow R_s &= 835\Omega \end{aligned}$$

Opto-Couplers:

- Also known as Opto-isolators. Hence they are optically coupled but electrically isolated.
- Opto couplers are faster than conventional devices.

Unit-I

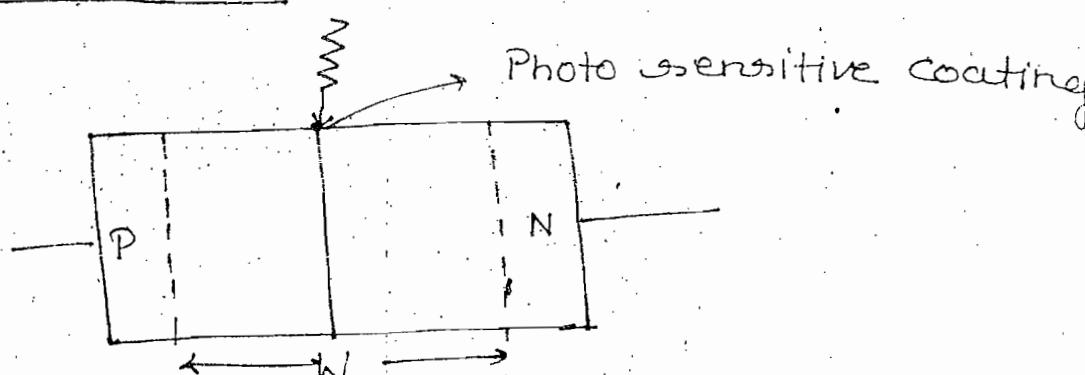
Light source
eg:- LAMP
LASER
LENS

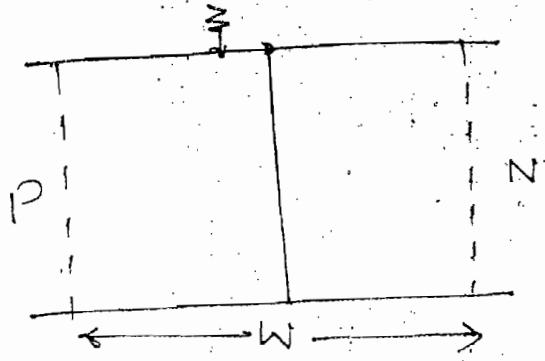
Unit-II

Light sensors
eg:- Photo diode
Photo trans.
LDR
Photo SCR

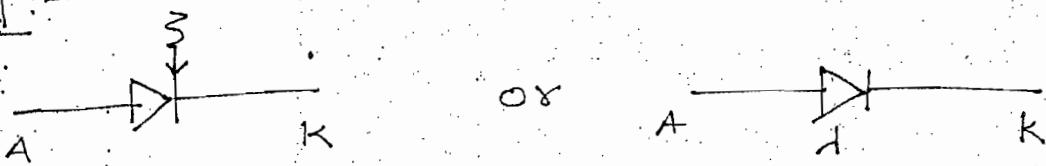
- Optocouplers are widely used in the industrial application where very good dc isolation better than a transformer is required.

Photo-Diode (PD):





Symbol :-



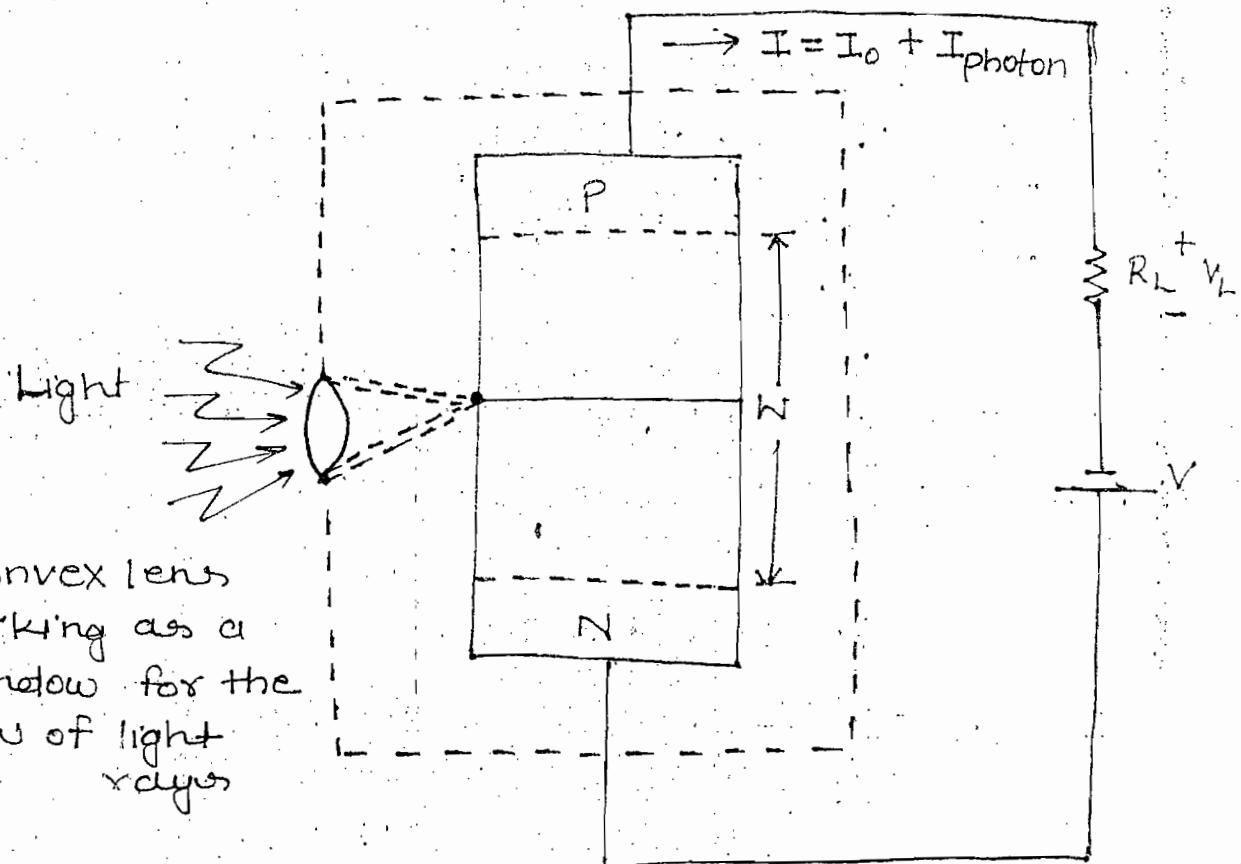
→ Photo sensitive device

Principle :-

: Photoconductive effect

- Basically a pn junction and junction is coated with one of the photo sensitive material like CdS, Se, ZnS, PbS.
- In a photodiode, photo sensitive coating is provided only at the junction.
- If light falls slightly away from the junction, the photodiode will not respond to the light.
- Photodiode has a very larger depletion layer width and this is obtained by reducing the doping conc. of p- & N-region.
- Photodiode has higher sensitivity and this is due to larger depletion layer width.
- Photodiode can be operated with open circuit or short-circuit condition but the conductivity is very small and there are no practical application.
- Photodiode is always operated at reverse bias.
- Ge photodiode will respond to visible light
- Si photodiode will respond to IR light.

- When compare to a normal diode, photodiode
- (I) 10 times faster → Advantage
 - (II) 100 higher sensitivity
 - (III) Low power handling → disadvantage.



→ Reverse bias is kept under darkness

Photodiode will be working as a normal diode under reverse bias & the current is

$$I = I_0$$

- Reverse saturation current
or
Thermally generated current
- 10^{-12} A for Ge photodiode
- 10^{-9} A for Si photodiode
- Dark current (I_{dark}).
↓
Thermally generated current
↓
Drift current

→ When light falls on the convex lens, the max. intensity of this light will be focus at the junction and because of the photon energy a large no. of covalent bonds are broken and large no. of minority carriers are generated and this will inc. the conductivity. This is called as a photoconductive effect. The photodiode is ON-state & the current is

$$I = I_0 + I_{\text{photon}}$$

↓
dark current

→ Photodiode has two current components.

(i) $I_0 \rightarrow$ Thermally generated current
OR
dark current & it is due to temperature

(ii) $I_{\text{photon}} \rightarrow$ It is the current passing in photodiode because of photon energy

→ Photodiode current is the sum of thermally generated current & photon current.

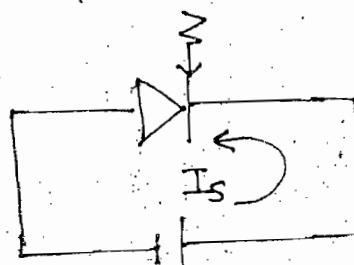
→ In a photodiode, photon current is added to thermally generated current.

$$I_{\text{photon}} > I_0 \text{ or } I_{\text{dark}}$$

(mA) (nA)

**

$$\Rightarrow I \approx I_{\text{photon}}$$



- Photodiode current flows from N to P
- Photodiode current is a reverse current
- Photodiode current is a minority carrier current.
- Photodiode current is a diffusion current

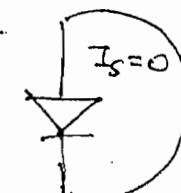
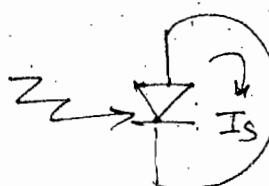
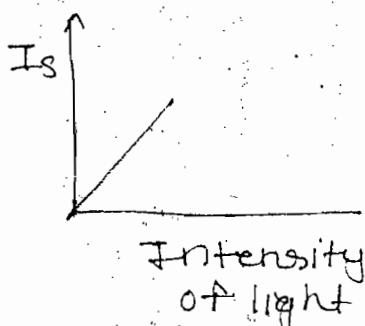
$$I = \underbrace{I_0}_{\text{Drift}} + \underbrace{I_{\text{photon}}}_{\text{Diffusion}}$$

$$I \approx I_{\text{photon}} \quad (\text{Diffusion current})$$

- Photodiode current \propto light flux
- Photodiode current depends on no. of photons falling at the junction.
- Photodiode is basically a light operated switch
- Photodiode is a minority carrier injector
- Photodiode current equation is

$$I = I_s + I_0 [1 - e^{-\frac{V}{nV_T}}]$$

where I_s = short circuit current of photo diode.



- Short circuit current of photodiode inc. with intensity of light falling at junction

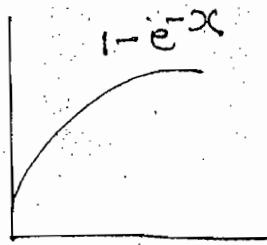
→ I_s is very small

$$I \approx I_0 [1 - e^{-V/nkT}]$$

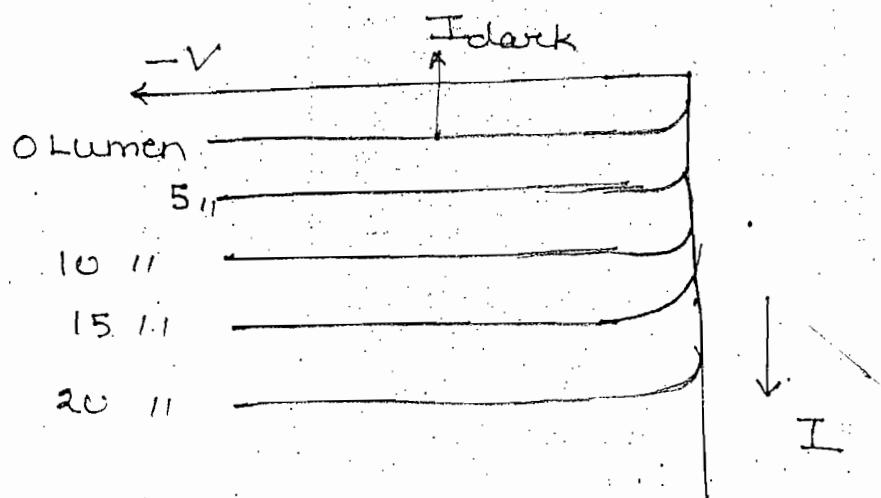
$$\Rightarrow I \propto [1 - e^{-V/nkT}]$$

$$[1 - e^{-x}]$$

exponentially increasing function.



→ Photodiode characteristics will be plotted in third quadrant.



Lumen → Unit for intensity of light

→ The magnitude of reverse current in the photodiode increases with intensity of light falling at the junction.

→ For a good photodiode the essential requirement is larger I_{photon} ratio.

I_{dark}

Ge P.I. Si P.I. → Better

performance

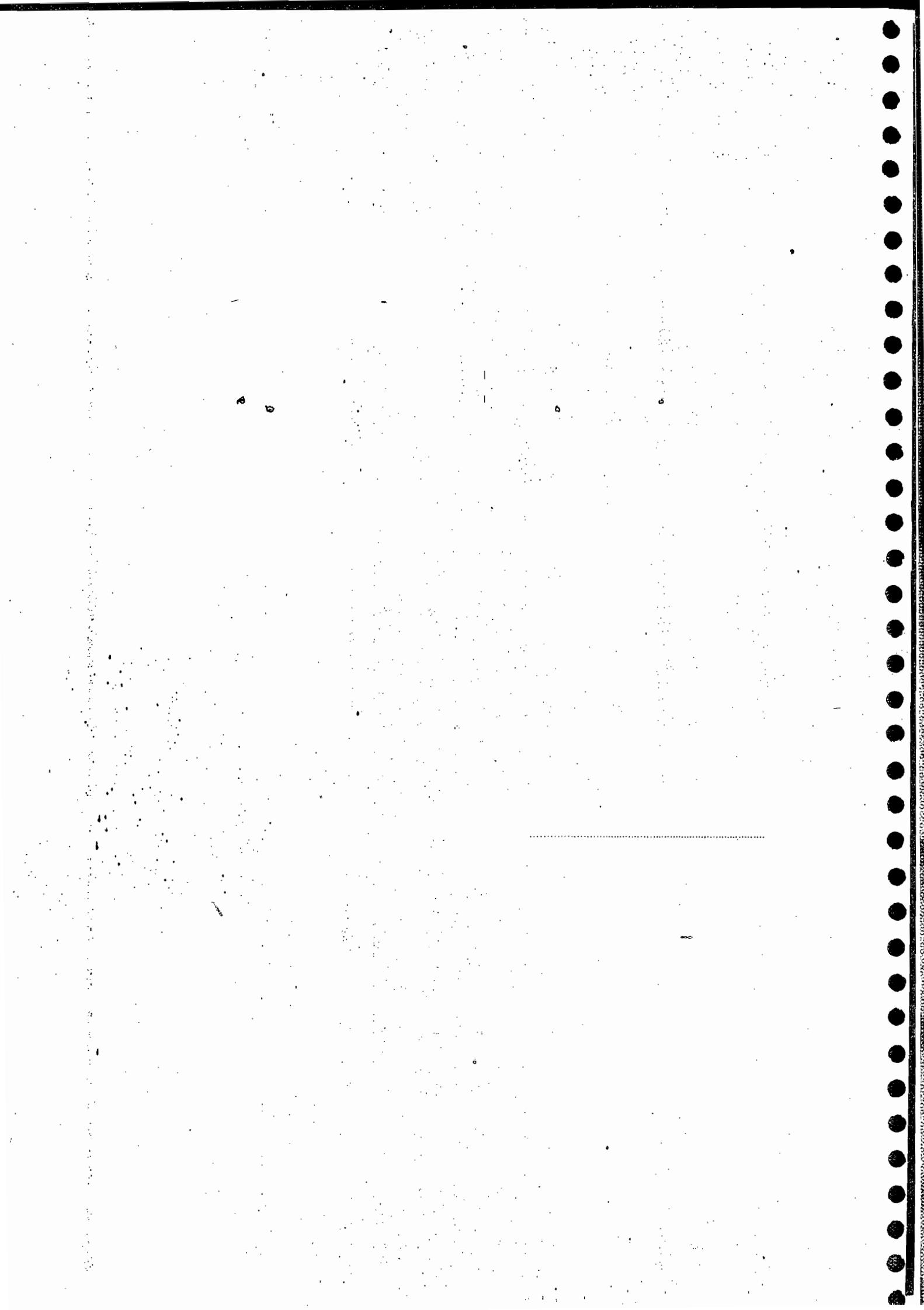
$$\frac{I_{photon}}{I_{dark}} = 10^3 : 1 \quad 10^6 : 1$$

Application:

- As a remote control sensor
- As a light operated switch
- In designing of opto-couplers
- * * → To read the audio track recorded on motion picture film

NOTE:-

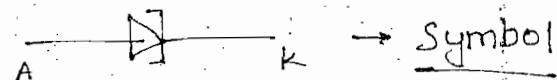
- If photodiode is forward biased and light is focussed at the junction
- The A forward biased photodiode will be working as a normal diode under FB and current is due to majority carriers and it is large i.e. mA
- When light is focused at the junction minority carriers are generated and these minority carriers will be blocked in the FB Photodiode and therefore there is no effect of light on the forward current
- The forward biased photodiode cannot work as a light operated switch (as it is always ON, never goes to off state) (RB)



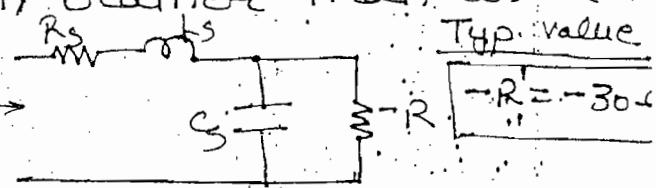
Lecture - 14

Tunnel diode :-

- Also called ESAKI diode
- Basically P^+N^+ diode with a doping conc. of $1:10^3$
- Highly doped P-N junction diode
- Narrow depletion layer (100 \AA unit to 200 \AA)
- Exhibit tunneling effect.
- Tunneling effect is due to narrow depletion layer



- Properly Popularly used material is GaAs
- Fastest switch
- switching times $\rightarrow PS(10^{-10} \text{ s})$
- -ve overistance device
- Tunnel diode is more popular as a -ve resistance device whether than as a fastest switch.



- Advantages:-
- Very smaller in size, easier to fabricate, economical device, low noise device, very low internal power consumption & offers very high resistance to radiation

Disadvantages:-

- It is a two terminal device & therefore there is no proper dc isolation b/w o/p & i/p connection
- Smaller voltage swing

NOTE :-

- Negative resistance devices are tunnel diode → UJT & Gunn-diode.

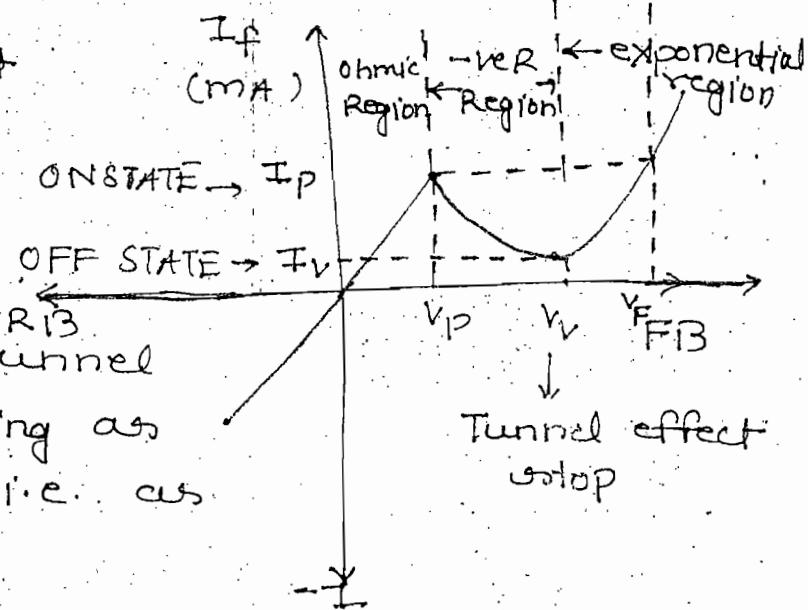
Tunneling Effect :-

- Tunnel diode has very narrow depletion layer and this value is equal to $\frac{1}{50}$ th of the wavelength of visible light and therefore the charge carriers in the device will be penetrating through the narrow depletion layer almost at the speed of the light. As if there is a tunnel in the device and this quantum mechanical behaviour of the charge carrier is called tunneling effect.
- No tunnel is present.

V-I characteristics of tunnel diode :-

I_p = peak current

I_v = Valley "



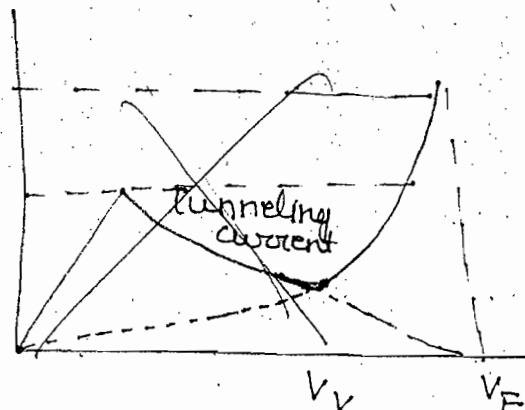
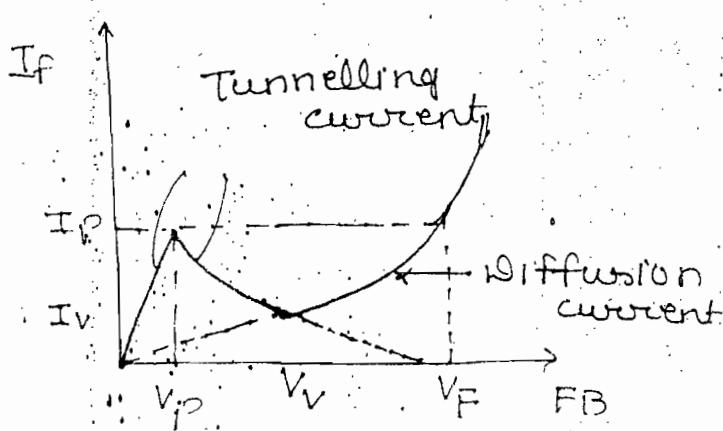
- A reverse bias tunnel diode will be working as a linear device, i.e., as a resistor
- In the exponential region, tunnel diode will be working as a normal diode
- Tunnel diode is always operated in the -ve resistance region.
- -ve resistance of tunnel diode is due to tunneling effect.
- -ve resistance of tunnel diode can be used in designing of
 - (I) Microwave oscillators
 - (II) -ve resistance oscillators.

Cg:- Relaxation oscillator

- Relaxation oscillator, a non-sinusoidal oscillator and it can be designed with UJT or tunnel diode. It generates saw tooth voltage waveform.
- If β is also called voltage sweep generator.
- In tunnel diode, -ve resistance means a forward voltage inc., forward current decreases.
- For tunnel diode cut-in voltage is zero.
- The α -point or operating point of the tunnel diode is located at the centre of the -ve resistance region.
- Tunnel diode exhibits -ve resistance property when the device changes its state from ON state to OFF state.
- Tunnel diode exhibits -ve resistance when
 - (i) forward voltage changes from V_p to V_r
 - (ii) forward current changes from I_p to I_r
- In the -ve resistance region, the tunnel diode is voltage control -ve resistance device.
- Tunnel diode exhibits multifeature property or triple valued property i.e. any value of forward current b/w I_r & I_p can be obtained with three different sets of forward voltages & due to this feature tunnel diode is having multi application in pulse circuit & in designing of industrial circuit.
- For a good tunnel diode, the essential requirement are
 - (i) larger I_p/I_r ratio
 - (ii) larger voltage swing. ($V_F - V_r$)

$$\rightarrow \text{In tunnel diode, } \frac{I_P}{I_V} = \frac{\text{Garts}}{15} \frac{G_E}{7.5} \frac{S_I}{2.5}$$

- For high quality tunnel diodes are fabricated with Garts.
- For commercial tunnel diode are fabricated with G_E.
- Tunnel diode can also be used as a PARA amplifier.



- Tunnelling current is large at peak point
- Tunnelling current is very small at valley point
- Beyond valley voltage, tunnelling current reduces to zero
- Beyond valley voltage, diffusion current exponentially increases with forward voltage
- Diffusion current is large at peak point.

Zener Diode (ZD) :-

Symbol :-

- A breakdown diode
- Basically a p-n junction with little inc. in doping level ($\approx 10^5$)

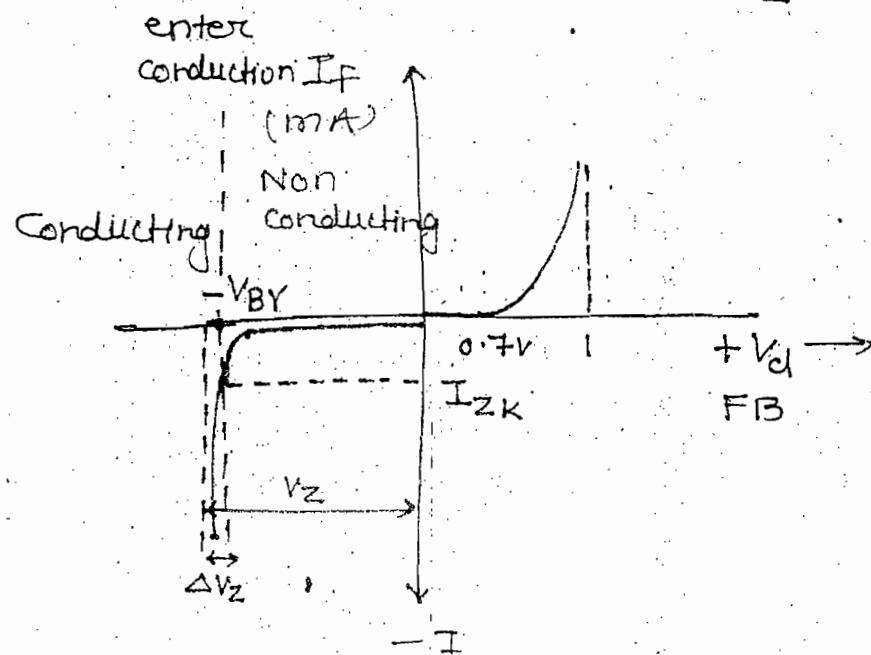
- Generally designed with a normal junction.
- Popularly known as constant voltage device
- Major application is as a voltage regulator device
- Can be used as a reference voltage device
- Can be used as a switch (faster than a normal diode because of higher doping conc.)
- Fabricated only with the Si.
- Always operated under reverse bias
- Zener diode will be working as a voltage regulator circuit when operated under reverse bias.
- When forward bias it will be working as a normal diode
- Cut in voltage 0.6V or 0.7V
- Can be used as a clipper.
- can be used to convert the given sine wave into square wave.
- The principle of zener diode is tunnelling effect or tunnelling of charge carriers across the junction.
- zener diode when designed with abrupt junction and operated under reverse bias will have narrow depletion layer and the device will exhibit tunnelling effect.
- zener diode is specified in terms of breakdown voltage and max. power dissipation.

$$V_{BZ} \rightarrow 10V \quad P_{max} = 400mW$$

- zener diode are commercially available with breakdown voltage in the range of 2.5V to 300V

V-I characteristics of zener diode:-

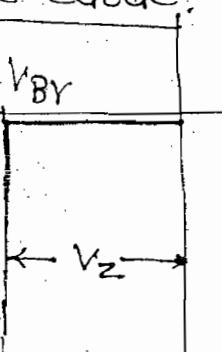
I_{ZK} = zener knee current or min. I_Z



- When zener diode is reverse biased below the breakdown voltage, current is practically 0 & zener diode is non-conducting and it is now working as a normal diode
- When Reverse voltage = breakdown voltage, the current passing through the zener diode suddenly inc. to I_{ZK} and this is due to breakdown phenomenon and now zener diode will be enter into the conduction.
- When reverse voltage is greater than breakdown voltage, more and more current will be passing into the zener diode, the voltage drop across the device will be maintain almost as constant and is equal to around the breakdown voltage of the device.

V-I characteristics of zener diode:-

In ideal zener diode R_B when reverse voltage $>$ breakdown voltage, the zener diode will be conducting with larger current



but voltage across it exactly equal to breakdown voltage of the device

Dynamic resistance of zener diode :-

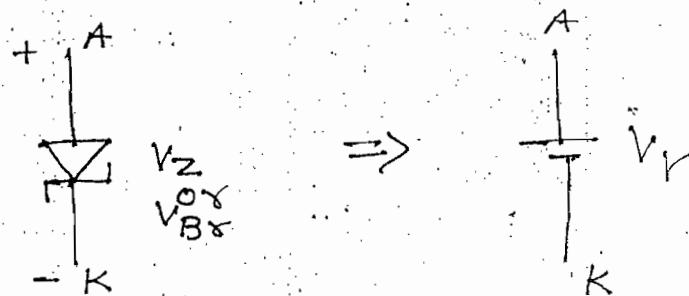
→ Internal resistance of zener diode.

$$R_Z = \frac{\Delta V_Z}{\Delta I_Z} \quad \Omega$$

→ For ideal zener diode, dynamic resistance is 0.

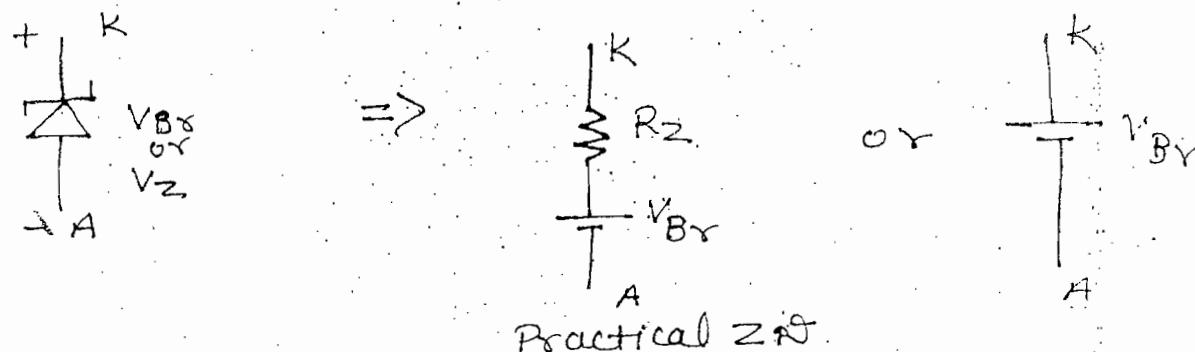
Equivalent circuit of zener diode :-

(a) When zener diode is forward biased:-



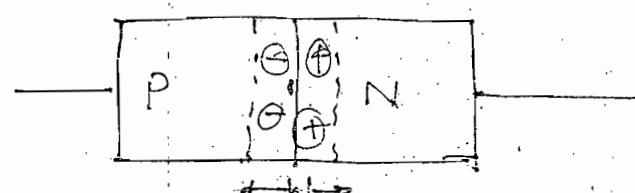
When zener diode is forward bias, it can be replaced by cut-in voltage.

(b) When zener diode is reverse biased:-



Practical ZD.

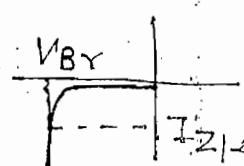
Zener breakdown phenomena:-



$$|E| = 2 \times 10^7 \text{ V/cm}$$

$$w \propto \frac{1}{\sqrt{V_{Zing}}}$$

$$|E| \propto \frac{1}{w}$$

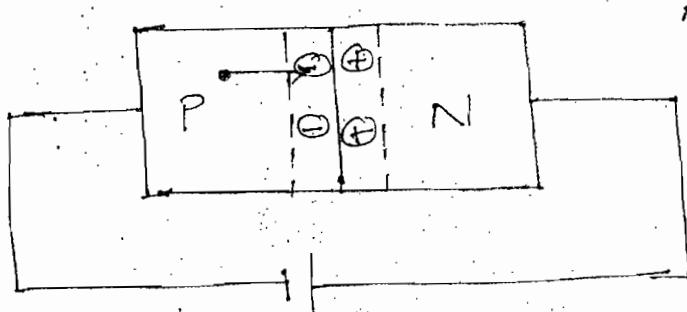


$$V_B < V_BZ \quad V_B > V_BZ$$

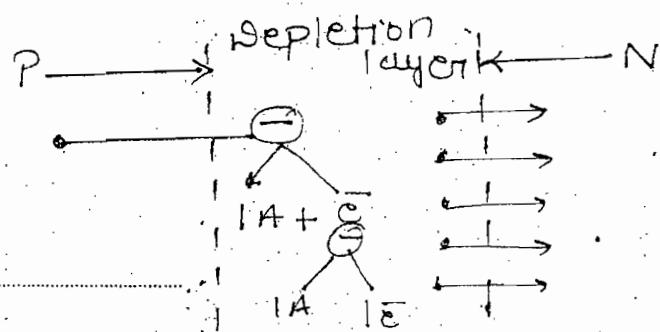
A-E

- It is due to larger electric field intensity
- It is due to tearing off or rupturing of covalent bonds within the depletion layer
- Zener breakdown occurs for breakdown voltage below 6V.
- Zener breakdown voltage dec. with the temperature (NTC)
- The temperature coefficient of zener breakdown voltage is -ve.

Avalanche Breakdown Phenomena



Avalanche
→ e^- multiplication



- It is due to e^- multiplication
- It is due to multiple collision b/w e^- & ions in the depletion layer
- It is due to impact ionization
- Avalanche breakdown occurs for breakdown voltage greater than 6V
- Avalanche breakdown voltages inc. with temp.
- The temperature coefficient of Avalanche breakdown voltage is +ve

Lecture - 15

Zener diode :-

- Impact ionisation occurs in zener diode
- The large flow of current to the zener diode is due to the flow of minority carrier.
- If the current passing to the zener diode is doubled then the voltage drop across the zener diode will remain almost a constant.
- In highly doped diode the breakdown is due to zener effect.

Explanation:-

$$(i) V_{BR} \propto \frac{1}{\text{Doping}}$$

Smaller V_{BR} ,

i.e. $< 6V$

→ zener effect

$$(ii) \text{ Doping} \uparrow, W \downarrow E \uparrow$$

larger IE!

→ zener effect

- In a lightly doped diode, the breakdown is due to Avalanche effect.

- Zener breakdown requires comparatively large doping conc. and larger clamping level compare to Avalanche effect or breakdown.

Step Graded Diode / Abrupt PN Junction diode :-

- Designed with Abrupt junction
- p^+N junction diode or PN^+ diode
- Faster than normal diode.
- Separation layer will penetrate more into the lightly doped region and lesser into higher doped region

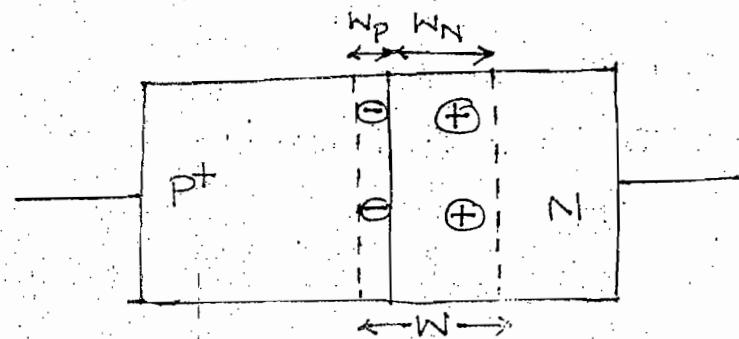
→ Considering P⁺N junction diode

$$N_A > N_D$$

$$W_N > W_P$$

$$W = W_N + W_P$$

$$\approx W_N$$



→ If P⁺N junction diode is now reverse bias then

$$W = \sqrt{\frac{2\epsilon}{q} \left(\frac{1}{N_A} + \frac{1}{N_D} \right)} V_j \text{ metres}$$

$N_A \rightarrow$ large

$\frac{1}{N_A} \rightarrow$ small

Width of the depletion layer on the slightly doped side is

$$W \approx W_N$$

$$W \approx \sqrt{\frac{2\epsilon V_j}{q N_D}} \text{ metres}$$

→ The junction voltage V_j in step graded diode, i.e. P⁺N is

$$V_j = \frac{q N_D W^2}{2\epsilon} \text{ volts}$$

→ The junction voltage formula is a universal formula for any type of PN junction.

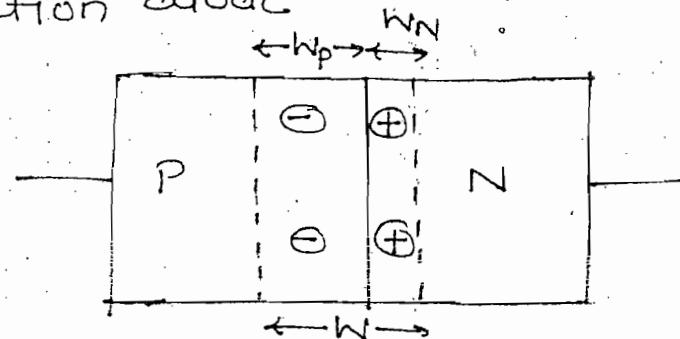
→ Considering P+N⁺ junction diode

$$N_D > N_A$$

$$W_P > W_N$$

$$W = W_N + W_P$$

$$\approx W_P$$



→ If PN^+ junction diode is Reverse bias

$$W = \sqrt{\frac{2\epsilon}{q} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) V_j} \text{ metres}$$

$N_D \rightarrow$ Large

$\frac{1}{N_D} \rightarrow$ smaller

Width of the depletion layer on the lightly doped side is $W \approx W_p$

$$\Rightarrow W = \sqrt{\frac{2\epsilon V_j}{q N_A}} \text{ m}$$

→ The junction voltage V_j in step graded diode i.e. (PN^+) is

$$V_j = \frac{q N_A W^2}{2\epsilon} \text{ Volts}$$

NOTE:-

→ In a step graded diode, most of the depletion layer will be existing only in the lightly doped region

→ In p^+N junction diode most of the depletion layer exist in N^- region.

→ The ratio of depletion layer width on the P side and N^- side can be directly obtained by charge equality equation

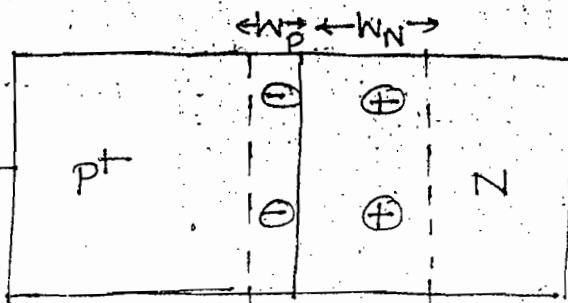
$$q A W_N N_D = q A W_p N_A$$

$$W_N N_D = W_p N_A$$

$$\frac{W_N}{W_p} = \frac{N_A}{N_D}$$

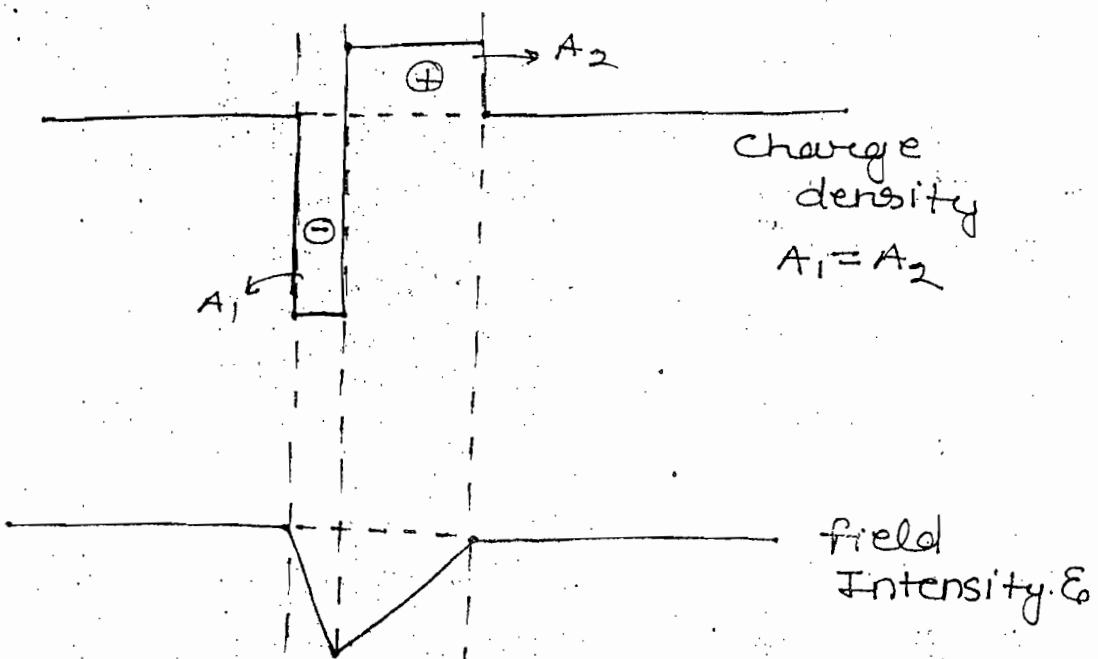
→ Sketch charge density diagram and field intensity diagram of a step graded diode

Consider a p^+N junction diode



$$N_A > N_D$$

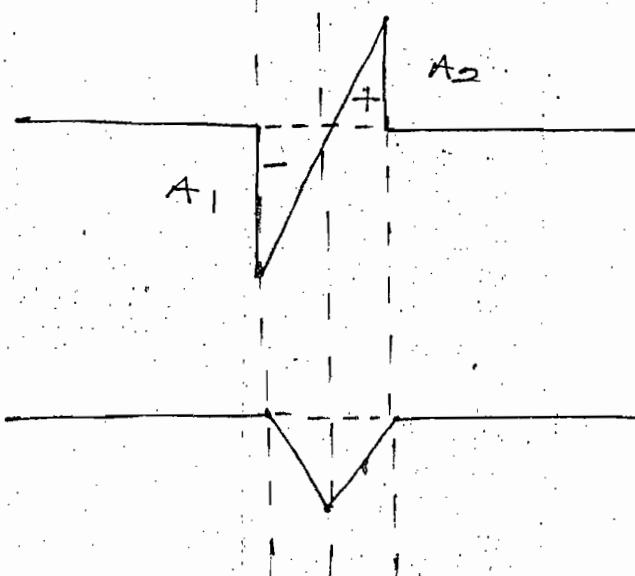
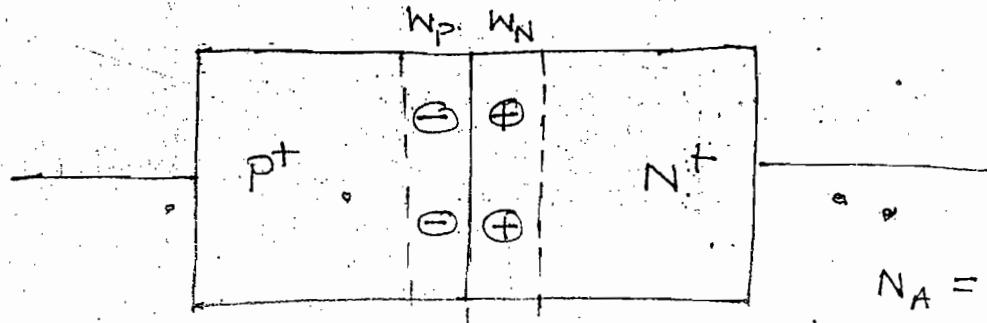
$$w_N > w_p$$



→ In a step graded diode field intensity is maximum at the junction but it is not max. at the centre of depletion layer.

Linear Graded diode:-

- It is designed with normal junction with very high doping level on both the side i.e. $p^+ N^+$ diode with $N_A = N_D$.
- The charge density diagram and field intensity diagram for linear graded diode is given below



charge
density
($A_1 = A_2$)

Field intensity
 E

→ In linear graded diode field intensity is max. at the junction or p^+N^+ junction. It is also max. at the centre of the depletion layer.

Variactor Diode:

- Linear graded diode
- p^+N^+ junction diode
- Principle: —

Transition capacitance (C_T)

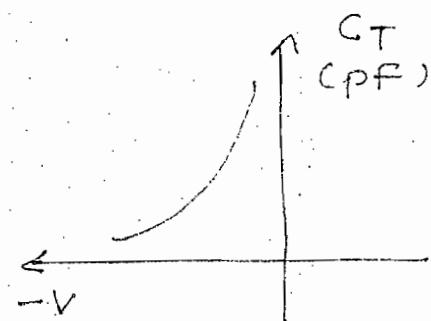
- Always operated under reverse bias
- $C_T \propto V^{-n}$ where $n = \frac{1}{3}$ for V_{RF}
 n = grading coefficient

$$\rightarrow C_T \propto \frac{1}{\sqrt[3]{V_i}}$$

$$\rightarrow C_T \propto \frac{1}{\sqrt[3]{V_{bi} + V_{RB}}}$$

$$\rightarrow C_T \propto \frac{1}{\sqrt[3]{R_B \text{ Voltage}}}$$

- \rightarrow By increasing R_B voltage, C_T is reduced
Characteristic curve :-

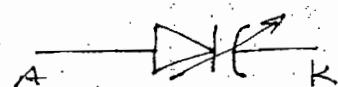


\rightarrow In the varactor diode by varying reverse bias voltage we get a minute variation in the transition capacitance C_T (i.e. 0.1F).

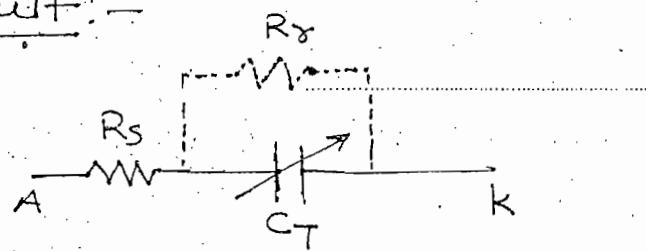
Therefore varactor diode is widely used in the unique application of communication.

- \rightarrow Popular used material is GaAs
 \rightarrow Low noise microwave device

Symbol :-



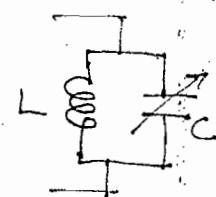
\rightarrow Equivalent circuit :-



- \rightarrow Red dotted lines are reverse resistance of the varactor diode (i.e. $R_R > 1M\Omega$)
- \rightarrow R_S called contact resistance or ohmic resistance. (Below 1Ω .)
- \rightarrow Also called VARI-CAP Diode (variable capacitance diode) / VOLTA - CAP Diode (Voltage variable capacitance diode)

Application:-

- For direct generation of FM by using varactor diode modulator circuit
- In designing of voltage control oscillator (V_{CO}) in PLL circuit
- For tuning in communication circuit.
- For electronic tuning or automatic tuning of receivers.
- For fine tuning of receivers
- For self balancing of AC bridges.
- For tuning of LC resonant circuit
- In designing of PARA - Amplifier (parametric amplifier) i.e. a low noise microwave power amplifier used with satellite communication



NOTE:-

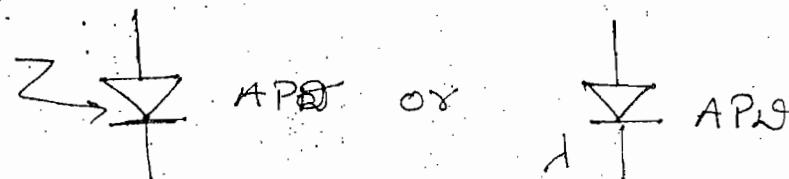
- In discrete components, joints are created by using soldering.
- In IC fabrication soldering is never used.
- In IC fabrication all the interior joints are simultaneously formed by metallization.
- Metallization is a process of creating joint in IC fabrication.
- In IC fabrication Sputnik technique is used. i.e. gold or silver will be maintained and sprayed so that joints are created.

STATE NOTES

Application of photodiode:- WORKBOOK - 2

1 → C	2 → B	3 → B	4 → C	5 → A
6 → B	7 → B	8 → B	9 → B	10 → B
11 → B	12 → C	13 → B	14 → A	15 → C
16 → D	17 → B	18 → C	19 → F	20 → D
22 → A	23 → B	24 → A	25 → D	26 → 4-1-2-3 4-1-3-2
			27 → B	28 → A

Only for Gate Avalanche Photodiode:-



- Basically a photodiode along with Avalanche effect.
- Response time is very small $\rightarrow 25\text{nsec}$
- APD is faster than PD by 1.4 times
- Fabricated only with Si
- Always operated Reverse bias
- Larger signal power than a photodiode
- Major application is have a receiver in fibre optic communication.

Peak Inverse Voltage:-

It is the max. voltage appearing across reverse bias diode without being destroyed.

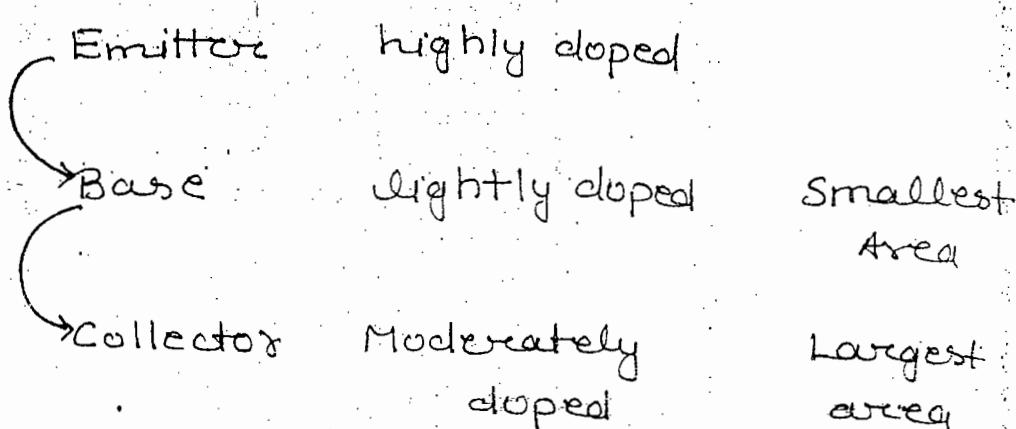
- In series connection PIV will be added up
- In series connection of diode, cut in voltage are also added.

Miscellaneous

1. C	9. C
2. A	10. D
3. C	11. D.
4. C	12.
5. D	13. D
6. D	
7. C	
8. A	" "

Bipolar Junction Transistor (BJT)

- Invented in 1947 by William Schokley, BARTEIN and BARDEEN
- Current control device (CCD)
- Bipolar device i.e. current is carried by e's and holes
- Having majority and minority carriers
- Noisy device due to the presence of minority carriers.
- Leakage currents are existing therefore temperature effect on device is more.
- Temperature sensitive device.
- Thermal stability is less when compare to FET.
- Offers larger gain.
- Gain is more in BJT when compare to FET
- Gain bandwidth product is a constant
- Gain bandwidth product of BJT is greater than gain bandwidth product of FET.
- Major application is as an amplifier.
- can be fabricated with Ge or Si.
- Cut in voltages are existing.

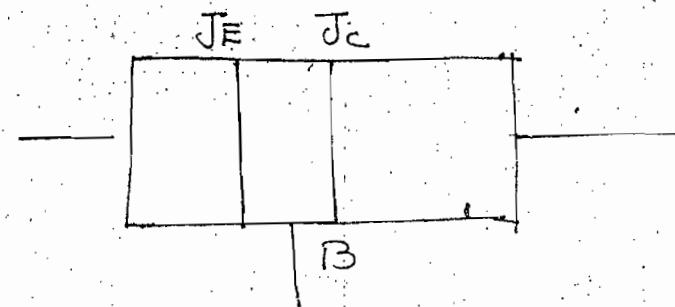


- Emitter is highly doped to inject its majority carriers into the base
- Emitter is provided with medium area
- Base is lightly doped to reduce the recombination
- Base is provided with smaller area to reduce the transit time

It is the time taken by the charge carriers in moving from emitter to collector

- Transistor action takes place in base region
- Collector is moderately doped
- Collector is provided with the largest area to overcome with heat dissipation

Lecture - 16



$$J_E = E + B$$

$$J_C = C + B$$

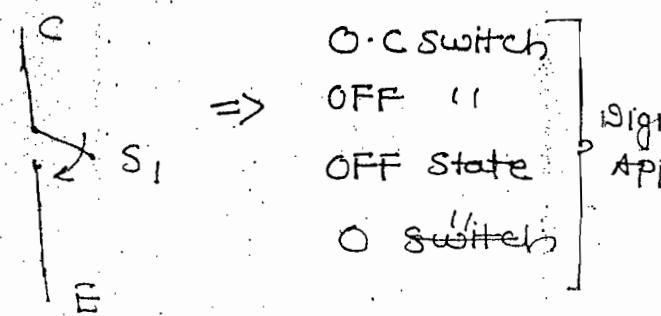
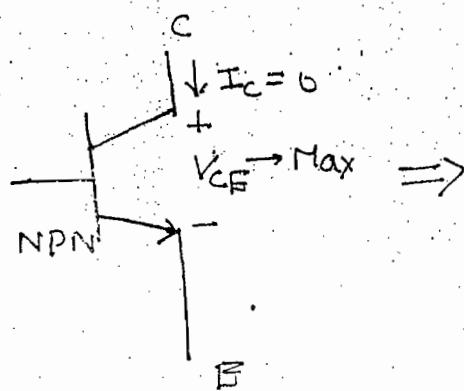
Case - I

J_E J_C

R_B R_B

Transistor (a)

Cut-off region (OFF)

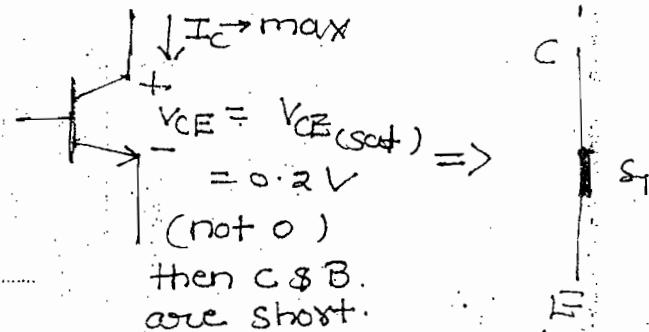


Case - (II) :-

J_E J_C (a)

F_B F_B saturation

(because
currents
are large)



→ If the emitter junction voltage is greater than collector junction voltage in magnitude, the transistor is under forward saturation region.

S.C. switch
ON " "
ON state
1 state

→ If the collector junction voltage is greater than emitter junction voltage in magnitude, the transistor is under reverse saturation region.

Case - (III) :-

J_E J_C (a)

F_B R_B Active Region

[Forward
active region]

→ Excellent Amp.

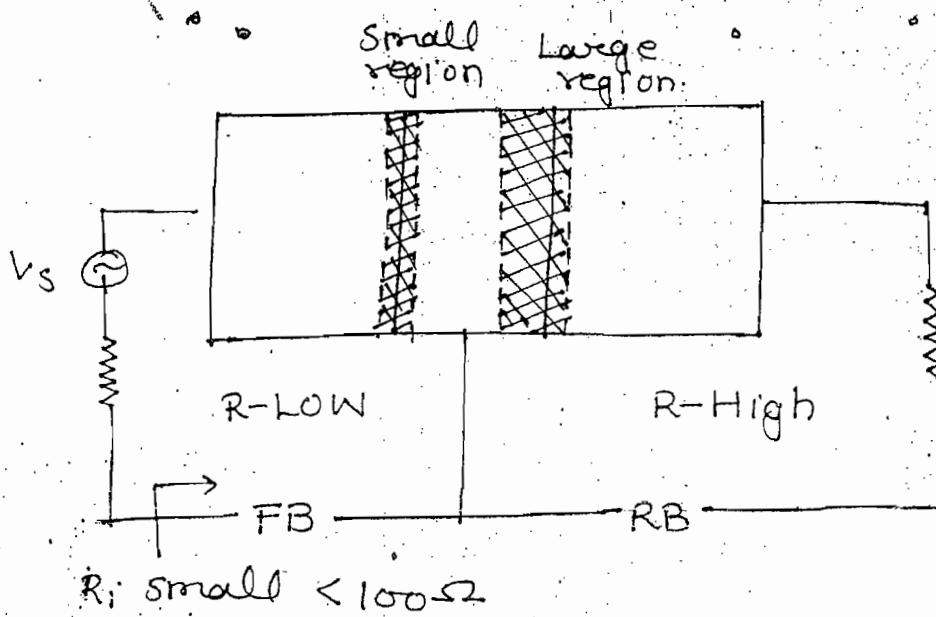
→ High gain Amp.

Case-(IV) :-

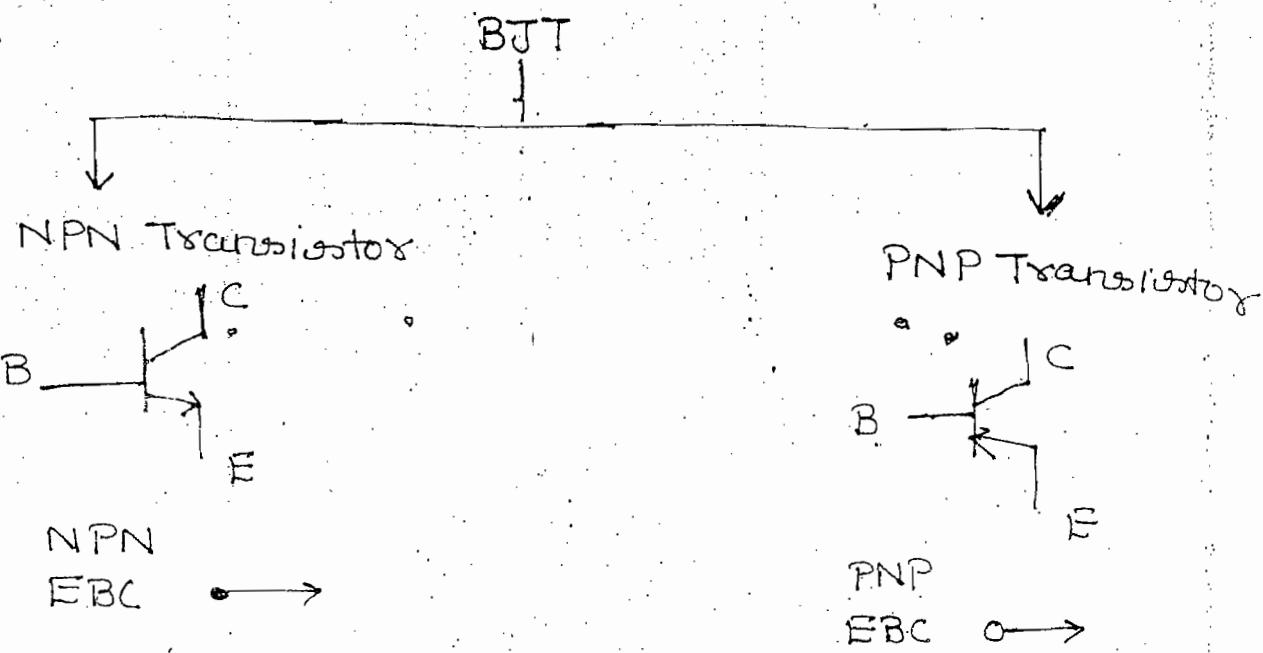
JE	J _c	P _e	→ Very low gain Amp
FB	R _B	Reverse active region	→ Attenuator
			→ Digital ckt

NOTE:-

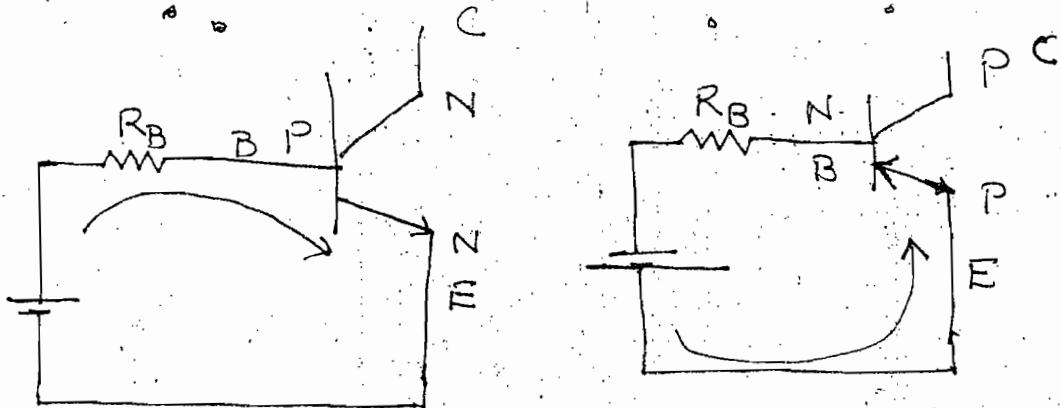
- Transistor will be working as an amplifier when operated in forward active region.
- Transistor will be working as a switch when operated in
 - (a) Saturation
 - (b) cut-off region
 - (c) Both a & b
 - (d) cut off, saturation & Active region
- In digital circuit transistor is operated in
 - (a) Saturation region
 - (b) cut-off & saturation region
 - (c) cut-off, saturation & Active
 - (d) cut-off, saturation reverse active region
- ECL is operated in the active mode
- In a transistor, arranging the doping conc. of E, B & C in the ascending order the correct sequence is $\xrightarrow{B \ C \ E}$
- In a transistor arranging the physical dimensions of E, B & C in descending order, the correct sequence is CEB



- In a transistor under active region, more the depletion layer will be penetrating more into the base.
- In a transistor signal is transferred from low resistance region to high resistance region and hence the name transfer resistor.
- Transistor is a combination of two words transfer resistor.
- The smaller i/p resistance in the BJT is due to forward biasing emitter base junction.



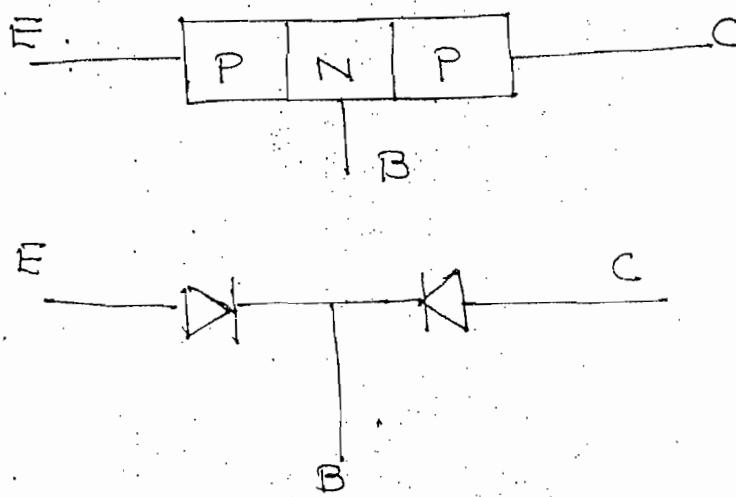
- In NPN transistor, current is predominantly dominated by e's
- In PNP transistor, current is dominated by holes
- NPN transistor is faster than PNP ~~is great~~
bec. $\mu_n > \mu_p$
- The arrow mark on the symbol denotes the direction of emitter current when emitter base junction is FB.



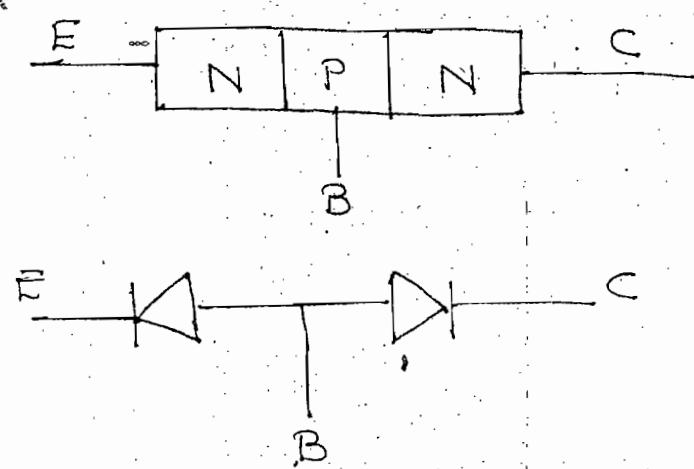
→ NPN and PNP transistor are called complementary transistors.

Diode equivalent circuit of the transistors :-

(I) PNP transistor :-

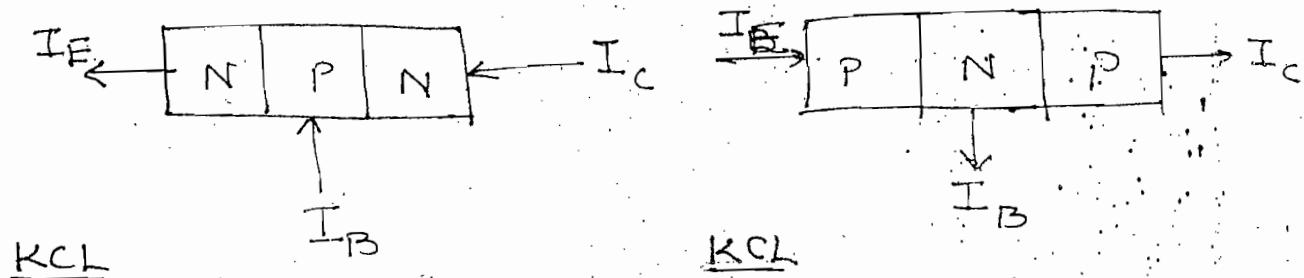
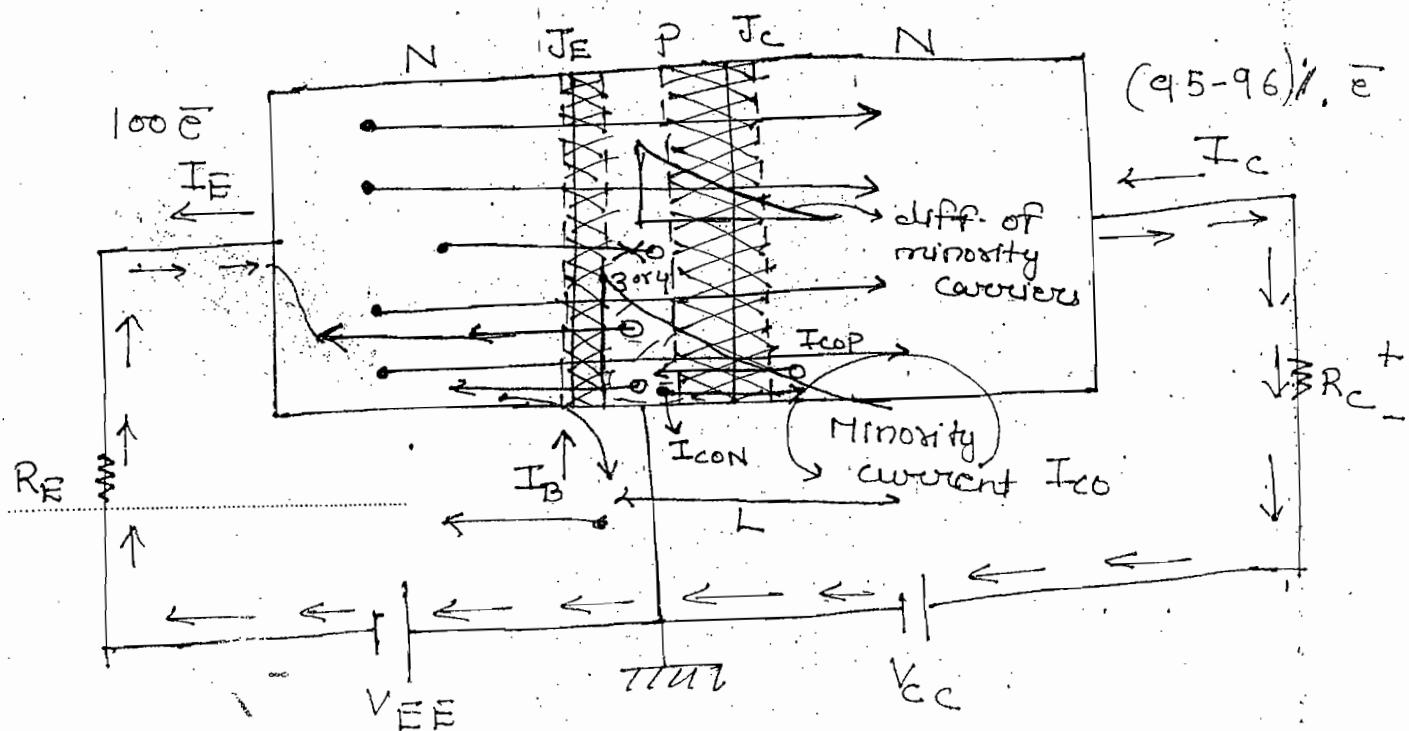


(II) NPN Transistor :-



- A transistor can be represented as a combination of two diodes connected back to back
- When two diodes are connected as shown above, it will not work as a transistor because
 - there is no bonding force in b/w the two diodes
 - Even if a bonding force is created, the base width will become very large. Therefore charge carriers cannot reach the collector

Operation of NPN Transistor under active region:-



$$I_E = I_C + I_B$$

NOTE:-

$I_B \rightarrow$ Small (μA)

$I_c \approx I_E$

- In a transistor circuit, internal current is bipolar and external current is only due to \bar{e} 's
- In NPN transistor, recombination takes place in base and emitter
- In PNP transistor, recombination takes place base & collector
- In a transistor, recombination takes place in all the three regions (E,B,C)
- Emitter current is a majority carrier current
- Emitter current is a diffusion current
- Base current is a majority carrier current
- In NPN transistor, base current is due to holes.
- In PNP transistor, base current is due to \bar{e} 's
- In NPN transistor, base current is due to no. of holes getting recombine with the incoming \bar{e} 's
- Base current is also called recombination current.
- Recombination current flows only in BJT
- Base current is a diffusion current.
- Collector current is a diffusion current.
- I_{CO} is a drift current.
- In a transistor all the three major current (I_E , I_B & I_c) are diffusion current.

- In a transistor various current components are
 - (i) Diffusion current
 - (ii) Drift current
 - (iii) Recombination current
- collector current is made up of two current components

(i) Majority current :-

It is due to 95-96% of the emitter E's reaching the collector.

(ii) Minority current :-

It is generated because of temperature in the reverse bias collector junction.

- The general equation of the transistor is

$$I_c = \alpha I_E + I_{C0}$$

where

$$\alpha = 0.95 \text{ to } 0.96$$

Majority Minority
carrier carrier

$$I_c \approx \alpha I_E$$

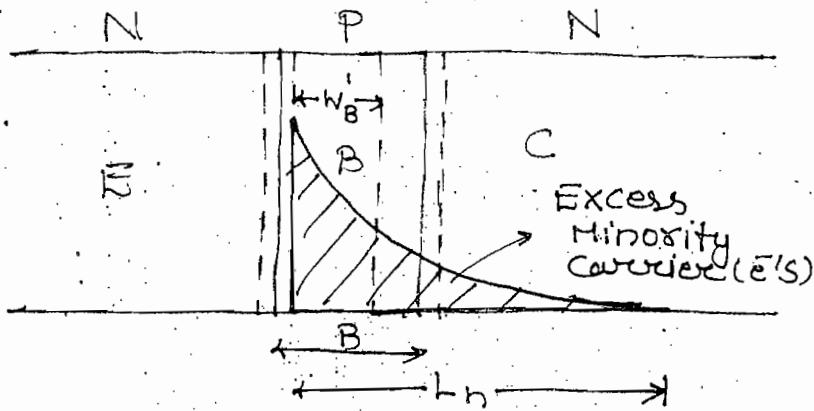
Majority carrier → Diffusion current

Minority carrier → Drift current

- The majority carriers of the emitter or entering into the base will become minority carrier & they are called excess minority carrier in the base region.

- In a transistor the movement of charge carriers b/w base & collector is due to the diffusion of minority carrier or the diffusio

of excess minority carriers in the base
 → (This property in the transistor called
 transistor action.)



W_B^1 = Effective base width of the transistor

→ For best performance of the transistor or
 for the transistor action to take place, the
 condition is $[W_B^1 < L_n]$

$$\Rightarrow W_B^1 < \sqrt{\mu_n V_T L_n}$$

$$\Rightarrow W_B^1 < \sqrt{\mu_n V_T C_n}$$

I_{CO} -

→ Collector reverse saturation current
 OR

Minority carrier current in the transistor.

OR

Leakage current in the transistor

OR

Thermally generated current in the
 transistor.

Gie Tr. Si Tr.

I_{CO}	mA	nA
----------	----	----

I_{CO} of Gie Tr. $>$ I_{CO} of Si Tr.

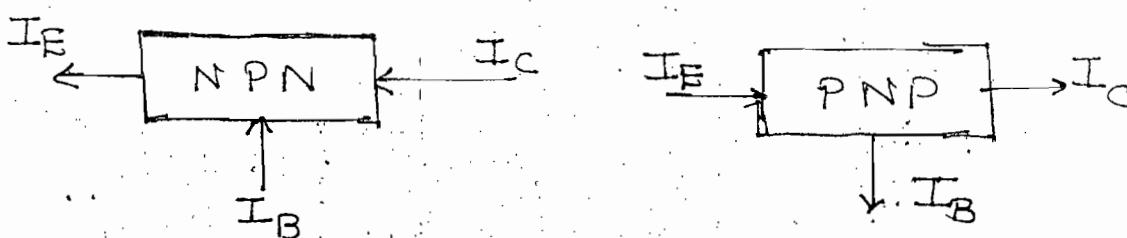
- I_{CO} is highly sensitive to temperature
- I_{CO} is independent of collector junction voltage
- For $1^{\circ}C$, I_{CO} approximately increases by 7% in both Ge & Si transistors.
- I_{CO} doubles for every $10^{\circ}C$.
-

$$I_{CO(T_2)} = I_{CO(T_1)} \left[\frac{T_2 - T_1}{2 \cdot 10} \right]$$

- For better performance of transistor, I_{CO} must be as small as possible.
- I_{CO} is a drift current

Current directions in a transistor:

- It is the universal custom that any current entering into the transistor is given with a +ve sign and current leaving the device is denoted by -ve sign



I_E is -ve

I_C, I_B, I_{CO} is +ve

NPN
EBC
↓
 I_E

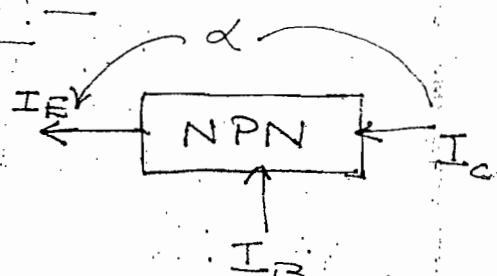
I_E is +ve

I_C, I_B, I_{CO} all -ve

PNP
EBC
↓
 I_E

Alpha (α) of the transistor:

$$\alpha = -\frac{I_C}{I_E}$$



→ Since I_C & I_E have opposite sign
 α is +ve

$$\alpha = \left| \frac{I_C}{I_E} \right|$$

α is always < 1 b.c. $I_E > I_C$

$$\alpha \approx 1$$

Typical value of $\alpha = 0.98$

Max. value of $\alpha = 1$ (For ideal transistor)

$$\alpha = 0.6 \text{ to } 0.999$$

→ α is called current gain of common base transistor.

→ α in terms of β is given by

$$\alpha = \frac{\beta}{\beta + 1}$$

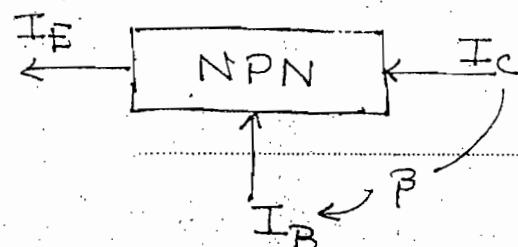
β of the transistor —

$$\beta = \frac{I_C}{I_B}$$

$$\beta \gg 1$$

Typical value = 49

$$\beta = 30 \text{ to } 300$$



→ β is called current gain of common emitter transistor

→ β in terms of α is given by

$$\beta = \frac{\alpha}{1 - \alpha}$$

→ β in terms of ~~h~~^h parameters is given by h_{FE} or h_{FE}

h_{FE} or h_{FE} \rightarrow Forward current gain in common emitter transistor

$\rightarrow \beta$ is sensitive to temperature i.e. $\beta \uparrow$ as $T \uparrow$

In GIE transistor, β doubles for every $50^\circ C$

In Si β \uparrow \uparrow \uparrow \uparrow \uparrow \uparrow $75^\circ C$

$\rightarrow \beta$ is the most important specification of the transistor (bec. it gives max. current gain in common emitter transistor)

$$\begin{array}{c} \text{Beta} \\ \downarrow \qquad \downarrow \\ \beta_{dc} \text{ or } \beta \\ \text{or } h_{FE} \rightarrow \text{capital letter} \\ = \frac{I_C}{I_B} \text{ shows dc} \\ \beta_{ac} \text{ or } \beta' \\ \text{or } h_{fe} \end{array}$$

$\rightarrow \beta_{dc}$ when signal is not applied

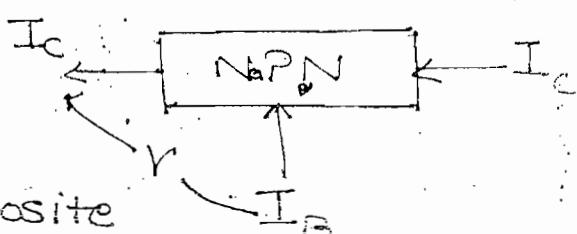
$\rightarrow \beta_{ac}$ when signal applied to the transistor

$$\boxed{\beta_{ac} = \frac{\delta I_C}{\delta I_B} = \frac{\Delta I_C}{\Delta I_B}}$$

$$\rightarrow \boxed{\beta_{dc} > \beta_{ac}} \quad \text{or} \quad \boxed{h_{FE} > h_{fe}}$$

Gamma (γ) of the transistor :-

$$\gamma = -\frac{I_E}{I_B}$$



Since I_E & I_B have opposite sign

γ is always +ve

$$\boxed{\gamma = \left| \frac{I_E}{I_B} \right|}$$

$$V = \left| \frac{I_C + I_B}{I_B} \right|$$

$$= \beta + 1$$

Typical value = 50

→ V is called the current gain of common collector transistor.

Relationship b/w α , β & V of the transistor:-

$$V = \beta + 1 = \frac{1}{1 - \alpha}$$

→ In a transistor various current gains are α , β & V and arrange in them in the ascending order, the current sequence is $\alpha, \beta \& V$

I_E in terms of I_B :-

$$I_E = I_C + I_B$$

From the def. of β , $I_C \approx \beta I_B$

$$I_E \approx \beta I_B + I_B$$

**

$$I_E \approx (1 + \beta) I_B$$

Derive an equation of for collector current:-

→ In the active region of transistor, the general equation of the transistor is

$$I_C = \alpha I_E + I_{CO}$$

$$\text{But } I_E = I_C + I_B$$

$$I_C = \alpha [I_C + I_B] + I_{CO}$$

$$\Rightarrow I_C = \alpha I_C + \alpha I_B + I_{CO}$$

$$\Rightarrow I_C(1-\alpha) = \alpha I_B + I_{CO}$$

$$\Rightarrow I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \frac{I_{CO}}{1-\alpha}$$

But $\frac{\alpha}{1-\alpha} = \beta$ & $\frac{1}{1-\alpha} = \beta + 1$

$$\Rightarrow I_C = \beta I_B + (\beta + 1) I_{CO}$$

Effect of temperature on collector current

$$I_C = \beta I_B + (\beta + 1) I_{CO}$$

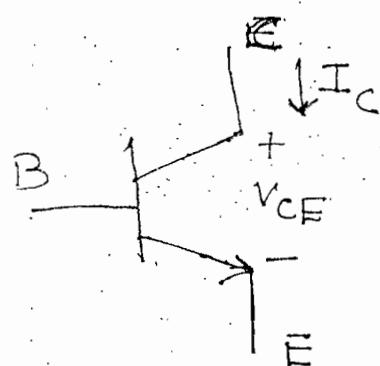
As $T \uparrow \beta \uparrow$ & $I_{CO} \uparrow$

Hence $I_C \uparrow$ with temperature

Power dissipation in transistor (P_T) :-

Internal Power

$$P_T = |I_C| V_{CE} \text{ Watts}$$



In cut-off region :-

$$P_T = 0$$

bec. $I_C = 0$ & $V_{CE} = \text{Max}$

→ In cut-off region, transistor will not consume any power

$$V_{CE} = V_{CE(\text{sat.})} = 0.2 \text{ V}$$

$P_T = \text{negligible.}$

In the saturation region:-

$I_c \rightarrow \text{Max}$

$$V_{CE} = V_{CE(\text{sat.})} = 0.2V$$

$P_T \rightarrow \text{negligible}$

$\downarrow I_c \rightarrow \text{max}$

$$\begin{aligned} V_{\text{max}} &= V_{CE(\text{sat.})} \\ &= 0.2V \end{aligned}$$

In the active region:-

$P_T \rightarrow \text{Max}$

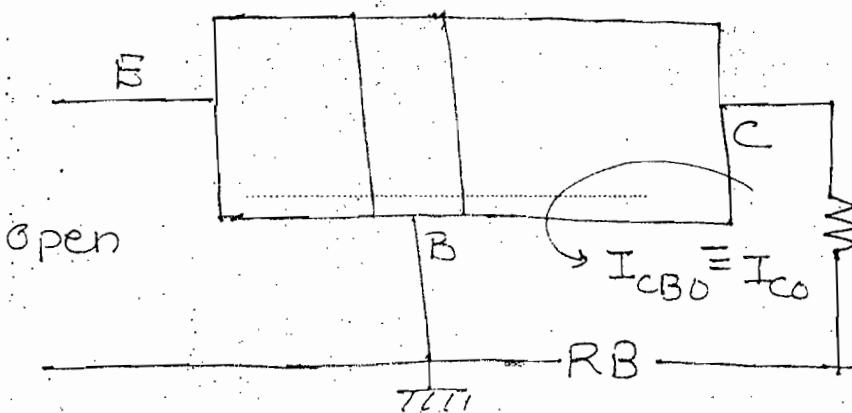
$I_c \rightarrow \text{medium}$

$V_{CE} \rightarrow \text{medium}$

- The transistor will be consuming maximum power when operated in the active region.

I_{CBO} :-

- It is the leakage current passing from collector to base with an emitter open circuited.



$$I_{CBO} = I_C$$

↓

Collector reverse saturation current.

- Also known as emitter cut-off current.

At low frequency :- For GATE & PSU

$$I_{CBO} \equiv I_{CO}$$

At High frequency :- For IES

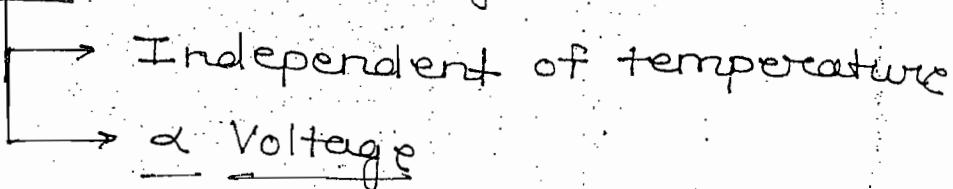
$$I_{CBO} = \text{Leakage current} + \text{surface current}$$

$$= I_{CO} + I_{\text{surface}}$$

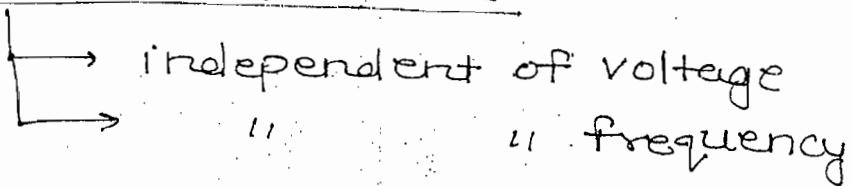
↓

due to skin effect

→ $I_{\text{surface}} \propto \text{frequency}$



→ $I_{CO} \propto \text{Temperature}$



I_{CEO} :-

- It is the leakage current passing from collector to emitter with base open circuited
- It is also called base cut-off current
- It is the current passing in the transistor when the base terminal is suddenly open circuited
- If base is open
i.e. $I_B = 0$

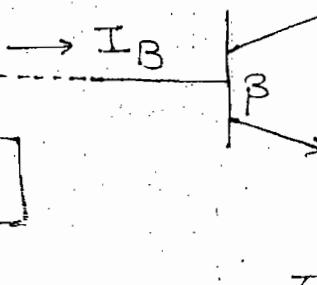
then $I_C \equiv I_{CEO}$

$$I_{CEO} = (1+\beta) I_{CO}$$

Since $I_{CO} \equiv I_{CBO}$

$$I_{CEO} \equiv (1+\beta) I_{CBO}$$

$$\downarrow I_C \\ = \beta I_B + (1+\beta) I_{CO}$$



$$\text{or } I_{CEO} \equiv \frac{I_{CBO}}{1-\alpha}$$

→ In a transistor, the various leakage currents are I_{CEO} , I_{CO} & I_{CBO} and arranging them in ascending order the current sequence is $I_{CO}, I_{CBO} \& I_{CEO}$

For GATE:- $I_{CO} = I_{CBO} < I_{CEO}$

Standard equation for collector current:-

→ $I_C = \beta I_B + (1+\beta) I_{CO}$

⇒ $I_C = \beta I_B + (1+\beta) I_{CBO}$

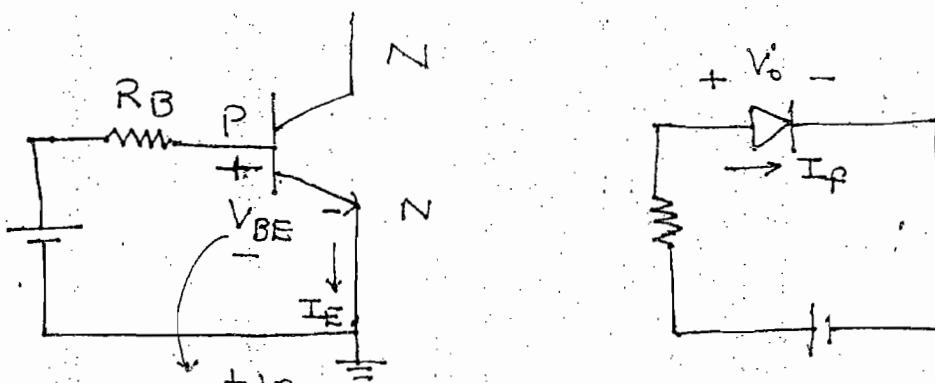
⇒ $I_C = \beta I_B + I_{CEO}$

⇒ $I_C \approx \beta I_B$

Lecture - 17

Equation for emitter current (I_E) :-

Emitter current is the forward current of emitter diode



$$I_E \approx I_{C0} e^{V_{BE}/nV_T}$$

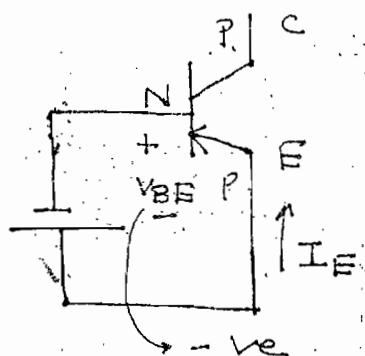
$$I_f \approx I_0 e^{V_o/nV_T}$$

V_{BE} (Base to emitter voltage of transistor) :-

$$V_{BE} \downarrow \approx nV_T \downarrow \log \left(\frac{I_E}{I_{C0}} \uparrow \right)$$

V_{BE} decreases with temperature.

For pnp transistor :-



For pnp transistor V_{BE} is -ve

For npn transistor V_{BE} is +ve

At room temperature, for npn Ge transistor

$$V_{BE(\text{active})} = 0.2V$$

For " " Si 11

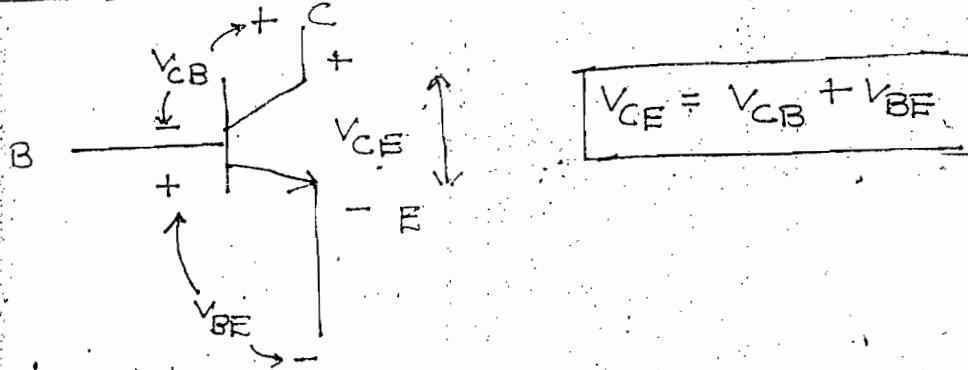
$$V_{BE(\text{active})} = 0.7V$$

For pnp transistor, just reverse the polarity

V_{BE} increases by 2.3 mV for 1°C

$$\frac{\partial V_{BE}}{\partial T} = -2.3 \text{ mV}/{}^\circ\text{C}$$

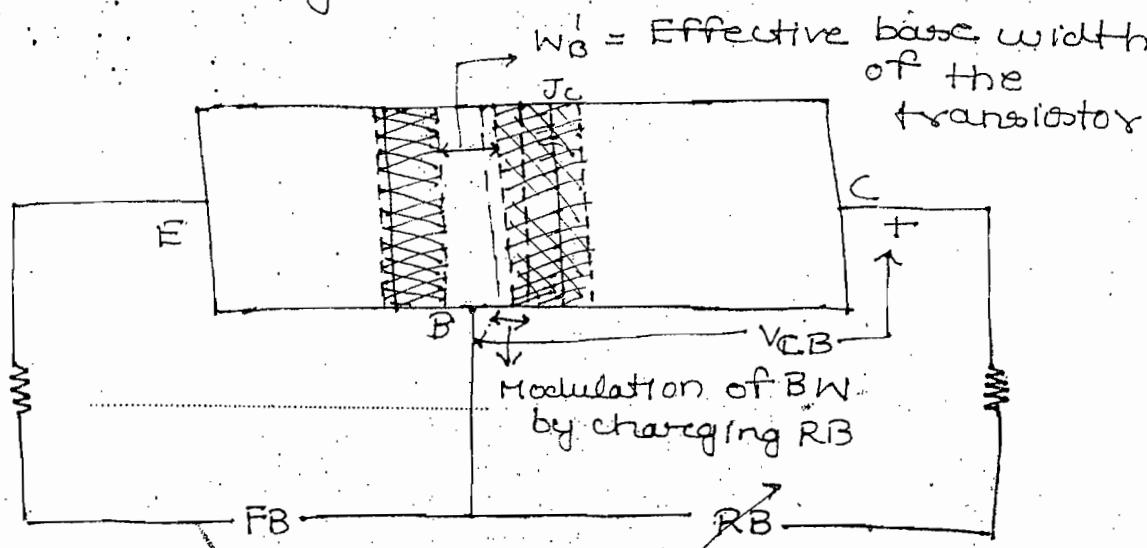
Relationship b/w terminal voltage of a transistor:-



$$V_{CE} = V_{CB} + V_{BE}$$

Base Width Modulation:-

- Also called early effect
- The process where the effective base width of the transistor is altered by varying collector junction voltage is called base width modulation



Base narrowing in the transistor is called base width modulation

- In a transistor if collector junction voltage (V_{CB}) is more than R_B then the base width of transistor is reduced
- Base narrowing in the transistor refers to early effect.
- Due to early effect
 - (1) Effective base width of the transistor is reduced & therefore transit time decreases

and the transistor will become faster.

- (ii) The chances of recombination in the base region is reduced and therefore more charge carrier will be reaching the collector.
- (iii) Collector current slightly increases
- (iv) Recombination current decreases
- (v) Base current reduces
- (vi) α of the transistor slightly increases

$$\uparrow \alpha = \left| \frac{I_C \uparrow}{I_E} \right| \quad \uparrow \beta = \frac{I_C \uparrow}{I_B \downarrow}$$

$$\alpha = 0.9 \text{ to } 0.999$$

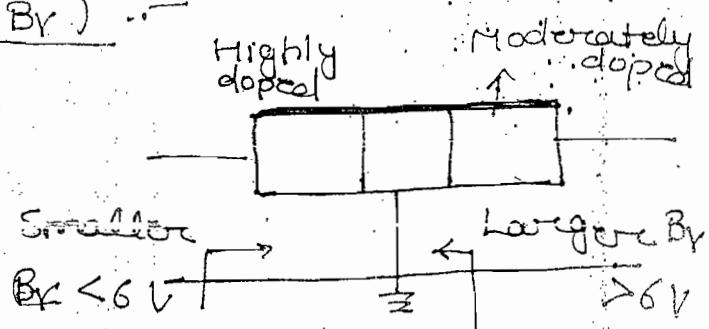
- (vii) β of the transistor increases by a larger value.

- The effective base width of the transistor will offer a resistance r_{bb} (Base spread resistance. (Typ. value = 100Ω) to the high frequency signal and therefore reduces the performance of transistor at high frequencies.
- The property where the effective base width of the transistor is reduced to 0. By applying a larger collector voltage is called punch through or reach through (since effective BW of the transistor is 0, the collector is electrically short circuit to the emitter and the transistor is destroyed. During punch through collector junction voltage has exceeded the collector junction breakdown voltage & thereby transistor is destroyed).

Breakdown voltages (B_V or B_F) :-

In any pn junction,

$$V_{BR} \propto \frac{1}{\text{doping}}$$



→ Collector junction B_V is always greater than emitter junction B_V

$$B_{V_{C-B\text{junc}}} > B_{V_{E-B\text{junc}}}$$

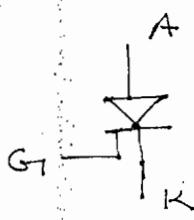
→ In a transistor, Emitter-base junction breakdown is due to zener effect & collector-base junction breakdown is due to Avalanche effect

Thus does not depend on high freq. or low freq. signal applied.

Thyristors:-

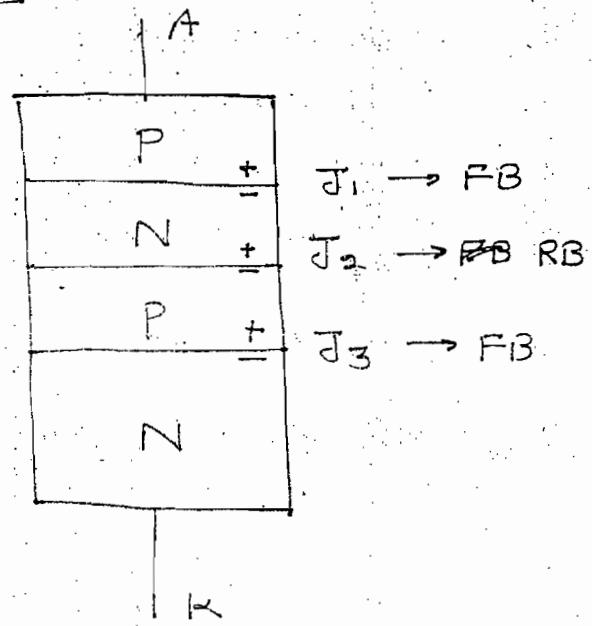
- Basically a latch (having two stable states i.e. ON state and off state)
- Power switching devices
- Power control devices i.e. they can handle large amount of power with negligible internal power consumption
- fabricated only with Si
- Gt thyristors are not practical
- can be unidirectional or bidirectional device
- multilayer solid state device
- can be voltage operated or current operated or suitable for both the operation
- In a thyristor, changes its state from OFF to ON bec. of applied voltage. It is called voltage operation.
- If a thyristor changes its state from OFF to ON bec. of applied current. It is called current operation.
- Thyristor family members are
 - SCR → Silicon controlled Rectifier → TRIAC
 - SUS → SIAC
 - SCS → PNPN Diode
 - SBS
- Thyristor are faster than BJT

SCR → Silicon Controlled Rectifier:-

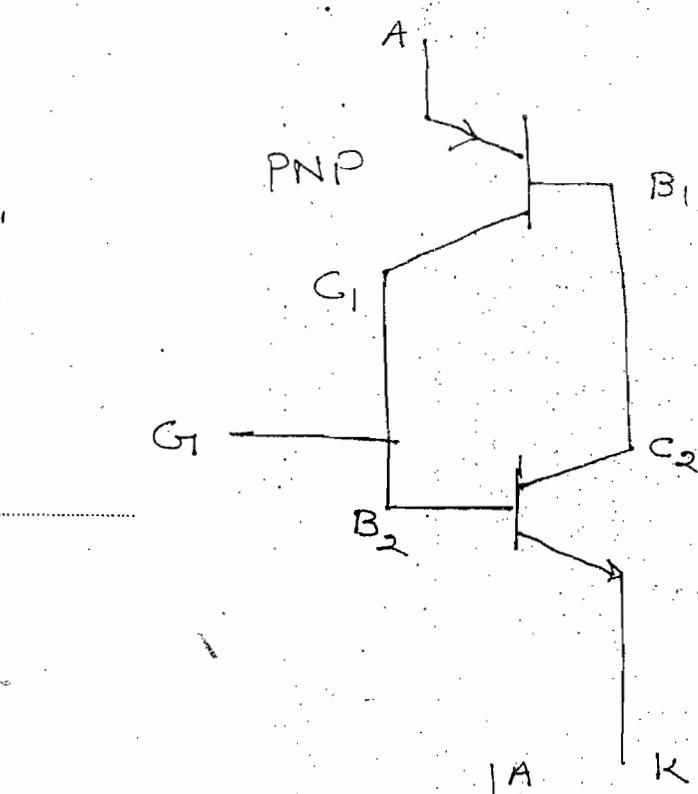


Symbol :-

Structure :-

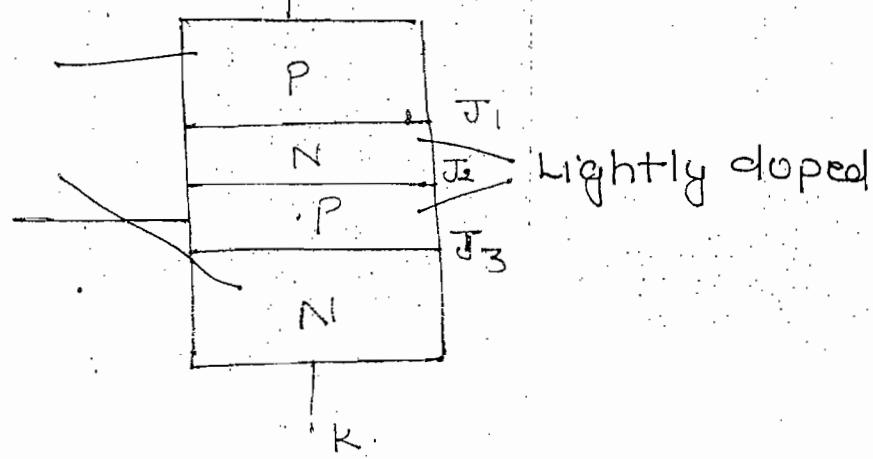


Equivalent circuit :-



Highly doped

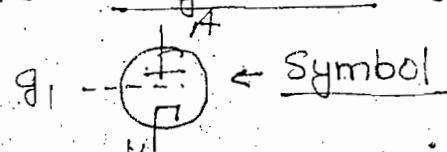
G



- Power switching device
- Power control device (can handle large amount of power with negligible internal power consumption)
- Three terminal device i.e. Anode, cathode & Gate
- Four layer solid state device with three junctions.
- In SCR, gate is made up of p-type material
- The equivalent ckt of SCR is given by a transistor latch
- In transistor latch, one transistor is ON while other is OFF.
- The equivalent ckt of SCR consist of one PNP transistor and one NPN transistor connected such that collector of first transistor is given to base of second transistor and collector of second transistor is given to base of first transistor.
- In SCR transistor, inner most layers are relatively lightly doped than the outermost layers.
- SCR is generally specified in terms of break over voltage
- SCR is a unidirectional device i.e. it will conduct only when anode is given the voltage w.r.t. cathode
- If anode is given a -ve voltage w.r.t. cathode SCR will never conduct.
- SCR is always operated under forward bias
- When SCR is forward bias with a small voltage below the breakdown voltage. Junction J₁ & J₃ are FB and J₂ is RB and therefore the internal resistance of SCR is very large & no current will be passing into SCR and

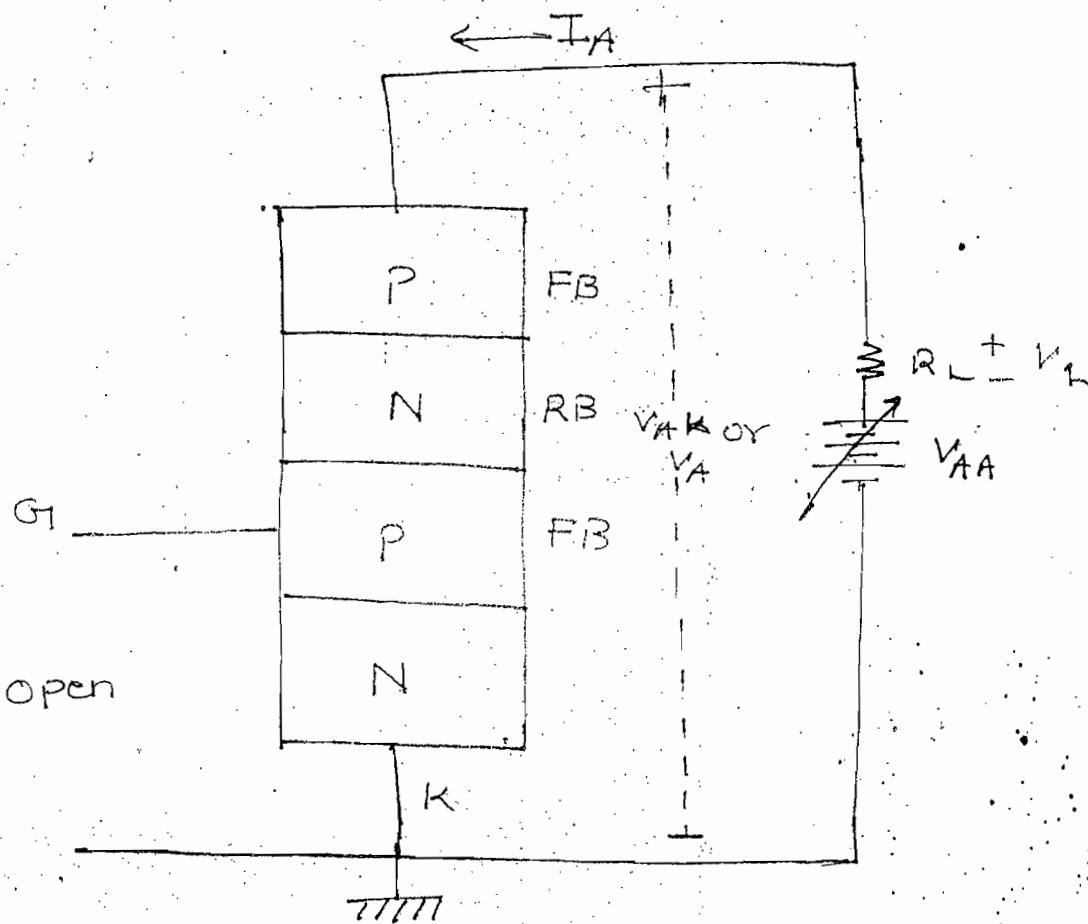
SCR is OFF i.e. non-conducting

- SCR is fabricated with MESA technology
- Fast switch
- switching time (ns)
- SCR is faster than BJT (Tunnel diode is fastest switch)
- SCR is a power rectifier
- SCR can be used as a control rectifier
- SCR can be used in designing of polyphase rectifier.
- SCR can be used for speed control of DC motor.
- SCR is charge control device
- SCR works under principle of current regeneration
- The tube version of SCR is Thyatron or gas triode
- Thyatron is gas triode
- Thyatron can handle more power than SCR
- SCR is faster than thyatron
- SCR will consume less power when compare to thyatron
- SCR can be operated either with voltage operation or current operation



Voltage operation of SCR:-

- Under voltage operation of SCR, gate must be open circuited or gate current must be kept zero.
- When anode supply voltage V_{AA} is kept below the breakdown voltage of the SCR, junction J_1 & J_3 are FB and J_2 is RB and the internal resistance of the SCR is very large and there will be no current will be passing into



SCR and SCR is in the OFF state i.e. non-conducting.

→ As anode supplied voltage is gradually increasing (below the breakdown voltage), the junction J_2 will become more reverse bias and SCR will remain in the OFF state.

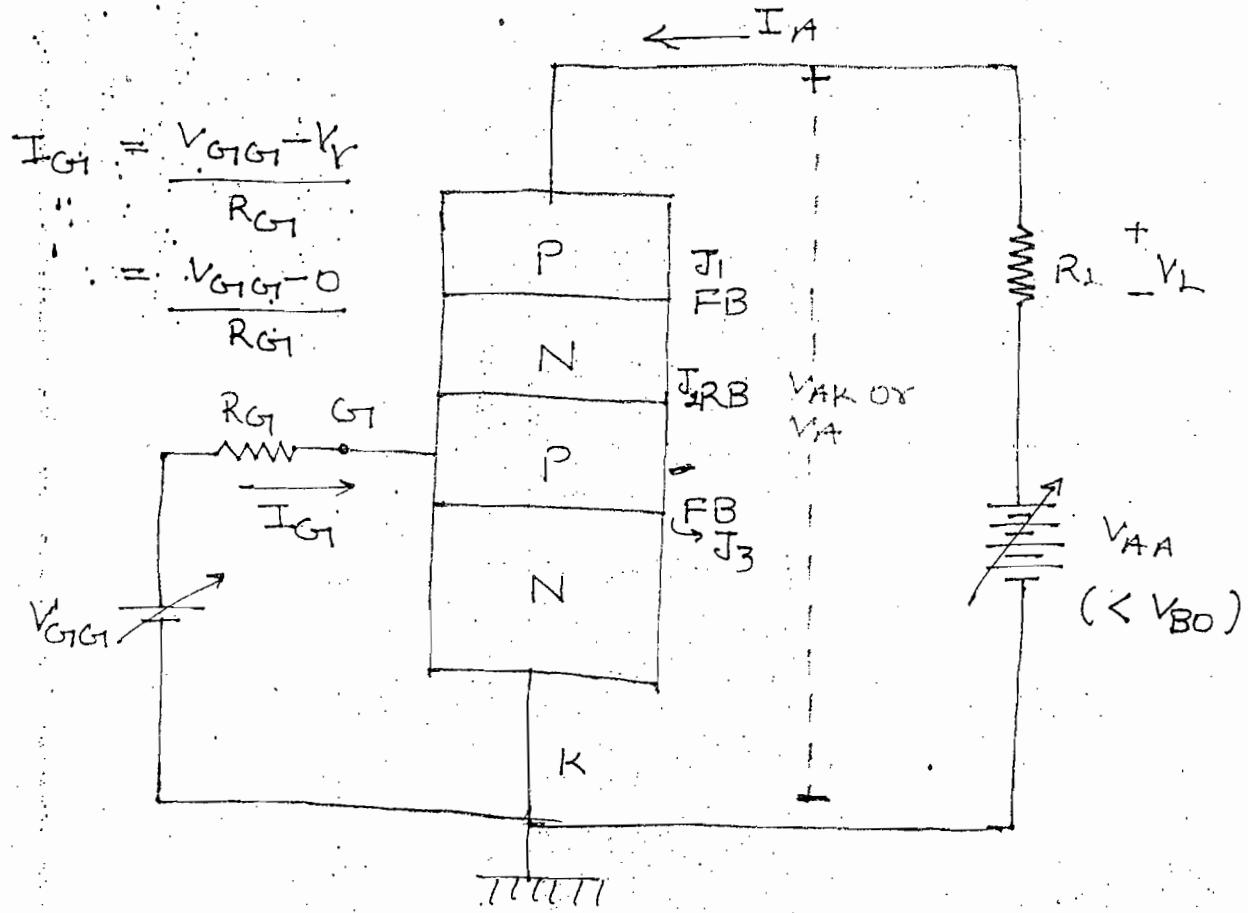
When anode supplied voltage is equal to breakdown voltage of the SCR, the junction J_2 enter into breakdown and a large current flows into the SCR and SCR is in the ON state.

→ The SCR can be switched OFF by reducing anode supply voltage so that anode voltage falls below the holding voltage V_H and SCR will be automatically OFF.

→ The main disadvantage of voltage operation is we can't operate the SCR we require anode supplied voltage which is equal to breakdown voltage of the device.

Current Operation of SCR :-

- Also called gate operation of SCR
- Current operation is more popular than voltage operation of SCR



Let \$V_{AA} < V_{BO}\$ & Let \$I_{GG}\$ is kept zero :-

In the OFF state of SCR :-

- (I) Junctions \$J_1\$ & \$J_3\$ are FB & \$J_2\$ is RB
- (II) Internal resistance of SCR is very large (\$\geq 1M\Omega\$)
- (III) Anode current (\$I_A\$) is zero
- (IV) Load voltage \$V_L = 0\$ bec. \$V_L = I_A R_L\$
\$\& I_A = 0\$
- (V) The voltage drop across the SCR is ~~\$V_{AK}\$~~
i.e. \$V_{AK}\$ is very large & \$V_A \equiv V_{AA}\$
- (VI) Power delivered to load i.e. \$P_L = 0\$
- (VII) Internal power consumption by SCR i.e. \$P_S = 0\$

→ The function of the gate is to trigger the SCR so that the SCR is fired.

Let $V_{AA} < V_{BO}$ & Let I_{Gt} is applied & SCR goes to ON state! -

In the ON State of SCR :-

- (I) Junctions J_1 , J_2 & J_3 are FB
- (II) Internal resistance of SCR suddenly reduce from ($> 1M\Omega$) to a smaller value ($< 1\Omega$)
- (III) Anode current (I_A) suddenly \uparrow to a very larger value
- (IV) Load voltage is very large ($V_L \approx V_{AA}$)
- (V) The voltage drop across the SCR i.e. V_{AK} suddenly decreases from a very large value to a value < 1 volt
- (VI) Power delivered to load is very large.
 $(P_L \rightarrow \text{large})$
- (VII) Internal power consumed by SCR (P_S) is small

→ Once SCR is fired, the anode current suddenly inc from 0 to a very larger value and at the same instant of time the anode to cathode voltage of SCR suddenly dec from a very larger value to less than 1V.

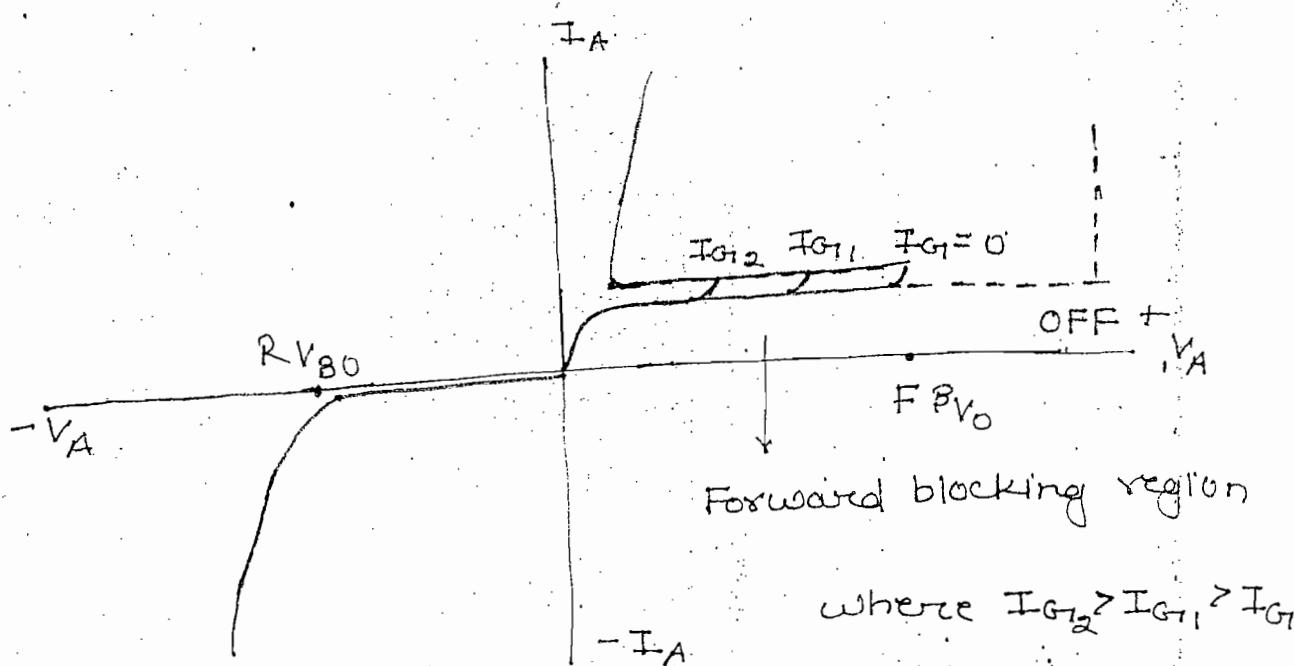
→ SCR is not a negative resistance device & there is no \downarrow ve resistance in the device bcc as current is increasing, voltage will be decreasing is at the same instant of time

→ The function of the gate is to trigger the SCR so that SCR will fire and once SCR is fired, the gate terminal will be loosing its total control on the SCR and also on the anode current.

Ques:- In a conducting SCR, if the gate current is suddenly reduced to zero, the SCR will be in ON state.

- If An SCR is bigger with a gate current of $1mA$ to get anode current of $80A$. If gate current is now doubled then anode current of SCR is $80A$.
- The SCR can be switched off with anyone of the following three methods:-
- (i) Disconnect the power supply i.e V_{AA}
 - (ii) Give a -ve anode voltage w.r.t cathode.
 - (iii) By reducing anode supply voltage, the anode current gradually dec. and will fall below a value of current called holding current (I_H) and the SCR will be automatically switched off and this method is called Low current knock out technique.
- Once SCR is OFF, the gate terminal will be regain its control on the device.
- When anode current falls below the holding current and it will remain for a minimum interval of time called gate recovery time and then SCR will be switched OFF.
- The firing voltage of the SCR $\propto \frac{1}{I_G}$
- By applying larger gate current, we can fire the SCR to a smaller anode supply voltages.
- The main advantage of current operation is we can fire the SCR with a anode supply voltage much less than breakover voltage by applying larger gate current.

VI Characteristics of SCR



→ Forward blocking region is also called OFF state

Holding current:-

Holding current is defined as the minimum anode current required to hold the SCR in its ON state.

Latching current:-

It is the minimum anode current required in the SCR of the removing the gate current so that SCR will be remain in the ON state.

NOTE!:-

In a conducting SCR always holding current is less than latching current.

Turn ON Time:-

It is the time required for the SCR to shift from OFF state to ON state.

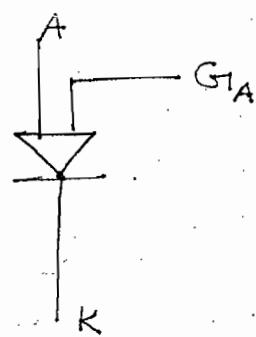
→ Turn ON Time increases with temperature

Turn OFF Time :-

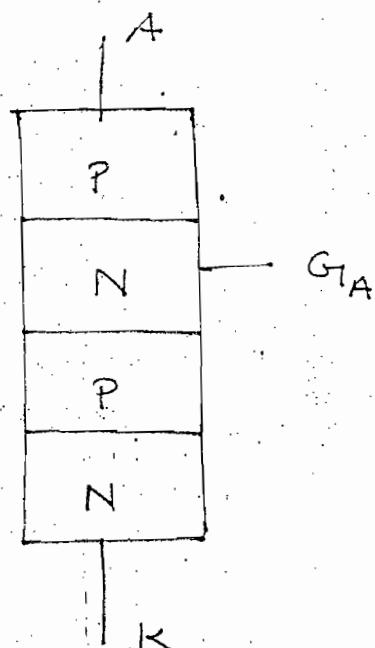
- Time taken by the SCR to shift the ON state to OFF state
- Turn OFF time increase with temperature

Silicon Unilateral switch (SUS) :-

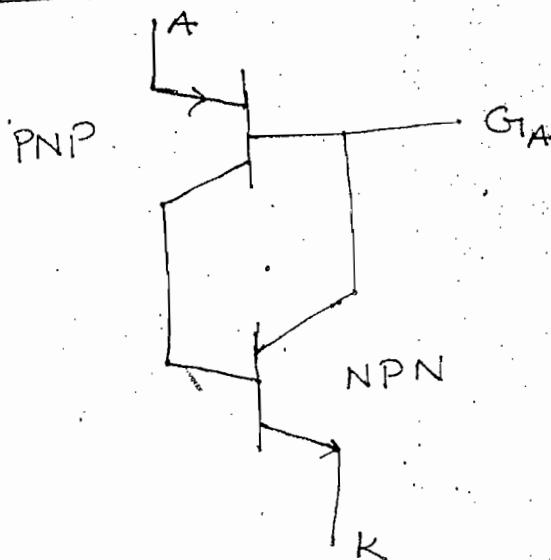
Symbol :-



Structure :-



Equivalent circuit :-



- Three terminal device having cathode, anode and gate
- Four layer solid state device with three junction
- Unidirectional device

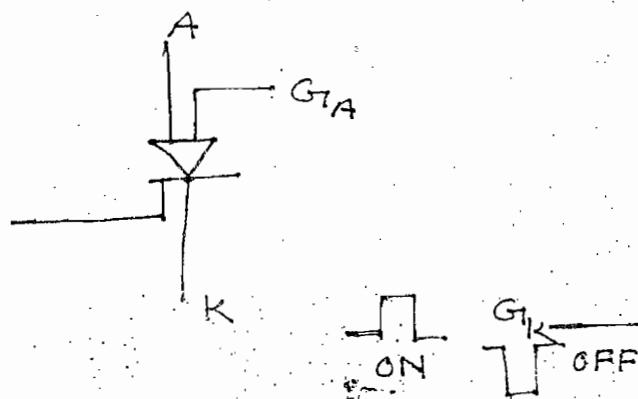
- Current operation is more popular
- Equivalent circuit is given by a transistor latch
- Gate is made up of n-material
- Normal SCR is +ve trigger but SCS is -ve trigger
- Popularly known as complementary SCR denotes as CSCR
- characteristics is similar to SCR

Application:-

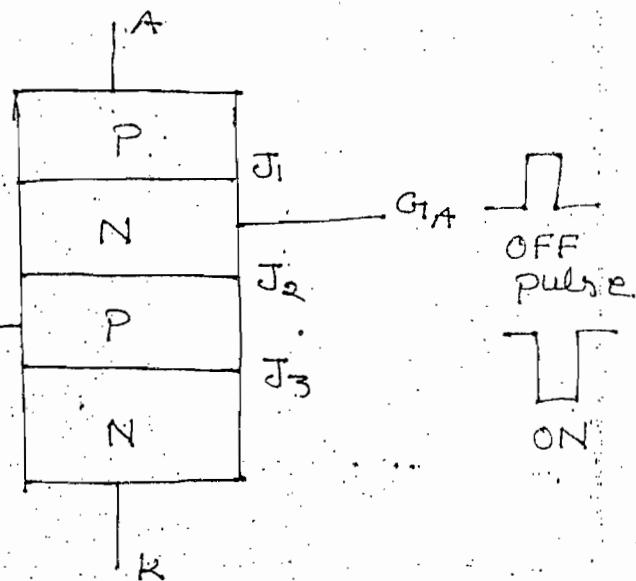
- Relaxation oscillators
- PUT (Programmable unijunction transistor)

Silicon controlled switch (SCS) :-

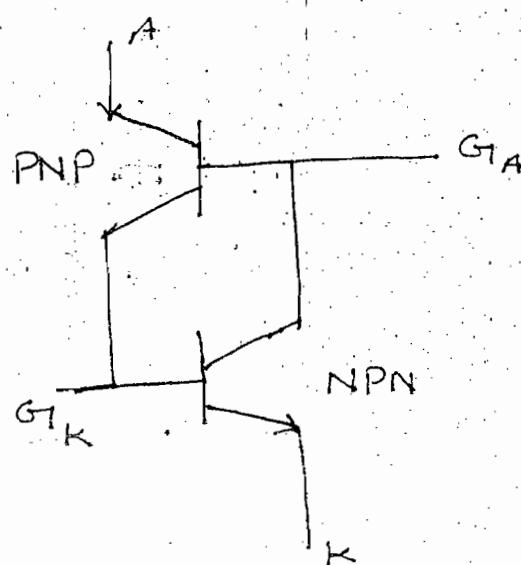
Symbol



Structure



Equivalent circuit :-

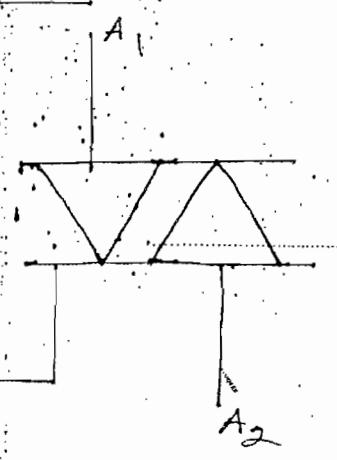


- Four terminal device (anode, cathode & two gate)
- Four layer solid state device with three junctions
- Uni-directional device
- Current operation is more popular
- Equivalent circuit is given by transistor latch.
- Characteristic and application is similar to SCR.
- SCS is also called An "SCR with two gate" or "Low current SCR with 2-gates" or Low current SCR with additional gate
- SCS can be operated with either gate terminal and with either pulse.

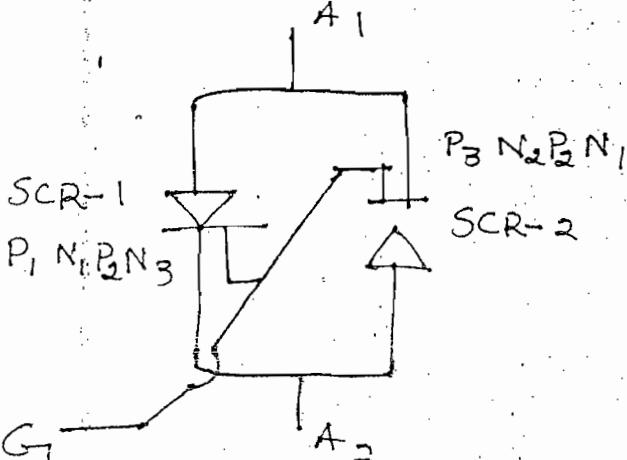
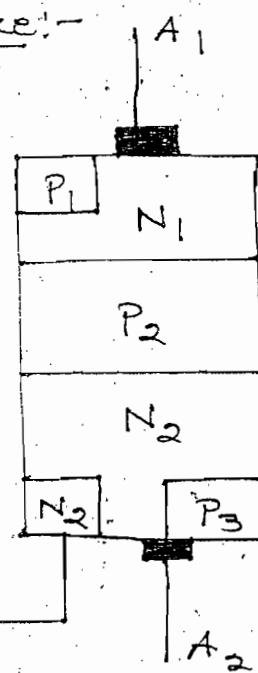
TRIAC (TRI-AC) :-

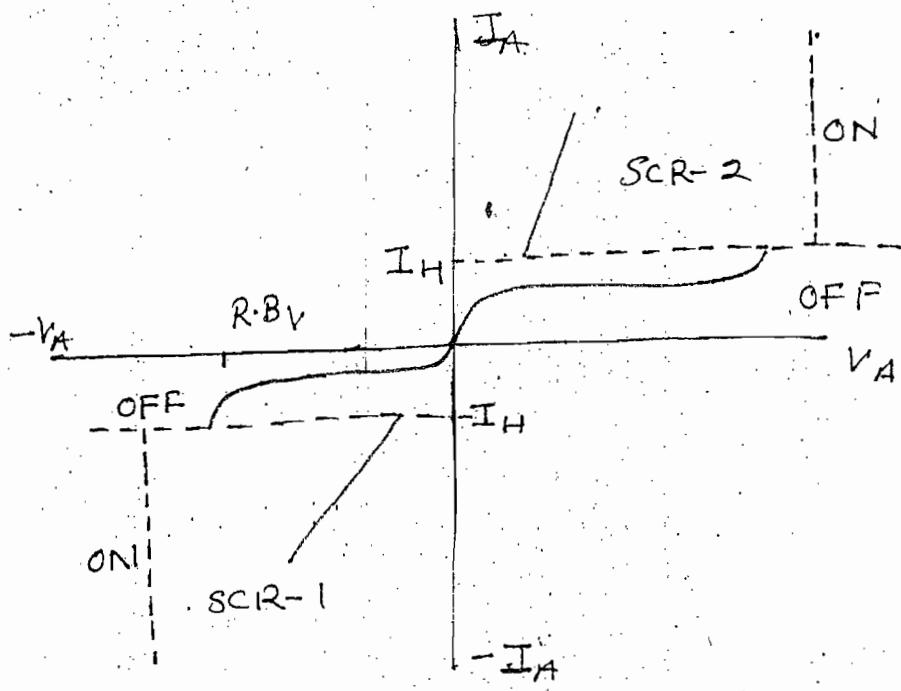
- Means three terminal AC switch

Symbol :-



Structure :-

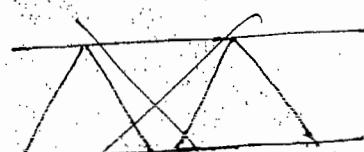




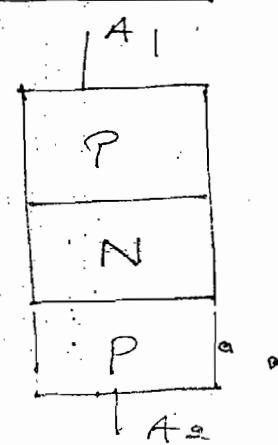
- Three terminal device having anode-1, anode-2 and common gate
- Bidirectional device
- Popularly known as dual SCR
- TRIAC internally consists of 2-SCR in anti-parallel
- Five layer solid state device
- characteristic similar to SCR but reflected in 1st and IIIrd quadrant
- SCR is a d.c switch and TRIAC is A.C switch
- TRIAC is used for speed control of AC motors
- TRIAC is used in designing of inverter circuit

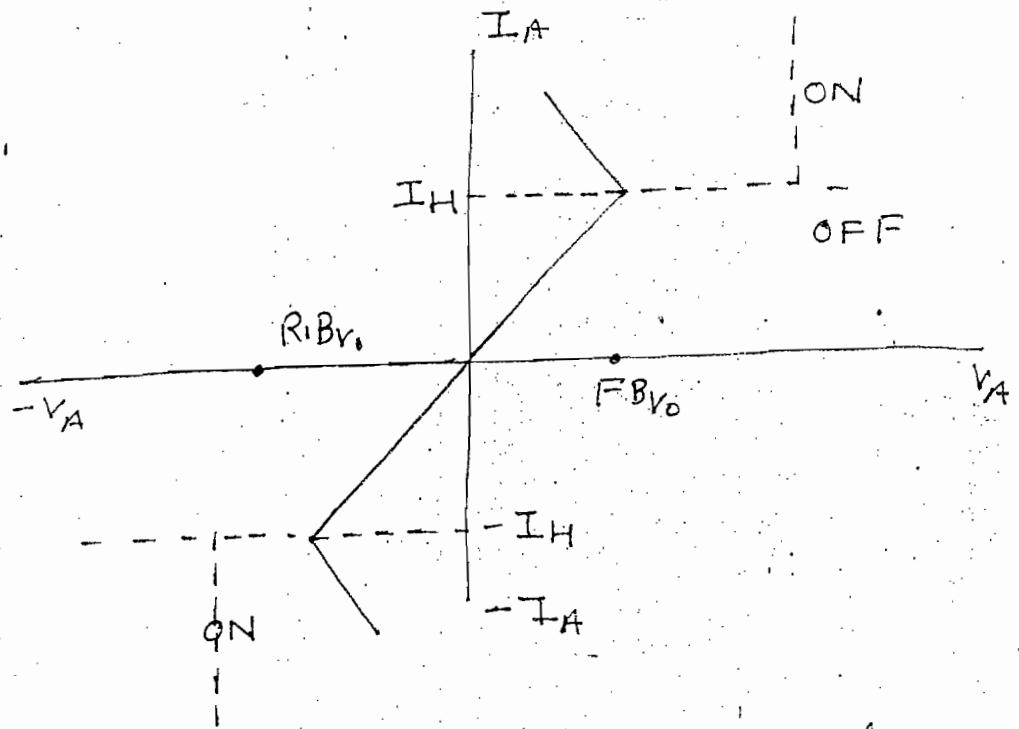
DIAC (DI-AC) :-

Symbol :-

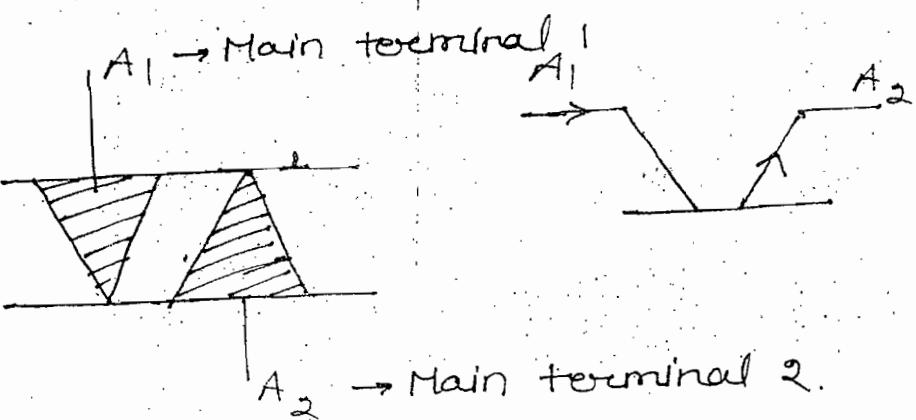


Structure :-





Symbol:-



- Two terminal device
- Bi-directional device, only voltage operated device
- Three layer solid state device
- Major application of DIAC is to trigger the SCR

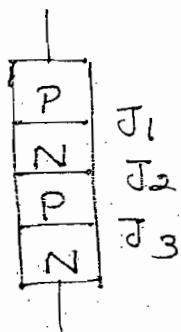
PNPN Diode / Shockley Diode / 4 layer Diode:-

Symbol:-



Structure:-

→ Unidirectional device.

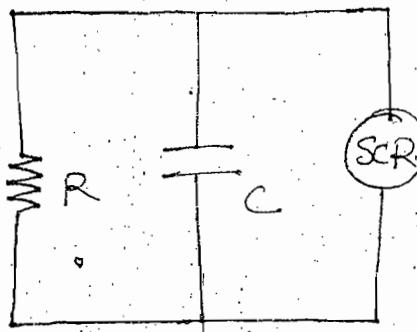


Snubber Circuit :-

It is used to protect the SCR against breakdown.

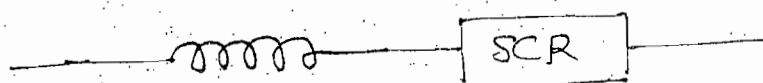
Voltage Snubber Circuit :-

- It is used to protect the SCR against high $\frac{dv}{dt}$ rating and it is done by using a resistor and capacitor in parallel with SCR.



Current Snubber circuit :-

- It is used to protect the SCR against high $\frac{di}{dt}$ rating and it is done by connecting the inductor in the series with SCR.



$\frac{di}{dt} \rightarrow$ Anode current / forward current

Field Effect Transistor (FET) :-

- The operation of the device depends on electric field intensity produced in the channel.
- Voltage controlled device (VCS)
- High i/p resistance device ($\geq 1M\Omega$)
- Power dissipation is very small
- In most of the measuring instrument, FET is connected on the i/p side to offer larger i/p resistance
- Unipolar device
- Majority carrier device
- No minority carriers
- Less noise device than BJT, due to absence of minority carriers
- No leakage current and therefore temperature effect on the device is very less and therefore excellent thermal stability
- FET having higher thermal stability than BJT
- Fabricated only with Si
- Offset voltage is zero
- FET can be used as a excellent signal chopper and this is due to zero offset voltage
- Offers a larger bandwidth and therefore reproduction of i/p signal is excellent
- Gain bandwidth product is a constant
- Gain bandwidth product of BJT is greater than the gain bandwidth product of FET
- Gain is more in BJT than FET
- When compare to BJT, FET is small in size and easier to fabricated.

Disadvantage:-

- Smaller Gain
- Smaller Gainbandwidth product.

Source:-

Region of FET:-

It is the source of majority carriers (inlet)

Drain:-

It draws of majority carriers (outlet)

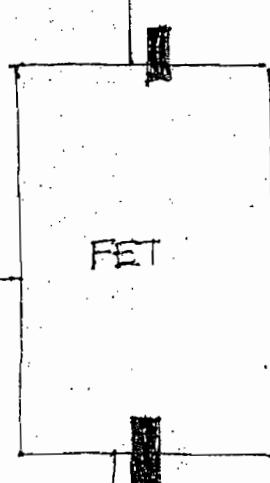
Gate:-

It is the terminal which control the majority carriers moving from source to drain or indirectly controlled the drain current

Channel:-

It is the region b/w the two gates
Drain (outlet)

Drain currents denotes
on the number of
majority carriers
reaching the gate
drain

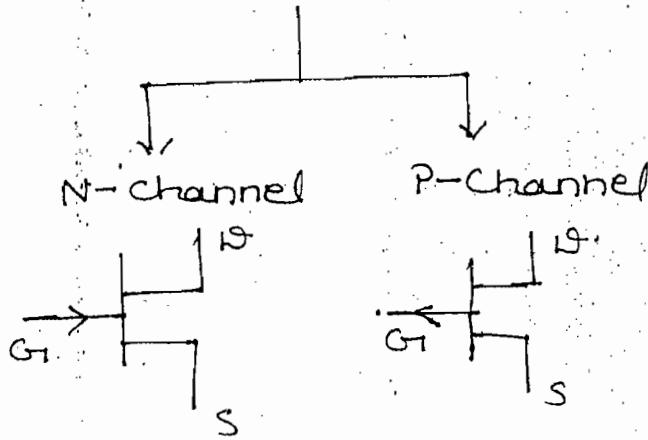


Source (inlet)

FET

JFET

- 3-terminal device
- $R_i = 10^6$ to $10^8 \Omega$



Metal oxide semiconductor FET

OR

IGFET → Insulated Gate FET

OR

MOST → Metal oxide semiconductor transistor

OR

Metal oxide silicon transistor

- 4-channel device (S, G_1, S , substrate)

$$\rightarrow R_i = 10^{10} \text{ to } 10^{15} \Omega$$

- Highest I/P resistance device is MOSFET

Depletion MOSFET (N-MOS)

- There is a pre-existing channel

- Suitable to operate in the depletion mode and enhancement mode (NE-MOSFET)

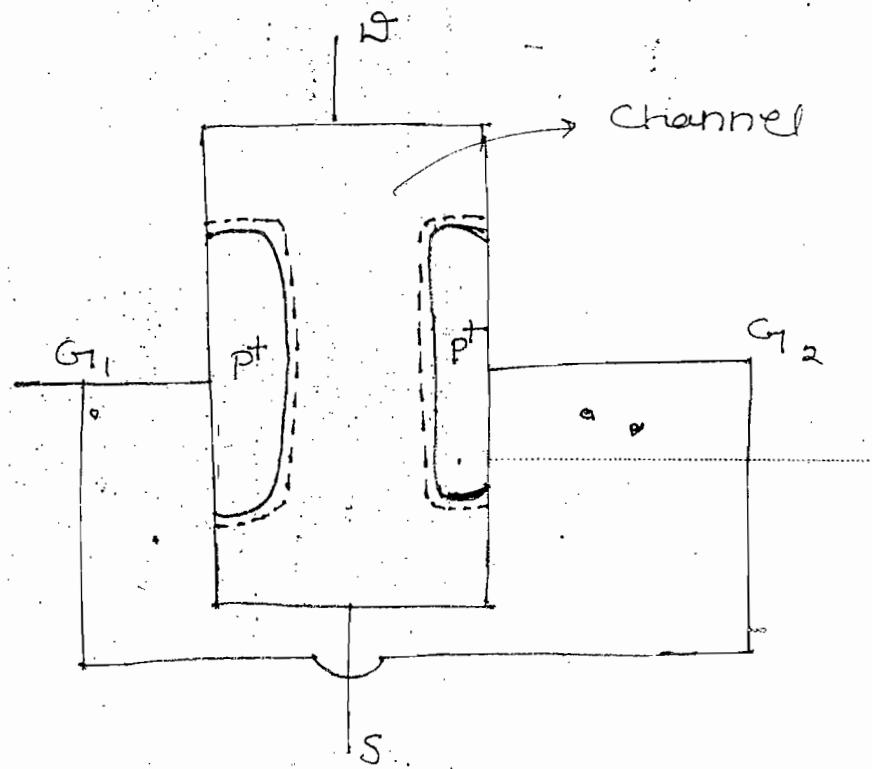
Enhance MOSFET (E-MOS)

- No pre-existing channel

- Suitable to operate in the enhancement mode (E only MOSFET)

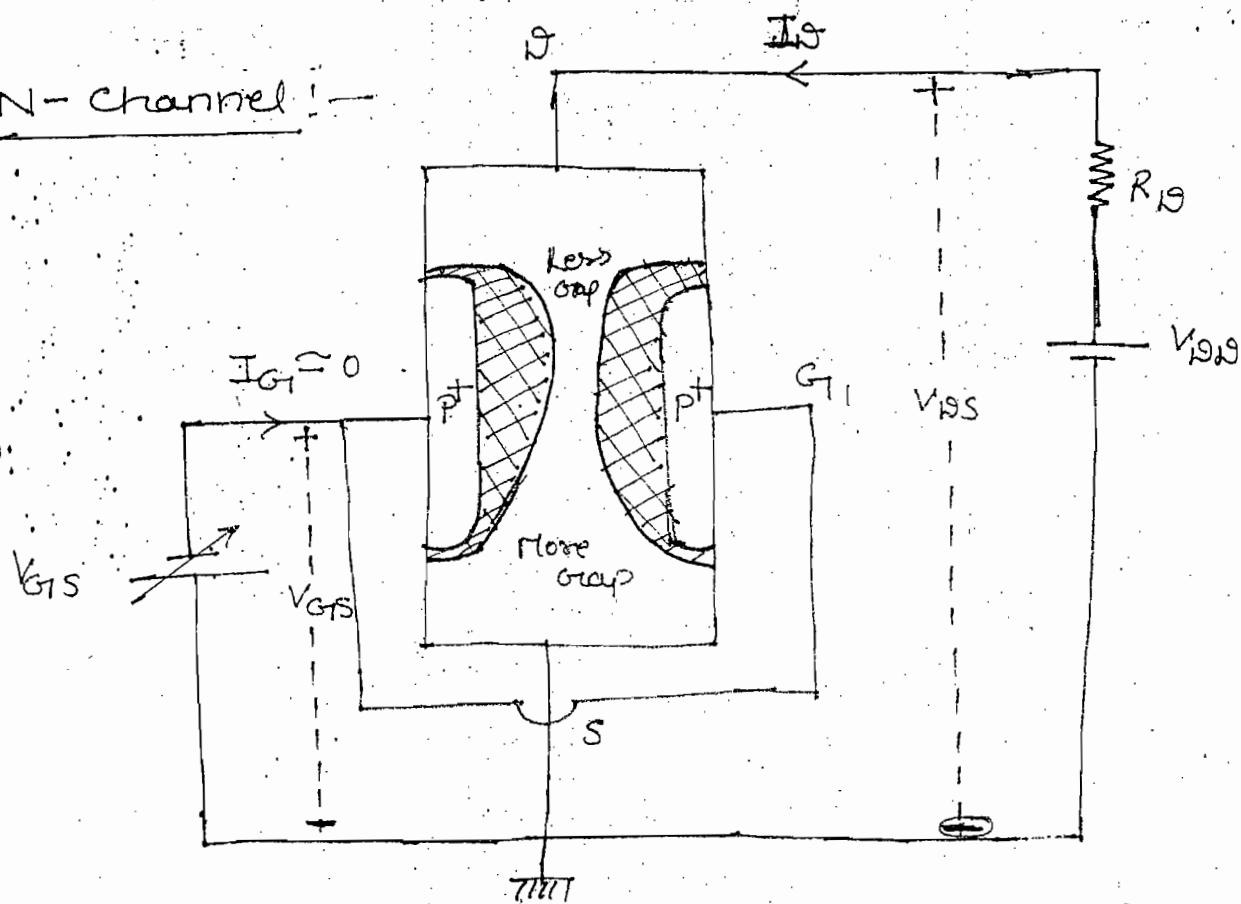
- Input resistance of MOSFET > Input resistance of JFET
- Power dissipation is less < Power dissipation in JFET
- FET is better device as an amplifier when compare to BJT
- BJT is asymmetrical device and therefore emitter and collector terminals cannot be interchange practically.
- FET is a symmetrical device and therefore source and drain terminal can be changed practically.

N - Channel JFET :—

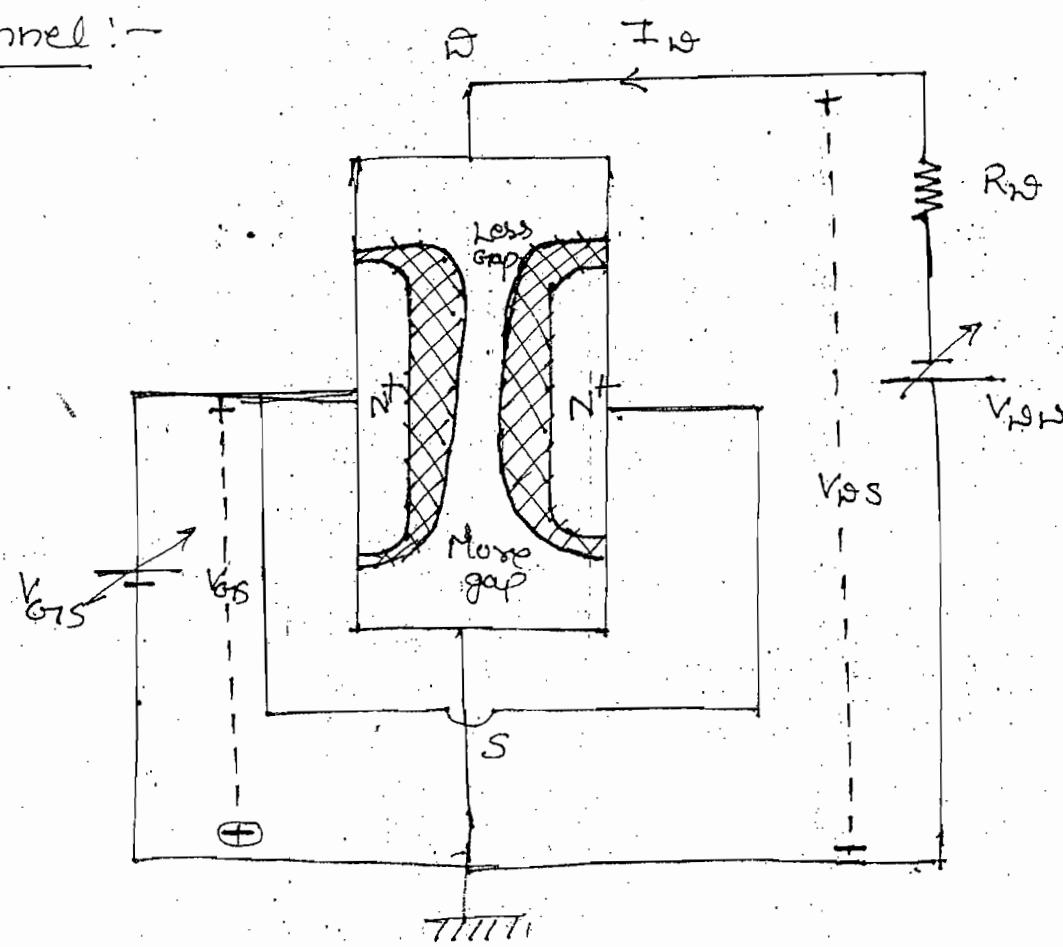


- When JFET is open-circuited, channel cross sectional area is maximum and therefore channel current density is minimum
- JFET is a symmetrical device

N-channel :-



P-channel :-



- In JFET when V_{GS} is applied channel width decreases
- In JFET, when V_{GS} is applied, the channel cross-sectional area decreases and channel current density increases
- In JFET, channel is wedge shaped
- Channel width is narrow near the drain
- Depletion layers will penetrate more into the channel near the drain
- In JFET, gate to source is always operated under reverse bias
- Magnitude of gate leakage current is in nA and it is neglected
- The larger i/p resistance is due to
 - Reverse biasing gate to source junction
 - due to negligible gate leakage current

$$R_i = \left| \frac{V_{GS}}{I_s} \right|$$

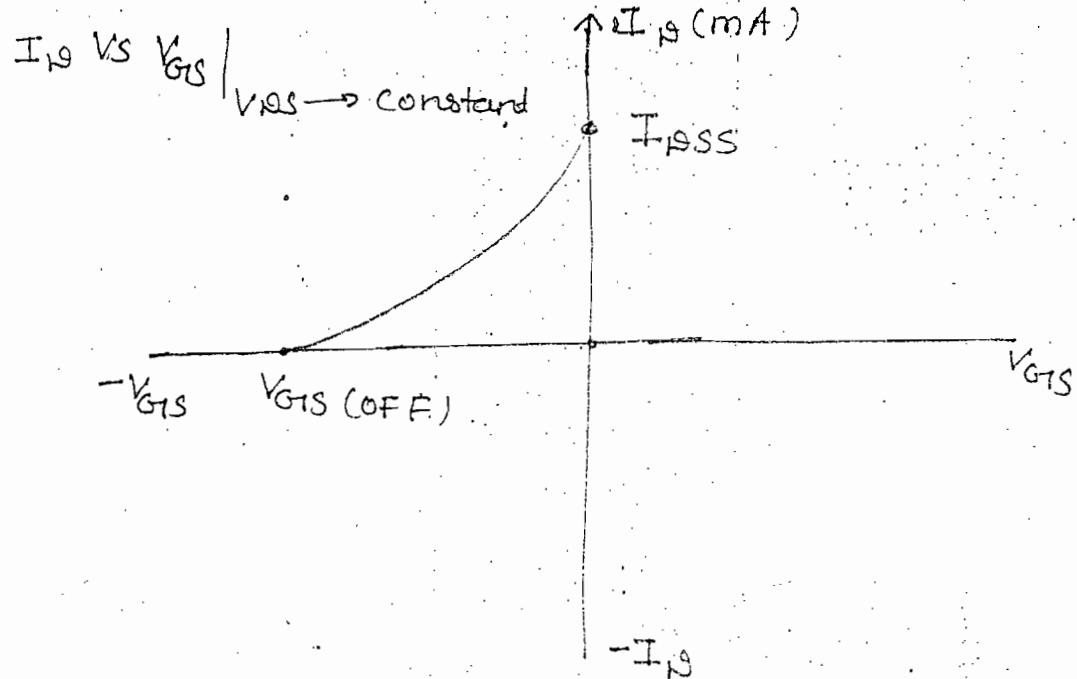
- In FET, i/p characteristic cannot be plotted because there is no i/p current (i.e. gate current)
- In n-channel JFET, gate voltage is -ve.
- In p-channel JFET, gate voltage is +ve.
- In JFET, gate to source is FB and we get following disadvantages
 - Larger gate current source
 - Power dissipation increases
 - i/p resistance will become very small (below 100Ω)

NOTE:-

Hence in JFET, Gate to source should not be operated under forward bias.

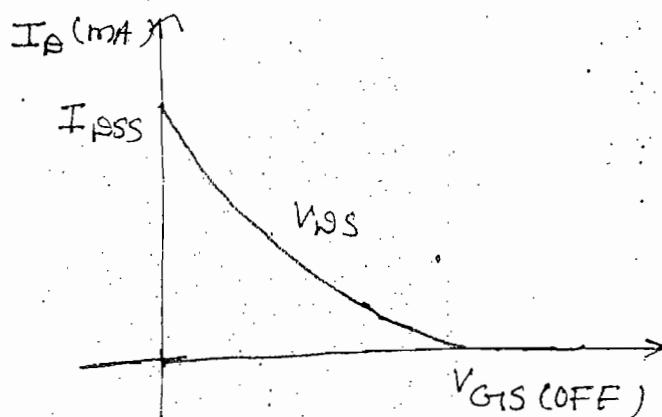
Step-I :-

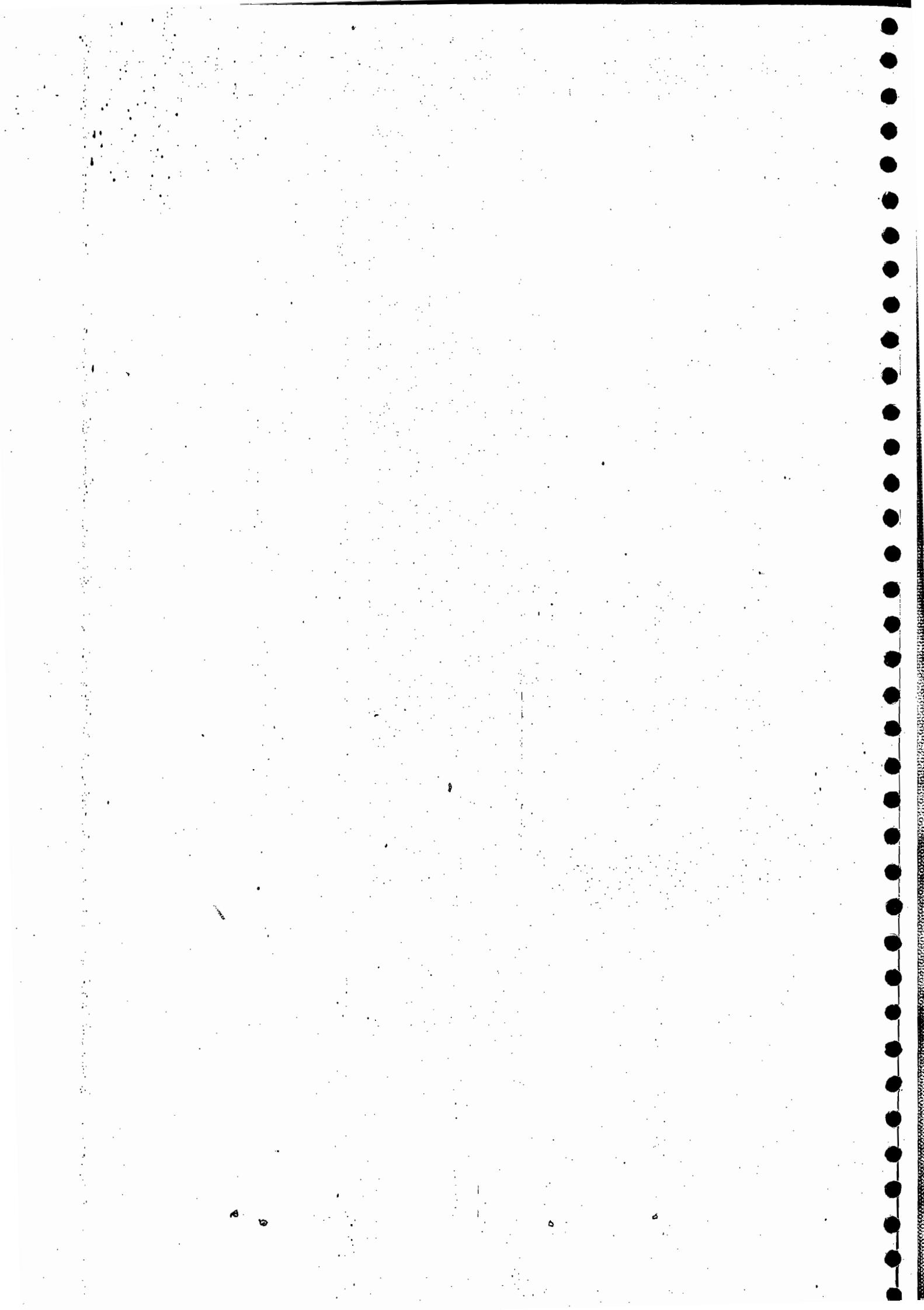
Keeping V_{DS} constant and varying V_{GS} in n-channel.



- In JFET, the max. drain current is I_{DSS} .
- I_{DSS} is drain to source safe current or drain to source saturation current.
- In JFET, $I_D = I_{DSS}$ when $V_{GS} = 0$
- The concentration of majority carriers in the channel depends on
 - Cross-sectional area of the channel.
 - Doping conc. of the channel.
- In n-channel JFET, if gate is given more +ve voltage then I_D decreases
- In JFET, if gate to source is more R_B then
 - The depletion layer penetrate more into the channel and reduces the channel width
 - Less majority carrier will be reaching the drain and I_D will be decrease

- The minimum gate to source voltage required to cutoff the channel or to reduce the drain current to zero is called $V_{GS}(\text{cut-off})$ or $V_{GS}(\text{OFF})$
- The process where the channel width can be altered by vary gate to source voltage is called channel width modulation.
- Channel width modulation occurs in JFET and MOSFET
- Channel width modulation is similar to base width modulation or early effect in BJT
- The transfer characteristics of p-channel JFET is given below! —



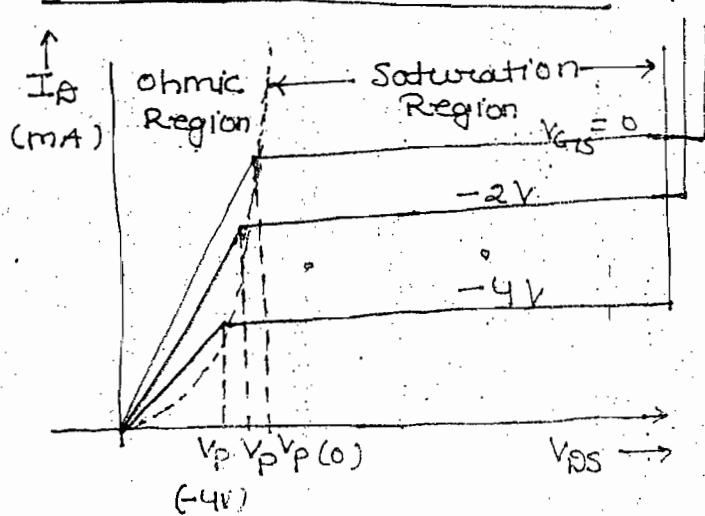


Lecture -19

Step-(II) :-

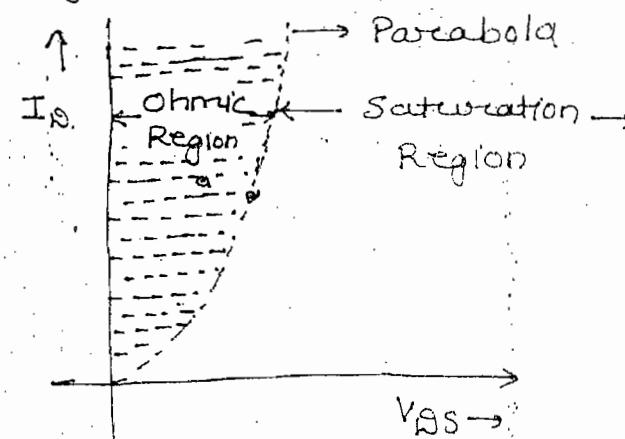
Keeping V_{GS} constant and varying V_{DS} :-

Output Characteristics :-



Breakdown Region

Region



- Drain characteristics of FET is also called constant current characteristics (and they are similar to collector characteristics of common base transistor)
- FET can work as a current source
- FET is voltage controlled current source (V_{GDS})
- Common base transistor is current controlled current source (CCCS)
- In FET breakdown is due to Avalanche effect
- In FET breakdown is b/w drain and gate junction
- It is operated under reverse bias
- In the ohmic region, FET will work as a linear device i.e. a resistor
- In the ohmic region, FET will work as voltage variable resistor (VVR) or voltage dependent resistor (VDR)
- In the ohmic region, FET will work as VVR by varying gate to source (V_{GS}) voltage
- In JFET, channel behave as a resistor
- Saturation region is also called current saturation or pinch off region

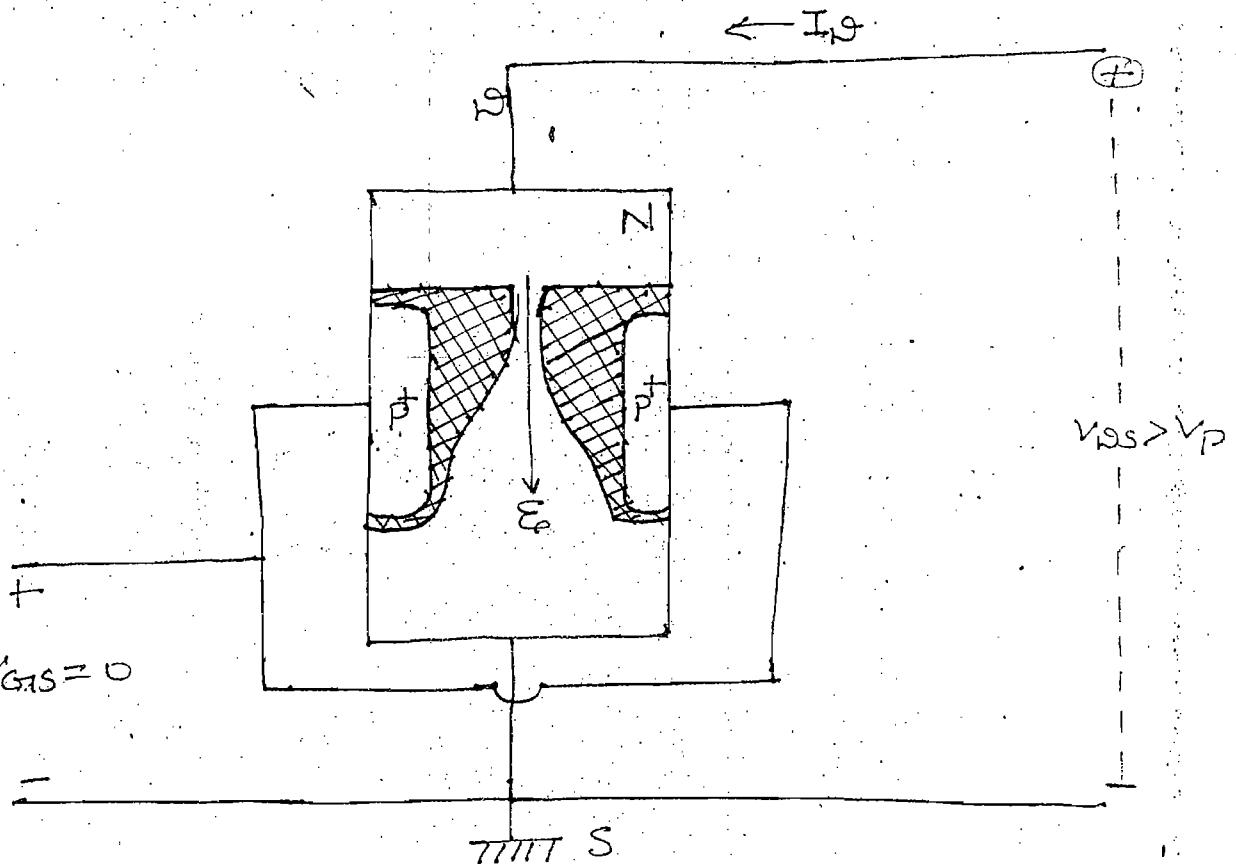
- In the saturation region, FET will be working as.
 - (i) Excellent Amplifier
 - (ii) ON switch
- FET is generally operated in the saturation region
- In the pinch off region as V_{DS} is increases, the drain current will remain almost a constant.
- FET is generally operated with
 - (a) $V_{DS} = V_p$
 - (b) $V_{DS} > V_p$
 - (c) $V_{DS} < V_p$
 - (d) $V_{DS} \gg V_p$

Pinch - OFF Voltage (V_p):-

- Pinch off voltage is define as the minimum drain to source (V_{DS}) voltage where I_D enters into the saturation or where I_D levels off.
- Pinch off voltage (V_p) is a function of V_{GS}
- In JFET maximum V_p is $V_p(0)$ or V_{po}
- Max. pinch-off voltage occurs when $V_{GS} = 0$
- When V_{GS} is applied, pinch-off voltage is reduced
- The locus of the pinch-off voltage corresponds to a parabola

Swing Pinch-off:-

- During the pinch-off, as $V_{DS} > V_p$, upper end of the channel will become more the and P^+N junctions will become more reverse bias and depletion layer will be penetrating more into the channel. The two depletion layer will becoming extremely closer to

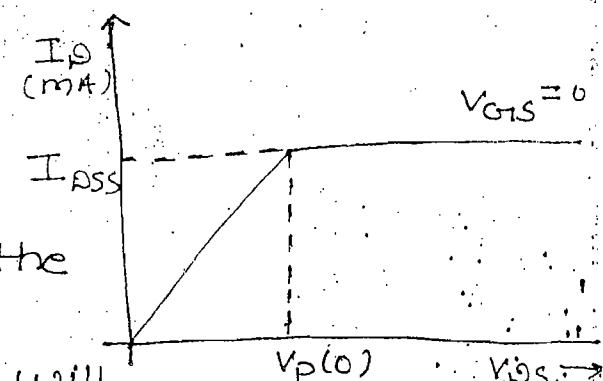


touch each other but

during the pinch off
the two depletion layer
can't touch each other

→ Since upper end of the channel is more tre,
electric field intensity will
become larger and it is pointing towards
the source. The field intensity will extend
over the entire length of the channel and
due to this field intensity the two depletion
layers are separated and they can't touch
each other (or the field intensity is preventing
the depletion layers from touching to each
other)

→ During pinch-off, channel width will become
very narrow but due to the higher velocity
of the e's in the channel, the channel e's
will be moving to the narrow channel width
and reaching the drain with the higher velocity

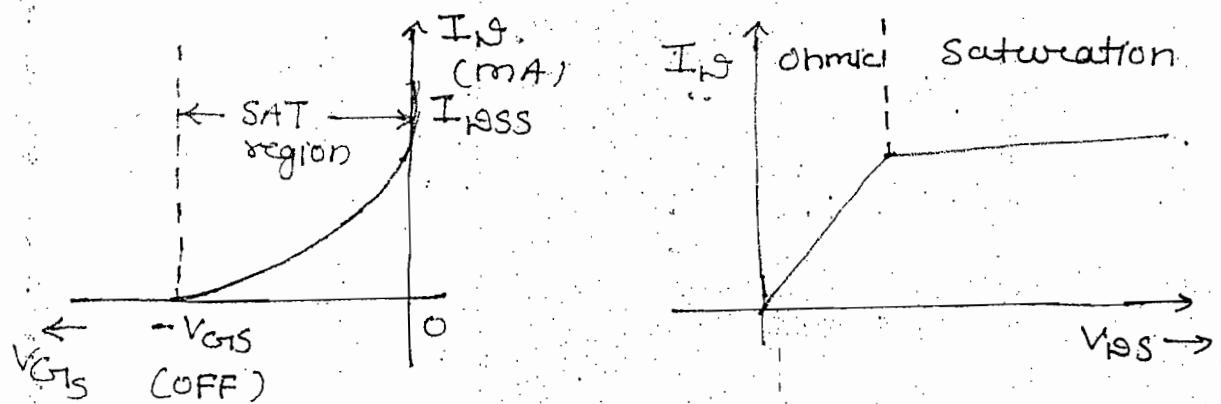


The drain is now receiving max. E's from the channel and therefore the drain current will remain almost a constant in the saturation region.

Equation for Drain Current:

In the saturation region of FET

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$



- FET is a square law device
- In JFET, I_D dec. as a parabolic variations with V_{GS}
- Transfer characteristics are plotted only for saturation region
- Drain characteristics are plotted for ohmic region and saturation region
- I_D is a majority carrier current
- I_D slightly decreases with the temperature
- As temperature increases, majority carrier conc. will remain independent of temperature but mobility of charge carriers decreases and therefore I_D slightly decreases with the temperature
- For 1°C , I_D decreases by 0.7%

→ FET is having excellent thermal stability and this is due to

(i) the absence of leakage current

(ii) As temperature \uparrow $I_S \downarrow$

→ I_S is a drift current because this current will be passing through the channel under the influence of electric field intensity

Equation for Gate to source voltage (V_{GSS}):

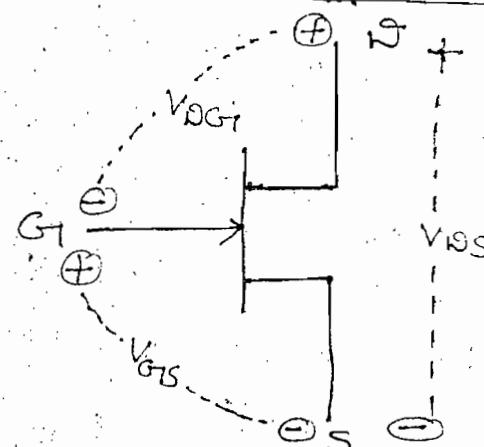
$$I_S = I_{BSS} \left[1 - \frac{V_{GSS}}{V_P} \right]^2$$

$$\Rightarrow 1 - \frac{V_{GSS}}{V_P} = \sqrt{\frac{I_S}{I_{BSS}}}$$

$$\Rightarrow V_{GSS} = V_P \left[1 - \sqrt{\frac{I_S}{I_{BSS}}} \right]$$

Relationship b/w terminal voltages of FET

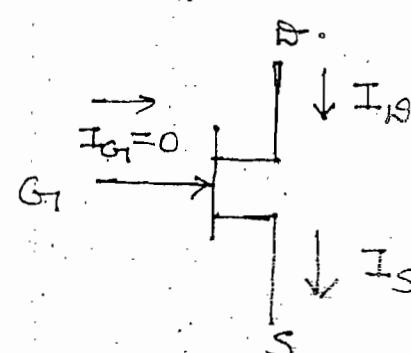
$$V_{DS} = V_{SG} + V_{GS}$$



Source Current (I_S)

In magnitude

$$I_S = I_D$$



FET Parameters:-

→ I_D is a function of V_{GS} & V_{DS}

(i) Output resistance:-

→ Internal resistance of FET.

$$r_d = \left| \frac{\Delta V_{DS}}{\Delta I_D} \right|_{V_{GS}}$$

$$r_d = 10 \text{ k}\Omega - 600 \text{ k}\Omega$$

$$\text{Typ.} = 500 \text{ k}\Omega$$

→ r_d is graphically obtained from drain characteristics and also from transfer characteristics.

(ii) Transconductance (g_m):-

→ mutual conductance

$$g_m = \left| \frac{\partial I_D}{\partial V_{GS}} \right|_{V_{DS}} \equiv \left| \frac{\Delta I_D}{\Delta V_{GS}} \right|_{V_{DS}}$$

→ $g_m = 0.1 \text{ ms}$ to $10 \text{ ms} \rightarrow \underline{\text{JFET}}$

= 0.1 ms to $20 \text{ ms} \rightarrow \underline{\text{MOSFET}}$

= 50 ms to $600 \text{ ms} \rightarrow \underline{\text{BJT}}$
↓
siemen

→ In any device or amplifier, gain A

$$|A| \propto g_m$$

→ Gain is large in BJT when compared to FET.

→ In FET, gain is small due to

(i) Larger Bandwidth

(ii) Smaller value of g_m

→ g_m is graphically obtained from transfer characteristics & also from drain characteristics

(III) Amplification factor (μ)

→ Also called voltage amplification factor

$$\boxed{\mu = - \left(\frac{\Delta V_{DS}}{\Delta V_{GS}} \right) |_{I_D}}$$

always +ve & $\mu = 2.5$ to 150

→ μ is the most important specification in the FET

→ μ indicates the max. voltage gain in the FET

→ In BJT, β is most important factor because it indicates max. current gain and it is current controlled device

→ μ is graphically obtained only from transfer characteristics

→ In FET, $\boxed{\mu = v_{sd} \times g_m}$

Derive an equation for transconductance in FET

→ In the saturation region of FET,

$$I_S = I_{SS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

By definition,

$$g_m = \frac{\partial I_S}{\partial V_{GS}}$$

$$\frac{\partial I_S}{\partial V_{GS}} = 2 I_{SS} \left[1 - \frac{V_{GS}}{V_P} \right] \left[-\frac{1}{V_P} \right]$$

$$\Rightarrow \boxed{g_m = - \frac{2 I_{SS}}{V_P} \left[1 - \frac{V_{GS}}{V_P} \right] - v}$$

Equations for g_m in the FET :-

In the saturation region of FET,

$$g_m = -\frac{2I_{DS}}{V_p} \left[1 - \frac{V_{GS}}{V_p} \right] \quad \text{---(1)}$$

From the equation of I_D

$$1 - \frac{V_{GS}}{V_p} = \sqrt{\frac{I_D}{I_{DS}}}$$

$$\Rightarrow g_m = -\frac{2I_{DS}}{V_p} \sqrt{\frac{I_D}{I_{DS}}}$$

$$\Rightarrow g_m = -\frac{2}{V_p} \sqrt{I_{DS} I_D}$$

$$\text{Let } I_D = I_{DS}$$

$$g_m = \frac{2}{|V_p|} \sqrt{I_{DS} \cdot I_{DS}}$$

In equation - (1), if V_{GS} is kept zero

$$g_m = -\frac{2I_{DS}}{V_p} \quad \text{---(2)}$$

$$g_{m0}$$

→ g_{m0} is the value of g_m when $V_{GS} = 0$

→ g_{m0} is the max. value of g_m in FET

In JFET, Max. g_m occurs when $V_{GS} = 0$

$$\boxed{\text{Max } g_m \text{ or } g_{m0} = -\frac{2I_{DS}}{V_p}} \quad \text{---(3)}$$

If $V_{GS} = 0$ then $V_p = V_{PO}$

$$\boxed{V_{PO} = -\frac{2I_{DS}}{g_{m0}}} \text{ volts}$$

$$g_m = g_{mo} \left[1 - \frac{V_{GDS}}{V_p} \right]$$

$$g_m = g_{mo} \sqrt{\frac{I_D}{I_{DSS}}}$$

Relationship b/w V_{GDS} (cut-off) and Pinch-off voltage:-

$$I_D = I_{DSS} \left[1 - \frac{V_{GDS}}{V_p} \right]^2$$

Let $V_{GDS} = V_p$ then $I_D = 0$

\downarrow
 V_{GDS} (off)

\downarrow
condition for cut-off

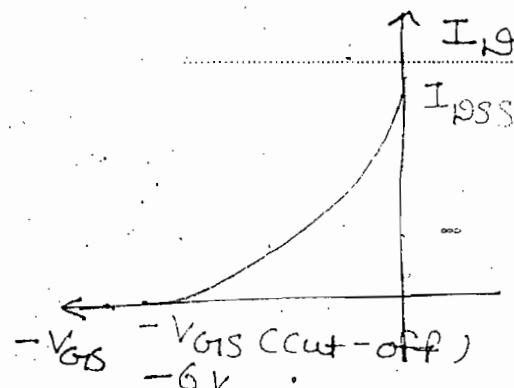
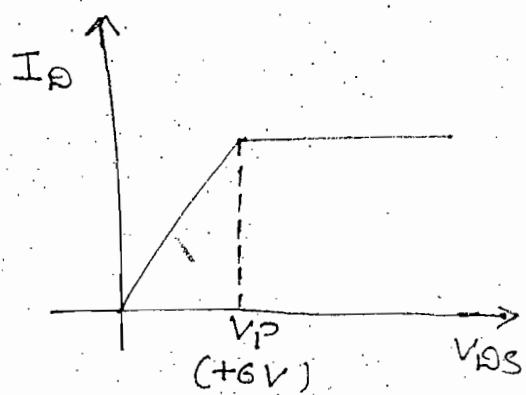
Hence

$$V_{GDS \text{ (cut-off)}} = V_p$$

In N-channel JFET

$$V_p = |V_{GDS \text{ (cut-off)}}|$$

are equal in magnitude



Approximate definition for V_p (Second definition)

- Pinch-off voltage V_p is also defined as the min. gate to source voltage (V_{GDS}) where I_D reduced to zero

Ques:- Pinch off voltage is defined as

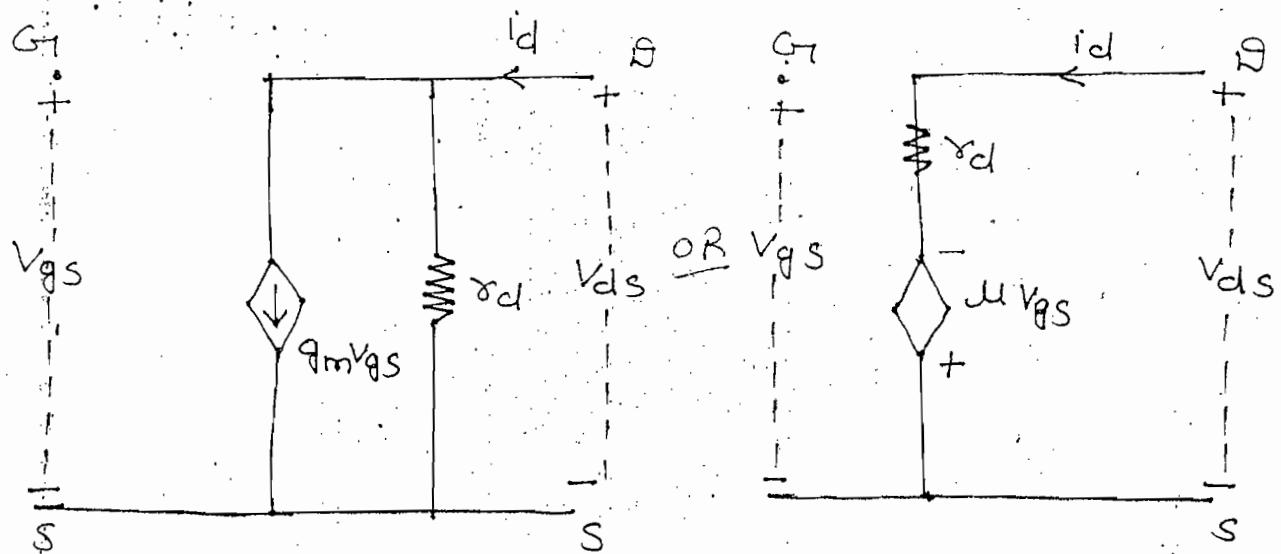
- (a) min. V_{GS} where $I_D = 0$
- (b) min. V_{GS} where $I_D = \text{max}$
- (c) min V_{GS} where $I_D = \text{max}$
- (d) min. V_{GS} where $I_D = 0$

Soln:- For multiple answers \rightarrow a, b, c

For single answer \rightarrow c

Equivalent circuit of FET (JFET & MOSFET) :-

\rightarrow Also called AC equivalent circuit of FET or small signal and low frequency equivalent circuit of FET



\rightarrow From the above circuit diagram we can calculate voltage gain and o/p resistance of FET amplifier

Internal equation of JFET:-

Considering the cross-sectional view of N-channel JFET

$L \rightarrow$ Length of the channel

$W \rightarrow$ Width of the silicon wafer

$x \rightarrow$ distance into the FET measured from the source end.

$2b(x)$ = channel width after the penetration of depletion layer and measured from the source end at the distance x into the JFET

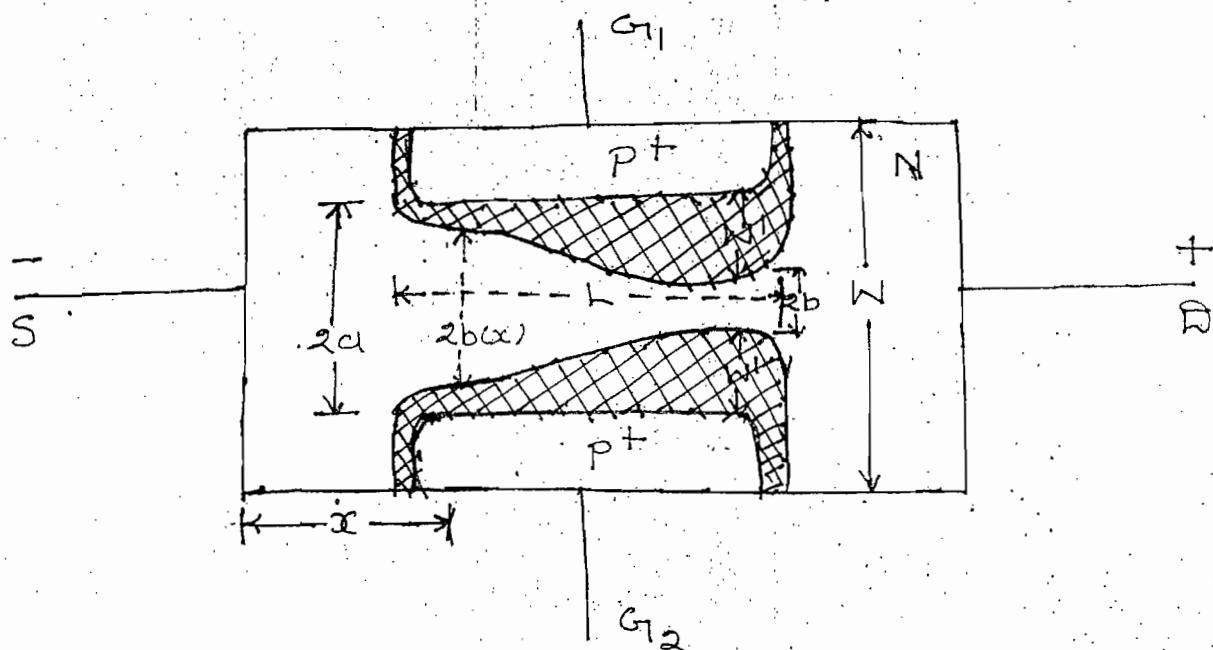
$2b$ = Min. channel width

w' = Max. penetration of depletion layer on each side

$$2b = 2a - 2w'$$

a = Actual channel width (i.e. before the penetration of depletion layers)

→ Half channel width



In N-channel JFET, pinch-off voltage (V_p)

$$V_p = \frac{q N_S a^2}{2\epsilon}$$

$$\epsilon = 11.7 \epsilon_0$$

N_S → doping conc. of N-channel in the N-channel JFET

→ V_p also called internal pinch-off voltage

→ In N-channel JFET the equation for drain current is

$$I_D = 2b \cdot q \cdot N_S \cdot \mu_n \cdot W \cdot \frac{V_{DS}}{L}$$

Let $2b \cdot W = A$ & $\frac{V_{DS}}{L} = \epsilon$

$$I_D = AqN_S\mu_n\epsilon$$

$$I_D \propto A$$

$$I_D \propto N_S$$

$$I_D \propto V_{DS}$$

$I_D \propto \epsilon \rightarrow$ Hence called drift current

$$I_D \propto \frac{W}{L}$$

$$I_D \propto \mu_n$$

as $T \uparrow \mu_n \downarrow$

$\therefore I_D \downarrow$ with temperature

Drain to Source resistance r_{ds}

$$r_{ds} = \frac{V_{DS}}{I_D}$$

→ r_{ds} ON

→ channel resistance

$$r_{ds} = \frac{L}{2bqN_S\mu_nW} \Omega$$

$$r_{ds} \propto \frac{L}{W}$$

In N-channel JFET

$$V_{GDS} = \left(1 - \frac{b}{a}\right)^2 V_P$$

?

$$b = a \left[1 - \left(\frac{V_{GDS}}{V_P} \right)^{\frac{1}{2}} \right]$$

Relationship b/w I_S & Temperature:-

In FET,

$$I_S \propto \frac{1}{T^{3/2}}$$

Ques:- In FET, if gate is short circuited to the source, the saturation current of the JFET get doubled when the temperature will be changed by the factor.

- (a) $(\frac{1}{2})^{1/3}$ (b) $(\frac{1}{2})^{3/2}$ (c) $(\frac{1}{4})^{1/3}$ (d) $(\frac{1}{8})^{3/2}$

Soln:- Gate is SC to S i.e. $V_{GSS} = 0$.

If $V_{GSS} = 0$ then $I_S = I_{DSS}$

$$\text{As } I_S \propto \frac{1}{T^{3/2}}$$

$$\text{Hence } I_{DSS} \propto \frac{1}{T^{3/2}}$$

$$\text{Now } \frac{I_{DSS_1}}{I_{DSS_2}} = \left(\frac{T_2}{T_1}\right)^{3/2}$$

$$\text{But } I_{DSS_2} = 2I_{DSS_1}$$

$$\Rightarrow \frac{1}{2} = \left(\frac{T_2}{T_1}\right)^{3/2} \Rightarrow \frac{T_2}{T_1} = \left(\frac{1}{2}\right)^{2/3}$$

$$\Rightarrow \frac{T_2}{T_1} = \left(\frac{1}{4}\right)^{1/3}, \text{ Ans.}$$

Ques:- Consider a JFET, given with a sideview the doping level is 10^{20} cm^{-3} and mobility is $1500 \text{ cm}^2/\text{Vsec}$, the depletion width on each side is $0.25 \mu\text{m}$ the r_{ds} is _____

- (a) 2.8Ω (b) 0.139Ω (c) 0.93Ω
 (d) 28Ω

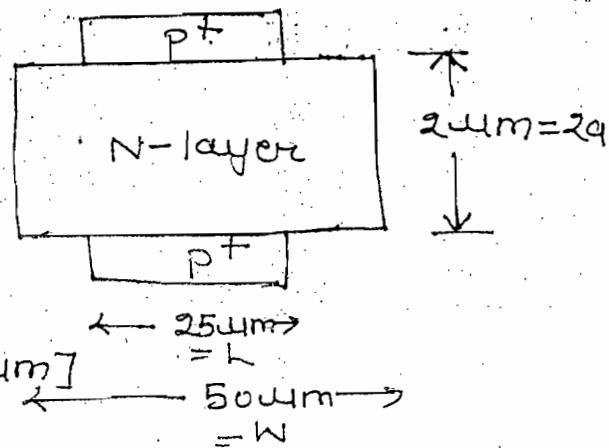
Soln:-

$$10^{20}/\text{cm}^3 \rightarrow N_S \rightarrow 10^{26}/\text{m}^3$$

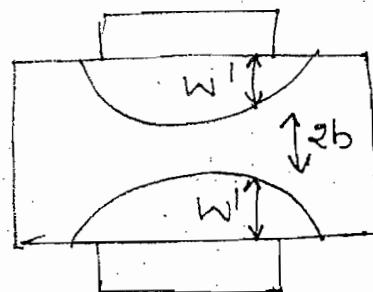
$$\begin{aligned} \mu_n &= 1500 \text{ cm}^2/\text{Vsec} \\ &= 0.15 \text{ m}^2/\text{Vsec} \end{aligned}$$

$$2b = 2a - 2w$$

$$\begin{aligned} &= 2\mu\text{m} - 2[0.25\mu\text{m}] \\ &= 1.5\mu\text{m} \end{aligned}$$



$$\begin{aligned} r_{ds} &= \frac{L}{2b \cdot N_S \mu_n W} \Omega \\ &= 0.139 \Omega \end{aligned}$$



Ques:- What is the max. voltage gain obtained from FET having $g_m = 5\text{ms}$ & $r_{ds} = 10\text{k}\Omega$

Soln:- Max. voltage gain in FET is ∞

$$\begin{aligned} \text{or } A_v &= r_{ds} \times g_m \\ &= 50 \end{aligned}$$

NOTE:-

In JFET, I_D is

$$I_D = I_{DSS} \left[1 - \frac{V_{GDS}}{V_P} \right]^2$$

where V_{GDS} & V_P must have same sign

OR

$$I_D = I_{DSS} \left[1 - \left| \frac{V_{GDS}}{V_P} \right| \right]^2$$

Ques:- What is the maximum transconductance in JFET having $I_{DSS} = 8\text{mA}$ and $V_p = -4\text{V}$

Soln:- Max. g_m is g_{m0} &

$$g_{m0} = \frac{-2I_{DSS}}{V_p} = 4\text{ms}$$

Ques:- calculate the g_m for a JFET having $I_{DSS} = 8\text{mA}$, $V_p = -4\text{V}$ and it is biased to operate at $V_{GDS} = -1.8\text{V}$

Soln:-

$$g_m = \frac{-2I_{DSS}}{V_p} \left[1 - \frac{V_{GDS}}{V_p} \right]$$

$$= \frac{-2 \times 8 \times 10^{-3}}{-4} \left[1 - \frac{-1.8}{-4} \right] = 2.2\text{mS}$$

Ques:- When gate to source voltage (V_{GDS}) of FET changes from -3V to -3.1V and I_D change from 1.3mA to 1mA assuming other parameters to be constant then $g_m = ?$

Soln:-

$$g_m = \frac{\Delta I_D}{\Delta V_{GDS}} = 3\text{ms}$$

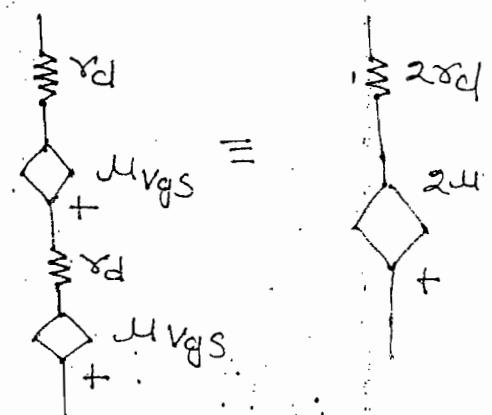
Ques:- If two identical FET's each having an amplification factor m & drain resistance r_d are connected in series for the composite circuit. Find its amplification factor and drain resistance.

Soln:- New drain resistance

$$r_{d\text{new}} = 2r_d$$

New Amp. factor $\rightarrow 2m$

Series \rightarrow Voltage

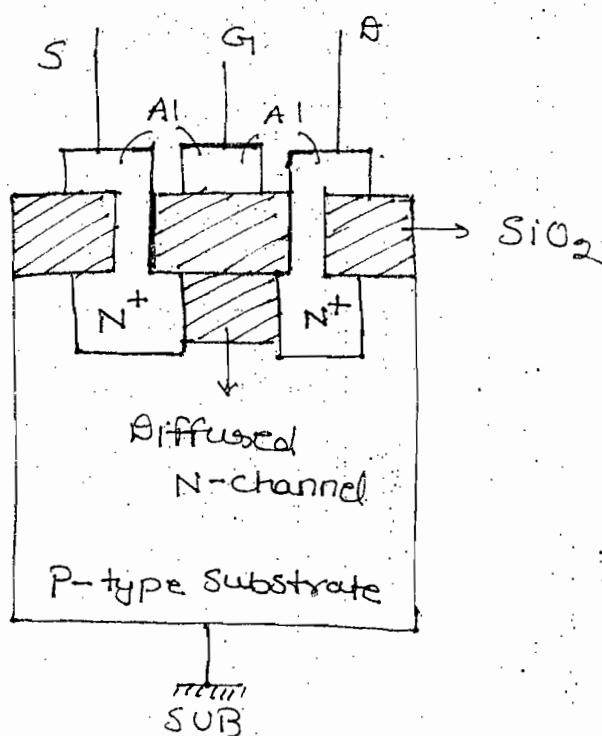


Ques:- If two identical FET's each having a transconductance g_m & drain resistance γ_d are connected in parallel for the composite circuit. Find a new value.

Soln:- In parallel conductances are added so $\rightarrow 2g_m$

& resistances gets halved so $\rightarrow \frac{\gamma_d}{2}$

MOSFET!-



- An integrated circuit or semiconductor chip
- fabricated by VLSI with planar technology
- In planar technology the entire IC or all the IC's will be fabricated on the same plane.
- Voltage Control Device (VCA)
- Symmetrical device
- For N-channel MOSFET, substrate is p-type
- For P-channel MOSFET, substrate is n-type
- Channel is sometimes called inversion layer
- Thickness of SiO_2 is $1000\text{\AA} - 2000\text{\AA}$
- The larger i/p resistance of MOSFET is due to SiO_2
- In depletion MOSFET there is a pre-existing channel.

- In depletion MOSFET, channel is diffused channel
- In the gate region, a parallel plate capacitor is created
- Al plate and semiconductor channel will be working as the two plates of the capacitor & SiO_2 as the dielectric
- MOSFET is basically a capacitor
- MOSFET is voltage control capacitor (V_{GS})
- MOSFET are very insensitive to static electrical noise and static electrical disturbances
- MOSFET are used widely as a switches in digital circuits.
- The main advantage of MOSFET is power dissipation are negligible
- MOSFET are less noisy when compare to JFET and this is due to grounding the substrate
- JFET is a discrete component
- When compare to JFET, MOSFET is smaller in size & easier to fabricate
- MOSFET is faster than JFET
- BJT is a discrete component
- When compare to BJT, MOSFET are very smaller in size and easier to fabricate.
- MOSFET is less noisy than BJT
- In BJT, there is a minority carrier storage time
- In MOSFET, minority carrier storage time is zero and therefore switching time is smaller. Hence MOSFET is faster than BJT
- MOSFET is relatively more suitable for high freq. application than BJT ($f = \frac{1}{T}$)

Depletion Mode

Max. $I_S \rightarrow I_{DSs}$

→ safe

→ saturation

Enhancement mode

Min $I_S \rightarrow I_{DSs}$

→ safe

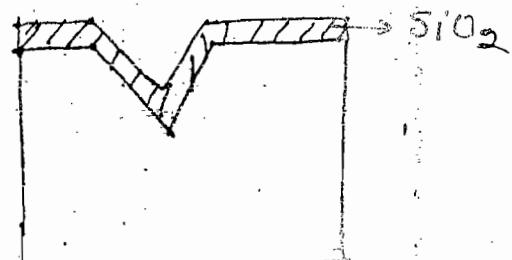
$I_S \geq I_{DSs}$

$I_S \leq I_{DSs}$

- JFET is always operated under depletion mode
- N-Channel depletion MOSFET is sometimes called dual MOSFET because it is suitable to operate in depletion mode and also in the enhancement mode
- P-Channel depletion MOSFET is more suitable for enhancement mode
- N-MOS is faster than P-MOS because $\mu_n > \mu_p$
- P-MOS is easier to fabricate
- N-MOS suffers from ion contamination problem during a fabrication
- In P-MOS, ion contamination problem is less
- P-MOS is bulky and also cheaper
- To get equal performance b/w N-Mos & P-Mos, P-Mos required twice the area of N-Mos
- The main advantage of N-Mos is higher package density i.e. it can store more amount of information in the smaller area.

Vertically Grooved MOSFET (VMOS)

- It is a power MOSFET
- It can handle larger power compare to MOSFET
- Response time is very small · Typ. value = 75 ns



→ It is faster than MOSFET (1.4 times)

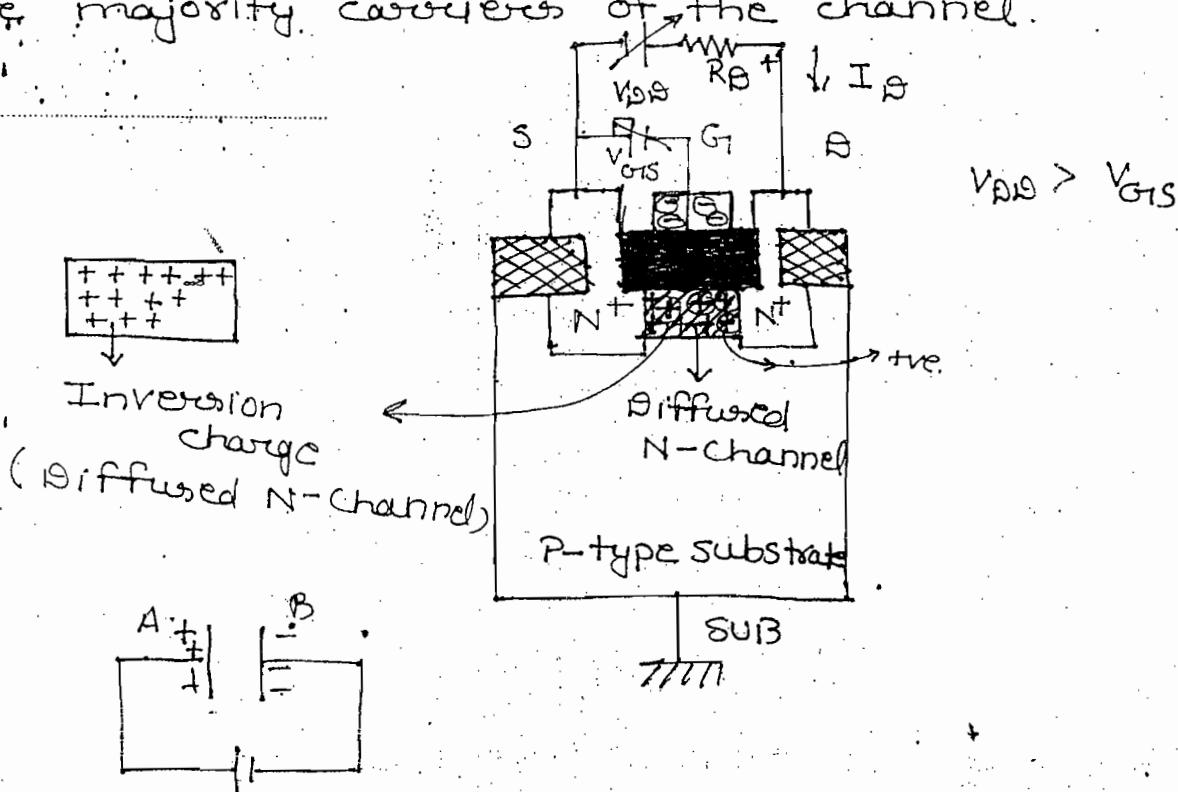
CMOS (Complementary MOSFET) :-

- It is a combination of P-MOS & N-MOS connected together
- i/p resistance = $10^{15} \Omega$
- C-MOS will not consume any power
- The greatest advantage of CMOS is zero power dissipation
- Major application of the C-MOS is, inverter
- In C-MOS inverter, whatever be the i/p signal applied, when one transistor is ON the other transistor is OFF

Operation of N-channel depletion MOSFET under depletion mode:-

Principle:-

The principle of the depletion mode is the applied gate to source voltage must reduce the majority carriers of the channel.



- In N-channel MOSFET, drain is truly biased w.r.t source and to operate under depletion mode gate is -vely biased w.r.t source
- In N-channel depletion MOSFET under depletion mode
 - Channel potential inc. from source to drain
 - Inversion charge dec. from source to drain

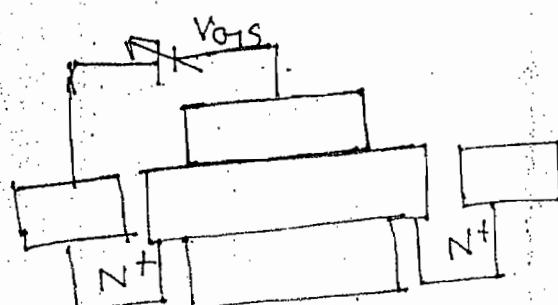
$$\therefore V_{GS} = 0$$

$$\text{Max } I_S = I_{SS}$$

V_{GS} is applied

-1V	$I_S \downarrow$
-3V	\downarrow
-5V	\downarrow

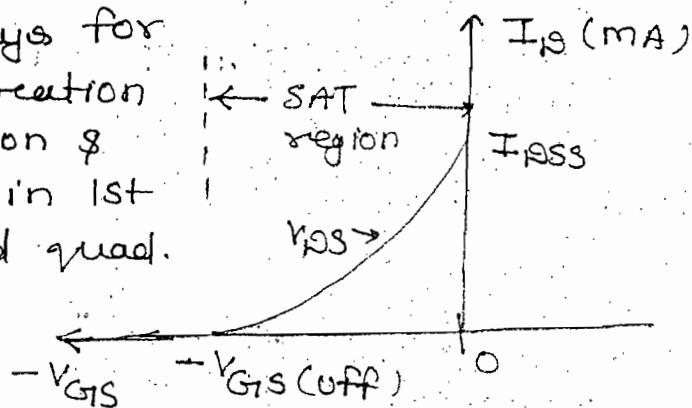
$$I_S = 0$$



- When $V_{GS} = 0$, inversion charge is zero & therefore max. no. of -ve charges will be moving from source to drain and drain current is max. and it is denoted by I_{SS} (drain to source source current / saturation current)
- When V_{GS} is applied, the gate is given with a -ve voltage and therefore the charges are accumulated in the semiconductor channel and due to recombination, less no. of -ve charges will be reaching the drain and I_S decreases.
- I_S further dec as gate is given with more -ve voltage
- If gate is given with sufficient -ve voltage, large no. of the charges are accumulated in the semiconductor channel and result in the total recombination. Hence no -ve charges will be reaching, and I_S decrease to 0 and the channel is cut-off.

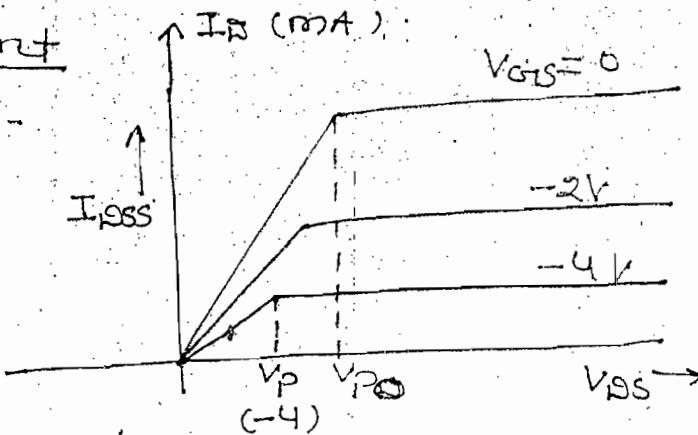
Transfer characteristics:-

- Always for saturation region & either in 1st or 2nd quad.



Constant current characteristics:-

Characteristics:-



- In depletion mode, V_P is the maximum pinch off voltage
- The equation for the drain current under depletion mode is

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

where V_{GS} & V_P must have same signs

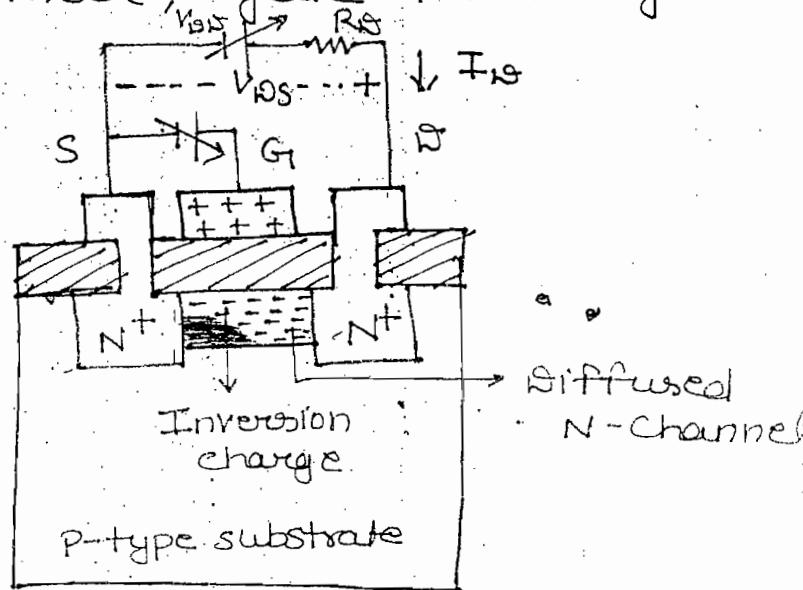
- In the depletion mode, I_D dec. as a parabolic variation with gate to source voltage

N-channel Depletion MOSFET under enhancement mode :-

Principle :-

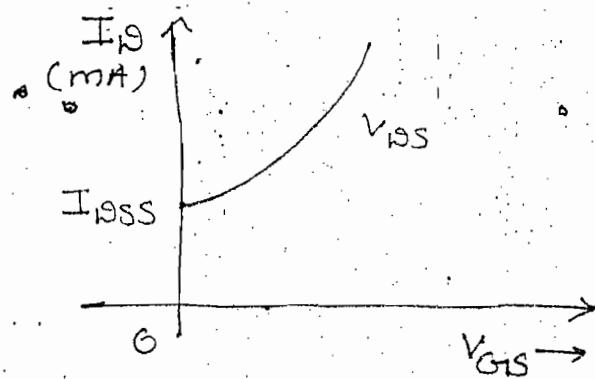
The principle of enhancement mode is applied gate to source voltage must be increases the majority carriers of the channel.

- In N-channel MOSFET, drain is truly biased w.r.t source and to operate under enhancement mode, gate is truly biased w.r.t source

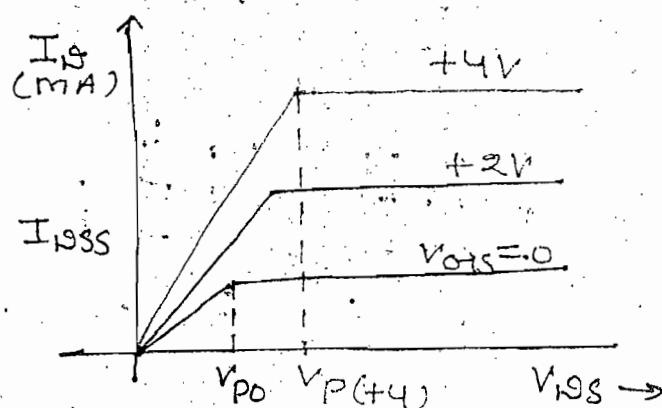


- When V_{GS} is kept 0, inversion charge is 0 & min. no. of -ve charges will be moving from source to drain and drain current is min and it is denoted by I_{DSS} (drain to source safe current).
- When V_{GS} is applied, gate is given with a true voltage and therefore -ve charges are accumulated in the semiconductor channel and this will inc. the -ve charges to drain. Hence I_D inc.
- I_D further inc. as V_{GS} is increasing

Transfer Characteristics :-



Constant current characteristics :-



- Under enhancement mode V_P is min. pinch off voltage
- The equation for drain current in the enhancement mode is

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

where V_{GS} & V_P must have opp. signs

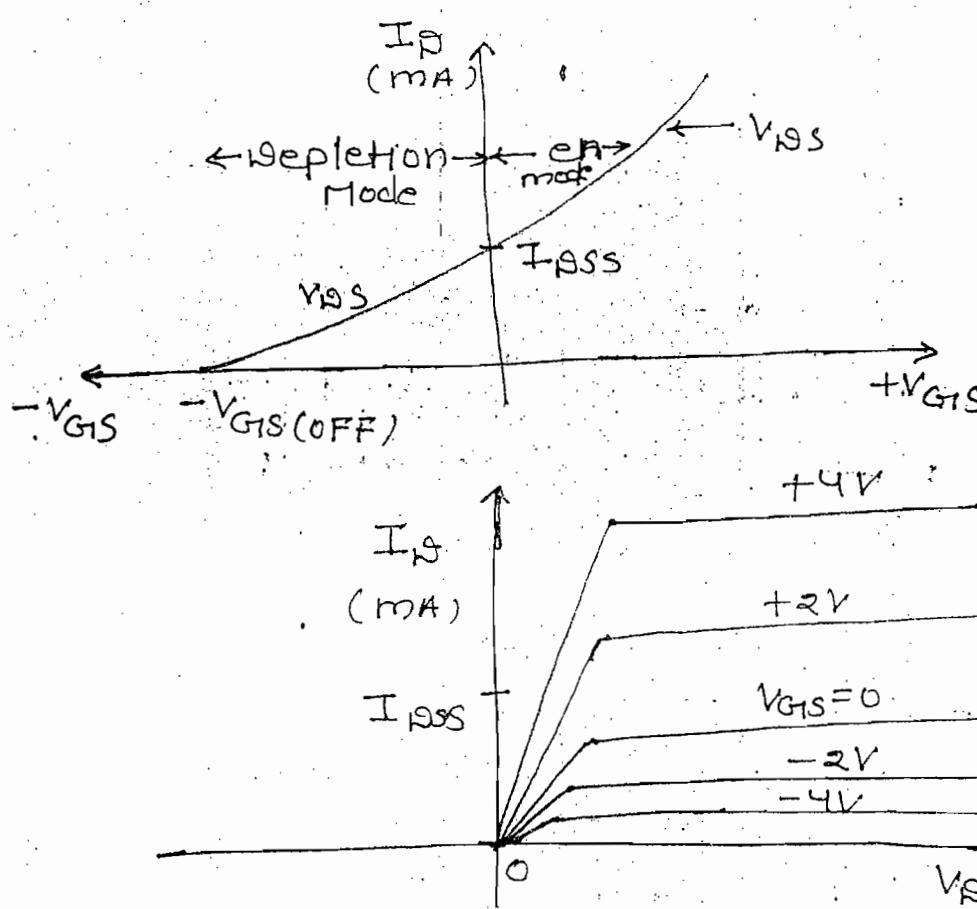
- In the enhancement mode, I_D inc. as a parabolic variation with gate to source voltage
- Depletion Mosfet when operating under enhancement mode it can be operated under pinch off conditions.

→ Under pinchoff condition min. V_{DS} required is

$$\min \cdot V_{DS} = V_{GS} + V_p$$

Characteristics of N-channel Depletion MOSFET :-

→ N-channel depletion MOSFET is dual MOSFET and it can operate under depletion mode and enhancement mode.



→ In the depletion MOSFET when V_{GS} kept 0 the $I_D = I_{DSS}$

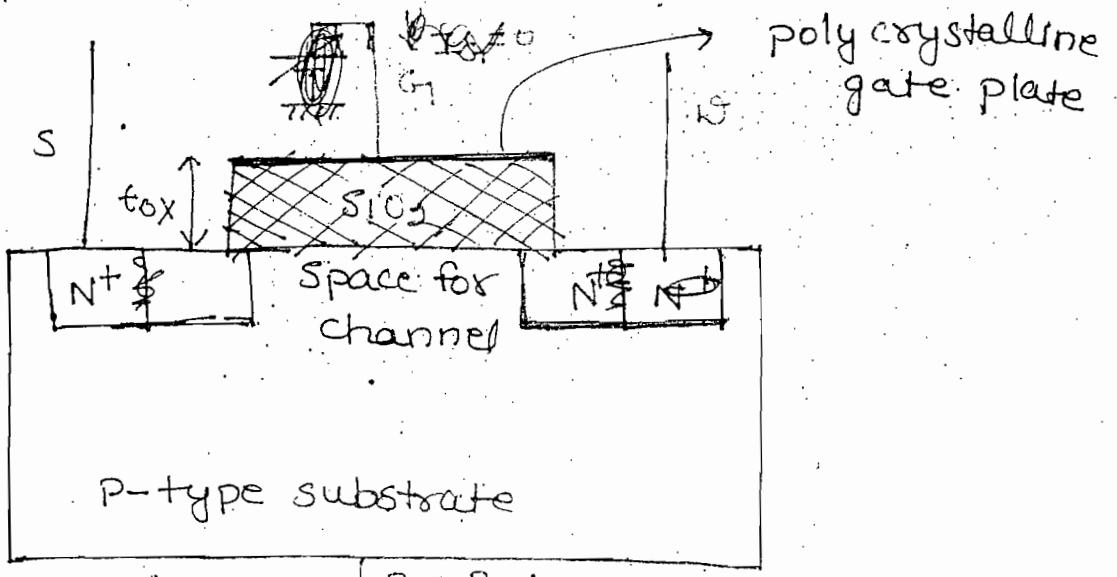
**** Enhancement MOSFET (E-Only MOSFET) :-

→ In E-only MOSFET, the source and drain regions will be kept apart and therefore the channel could not be formed in b/w source and drain region.

→ In enhancement MOSFET, there is no pre-existing channel.

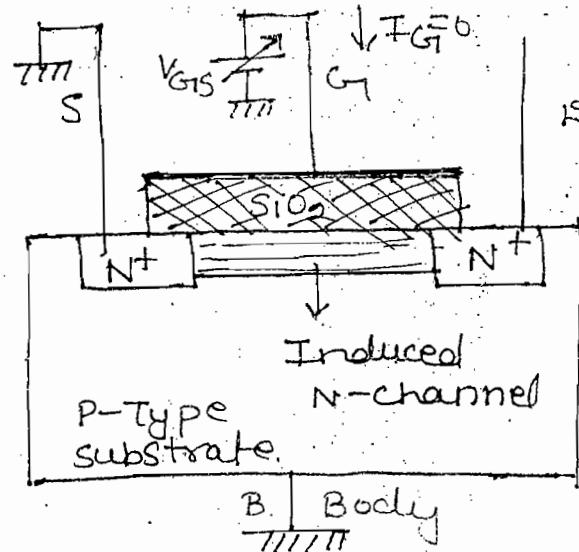
→ In E-only MOSFET, Al plates or metallic plates are replaced with polycrystalline Si material. and due to this we get the following advantages:-

- (I) The size of MOSFET is reduced.
- (II) The cost of the MOSFET is reduced.
- (III) Fabrication process has become easier.
- (IV) Gives better performance than depletion MOSFET.



t_{ox} = Oxide thickness, or thickness of SiO_2

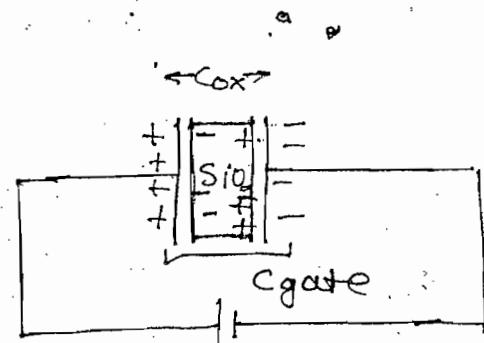
- E-only MOSFET is a symmetrical device.
- Voltage control device.
- In E-only MOSFET, channel has been created by applying proper gate to source voltage.
- When proper gate to source voltage is applied and if body of the MOSFET is grounded, V_{GS} is also reflected b/w gate and body of the MOSFET and due to electric field intensity created, the channel is induced b/w source & drain region and the channel is a flat channel.



- The channel is a flat channel
- In E-only MOSFET, channel is induced channel
- A parallel plate capacitor is created at the gate region with polycrystalline Si gate plate and induced channel has the two plates of the capacitor and SiO_2 as a dielectric material. The MOSFET is known working as MOS CAP

→ For a MOS CAP

The oxide cap per unit cross-sectional Area is C_{ox}



$$C_{ox} = \frac{A\epsilon_0\epsilon_r}{d} \text{ Farad}$$

$$\frac{C}{A} = \frac{\epsilon_0\epsilon_r}{d} \text{ F/m}^2$$

$$\Rightarrow C_{ox} = \frac{\epsilon_0\epsilon_r}{d} \text{ F/m}^2$$

$$\epsilon_r (\text{SiO}_2) = 3.9$$

$$\epsilon_0 = 8.854 \times 10^{-12} \text{ F/m}$$

where $\epsilon_{ox} = \epsilon_0\epsilon_r$ Relative permittivity of SiO_2

\downarrow Absolute permittivity of free space

$$\begin{aligned}\epsilon_{ox} &= 3.9 \epsilon_0 \\ &= 3.9 \times 8.854 \times 10^{-12} \\ &= 3.45 \times 10^{-11} \text{ F/m}\end{aligned}$$

**

$$C_{ox} = \frac{3.45 \times 10^{-11}}{t_{ox}} \text{ F/m}^2$$

→ The total capacitance at the gate is given by C_{gate}

$$C_{gate} = C_{ox} \cdot W \cdot L \quad \text{F/mad}$$

$$W > L$$

→ L = Length of polycrystalline Si gate plate

W = Width of " " " "

→ In the E-only MOSFET always $W > L$

$$\frac{W}{L}$$

→ Aspect Ratio

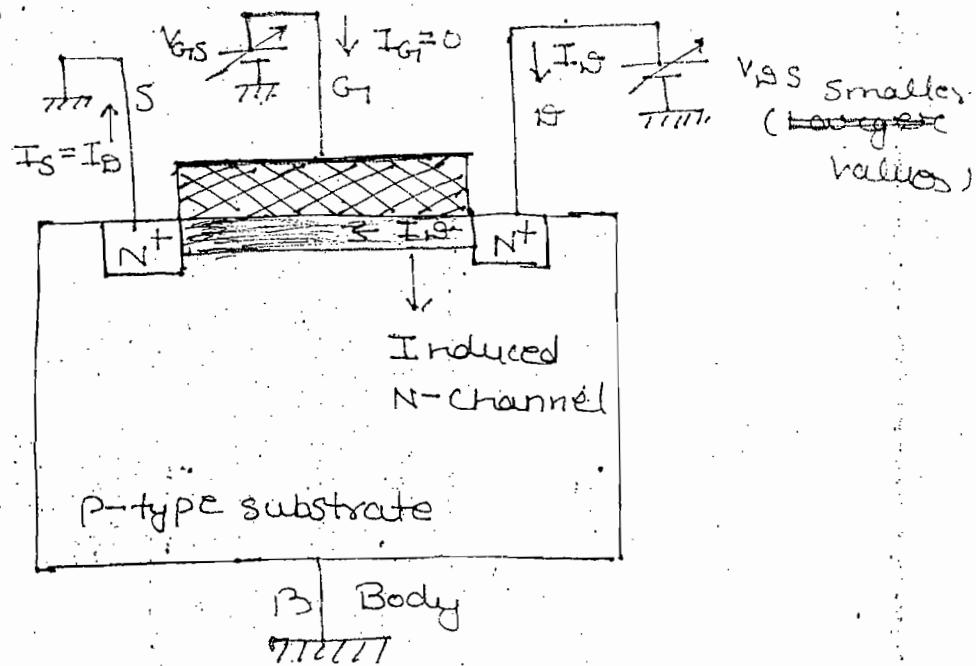
NOTE :-

MOS CAP

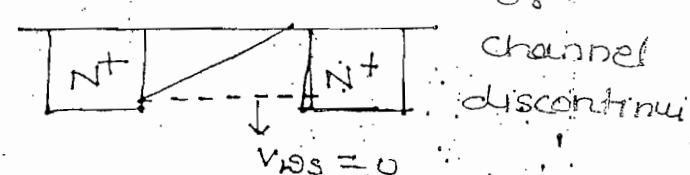
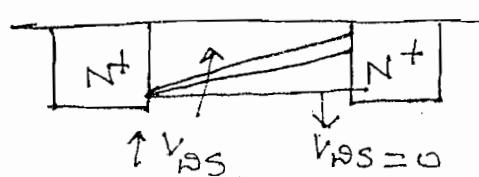
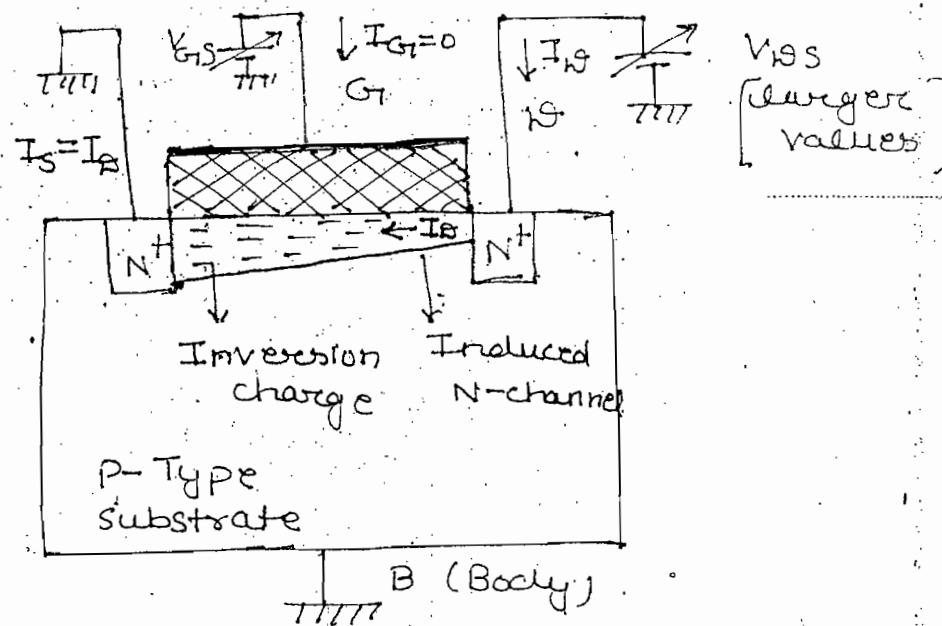
→ since drain terminal is floating Hence $I_D = 0$ i.e. no current will be passing into the channel.

Lecture - 21

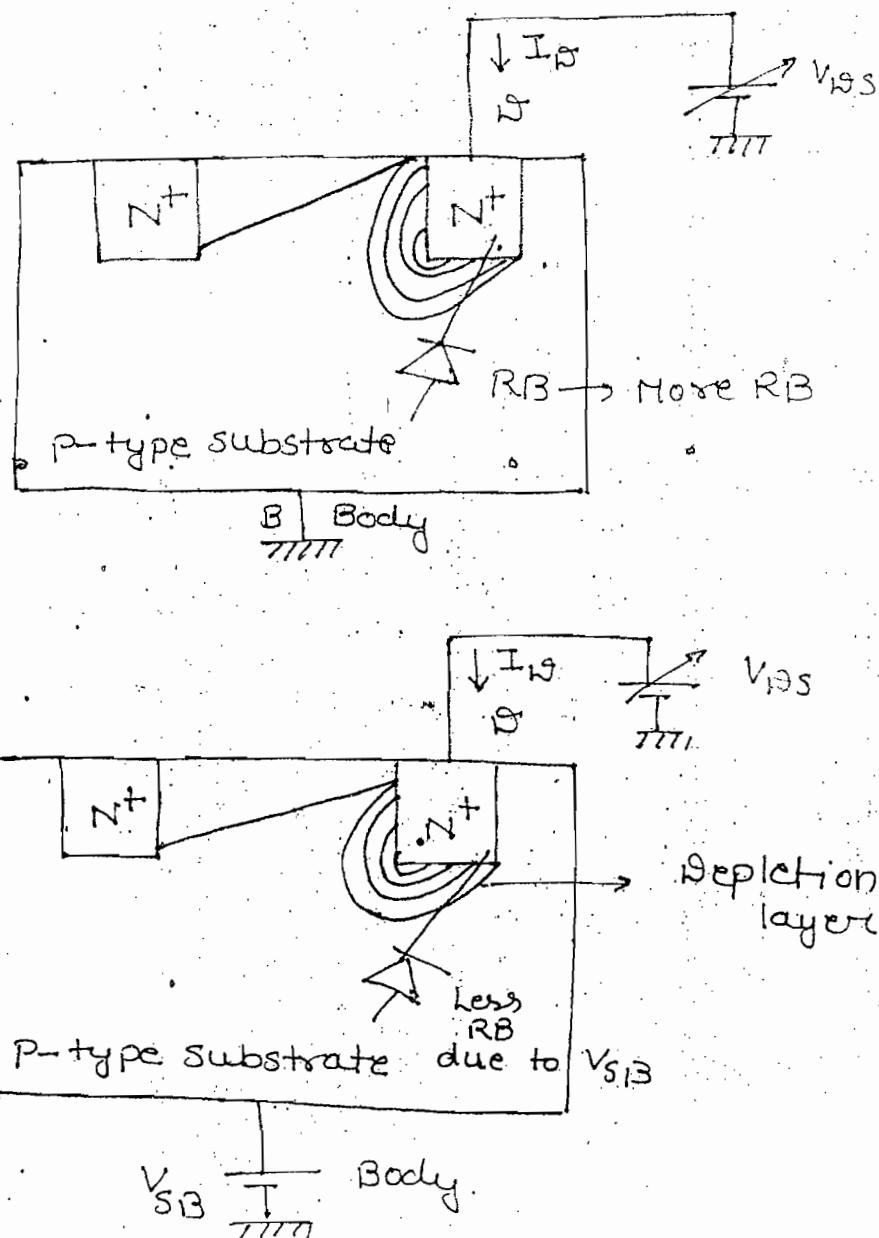
- When smaller values of V_{GS} is applied the channel will remain almost flat and the drain current remain zero.



- When larger values of V_{GS} is applied, the channels gets tapered as given in the diagram below



- When $V_{GS} = 0$, then channel will remain very flat.
- When V_{GS} is applied & increasing, channel gets more and more tapered.
- When very larger values of V_{GS} is applied channel gets more, tapered and can be broken or channel is discontinuous as shown in the above figure.



- When V_{GS} is applied and since the body is grounded, V_{GS} is also reflected b/w drain & body of the MOSFET and this region will be working as a RB diode (PN⁺ diode).

- When V_{GS} is kept zero, the PN^+ diode is unbiased and in the absence of depletion layer the channel will remain very flat.
- When V_{GS} is applied and increasing the PN^+ diode will become more RB and depletion layer will penetrate more into the channel and channel gets tapered.
- Tapering of the channel is due to V_{GS} .
- A larger values of V_{GS} is applied PN^+ diode will be highly RB and due to the larger depletion layer, channel gets highly tapered and can be broken.
- A channel is broken or ~~can~~ discontinuous due to the larger field intensity at the drain, the drain current will continue to flow into the channel.
- A larger $V_{DS,(\text{max})} \rightarrow V_{GS}$ is applied, the channel is broken and length of the channel is reduced.
- Channel length is reduced by applying larger V_{GS} .
- The process where length of the channel is altered by varying V_{GS} is called channel length modulation.
- Channel length modulation only occurs in E-only MOSFET.
- There is no channel length modulation in JFET and depletion MOSFET.
- E-only MOSFET can't be used in self designing of self-bias arrangement.
- The disadvantage of E-only MOSFET is broken channel or channel discontinuity.
- The channel discontinuity problem in the E-only MOSFET can be eliminated by connecting substrate voltage or body voltage. The body voltage is so connected to make PN^+ diode less RB.

thereby depletion layer gets less penetrated and channel will be restored i.e. the discontinuity of channel is eliminated

→ Channel discontinuity problem is eliminated with body voltage

NOTE:-

→ In E-only MOSFET, if ~~V_{DS}~~ = 0, then channel will disappear and drain current I_D becomes zero

→ In N-channel Enhancement MOSFET

(i) Channel potential increases from source to drain

(ii) Inversion charge decreases from source to drain.

Both the above statements are correct and they are due to V_{GS} and therefore related statements

Comparison b/w Depletion MOSFET and Enhancement MOSFET:-

Depletion MOSFET

(i) There is pre-existing channel

(ii)

(iii) Diffused channel

(iv) Can be operated under depletion mode and enhancement mode

Enhancement MOSFET

No pre-existing channel

The channel has to be created by applying proper gate to source Voltage
Induced channel

can be operated only under enhancement mode

Depletion MOSFET

(V) If $V_{DS} = 0$ then
 $I_D = I_{DSS}$

(VI) Continuous channel

(VII) No channel length modulation

(VIII) Can be designed with self bias arrangement

(IX) Relatively larger in size, expensive & difficult to fabricate due to the requirement of Al plate

Enhancement MOSFET

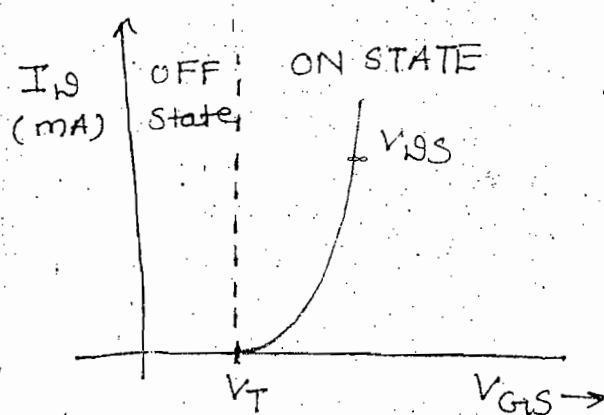
If $V_{DS} = 0$ then $I_D = 0$

Broken channel

channel length modulation exist can't be used in designing of self bias arrangement.

Relatively smaller in size, economical, easier to fabricate & offers better performance due to the replacement of Al plate with poly-crystalline Si material

Transfer Characteristics of N-channel enhancement



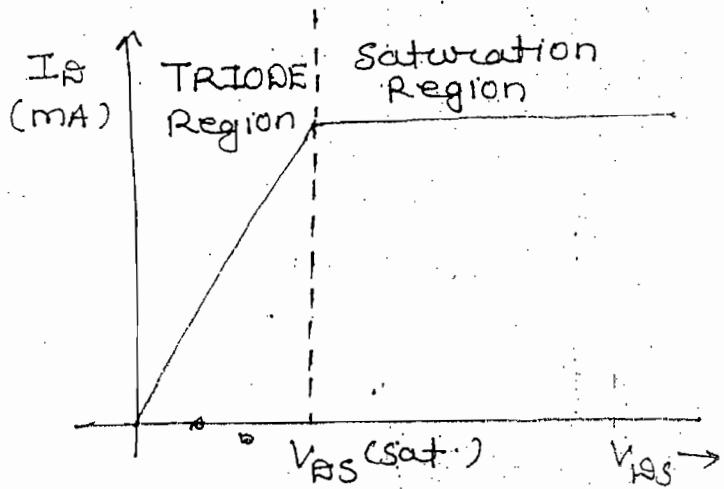
V_T = Threshold voltage

If $V_{GS} < V_T$, MOSFET is OFF state i.e. O.C

If $V_{GS} \geq V_T$, MOSFET is in ON state i.e. S.C

→ Always in 1st quadrant
Graph Characteristics of N - channel enhancement MOSFET :-

-ment MOSFET :-



TRIODE Region :-

→ Also called ohmic region or linear region or active region or non-saturation region

→ $V_{DS} < V_{DS(Sat.)}$

or

$V_{DS} < (V_{GS} - V_T)$

Condition for TRIODE Region

Saturation Region :-

→ Also called pinch-off region or Pentode region

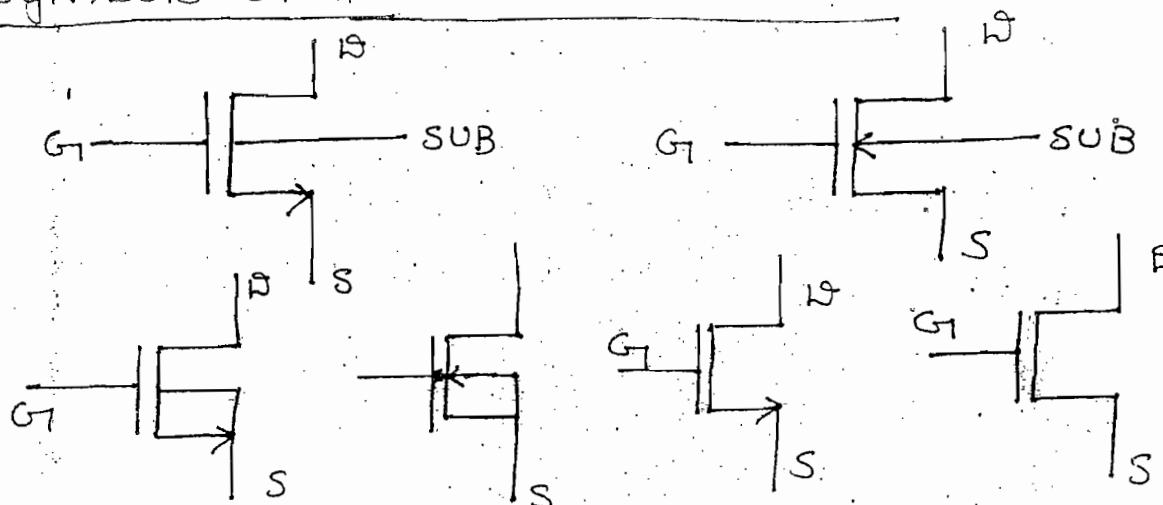
→ $V_{DS} \geq V_{DS(Sat.)}$

OR

$V_{DS} \geq [V_{GS} - V_T]$

Condition for saturation Region

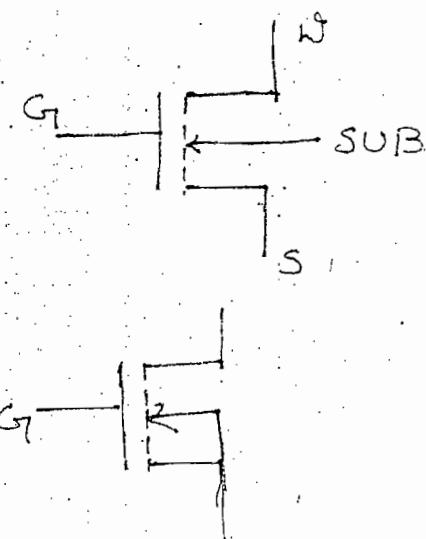
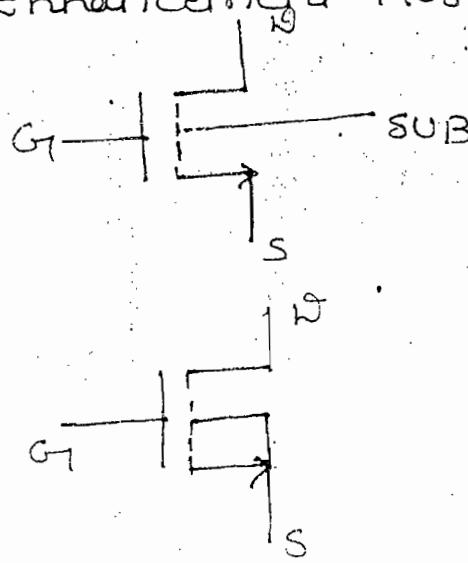
Symbols of N - channel MOSFET :-



→ The above symbols are for DEPLETION MOSFET and Enhancement MOSFET

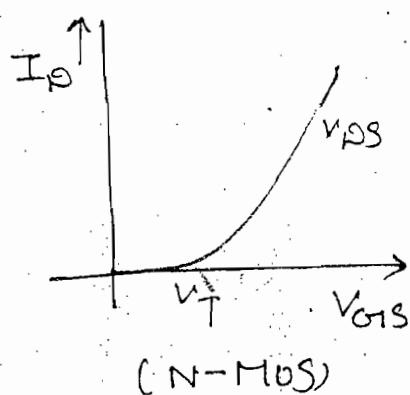
NOTE! -

The following are symbols for only Enhancement MOSFET

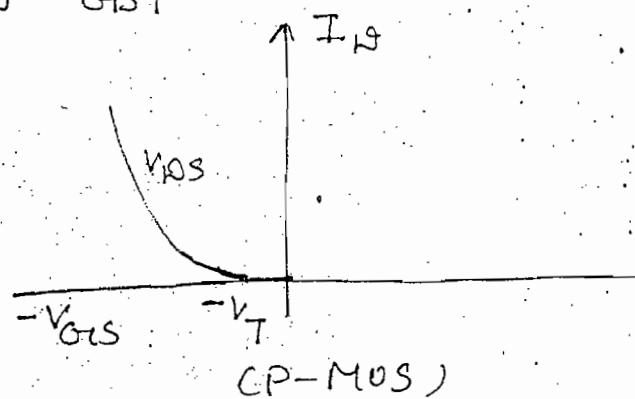


Threshold Voltage (V_T or V_t or V_{th}) :-

→ Also called gate to source threshold voltage if it is denoted by V_{GSt}



(N-MOS)



(P-MOS)

- For N-MOS, threshold voltage is +ve
- For P-MOS, " " " " " -ve
- V_T is in the range of 0.5V to 3V
- Threshold voltage is defined as min. gate to source voltage where the MOSFET enters into ON state

- For better performance of MOSFET, V_T must be as small as possible
- In modern MOSFET, V_T is in the range of 0.5V to 3V

(i) Advantage of smaller V_T :-

- It enables the device to operate with smaller supply voltage (V_{DS})
 - It inc. the compatibility of the device
 - It reduces the switching times of the device and MOSFET will become faster
- (ii) Equation for V_T :-

For N-channel E-only MOSFET

$$V_T = V_{to} + V \left[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f} \right]$$

where $V = \frac{\sqrt{2qN_A\epsilon}}{C_{ox}}$

OR

$$V = \frac{t_{ox}\sqrt{2qN_A\epsilon}}{3.45 \times 10^{-11}} \quad \epsilon = 11.7\epsilon_0$$

N_A = Doping conc. of p-type substrate in N-MOS

V_{SB} = Substrate voltage / body voltage

ϕ_f = Fermi voltage (Typ. value $\rightarrow 0.6V$)

V = Fabrication process parameter

V_{to} = the value of threshold voltage when substrate voltage is kept zero

→ V_{to} is also called min. threshold voltage of the MOSFET

→ The threshold voltage of MOSFET can be increased by connecting and by increasing substrate voltage.

→ If there is small variation in V_{SB} , we get small variation in V_T and this causes minute variation in I_S . This indicates the drain current is controlled by body voltage & therefore the body will be working as the second gate in MOSFET & this property in device is called body effect in MOSFET.

(iii) Procedure to reduce V_T :-

The threshold voltage of the MOSFET can be reduced in any one of the following methods but only during the fabrication of the device.

④ Once the device fabricated, we can't reduce the threshold voltage but we can inc. the threshold voltage by connecting substrate voltage

(i) $\downarrow N_A$ (ii) $\uparrow C_{ox}$ (iii) $\downarrow t_{ox}$

(iv) By using ion-implantation technique

It is outdated for MOSFET fabrication

(v) By replacing Al plates with the polycrystalline Si material

NOTE:-

(i) Polycrystalline Si is also called polysilicon

④ ~~an~~ alternative material for polycrystalline Silicon nitride.

(ii) In modern MOSFET, the material used for the gate is polycrystalline Si.

Equation for N-MOS +

N-MOS Transistor :-

(I) Operation in TRIODE Region :-

(a) Condition :-

$$V_{DS} < V_{GS} (\text{sat})$$

or

$$V_{DS} < [V_{GS} - V_T]$$

$$(b) I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

TRIODE region exists for smaller values of V_{DS} & therefore neglecting $\frac{V_{DS}^2}{2}$

$$I_D \approx \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_T) V_{DS}]$$

Let $\mu_n C_{ox} = k_N \rightarrow$ Process trans-conductance parameter in A/V^2

$$I_D \approx k_N \frac{W}{L} (V_{GS} - V_T) V_{DS}$$

Let $k_N \frac{W}{L} = k'_N \rightarrow$ constant in A/V^2

$$I_D \approx k'_N [V_{GS} - V_T] V_{DS}$$

→ First order equation and thus indicates I_D inc. linearly with V_{DS}

(II) Drain to source resistance :-

$$r_{ds} = \frac{V_{DS}}{I_D} \Omega$$

→ r_d ON

→ Channel resistance

$$g_{c_{ds}} = \frac{1}{k'_N [V_{G_{DS}} - V_T]} \quad \text{OR} \quad 5$$

$$g_{c_{ds}} = \frac{1}{\mu n C_{ox} \frac{W}{L} (V_{G_{DS}} - V_T)} \quad \text{OR} \quad 5$$

- This indicates channel resistance can be altered by varying gate to source voltage
- In the TRIODE region, FET will be working as voltage variable resistor [VVR] by varying gate to source voltage

(IV) Transconductance (g_m) :-

$$g_m = \frac{\delta I_D}{\delta V_{G_{DS}}}$$

$$I_D = k'_N [V_{G_{DS}} - V_T] V_{D_S}$$

$$\frac{\delta I_D}{\delta V_{G_{DS}}} = k'_N V_{D_S}$$

$$g_m = k'_N V_{D_S} \quad \text{OR}$$

$$g_m = \mu n C_{ox} \frac{W}{L} V_{D_S} \quad \text{OR}$$

(B) Operation in saturation region :-

(a) Condition :-

$$V_{D_S} \geq V_{D_S(\text{sat.})}$$

OR

$$V_{D_S} \geq [V_{G_{DS}} - V_T]$$

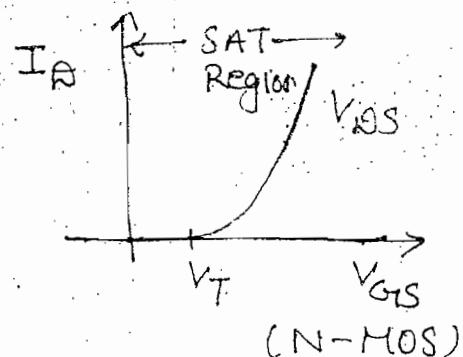
$$(b) I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

$$= \frac{1}{2} k_N \frac{W}{L} (V_{GS} - V_T)^2$$

Let $\frac{1}{2} k_N \frac{W}{L} = k \rightarrow \text{constant}$ in A/V^2

$$I_D = k [V_{GS} - V_T]^2$$

→ Second order equation and this indicates I_D will be increasing, as a parabolic variation with V_{GS}



(c) Transconductance (g_m): -

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

$$I_D = K [V_{GS} - V_T]^2$$

$$\frac{\partial I_D}{\partial V_{GS}} = 2K [V_{GS} - V_T]$$

$$g_m = 2K [V_{GS} - V_T]$$

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)$$

Equations for P-MOS Transistor:-

(A) Operation in TRIODE Region :-

(a) Condition:-

$$V_{DS} > V_{DS(\text{sat.})}$$

or

$$V_{DS} > [V_{GDS} - V_T]$$

$$(b) I_D = \mu_p C_{ox} \frac{W}{L} \left[(V_{GDS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$\approx \mu_p C_{ox} \frac{W}{L} (V_{GDS} - V_T) V_{DS}$$

Let $\mu_p C_{ox} = k_p \rightarrow$ Process Transconductance parameter in A/V^2

$$I_D \approx k_p \frac{W}{L} (V_{GDS} - V_T) V_{DS} \rightarrow \text{constant in } A/V^2$$

$$\text{Let } k_p \frac{W}{L} = k_p' \rightarrow$$

$$I_D \approx k_p' (V_{GDS} - V_T) V_{DS}$$

(c)

$$r_{ds} = \frac{1}{\mu_p C_{ox} \frac{W}{L} (V_{GDS} - V_T)} \Omega$$

(d)

$$g_m = k_p' V_{DS}$$

$$g_m = \mu_p C_{ox} \frac{W}{L} V_{DS}$$

(B) Operation in Saturation Region :-

(a) Condition:-

$$V_{DS} \leq V_{DS(\text{sat.})}$$

$$V_{DS} \leq [V_{GDS} - V_T]$$

$$\begin{aligned}
 (b) \quad I_D &= \frac{1}{2} \mu_P C_{ox} \frac{W}{L} (V_{GDS} - V_T)^2 \\
 &= \frac{1}{2} K_P \frac{W}{L} (V_{GDS} - V_T)^2 \\
 \Rightarrow \quad I_D &= K [V_{GDS} - V_T]^2
 \end{aligned}$$

$$(c) \quad g_m = \mu_P C_{ox} \frac{W}{L} (V_{GDS} - V_T) - U$$

NOTE:-

In CMOS inverter whatever be the i/p voltage applied one transistor is ON & other transistor is OFF. Therefore current passing through CMOS is negligible (mA).

Unit-4 Field Effect Transistor

1. A	7. B	13. S	19. S
2. A	8. B	14. S	20. S
3. C	9. S	15. C	21. S
4. S	10. S	16. C	22.
5. A	11. S	17. B	23.
6. B	12. A	18. B	24.

NOTE:-

→ ω_d , g_m , u & V_T all are obtained from graph

→ If gate and drain are short circuited

Ques:- Repeat a. No-21 when $V_T = 3V$

Ans - 5V (a)

NOTE:-

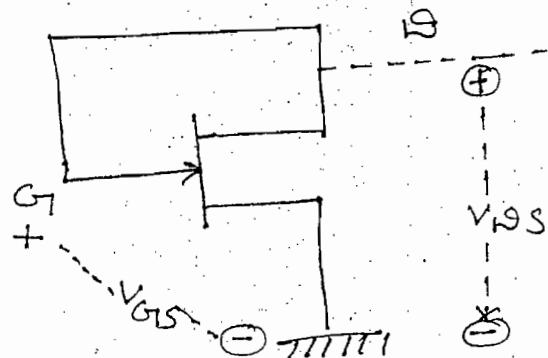
- R_i of BJT in CB mode $\Rightarrow < 100 \Omega$
- R_i of BJT in CE mode \Rightarrow around $1 k\Omega$
- R_i of BJT in CE with R_e $\Rightarrow 50 - 500 k\Omega$
- R_i of BJT in CC mode
or $\Rightarrow 50 - 500 k\Omega$

Emitter follower (EF)

- R_i of Darlington Emitter follower $\Rightarrow > 1M\Omega$
(1EF)
- R_i of OP-Amp $\Rightarrow 10^6 \Omega$
- R_i of JFET $\Rightarrow 10^6$ to $10^8 \Omega$
- R_i of MOSFET $\Rightarrow 10^{10}$ to $10^{15} \Omega$

NOTE:-

- If gate and drain are short circuited



$$\text{we get } V_{GDS} = V_{DS}$$

& MOST is ON state (i.e. SAT)

For GATE :- Diode Problems & FET

