## Quantum Algorithms 2021/2022: Exercices 3

Benoît Vermersch (benoit.vermersch@lpmmc.cnrs.fr) -October 24, 2021

## 1 Measurement of ZZ stabilizers

The error syndromes in the three qubit bit flip code correspond to the measurement of the operators  $Z_1Z_2$  and  $Z_2Z_3$ .

- 1. Explain the physical process underlying the measurement of an operator  $Z_1Z_2$ . Why cannot we simply measure the state of each qubit to perform an error syndrome?
- 2. How can we measure  $Z_1Z_2$  using an ancilla qubit?

## 2 The three qubit phase flip code

The three qubit phase flip code can correct against qubit phase errors  $Z_1, Z_2, Z_3$ . This is achieved via the error syndromes associated with the measurements of the operators  $X_1X_2$  and  $X_2X_3$ .

- 1. Prove that such code is a [3,1] stabilizer code.
- 2. Show that the code can correct against phase errors.
- 3. Define the two logical states  $|0_L\rangle$ ,  $|1_L\rangle$
- 4. Write a circuit to encode a logical qubit from a physical qubit  $|\psi\rangle = a|0\rangle + b|1\rangle$ .
- 5. Write a circuit to perform an error syndrome  $X_1X_2$  using an ancilla qubit.

## 3 Fault tolerance with the surface code

We consider the surface code. We will illustrate the concept of fault tolerance by studying the scaling of false detection of X errors with increasing sizes of the code.

1. Consider a single row of the code of length d=5 (number of white physical qubits)



Describe the state of the system after initialization, and after one X error (bit flip).

- 2. Suppose the error syndrome step gives -1, 1, -1, 1. Gives a possible error assignment with two errors. Show that the complementary error assignment with three errors also explain the error syndrome. Comment.
- 3. For an arbitrary value of odd d, the most likely undetected errors corresponds to an error of  $d_e = (d+1)/2$  qubits (wrongly attributed to the complementary error assignment with d (d+1)/2 = (d-1)/2). Assume a physical qubit error occurs with probability p after one circuit operation. What is the probability  $p_L$  for such a logical error as a function of p and d, after one logical cycle? We consider here that a logical cycle is assumed to be of duration 8 circuit operations.
- 4. Adapt the expression for a logical error for a 2D surface code. Plot  $p_L$  as a function of p and d. Comment w.r.t the notion of fault tolerance.