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Electronic-photonic integrated circuits on the CMOS platform

L. C. Kimerling*[1], D. Ahn[1], A. B. Apsel[2], M. Beals[1], D. Carothers[3], Y-K. Chen[4], T. Conway[3], D. M. Gill[4], M. Grove[3], C.-Y. Hong[1], M. Lipson[2], J. Liu[1], J. Michel[1], D. Pan[1], S. S. Patel[4], A. T. Pomerene[3], M. Rasras[4], D. K. Sparacin[1], K-Y. Tu[4], A. E. White[4], C. W. Wong[5]
[1]Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge, MA, 02139-4307
[2]Cornell University, Phillips Hall, Ithaca, NY 14853
[3]BAE Systems North America, 1300 N. 17th Street, Suite 1400, Arlington, VA 22209
[4]Bell Laboratories, Lucent Technologies, 600 Mountain Avenue, Murray Hill, NJ 07974-0636
[5]Columbia University, 2960 Broadway, New York, NY 10027-6902

ABSTRACT

The optical components industry stands at the threshold of a major expansion that will restructure its business processes and sustain its profitability for the next three decades. This growth will establish a cost effective platform for the partitioning of electronic and photonic functionality to extend the processing power of integrated circuits. BAE Systems, Lucent Technologies, Massachusetts Institute of Technology, and Applied Wave Research are participating in a high payoff research and development program for the Microsystems Technology Office (MTO) of DARPA. The goal of the program is the development of technologies and design tools necessary to fabricate an application-specific, electronic-photonic integrated circuit (AS-EPIC). As part of the development of this demonstration platform we are exploring selected functions normally associated with the front end of mixed signal receivers such as modulation, detection, and filtering. The chip will be fabricated in the BAE Systems CMOS foundry and at MIT's Microphotonics Center. We will present the latest results on the performance of multi-layer deposited High Index Contrast Waveguides, CMOS compatible modulators and detectors, and optical filter slices. These advances will be discussed in the context of the Communications Technology Roadmap that was recently released by the MIT Microphotonics Center Industry Consortium.

Keywords: waveguides, modulators, photodetectors, optical filters, EPIC

1. INTRODUCTION

Electronics technology increasingly requires integration with photonics to maintain the performance roadmap known as Moore's Law. Parallelism is already delivering an aggregate system performance of 1000x every ten years that outpaces the 2x every eighteen months "Moore's Law" rate. Data rates of 10Gb/s per channel dictate a virtual threshold for links of >1m that make photonic interconnection easier to implement than electronics with complex compensation circuits. Beyond interconnection, in areas such as Fast Fourier Transforms, combined electronic-photonic signal processing, is beginning to show value. For these reasons, the future is less a replacement of electronics by photonics than a partitioning of function that will continually develop as designers become more skilled in the art. One of the necessary infrastructure elements for the near term is the use of a CMOS chip fabrication technology that is capable of seamless integration of electronic and photonic signal carriers, devices, and functional circuits.

The MIT Communications Technology Roadmap [1] recently published an evaluation of the vast array of new photonic technologies that have disrupted the telecommunications industry. The report contained four primary findings:

- The future of components technology will be determined by electronic-photonic convergence.
- The functional emphasis will be short (<1km) reach interconnection.
- This direction will trigger a major shift in the leadership of the component industry from information transmission (telecom) to information processing (computing, imaging).
- The skill set required for this path does not exist at any single institution.

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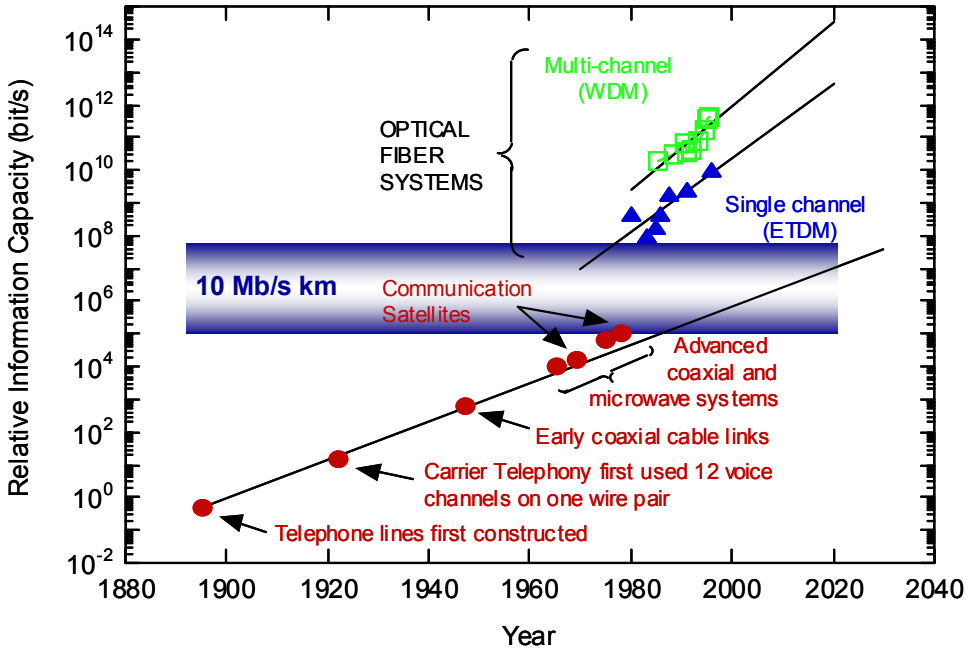

Figure 1: Time evolution of information transport technology: plot of equivalent data rate of a single line against year with technology introduction identified. Optical transport introduces a discontinuity in the rate of performance increase and a steeper slope.

The Roadmap's projected goals for the next ten years are: 1) a standard component platform; 2) a common manufacturing infrastructure; 3) industry-wide R&D that is leveraged to reduce the product development cycle time; and 4) establishment of a common platform across market sectors that can grow to $20B in annual revenue. The overarching expectation is that such an industry will then be driven by technology obsolescence through performance scaling with product lifetimes significantly shorter than the telecommunications network build cycle.

Electronic Photonic Integrated Circuit (EPIC) applications fall into two categories: interconnection and signal processing. Five years ago, one would have regarded interconnection as the only application for photonics. Today, applications in advanced signal processing, such as channelization, can realize higher processing performance with significantly lower power dissipation, footprint, and weight. This paper summarizes our team's learning and early achievements toward the first implementation of an EPIC optical signal processor in the BAE Systems CMOS foundry.

2. THE EPIC CMOS PLATFORM

Our AS-EPIC chip is one of the very first signal processing applications of monolithic electronic-photonic integration on the silicon wafer platform. It is designed to provide a high resolution, Fast Fourier Transform of an input RF signal. The RF signal is encoded on an optical carrier with an electro-optic modulator; frequency channelization is performed with an optical filter network; and the signal of each channel is read by a dedicated photodetector. The size, power dissipation, bandwidth, and noise of the individual devices are important, but the integrated E-P circuit functions (measured, for example, by the Spurious Free Dynamic Range) are the key performance metrics. Discrete device technologies used in 3R (reamplify, reshape, reclock) signal conditioning for long haul telecommunications depend on customized, ideal device performance at each signal node; whereas a CMOS EPIC design can utilize a circuit of many standardized devices that perform a more complex, signal processing function. Our channelizing application is one of a new class of 'technology shrink' functions that reduce the size, weight, and power of traditional microwave signal processors by encoding on an optical carrier. Many of the devices, such as ring resonators, have analogous devices in the microwave regime. We have learned that many of the circuit design paradigms for microwave circuits can be applied directly to EPIC.

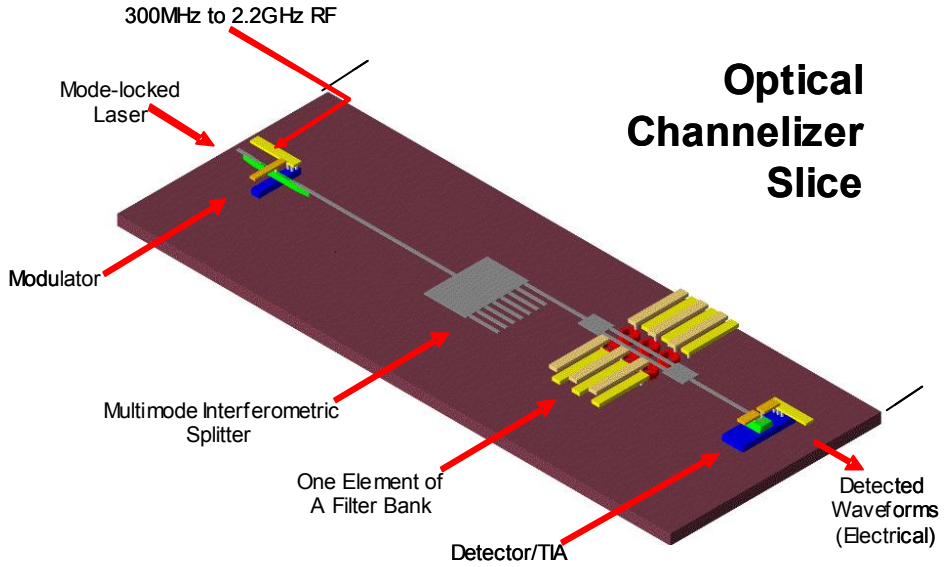

Figure 2: Schematic representation of a single channelizer link on the AS-EPIC chip.

A schematic of our circuit building blocks is shown in Figure 2. The first node of E-P integration is the modulator/driver where the RF signal is encoded on the optical carrier. We use an 'optical power supply' architecture where the carrier is coupled to the chip from an external mode-locked laser. The frequency of the optical carrier is always much higher than the RF signal frequency. The choice of wavelength is dictated by the source performance and the modulator/waveguide design. Current high performance sources are designed for long haul telecommunications applications and operate near the fiber transparency optimum at 1550nm. Therefore, E-P circuits that can operate at these wavelengths have an advantage.

Materials selection for CMOS compatibility is not a limiting constraint. Si, SiO_2, Si_3N_4, Ge, and their alloys perform well for our designs and, once the optical source constraint is removed, they meet the integration constraint best. Silicon is transparent in the 1550nm wavelength range and its high index contrast with a SiO_2 cladding (n_{Si}/n_{SiO2}~3.5/1.5) allows micron turn radii for ultra-dense integration. The high refractive index of silicon also facilitates impedance matching for waveguide coupling to the active modulator (n=3.5) and photodetector (n=4) devices. At this stage of development, we use silicon for waveguides, modulators, and filters and germanium for the photodetectors. While the performance of these devices meets specifications, ease of process integration may dictate some fine tuning in materials selection in the future.

The optical signal is filtered in the frequency domain using ring resonator structures. Each filter is tuned to a specific RF frequency channel and an array of filters provides an equivalent Fourier Transform of the input RF signal. After channelization, the next E-P node, photodetector/TIA, transduces the optical signal to the electronic regime for A/D conversion. The circuit performance of our AS-EPIC chip is dependent on achieving several key specifications. High linearity of the modulator/driver to detector/TIA signal path is required to meet the SFDR requirements of the circuit. Low loss optical waveguides are required for narrow band filters and for low power dissipation. Efficient photodetector/TIA nodes are required to achieve the specified high digital resolution. The focus of this initial EPIC development program is design, prototyping and qualification of device modules for each node in the circuit and demonstration of the process flow for monolithic integration in the BAE Systems CMOS foundry. These issues and their dependence on materials, processes, and process integration are discussed in this paper.

3. EPIC DEVICE PERFORMANCE

3.1. Optical waveguide

The waveguide design constraints for dense E-P integration are transmission loss (dB/cm), bend radius (μm), aspect ratio (width/height), and the number of vertical layers. CMOS is a layer-by-layer additive process technology and both wafer level and deposited upper level waveguides are used. The high index contrast of Si/SiO_2 dictates that this be the waveguide materials system for dense E-P integration. Two materials platforms were studied: single crystal silicon-on-insulator (SOI) for wafer level signal transmission; and chemical vapor deposited (CVD) silicon for upper level waveguides. The primary determinants for transmission loss are absorption by silicon impurities and defects, scattering by sidewall roughness, and radiation to substrate and adjacent features. SOI exhibited no material loss and performed best after post-process smoothing treatments [2]. Deposited silicon exhibited material loss that was minimized by choice of deposition conditions. Exclusion design rules were developed for vertical and lateral layout dimensions to quench radiative loss. Table 1 summarizes the loss performance under our standard processing conditions.

Waveguide Type	Layer Thickness	Cladding Thickness	Loss
SOI	200 nm	3 μm	0.35 dB/cm
Deposited Si	200 nm	3 μm	4 dB/cm

Table 1: Design and performance of silicon waveguides fabricated in the BAE CMOS line with 0.18μm technology design rules.

Two smoothing processes were used depending on process integration design rules. Dry oxidation smoothing (vapor phase) gave global sidewall roughness reduction. A sequence of two-step processes of oxidation and stripping gave the best results. Where dimensional control is critical, as in waveguide-resonator coupling, near monolayer control of the two-step smoothing process is required. The process consists of a wet chemical oxidation step using an agent such as HNO_3 followed by a reducing oxide strip in buffered HF. Optimized versions of this process gave the best loss performance. For long signal paths, loss of <0.5dB/cm is desired. We employ SOI waveguides with 0.35dB/cm using a 3μm oxide standoff from the substrate and deposited waveguides with 4dB/cm for upper level shorter signal paths.

Bend loss is dependent on the turn radius, the sidewall processing, and the waveguide design. We have demonstrated low loss signal transmission through 1μm bend radii and our most liberal designs show no measurable loss for bend radii greater than 10μm. Loss measurements were performed by two methods: cut-back (loss vs. waveguide length or number of identical turns) and functional loss (loss Q of a ring resonator). The measurements utilized a JDS Uniphase Swept Wavelength System for the cutback loss and a LUNA Optical Vector Analyzer for the ring resonator loss.

Figure 3 shows cut-back data from an SOI waveguide and Figure 4 shows an SEM image of a low-loss deposited waveguide/resonator coupler.

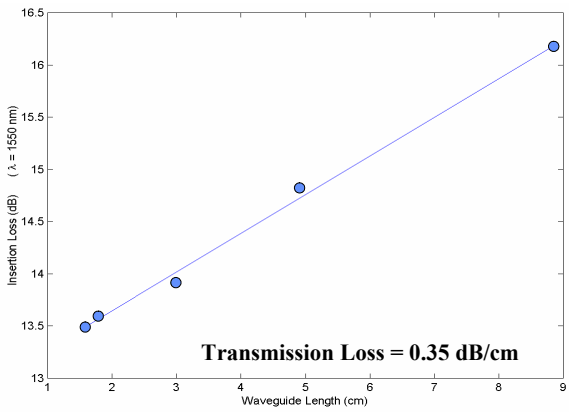

Figure 3: Cut-back loss measurement for an SOI waveguide clad by SiO_2 fabricated in the BAE CMOS line.

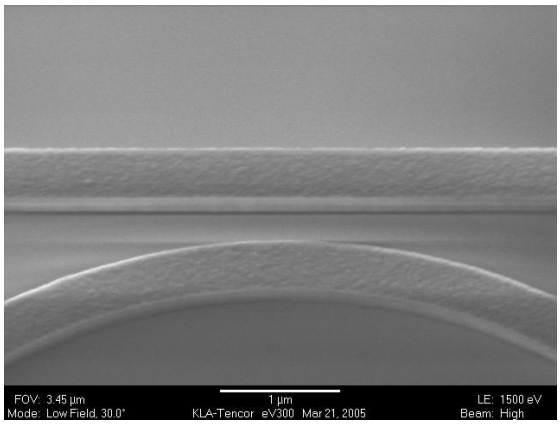

Figure 4: SEM image of a deposited silicon waveguide and ring resonator fabricated with 0.18μm CMOS technology. The transmission loss for the clad waveguide is 4dB/cm.

3.2. Optical modulator

We have developed an all-silicon modulator that provides high speed, low power consumption, and ease of integration [3]. This ring resonator design provides a small footprint, as well. The device is based on free carrier modification of the silicon index of refraction. The device function was first demonstrated using carrier injection by two photon absorption where the response time is determined by minority carrier lifetime. Application of an additional carrier sweep-out voltage significantly enhances the device speed. Our device employs a lateral p-i-n junction for both carrier injection and sweep-out. The resonator structure significantly reduces the device area, the required sweep-out current, and the power dissipation.

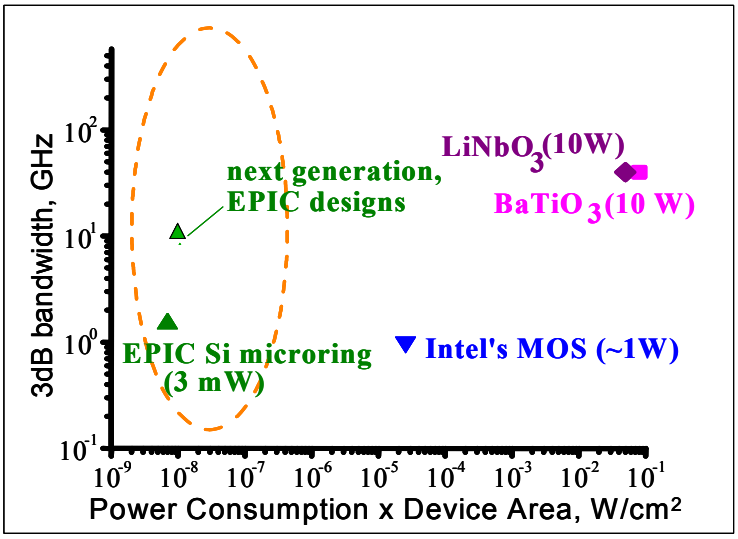

Figure 5: Modulator performance comparison of the Si ring modulator with other modulator designs. The dashed area specifies the performance target for monolithically integrated EPIC devices.

Figure 5 shows a modulator performance design diagram. The key design constraints are maximum modulation frequency, footprint, on-off transition rate, insertion loss, and operating voltage (equivalent V_π for full modulation depth). The Figure-of-Merit for an integrated active device is speed/(power x footprint). As shown in Figure 5, discrete devices made of $LiNbO_3$ or $BaTiO_3$ show high speed at a penalty of high (power x footprint). The integrated MOS modulator by Intel employs the same free carrier index modification, but, as a non-resonant device, requires high drive current and area. The ring resonator device is in a new class of micro-modulators that require mW powers for GHz modulation frequencies.

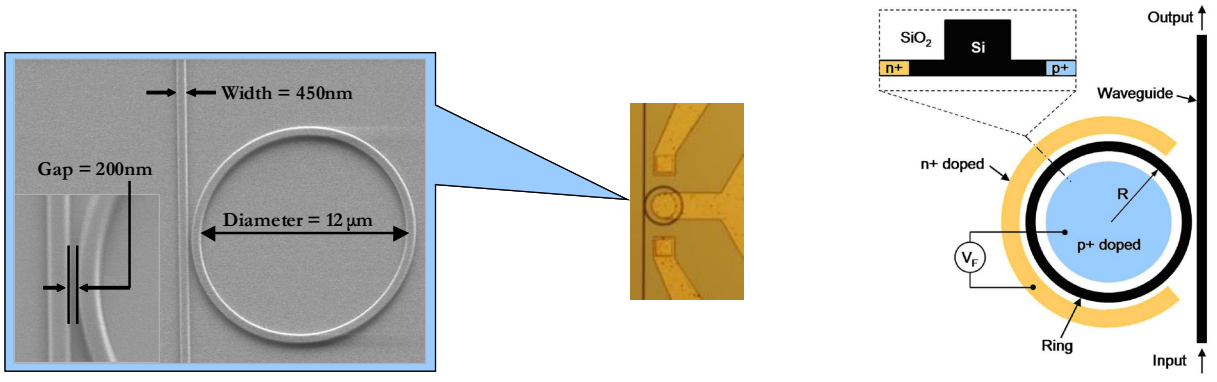

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Figure 6: Images of the Si ring modulator: (a) SEM micrograph of ring, bus waveguide, and contact pads; (b) schematic cross section view of ring with p-i-n junctions.

Figure 6 shows planar and cross sectional views of the device. Figures 7a and 7b show some of the data on device performance. In Figure 7a, the motion of the resonant frequency of the silicon ring with current injection is shown. Figure 7b shows the time dependence of the voltage drive and optical modulation demonstrating 1.5Gb/s return-to-zero (RZ) performance. This device has the lowest power consumption and smallest footprint for any modulator reported to date. Under dc conditions, less than 0.3V and 1mA are required for full 10dB modulation depth. Under ac conditions, 3.3V and 1mA are required. This performance falls within the 10mW power budget for the modulator section of our AS-EPIC circuit. Our channelization circuit provides an analog signal processing function, and additional attributes such as device linearity are important. The early data in the inset of Figure 7a show a good potential for a linear response by this device structure.

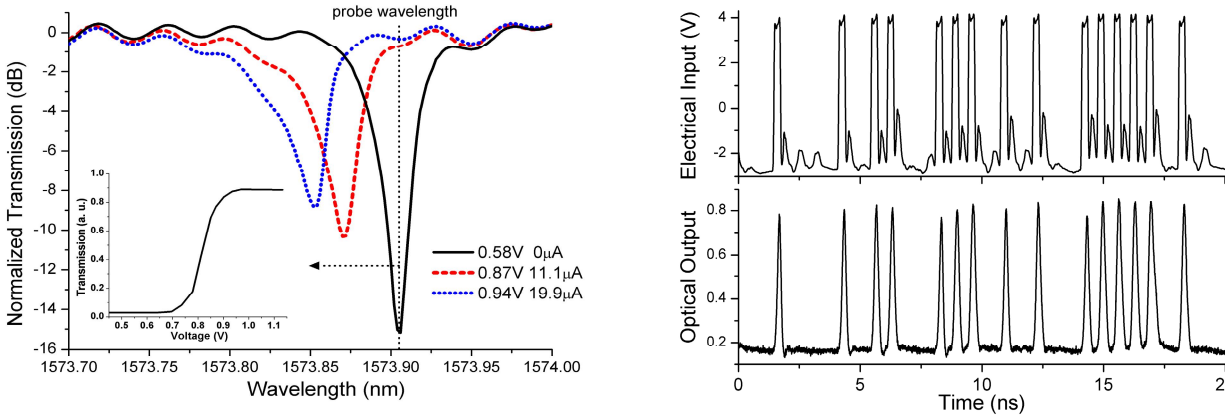

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Figure 7: Performance of Si ring modulator: (a) change in ring resonant wavelength with injection, inset shows full extinction with <1V bias; (b) electrically driven optical pulses to give 1.5Gb/s RZ data rate.

3.3. Optical filter

The optical filter in our circuit is designed to achieve precision frequency channels [4]. It is based on a ring resonator design with high Q and a higher order, Mach-Zehnder, filter configuration to give narrow channel definition. The performance specifications are size, channel shape (1.5dB and 25dB channel widths), center frequency, and insertion loss. These ultra-high resolution filters must deliver ~1GHz channel widths compared to ~100GHz for Wavelength Division Multiplexing applications in telecommunications. Figures 8a and 8b show the channel specification and the degradation of channel shape induced by waveguide loss. Besides a dramatic increase in insertion loss, the pass-band is rounded and broadened, and the stop-band is reduced.

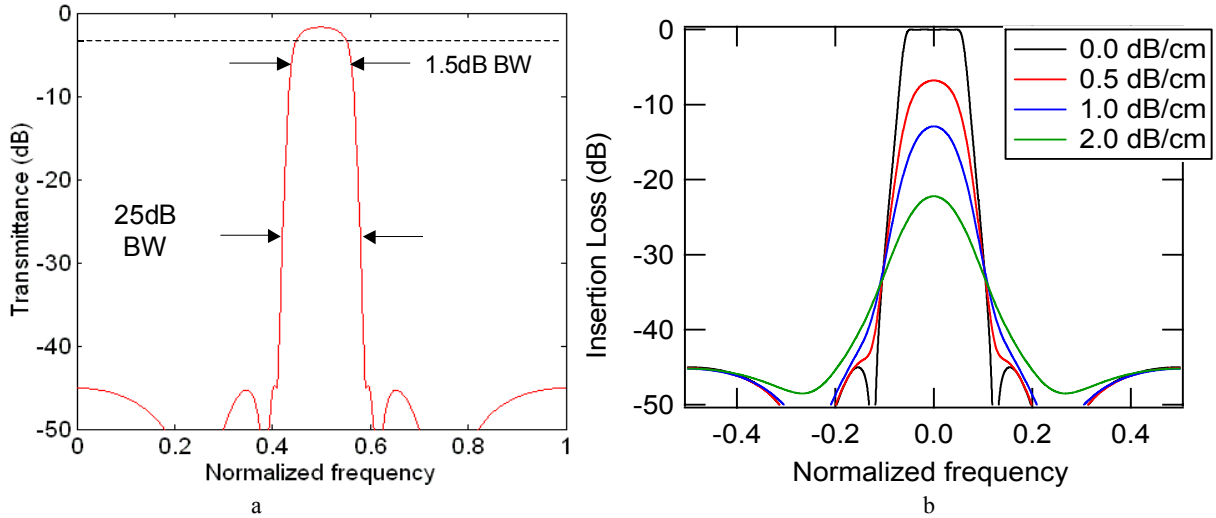

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Figure 8: Optical filter design: (a) channel shape specifications; (b) role of waveguide loss in channel shape.

Even though CMOS pattern transfer is capable of very high fidelity, it is not likely that wafer level uniformity can be achieved in the design and process development stage. In addition, integrated filter arrays cannot be 'binned' by performance as discrete devices can. A fault-tolerant, robust design must include provision for both trimming and tuning for optimum performance. We have previously demonstrated a frequency trimming capability using measured UV exposure to a polysilane clad layer [5]. In this program we have fabricated several filter design iterations in the BAE Systems CMOS foundry. We find that the CMOS platform is capable of precision thermo-optic tuning using the multi-layer, back-end CMOS metallization for heater placement. We have also demonstrated lossless thermo-optic switching in these circuits. The details of these achievements will be reported shortly. In summary, we have shown through process runs in the BAE Systems CMOS foundry that the CMOS architecture and process technology is compatible with the highest level of optical filter performance and that it provides a path to unprecedented densities of E-P integration.

3.4. Photodetector

Germanium is the ideal material for photodetector integration with CMOS electronics. It is compatible with silicon, forming a complete solid solution, and its bandgap is smaller than silicon, making it absorbent to wavelengths of light that flow with no loss in silicon waveguides. In addition, germanium is a high performance detector material [6]. Carrier mobilities are approximately 4 times higher than in silicon and the band structure is a highly absorbing direct gap near the 1550nm telecommunications standard wavelengths. The recently demonstrated ability to grow virtually dislocation-free Ge-on-Si makes true CMOS integration feasible because thick graded buffers are no longer required. Figure 9 shows a Ge photodetector performance design diagram. The traditional FOM for detector performance is the (bandwidth x quantum efficiency) product. For E-P integration the metric of footprint is added. Waveguide detector integration has the benefit of perfect focusing and impedance matching of the photon flux with the detector. There are two primary benefits. First, the detector size can be made as small as the waveguide cross-section. For single mode silicon waveguides operating at 1550nm, typical widths are 0.5-1μm. The detector length can be >100μm before device RC time constants begin to limit speed. Second, the waveguide-detector coupling can be designed for p-i-n detectors with ultra short transit distances.

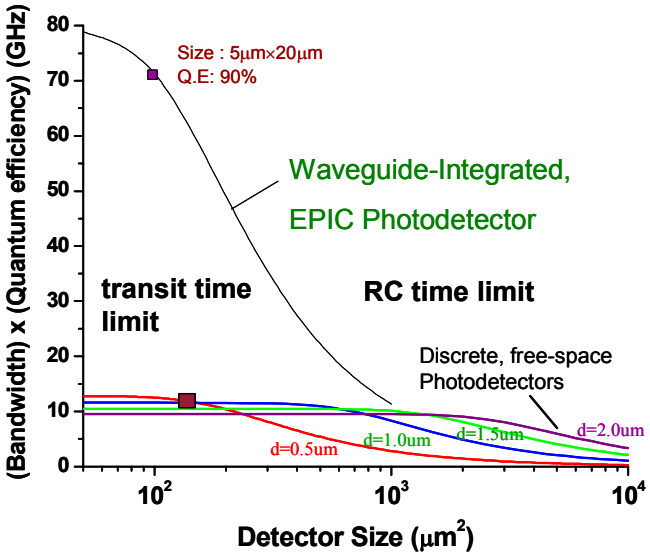

Figure 9: Design plot for Ge-on-Si photodetector integration. EPIC detectors will be smaller, faster with higher quantum efficiency.

The benefits of these attributes are dramatically demonstrated in Figure 10. The design constraints for integrated photodetectors are wavelength of operation, responsivity, size, speed, and waveguide coupling efficiency.

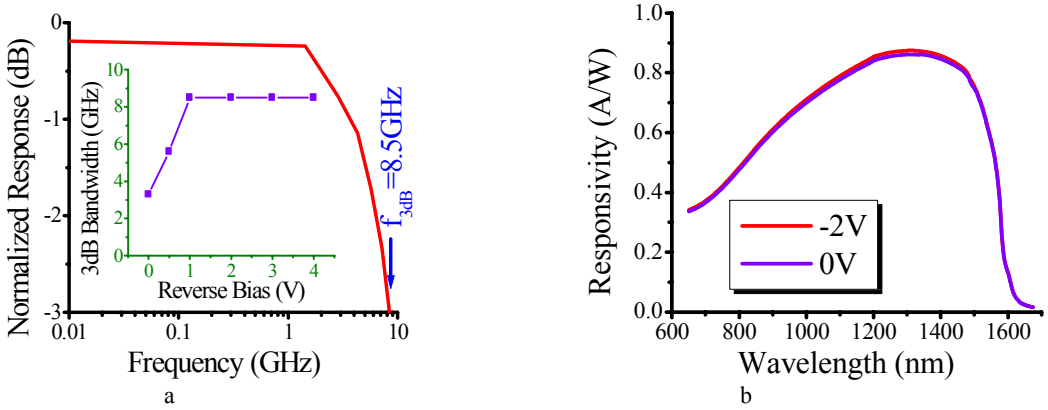

Figure 10: Ge-on-Si photodetector performance: (a) frequency response with inset showing 1V operation; (b) responsivity spectrum showing near ideal behavior for both biased and unbiased operation.

We have previously demonstrated Ge photodetectors with a broad detection spectrum of 650-1605nm that has been extended to 1625nm by strain engineering [7]. The internal quantum efficiency is greater the 90% over the range of 650-1340nm. The detector speed has been measured as a bandwidth of 8.5GHz at 980nm and 2.5GHz at 1550nm. The ultra thin transit region allows full performance at V_R<1V. Figures 10a and 10b show the measured speed and responsivity spectrum. The key to CMOS integration is the 'bufferless' Ge-on-Si deposition process. The main elements of the process are a two-step UHV-CVD growth and a post-deposition defect removal anneal. These Ge-on-Si detectors are currently the best performing Ge photodetectors of any kind.

At MIT we have designed, fabricated and tested waveguide-coupled detectors to create design rules for the EPIC program. Figure 11 shows the performance of silicon detectors with SiON waveguides where the refractive index of the waveguide was controlled by nitrogen composition. The results confirm our designs: for evanescent coupling the coupling efficiency and coupling length increase with decreasing index difference between waveguide and detector. For an index difference of 2 we have demonstrated 80% coupling efficiency for a 100μm long detector. We expect that for the lower index difference of the EPIC circuit ($n_{Si} - n_{Ge} = 0.5$) the coupling efficiency will approach 100% with a coupling length well below 50μm.

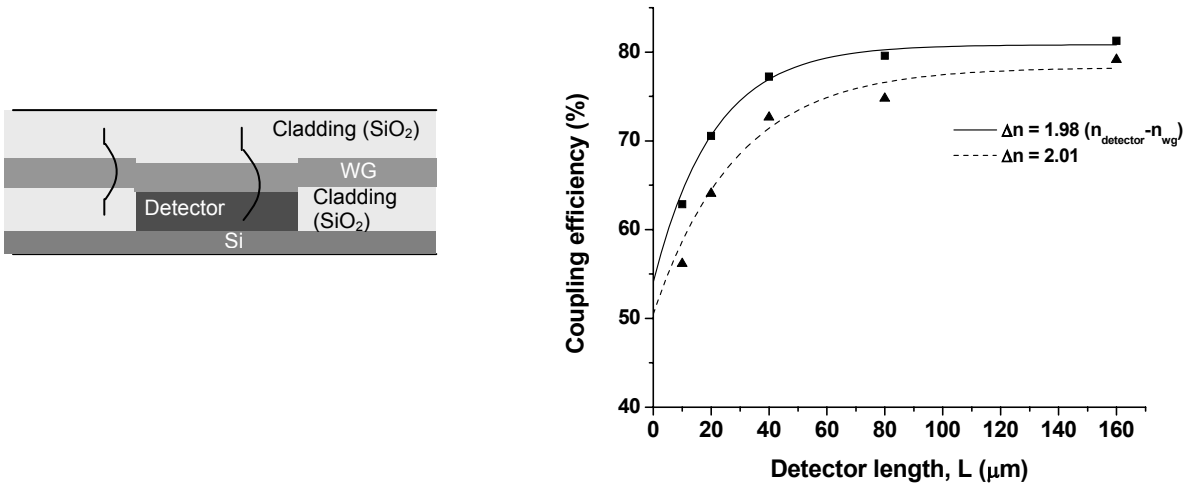

Figure 11: Schematic and performance of waveguide-coupled detectors for two waveguides with different index. The index difference between detector and waveguide representing the solid graph is 1.98, while the index difference for the dashed graph is 2.01. The higher index waveguide (lower Δn) shows a faster coupling to the detector and a higher coupling efficiency.

3.5. E-P circuit integration

Several important issues are being solved to allow high performance electronic-photonic circuit integration. Detector biases must be within the design rule for the applicable CMOS power supply voltage. The modulator driver circuit must be capable of large current swings. The heat from the high speed electronic circuits must not induce thermo-optic imbalance in the photonic circuits. The optical signal must be dielectrically isolated from surrounding electronics. Linearity in the channelization signal processor link must be maintained. We have completed robust, first order designs that provide the path to high performance.

4. CMOS PROCESS INTEGRATION

We have developed a set of design rules for our densely integrated optical signal processor chip. The metrics are number of photonic devices, number of electronic devices, size, and power dissipation. Process integration adds an additional set of constraints. Figure 12a shows a schematic CMOS chip cross-section that consists of a wafer level FET device 'front end' and a multilevel interconnection 'back end'. We define E-P CMOS integration as optimum placement of electronic and photonic devices in all levels to achieve the densest, highest performance process-compatible layout.

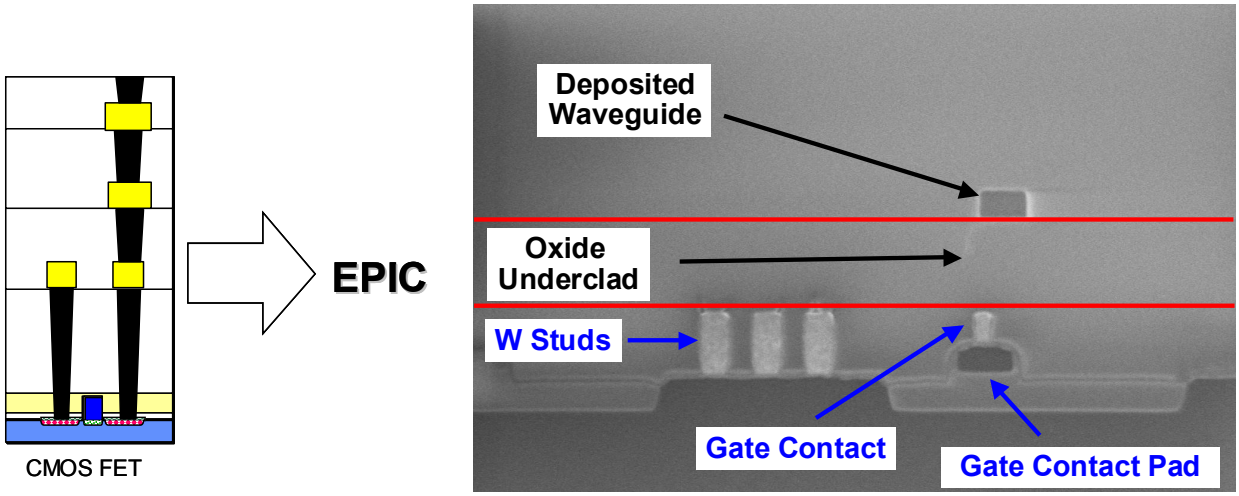

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Figure 12: Implementation of EPIC architecture in the BAE Systems CMOS foundry: (a) schematic of the multilevel, planarized CMOS architecture; (b) SEM micrograph of EPIC chip cross-section showing waveguides, transistors, contacts, and interconnection.

As mentioned earlier, we have found that the accuracy of 0.18 μm CMOS layout has yielded great benefits in precision thermo-optic tuning of our optical filter circuit. We determined the 3-D layout by executing tradeoffs among several options. Figure 12b shows an SEM cross-section of one such layout. For electrical isolation, the placement of junctions and dielectrics must preserve performance of the electrical circuits while allowing integral processing of active and passive photonic devices. Optical isolation from the substrate must be achieved while maintaining an epitaxial template for Ge growth. Inter-level isolation must be achieved by both layer thickness and lateral offsets. Electrical access to all levels must be maintained with plugs and vias that are designed with achievable aspect ratios. Both evanescent and butt optical coupling are employed in both horizontal and vertical directions. We have limited materials selection to Si, SiO_2, Si_3N_4, Ge, and SiGe. The current use of Ge in CMOS is at the Si-rich end of the SiGe alloy composition, while our chip is exclusively at the Ge-rich end. The thermal budget sequence for our level-by-level CMOS processing dictates that upper levels have lower process temperatures than lower levels, and that, to the extent possible, heat treatments be integrated with processes to minimize thermal excursions. Since E-P integration is not a simple extension of CMOS pattern transfer, contamination issues must be overcome for nearly every process qualification.

5. CONCLUSIONS

We have created early designs and process implementations in the BAE Systems CMOS foundry for the development of an Application Specific Electronic Photonic Integrated Circuit (AS-EPIC). Our chip will perform an RF channelization function that is equivalent to a Fast Fourier Transform in the frequency regime. We have produced device design rules, process integration design rules, and an optical signal processor link consisting of a waveguide, an optical modulator, an optical time domain filter, couplers, and photodetectors for CMOS implementation. The devices and circuits tested thus far perform at state-of-the-art levels. The silicon waveguides have a transmission loss of 0.35dB/cm for single crystal SOI and 4dB/cm for CVD-deposited, polycrystalline structures. The optical filter has narrow bandwidth with precision thermo-optic tuning and lossless thermo-optic switching. The silicon ring-resonator modulator has a 1.5 Gb/s digital performance, an extinction ratio of 15dB, a diameter of 10-12μm, and an ac power dissipation of 3mW. The germanium photodetector has a bandwidth of 2.5GHz with a responsivity of >0.8A/W under an applied bias of <1V at a photon wavelength of 1500nm.

The EPIC program is breaking new ground in both E-P integration and in performance. The continued success of this program should provide a size, weight, power, and cost shrink path for microwave signal processing while simultaneously enabling higher performance. Similarly, the commercial deployment of this technology will likely be advanced by as much as ten years. The tremendous progress we have already achieved with the demonstration of low loss silicon waveguides and adaptive optical filters fabricated on the BAE Systems CMOS production line combined with the promise of future integration with already demonstrated, CMOS-compatible modulator and detector building blocks bodes well for the successful demonstration of the full EPIC capability envisioned by DARPA MTO.

6. ACKNOWLEDGEMENTS

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