Technology and Device Scaling Considerations for CMOS Imagers

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Abstract— **This paper presents an analysis of the impact of device and technology scaling on active pixel CMOS image sensors. Using the SIA roadmap as a guideline, we calculate the device characteristics that are germane to the image sensing performance of CMOS imagers, and highlight the areas where the CMOS imager technology may need to depart from "standard" CMOS technologies. The impact of scaling on those analog circuit performance that pertain to image sensing performances are analyzed. Our analyses suggest that while "standard" CMOS technologies may provide adequate imaging performance at the 2–1 μm generation without *any* process change, some modifications to the fabrication process and innovations of the pixel architecture are needed to enable CMOS to perform good quality imaging at the 0.5 μm technology generation and beyond. Finally, the challenges to the CMOS imager research community are outlined.**

I. Introduction

ACTIVE Pixel Sensors (APS) using "standard" CMOS technologies [1]–[4] (hereinafter referred to as "CMOS imagers") have attracted much attention in the past few years [5]–[12]. The advantages of CMOS imagers are: 1) low voltage operation and low power consumption, 2) compatibility with integration on-chip electronics, (control logic and timing, image processing, and signal-conditioning such as A/D conversion), 3) random access of the image data, and 4) potentially lower cost as compared to the conventional CCD. Low power consumption is achieved for CMOS imagers: a) because only one row of pixels needs to be active during the readout [8] and b) because of low voltage operation. Integration of on-chip timing, control, signal chain, and analog-to-digital converter electronics lowers sensor system cost since these components must otherwise be supplied and assembled with the sensor chip. The lower cost of CMOS imagers derives from the *assumption* that the cost of technology development will have been amortized by the huge sales volume of "standard" CMOS logic and memory chips (for which the technology is developed). Other advantages of CMOS imagers include much lower system power requirements (enabling mobile applications) and low voltage operation.

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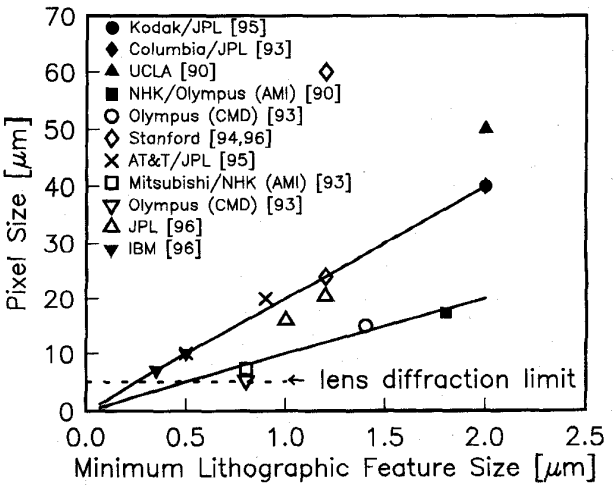

Fig. 1. Scaling trend of CMOS imager pixel size. Symbols are experimental data reported in the literature. The line represents linear scaling. The upper solid line shows pixel size scaling as $20L_g$ (typical of 4-transistor photogate designs), the lower solid line shows pixel size scaling as $16L_g$ (typical of 3-transistor photodiode designs). L_g is the minimum lithographic feature size.

CMOS imagers with reasonable image quality have been demonstrated in recent years using "standard" CMOS technologies [10] (Fig. 1). Most of the experimental work on CMOS imagers to date [13]–[33] employed relatively "old" technologies (channel lengths greater than 1 μm). On the other hand, the industry standard CMOS technology is 0.5 μm since 1993 and leading-edge 0.35 μm technology is being deployed generally across the industry in 1996 [34].

As CMOS technologies evolve at the unabated pace of 0.7× of the minimum feature size every three years, certain important device characteristics do change as the technology is scaled. While the industry standard CMOS technology has been developed to optimize the power-delay, reliability, and cost-performance of logic and memory circuits, some device characteristics that are germane to the imaging application have not been addressed as the technology evolves; and it is not so clear that CMOS imagers will continue to benefit from device scaling.

In this paper, we explore the question: "*Will the image sensing performance of CMOS imagers get better or get worse as CMOS technologies are scaled?*" Emphasis is placed on the impact of device characteristics on pixel architectures that utilizes either the p/n junction photodiode or the MOS photogate as the sensor element, with active transistors within the pixel to convert photo-charges to electrical output signals.

TABLE I

PRINCIPAL WAFER FABRICATION CHARACTERISTICS. DRAM HAS TRADITIONALLY BEEN THE TECHNOLOGY DRIVER. SRAM IS ALSO SHOWN BECAUSE IT RESEMBLES THE CMOS IMAGER ARCHITECTURE IN THAT SEVERAL TRANSISTORS ARE NEEDED WITHIN EACH CELL, HOWEVER, SRAM REQUIRES NO PHOTOSENSITIVE AREAS AND MINIMAL CHARGE STORAGE AREA. THE INFORMATION IS ADAPTED FROM THE SIA ROADMAP [37] AND VARIOUS CMOS LOGIC TECHNOLOGIES ACROSS THE INDUSTRY

Year of 1st DRAM shipment	1980	1983	1986	1989	1992	1995	1998	2001	2004	2007	2010
Minimum lithographic feature size (0.7×/generation) [μm]	2	1.5	1.0	0.7	0.5	0.35	0.25	0.18	0.13	0.1	0.07
DRAM bits/chip (4×/generation)	64K	256K	1M	4M	16M	64M	256M	1G	4G	16G	64G
DRAM chip size (1.5×/generation) [mm^2]	27	40	60	90	130	190	280	420	640	960	1400
DRAM cell size (0.4×/generation) [μm^2]	146.3	58.5	23.4	9.375	3.75	1.5	0.6	0.24	0.096	0.038	0.015
SRAM bits/chip (4×/generation)	16K	64K	256K	1M	4M	16M	64M	256M	1G	4G	16G
SRAM chip size (1.5×/generation) [mm^2]	31	47	70	100	150	220	330	490	740	1100	1600
SRAM cell size (0.4×/generation) [μm^2]	781	313	125	50	20	8	3.2	1.3	0.52	0.21	0.08
CMOS imager pixel size (0.7×/generation) [x μm × x μm]	40	28	20	14	10	7	5	5 (3.5)	5 (2.45)	5 (1.72)	5 (1.2)
CMOS imager fill factor [%]	25	25	25	25	25	25	25	63 (25)	82 (25)	91 (25)	96 (25)
Imager format/size (for HDTV & SVGA)					1"		2/3"		(1/3")		
Imager format/size (for NTSC-TV & VGA)		1"		2/3"		1/3"	1/4"				

Our analyses suggest that while "standard" CMOS technologies may provide adequate imaging performance at the 2–1 μm generation without *any* process change, some modifications to the fabrication process and innovations of the pixel architecture are needed to enable CMOS to perform good quality imaging at the 0.5 μm technology generation and beyond.

The impact of scaling on those analog circuit performance that pertain to the image sensing performance will be analyzed. Examples of quantities of interest include power supply, threshold voltage, analog voltage swing, charge-to-voltage conversion gain, charge capacity, dynamic range, etc.

II. CMOS SCALING

The evolution of CMOS technology has been governed by device scaling for the past twenty years [35] and [36]. In the past, the minimum lithographic feature size has been decreasing by 0.7 times every three years, while the chip size has been increasing at 1.5 times every three years. Technology drivers such as DRAM increases in the bits/chip by 4 times every 3 years.

Table I shows the principal wafer fabrication characteristics, using DRAM and SRAM as examples, and Table II shows the principal device technology and electrical characteristics for logic applications for minimum feature sizes from 2–0.07 μm [37]. The entries in Tables I and II corresponding to 1995 and beyond represent a prediction of the industry trend using assumptions as described in the SIA Roadmap [37]. The analyses in Sections III and IV will use the technology and device parameters illustrated in Tables I and II as a guideline.

III. TECHNOLOGY AND DEVICE PERFORMANCE

A. Pixel Size

The scaling of the CMOS imager pixel size is shown in Table I. The pixel size as a function of the minimum feature size reported by various researchers is plotted in Fig. 1. The trend basically follows the projections of Table I. Fig. 2 illustrates two pixel layouts using a 0.5 μm and a 0.35 μm technology. The pixel size and the photosensitive fill-factor scale linearly with the minimum feature size. Pixel design cleverness is not expected to provide more than a 50% improvement in pixel size or fill-factor [38]. It has been generally acknowledged that further decrease in the pixel size much beyond 5 μm × 5 μm is not needed because of the diffraction limit of the camera lens. Therefore, CMOS imagers will benefit from further scaling after the 0.25 μm generation only in terms of increased fill-factor and/or increased signal processing functionality within a pixel.

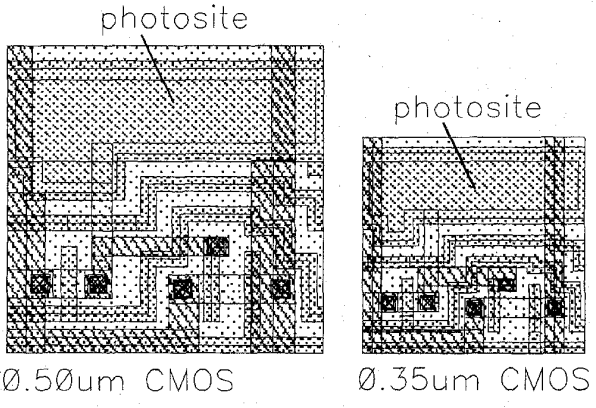

Fig. 2. Example layout for a 0.5 μm technology (10 μm pixel) and 0.35 μm technology (7 μm pixel).

B. Photo-Charge Collection

Carriers generated by photons within the depletion region are collected completely by the sensing element. Carriers generated by photons in the neutral bulk semiconductor are collected by the sensing element via diffusion of the minority carrier, which is characterized by the diffusion length, $L_{diff} = \sqrt{D\tau}$, where D is the diffusion constant and τ is the carrier lifetime [39] and [40].

Both the mobility and the carrier lifetime decrease with scaling due to the increase of the substrate doping. Fig. 3 shows the minority carrier diffusion length as a function of device technology generation (calculated using the empirical

TABLE II
PRINCIPAL DEVICE TECHNOLOGY AND ELECTRICAL CHARACTERISTICS. THE INFORMATION IS ADAPTED FROM THE SIA ROADMAP [37] AND VARIOUS CMOS LOGIC TECHNOLOGIES ACROSS THE INDUSTRY

Year of 1st DRAM shipment	1980	1983	1986	1989	1992	1995	1998	2001	2004	2007	2010
Minimum lithographic feature size [μm]	2	1.5	1.0	0.7	0.5	0.35	0.25	0.18	0.13	0.1	0.07
Nominal L_{eff} [μm]	1.6-2.0	1.2-1.5	0.8-1.0	0.6-0.7	0.42-0.5	0.28-0.35	0.2-0.25	0.14-0.18	0.1-0.13	< 0.1	< 0.1
Isolation	LOCOS	LOCOS	LOCOS	LOCOS	LOCOS	LOCOS, STI	STI, SOI	STI, SOI	STI, SOI	STI, SOI	STI, SOI
Gate oxide [nm]	41-71	29-50	20-35	14-24	10-17	7-12	4-6	4-5	2.7	1.9	1.9
Gate electrode	n^+ poly	n^+ poly	n^+ poly, silicide	n^+ poly, silicide	n^+, n^+/p^+ poly, silicide	n^+, n^+/p^+ poly, silicide	n^+, n^+/p^+ poly, silicide	n^+, n^+/p^+ poly, silicide	n^+, n^+/p^+ poly, silicide	n^+, n^+/p^+ poly, silicide	n^+, n^+/p^+ poly, silicide
Substrate doping [cm^{-3}]	10^{16}	2×10^{16}	4×10^{16}	8×10^{16}	1.2×10^{17}	2.5×10^{17}	3.4×10^{17}	5×10^{17}	7×10^{17}	1×10^{18}	2×10^{18}
Source/drain junction	abrupt	abrupt	LDD	LDD	LDD	LDD, S/D ext	LDD, S/D ext, raised S/D	LDD, S/D ext, raised S/D	LDD, S/D ext, raised S/D	LDD, S/D ext, raised S/D	LDD, S/D ext, raised S/D
Source/drain junction depth [μm]	0.5-0.6	0.45-0.55	0.4-0.5	0.35-0.45	0.3-0.4	0.2-0.3	0.1-0.15	0.07-0.13	0.05-0.1	< 0.07	< 0.05
Power supply [V]	5	5	5	5	5/3.3	3.3/2.5	2.5/ 1.2-1.8	1.2-1.8	1.2-1.5	< 1.2 (with SOI)	< 1.2 (with SOI, double-gate)
Threshold voltage variation [$\pm$ mV]	170	125	80	75	70	60-70	50	40	30	25	20
Threshold voltage [V]	1.0	0.9	0.8	0.7	0.6	0.5	0.45	0.4	0.3	0.3	0.3

expressions for minority carrier mobility and lifetime of [41] and [42]). The minority carrier lifetime is inversely proportional to the substrate doping at the doping levels of interest, while the mobility slowly decreases with increasing substrate doping. Therefore, the diffusion length scales almost linearly with the minimum feature size. The ratio of the diffusion length to the pixel size remains fairly constant until the pixel size ceases to scale with the minimum feature size (Fig. 4), which suggests that modulation transfer function (MTF) degradation (cross-talk) due to carrier diffusion should be fairly similar among various technology generations until the pixel size ceases to scale.

CCD technologies have always customized the fabrication process to properly position the junctions and depletion depths for optimal spectral sensitivities and minimum cross-talk (see, for example, pinned photodiode for interline CCD [43]). If "standard" CMOS technologies are used to build image sensors, then one needs to pay attention to the location and depth of the photodiode junctions and the depth of the depletion region of the photogate since they determine the spectral sensitivity and optical cross-talk of the image sensor. Fig. 5 plots the edge of the depletion region (junction depth plus the depletion depth of a source/drain diode at V_{DD} reverse bias for a photodiode, and the gate induced depletion depth for a photogate) versus the minimum feature size. Comparing Fig. 5 with the absorption length of visible light in silicon (Fig. 6) [44], it is apparent that for CMOS imagers, most photo-carriers are not generated in the depletion region, but rather in the neutral region, and most photo-carriers are collected via carrier diffusion, allowing for the possibility of cross-talk. This nonoptimal carrier collection situation for a "standard" CMOS process gets worse as CMOS is scaled down.

C. Isolation

At around the 0.35 μm generation, the isolation technology begins to shift from the conventional LOCOS to STI (shallow trench isolation) because of the narrower isolation width achievable with STI [45]. STI is typically 0.5 μm deep, filled with CVD oxides. Both electrically and optically, STI will not be much different from LOCOS, except that STI has the potential to be extended deeper than currently implemented to reduce carrier diffusion across pixels and thus improve the MTF.

D. SOI Substrates

Beyond the 0.25 μm technology, the use of SOI substrates seems imminent. The impact of SOI substrate are found

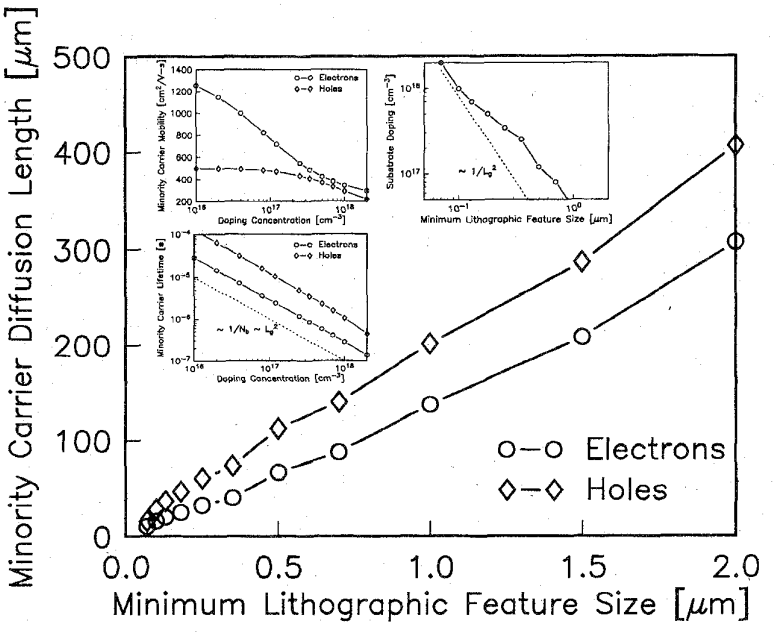

Fig. 3. Minority carrier diffusion length scales linearly with L_g.

in the: 1) charge collection volume, 2) isolation, 3) parasitic capacitances, and 4) substrate contacts. Typical SOI designs (depending on whether it is partially depleted or fully depleted) uses 40–200-nm thick silicon films [46]. At the outer limits of device scaling (0.07 μm technology and beyond), where the double gate MOSFET is required [47], the silicon film thickness is less than 25 nm. This means that the photo-charge collection volume for SOI substrates will be drastically reduced from the bulk substrate case, especially for long wavelength photons (Fig. 7). On the other hand, SOI technology offers full dielectric isolation between devices, and a significant improvement in MTF is expected due to the elimination of carrier diffusion from neighboring pixels. The smaller parasitic capacitances of SOI as compared to bulk substrates [48] is a clear advantage in terms of fixed pattern noise, power, clock feed-through, and charge-to-voltage conversion sensitivity. At this point, the substrate contact for SOI is still an active research topic. It is not clear that the SOI technology developed in the future will have substrate contacts or not and, if there are substrate contacts, how it is implemented. For SOI CMOS imagers, a means to drain away the photon-generated charge (similar to the substrate contact in bulk CMOS) is a necessity.

E. Spectral Sensitivity

The spectral sensitivity of the MOS photogate and the pn junction of the photodiode are largely determined by the gate electrode and junction materials and technologies, respectively. Beyond the 0.5 μm generation, CMOS logic is migrating to silicide technologies.

Silicides are fairly opaque to visible light (400–700 nm) as compared to doped-polysilicon. The absorption length (depending on process conditions) of titanium silicide at 633 nm wavelength is only 20 nm [49] compared to the absorption length of 0.2–5 μm for typical phosphorus doped polysilicon [50]. The typical silicide thickness employed in 0.25 μm technologies [45] is about 40–50 nm. This means that only about 10% of the light is transmitted to the silicon substrate, resulting in a significant reduction of photo-sensitivity of the sensor. Fig. 8 compares the spectral transmission of thin polysilicon with $TiSi_2$ and $CoSi_2$ at thicknesses commonly employed for advanced technologies.

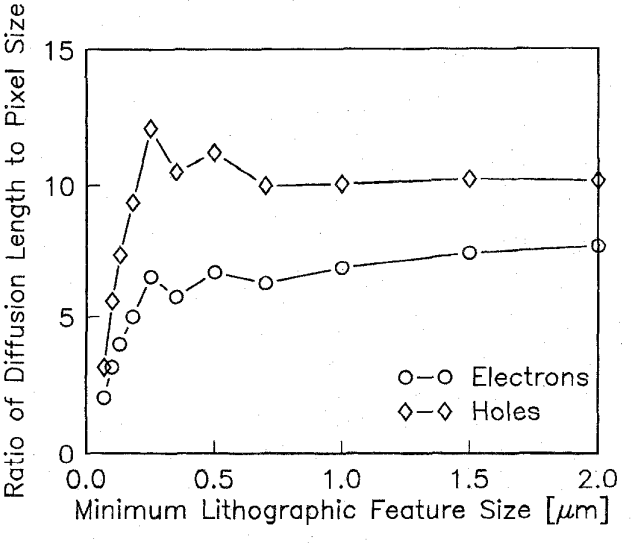

Fig. 4. The ratio of minority carrier diffusion length to the pixel size as a function of L_g.

F. Parasitic Currents

Several parasitic currents begin to increase rapidly as devices are scaled—some due to the fundamental physics, others due to shrinking design space as devices are scaled. These

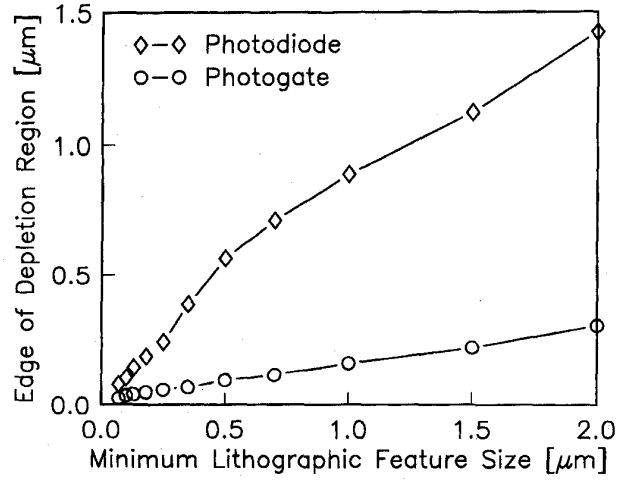

Fig. 5. The location of the edge of the depletion region as a function of L_g.

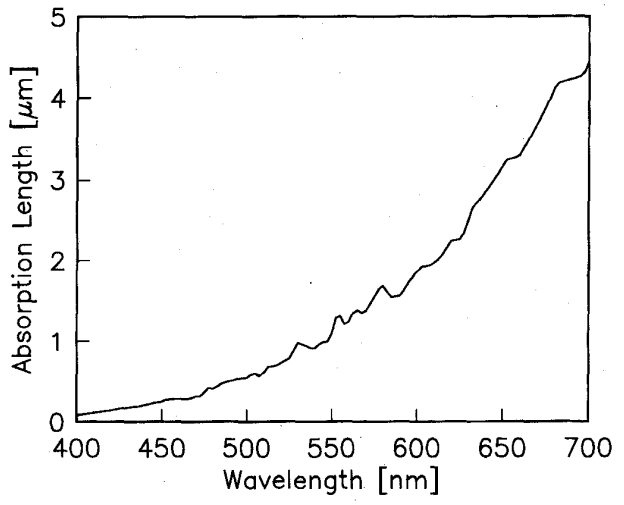

Fig. 6. Light absorption length in silicon. Data from E. Palik [44].

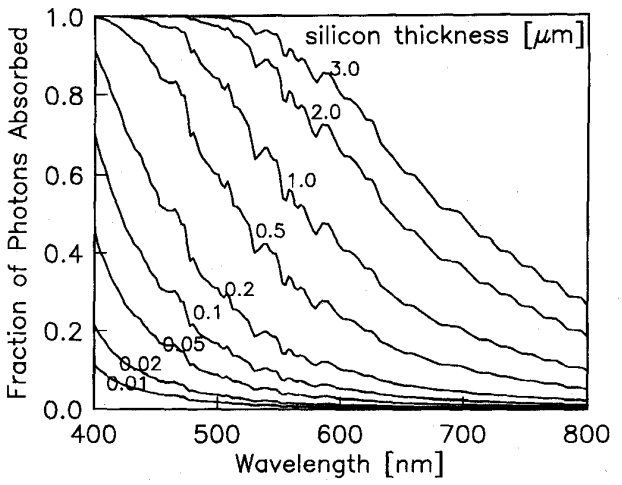

Fig. 7. Fraction of light absorbed in the SOI substrate for various SOI thickness. Data were calculated from silicon absorption data from E. Palik [44].

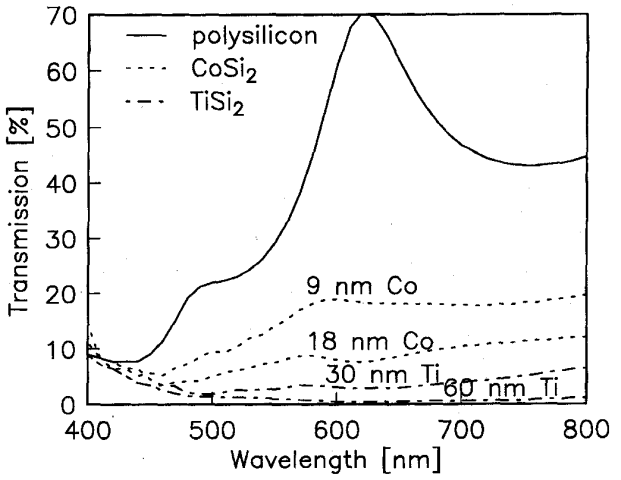

Fig. 8. Measured spectral transmission of: (a) 150 nm polysilicon and 150 nm polysilicon reacted with (b) 30 nm titanium, (c) 60 nm titanium, (d) 9 nm cobalt, and (e) 18 nm cobalt to form silicides. Films were deposited on quartz wafers in this measurement.

parasitic currents are sources of shot noise and should be minimized.

1) Dark Current: Dark current should remain fairly constant with technology and do not degrade imager performance as devices are scaled. For fully-depleted SOI devices, the back interface is typically poorer than the front interface (for SIMOX wafers) and dark current is expected to be larger. A typical value of dark current for bulk substrate is about 5–1000 pA/cm^2, where the lower values are obtained by surface pinning (accumulation) [51]–[54]. These values could be used as a gauge against which other parasitic currents are compared. It should be noted that CCD fabrication processes pay special attention to the reduction of dark current and it is expected that "standard" CMOS would have a larger dark current than CCD technology.

2) PN Junction Tunneling Current: Channel doping is increased as devices are scaled to smaller dimensions. The pn junction band-to-band tunneling current is estimated [36] and [55] to be about 2×10^{-14} A/cm^2 for a substrate doping of 5×10^{17} cm^{-3} at 1.8 V bias, and 500 pA/cm^2 for a substrate doping of 1×10^{18} cm^{-3} at 1.2 V bias. This means that around the 0.18–0.13 μm generations, the pn junction tunneling will begin to surpass the typical dark current observed today, and pixel architectures that employ the pn junction photodiode will have increased dark noise (with nonlinear voltage dependence) due to this tunneling current.

3) Off-Current: The off-current of a MOSFET increases significantly with device scaling to smaller sizes. This is because of the nonscalability of the subthreshold slope. As power supply voltages are scaled down, the threshold voltage is also scaled down to maintain current drive. The almost constant subthreshold slope of 85 mV/dec means that the device off-current increases exponentially when the threshold voltage is decreased. Fig. 9 illustrates the estimated off-current for advanced CMOS technologies optimized for high performance

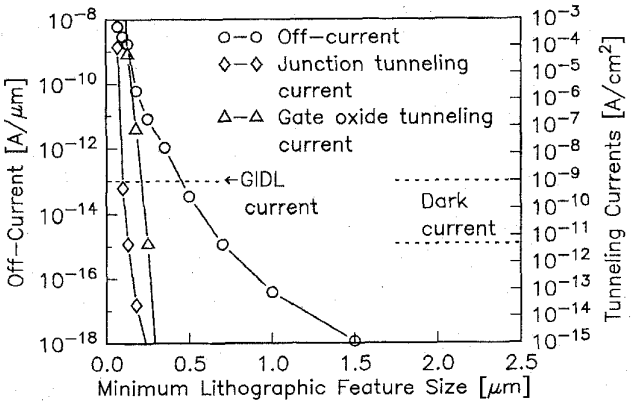

Fig. 9. Parasitic currents of MOSFET. The peak substrate current is $1\,\mu A/\mu m$ and is off the left scale. Junction tunneling current and off-current were calculated using expressions described in Sections III-F-2 and III-F-3; gate oxide tunneling current was compiled from experimental measurements in [57].

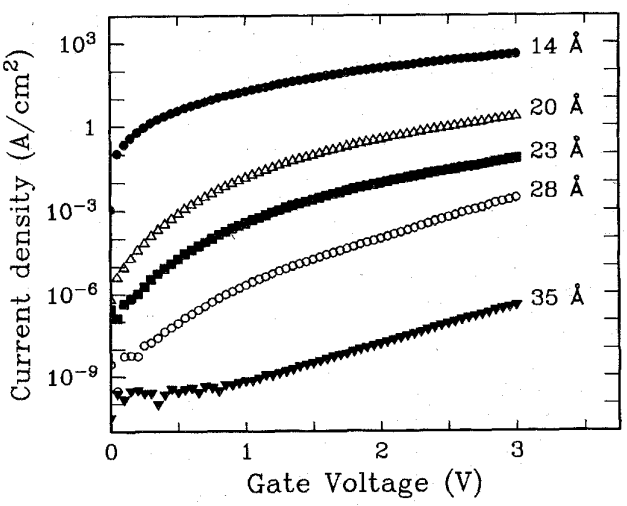

Fig. 10. After Buchanan and Lo [57]. Tunneling current density versus gate voltage for polysilicon gate capacitors with gate oxide thickness ranging from 1.4–3.5 nm measured at accumulation.

(assuming the threshold voltage to be scaled as aggressively as possible and a subthreshold slope of 85 mV/dec). Designing pixels with channel lengths longer than the minimum channel length will avoid off-current due to drain-induced barrier lowering (DIBL) but the nonscalability of the subthreshold slope remains.

The impact of off-current depends on the pixel architecture. Some pixel architectures employ a transistor to reset the high impedance charge-to-voltage conversion node, others have a switch or DC biased transfer gate isolating the high impedance node. Signal charge will leak from this node through these transistors even though these transistors are biased "off." For pixel architectures where the gate-to-source voltage of the "off" transistor (n-channel) is negative, the off-current problem is much reduced.

The present CMOS technology trend is to engineer the threshold voltage (multiple threshold voltages on the same chip) to optimize the power-performance of the chip [36] and [56]. This may bring some relief to CMOS imager designers.

4) Gate Current: Advanced CMOS technologies have always been optimized to minimize the gate current due to hot-carrier effects. However, as the minimum feature size approaches $0.18\,\mu m$, the gate oxide thickness required (see Table II) approaches the direct tunneling regime. At 2.8 nm oxide thickness, the experimental tunneling current is $1\,\mu A/cm^2$ at 1 V gate bias [36], [57], and [58] (Fig. 10). This value is 4 orders of magnitude larger than the typical dark current density.

Depending on the pixel architecture, the gate current may affect the photo-charge during signal integration (as in an MOS photogate) and/or during readout (e.g., signal charge may leak out from the high impedance charge-to-voltage conversion node).

During charge integration, photo-gates are pulsed into deep depletion during photon integration and thus a good fraction of the gate voltage will be dropped across the silicon before the silicon is inverted. This will alleviate the problem to some extent. For pixel architecture that employ signal integration [1], the readout time is much shorter than the signal integration time and the effect of gate current is correspondingly smaller. Hole tunneling current is several orders of magnitude less than electron tunneling current [59]. Thus, PMOS pixels may be used to minimize the gate tunneling current.

At present, there is a tendency to trade-off the increased gate current (and hence standby power) for higher performances [60]. It is estimated [36] that the tunneling current for a 2.5 nm gate oxide would still be acceptable for high performance ULSI systems.

5) Hot-Carrier Effects: Much effort has been put into minimizing the hot-carrier effects throughout all technology generations. The present industry standard is to keep the peak substrate current below $1\,\mu A/\mu m$ [61].

Another important source of hot-carrier induced minority carrier comes from hot-carrier-induced photon emission [62]–[65]. Hot-carrier-induced photon is more deleterious than substrate current in many ways because low energy photon can travel further in the substrate than minority carriers and conventional methods such as pn junction guard rings cannot isolate the source of photon from the photo-sensitive element. Since the active transistors are in close proximity with the photo-sensitive element in CMOS imagers, methods that rely on physical isolation (by placing the photon source away from the imaging pixels) cannot be used. Although [63] provided some indication of the extent of the problem, the full effect of hot-carrier-induced photon on CMOS imager performance has yet to be quantified. Hot-carrier effects can be effectively suppressed by not designing at the minimum gate length, since the pixel size is mainly metal pitch and contact size limited.

6) Relative Importance of Various Parasitic Currents: Fig. 9 compares the relative importance of various parasitic currents discussed in the previous sections. As an illustration, a 0.5 pA leakage current from the high impedance charge-to-voltage conversion node will result in 10 electrons noise for a $33\,\mu s$ readout time. Some of these parasitic currents may not play a significant role in certain pixel architectures. Nevertheless,

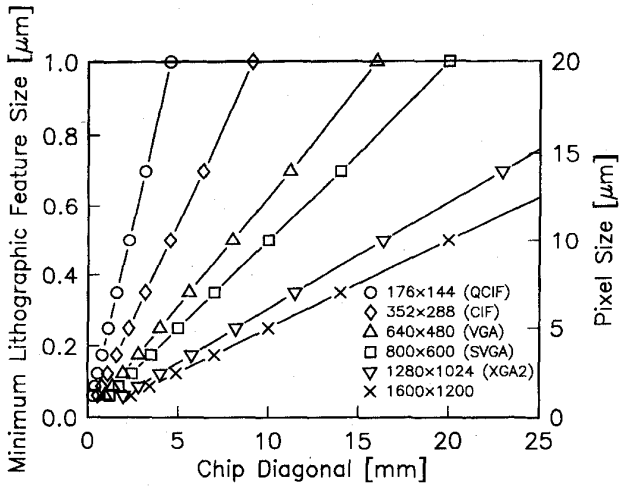

Fig. 11. Scaling trend of CMOS imager chip size.

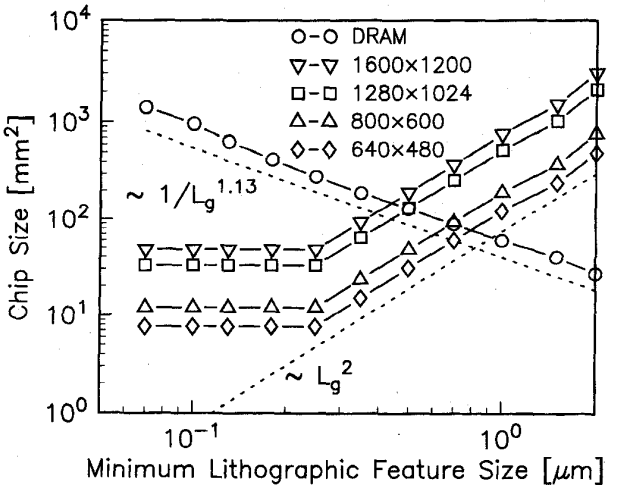

Fig. 12. The chip size of DRAM and CMOS imagers for several common formats as a function of the minimum feature size.

it does indicate that beyond the 0.13 μm generation, these parasitic currents begin to be comparable to the dark current.

G. Parasitic Capacitances

The fringe parasitic capacitance per unit length remains fairly constant throughout the generations. For example, the gate-to-drain overlap capacitance remains at about 0.2–0.3 fF/μm from 1.5–0.1 μm technology [36], [61], and [66]. The wiring capacitance per unit length also remains fairly constant at about 0.2 pF/mm independent of scaling [36]. For properly scaled pixel designs, the relative effects of parasitic capacitances should be fairly constant across technology generations.

IV. Circuit and System Performance

A. Chip Size and Integration

Fig. 11 illustrates the relation between chip diagonal and the minimum feature size for several commonly used imager formats. A practical limit of chip size from the point of view of yield and lithography tool exposure field size is about 18 mm × 18mm (25.5 mm diagonal). Imagers with a modest resolution (e.g., 1K × 1K pixels) would require technologies with 0.5 μm feature sizes and below.

Fig. 12 compares the chip size of DRAM with CMOS imagers for several commonly used imager formats. If we consider the current generation DRAM to be the largest chip that can be manufactured, then the cross-over point of the DRAM and the CMOS imager curves represent the technology generation required to manufacture the CMOS imager of that pixel count.

Technology commonality among DRAM, NVRAM, CMOS logic, and CMOS imager offers the unique opportunity of integrating memory on the image sensor. As an illustration, Fig. 13 shows the ratio of chip area that would be occupied by a full page of 8-bit DRAM to the area occupied by the pixels. This ratio is independent of the number of pixels on the sensor; it scales with $L_g^{0.75}$ when the pixel size scales with L_g, and scales with $L_g^{2.75}$ when the pixel size does not scale

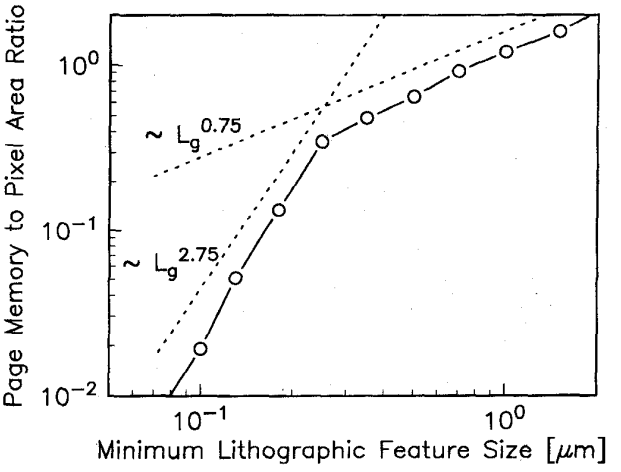

Fig. 13. The ratio of the chip area that would be occupied by a full page of 8-bit DRAM to the area occupied by the pixels. This ratio is independent of the number of pixels on the sensor as a function of the minimum feature size.

with L_g. For advanced technologies ($L_g \leq 0.18\,\mu$m), the page memory costs very little chip area.

B. Voltage Scaling

The full signal of a CMOS imager is essentially determined by the analog voltage swing. As the power supply voltage is scaled down, the analog swing decreases. There are so many pixel architectures that it is difficult to give a general expression for the analog swing. But most circuit topologies require voltage drops due to one or several V_{TH} and V_{Dsat}. Fig. 14 shows the scaling trend of the supply voltage (V_{DD}), the threshold voltage (V_{TH}), and the drain saturation voltage (V_{Dsat}) for a typical current of 10 μA and $W/L = 1/2$. For a given pixel rate, the current required is independent of scaling, therefore, we calculate (see Appendix) the V_{Dsat} for a fixed current. It is evident that as the power supply is reduced, the analog swing decreases rapidly. The voltage range for good

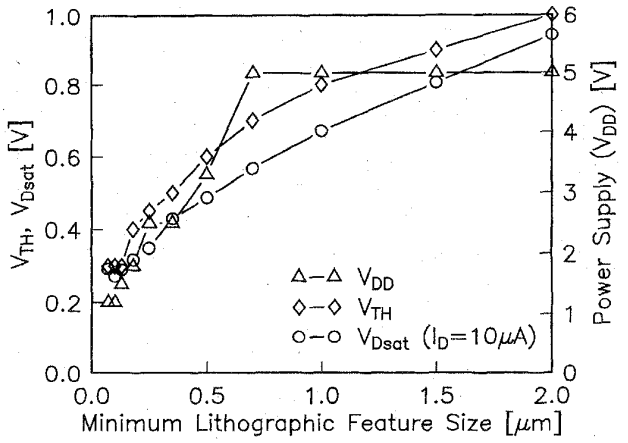

Fig. 14. The power supply voltage, threshold voltage, and drain saturation voltage as a function of the minimum feature size.

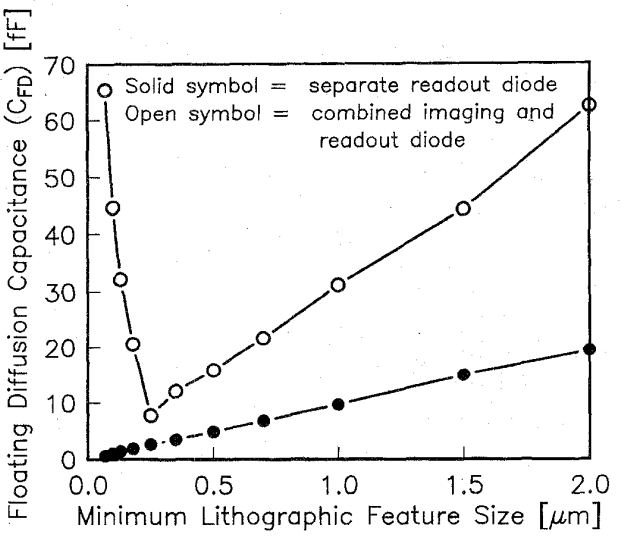

Fig. 15. Floating diffusion node capacitance as a function of the minimum feature size.

analog performance is further reduced by decreasing output resistances as the minimum feature size is decreased [67]–[69].

C. Dynamic Range

1) Signal Charge: The capacitance of the high impedance node (C_{FD}) that converts the signal charge to a voltage determines the charge conversion gain (Gain = C_{FD}^{-1}). Some pixel architectures employ a separate imaging and readout diode (e.g., photogate [14]); in other architectures the readout diode is either in parallel with or the same as the imaging diode (e.g., photodiode [3]).

The capacitance of the high impedance node (C_{FD}) scales linearly with the minimum feature size (Fig. 15). This is because both the areal ($C_{ox} \times A_{gate}$ and $C_{junction} \times A_{junction}$) and overlap ($C_{ov} \times W_{gate}$) capacitances scale linearly with the minimum feature size. As a result, high (compared to conventional CCD's) charge to voltage conversion gain (conversion gain $= 1/C_{FD}$) (Fig. 16) can be obtained as technology advances (especially true for the case where the readout diode is separate from the imaging diode), which helps to suppress referred to input noises. The C_{FD} for the case of a combined imaging and readout diode increases again at small features size after the pixel size ceases to decrease because the fill-factor increases, thus increasing the total capacitance of the imaging diode.

The full signal is the product of the conversion gain and the analog swing. Again, the analog swing depends on the pixel architecture and is difficult to generalize. Fig. 17 illustrates the full signal charge for two examples of analog swing. The decrease in full signal charge with the minimum feature size is due to the decrease of both the analog swing and the charge-to-voltage conversion node capacitance.

2) Noise Charge: Fig. 18 illustrates the scaling trend of several noise sources (see Appendix for expressions for the noise charge computation). $1/f$ noise and kTC noise can be effectively suppressed by on-chip correlated double sampling [70]. Fig. 19 illustrates the signal-to-noise ratio for the photon shot noise limited case. A S/N ratio of 50 at 20% full signal is usually regarded as good performance.

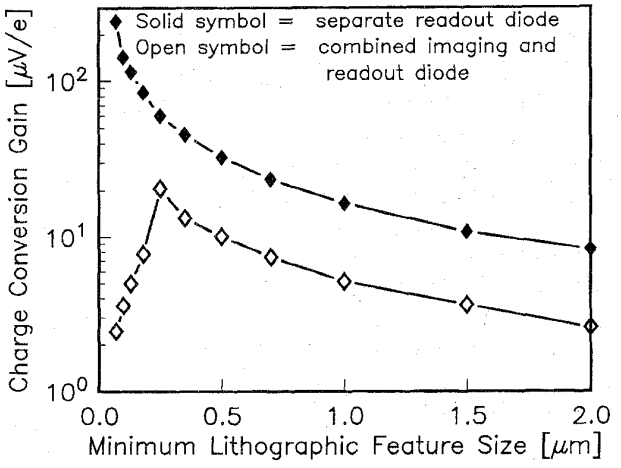

Fig. 16. Charge to voltage conversion gain as a function of the minimum feature size.

V. CMOS Imager Technology at the Limit of "Standard" CMOS Compatibility

Summarizing the discussion in Sections III and IV, we predict that CMOS imagers will begin to depart from "standard" CMOS logic and memory technologies at the 0.35–0.25 μm technology generation. This stems from the trend to use silicides on both the gate electrode and the source/drain junctions as well as the predicted trend to use SOI substrates. Furthermore, as technology advances, the need to tailor the depletion depths to maintain spectral sensitivity and reduce cross-talk becomes stronger since the depletion depths are shallower as feature size shrinks.

If CMOS imager technologies are willing to depart from "standard" CMOS technologies by tailoring the junction and/or channel implants and selectively or globally removing the silicide module from "standard" CMOS and accept the cost and/or performance degradation associated with doing so, then

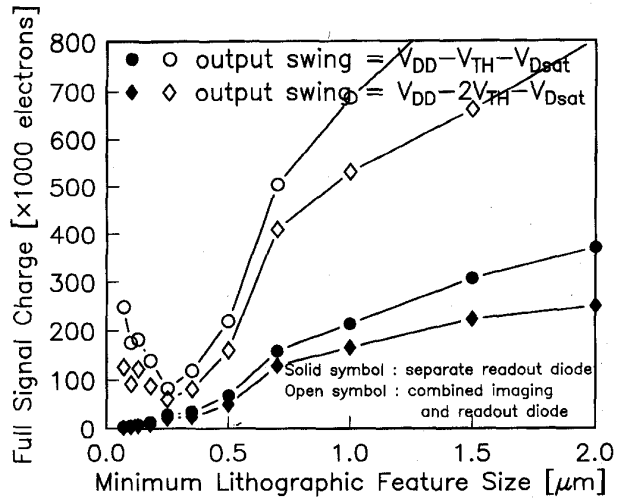

Fig. 17. Full signal charge as a function of the minimum feature size.

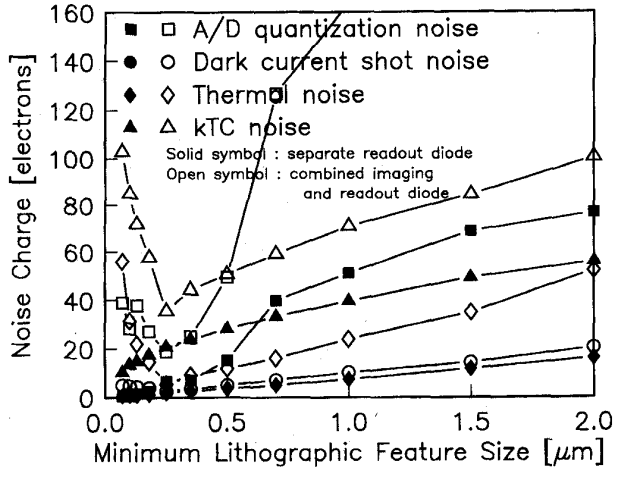

Fig. 18. Referred to input noise charges as a function of the minimum feature size. Thermal noise is calculated for a bandwidth of 30 MHz, $W/L = 4/1$, $\alpha = 10$. Dark current shot noise is calculated for a dark current of 0.5 nA/cm^2. Quantization noise is calculated for a 10-bit A/D conversion.

it is reasonable to expect that CMOS imagers can be scaled to 0.25–0.18 μm. The use of SOI substrates (beginning at the 0.25–0.18 μm generation) poses a significant problem for CMOS imagers. However, this is still an open issue even for the "standard" 0.25 and 0.18 μm CMOS, and it is reasonable to expect that there will be a mix of bulk and SOI technologies at these technology generations.

As CMOS technologies approach the 0.13 and 0.1 μm generations, off-current, gate tunneling current, and pn junction tunneling current begin to be comparable to the dark current density observed today, and both tunneling currents increase exponentially with further device scaling.

Voltage scaling imposes significant limitations on the dynamic range due to the decrease of the full signal charge capacity. Innovations in pixel circuit topologies will make a noticeable difference in extending the limitations imposed by voltage scaling.

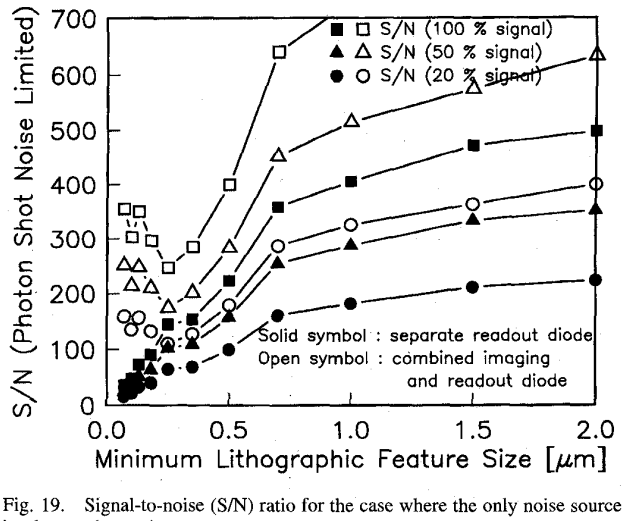

Fig. 19. Signal-to-noise (S/N) ratio for the case where the only noise source is photon shot noise.

VI. Concluding Remarks

Scaling can be beneficial (e.g., higher levels of integration) or detrimental (e.g., reduced voltage swing). This paper presents the scenario of CMOS imagers that are simply scaled without any optimization (which is unlikely in practice).

The above analyses suggest that while "standard" CMOS technologies may provide adequate imaging performance at the 2–1 μm generation without *any* process change, some modifications to the fabrication process and innovations of the pixel architecture are needed to enable CMOS to perform good quality imaging at the 0.5 μm technology generation and beyond. On the other hand, CMOS technology generations of 0.5 μm and beyond are needed to enable pixel arrays of moderate to high resolution (Table I, Figs. 11 and 12). A legitimate question to ask is: "*Will CMOS imagers eventually be left behind by the technological advancement and become a specialized technology just as costly as the CCD?*" And if the answer to the above question is affirmative, then "*What are the real advantages of CMOS imager technology compared to CCD?*"

Although our analyses suggest that there is only a technology window (0.5–0.18 μm) where CMOS imagers will (after "minor" process modifications) fit in with "standard" CMOS technologies, it does not necessarily follow that the advantages of CMOS imagers (over the conventional CCD) will disappear eventually, nor does it mean that CMOS imaging technology only has a limited useful lifespan. The reasons for the above assertion are: 1) using "standard" CMOS technologies for imaging does not automatically result in significantly lower manufacturing cost and 2) the real advantage of CMOS imagers is not its lower cost, but system integration, as elaborated below.

Firstly, a nonnegligible fraction of the cost of image sensor chips, be it CCD or CMOS imager, is due to optical-related processes such as optical testing, optical cleanliness, optical packaging, on-chip color filter arrays, and on-chip microlens. Therefore, CMOS imager chip itself should not be expected to offer a significant cost advantage over CCD chips. Secondly, "minor" changes to "standard" CMOS technologies

are relatively cheap and easy to qualify. A prime example is the mixed-signal analog-digital technology which is usually derived from its digital predecessor with some process changes to provide the resistors, precision capacitors, and perhaps better transistor output resistances and higher voltages of operation. The advantage of staying close to a "standard" CMOS technology is the reduction of development cost which needs to be recovered in the product.

The real advantage of CMOS imager is the high level of on-chip logic, memory, and signal processing function integration, and random access capability, which cannot be easily accomplished by the CCD. New ways to integrate imaging systems will enable new applications not possible today. For example, the high level of integration offers the possibility of integrating the entire camera on a chip (without the lens). In addition, and perhaps even more importantly, the lower operating voltage and low power consumption will be the determining factor in many applications (especially consumer electronics and mobile computing applications).

At present, there is a proliferation of activity to modify baseline processes to optimize cost-performance as well as to integrate traditionally "separate" functions on the same chip to build what has been called "system-on-a-chip" (SOC) [71] and [72]. Mixed signal transmitter/receiver chips are prime examples with resounding successes. With the high levels of integration of the 256 Mb DRAM, the industry is also looking into the opportunity to merge DRAM, SRAM, microprocessors, and other logic functions into a single chip [71]–[73]. The use of multiple threshold voltages on the same chip has also been argued to be necessary for power-performance optimization for advanced CMOS [36] and [56]. There are indications that the semiconductor manufacturing community are adapting to the changing environment that a mixed set of application-specific technologies are needed to keep up the production volume required of an expensive fabrication line. One may call this the era of "technology ASIC." Relatively "minor" modifications to "standard" CMOS technologies such as selectively removing the silicide module, adding a second layer of gate polysilicon to provide short-distance CCD-like charge transfer and precision capacitors, using separate implant masks to profile the pn junction of the photodiode and/or the channel under the photogate are some obvious examples of significant performance advantages at moderate costs. The challenge to the CMOS imager community is to determine where the cost-performance trade-offs are, how far CMOS technology has to be modified to accommodate the imaging function, and to use imaging-specific technologies judiciously without compromising its capability for system integration. Conventional CCD product differentiation is mostly found at the device and process design level. For CMOS imagers, product differentiation will increasingly be found in the circuit design, chip architecture, and system integration. Innovations in these areas will fundamentally change the way imaging systems are used and deployed.

Finally, and perhaps most importantly, a change in the pixel architecture may completely eliminate some of the device and process limitations predicted in this paper. It is in this area that some of the most revolutionary developments may come from.

APPENDIX

The drain saturation voltage (V_{Dsat}) is calculated using the model and carrier velocity and mobility parameters of K_o [74]:

$$V_{Dsat} = \frac{(V_{GS} - V_{TO})E_{sat}L_{eff}}{E_{sat}L_{eff} + (V_{GS} - V_{TO})} \tag{1}$$

where $V_{GS} - V_{TO}$ is related to I_{Dsat} through

$$I_{Dsat} = W v_{sat} C_{ox}(V_{GS} - V_{TO} - V_{Dsat}) \tag{2}$$

and V_{GS} is the gate to source voltage, V_{TO} is the threshold voltage, E_{sat} is the velocity saturation electric field, L_{eff} is the effective channel length, W is the channel width, v_{sat} is the saturation velocity, and C_{ox} is the gate oxide capacitance per unit area.

The referred to input noises are computed using the following expressions (for a summary, see Wong *et al.* [51] and references therein):

Dark current shot noise

$$N_{dark} = \sqrt{\frac{J_{dark}A_{coll}\tau_{coll}}{q}} \tag{3}$$

where J_{dark} is the dark current density, A_{coll} is the dark current collection area, and τ_{coll} is the dark current collection time.

Thermal noise of the charge to voltage conversion transistor

$$N_{thermal} = \frac{C_{FD}}{q}\sqrt{\frac{4kT\alpha\Delta f}{g_m}} \tag{4}$$

where C_{FD} is the total capacitance at the floating diffusion node, $\alpha = 10$, Δf is the bandwidth, and g_m is the transconductance.

kTC noise

$$N_{kTC} = \sqrt{\frac{kTC_{FD}}{q^2}} \tag{5}$$

where C_{FD} is the total capacitance at the floating diffusion node.

A/D conversion quantization noise

$$N_{quantize} = \frac{1}{\sqrt{b}}\frac{N_{signal}(full)}{2^b} \tag{6}$$

where b is the number of bits, and $N_{signal}(full)$ is the number of full signal electrons.

Photon shot noise

$$N_{photon} = \sqrt{N_{signal}}. \tag{7}$$

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