CMOS Imager Technology Shrinks and Image Performance

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Abstract

In this paper, we present a performance summary of CMOS imager pixels from 5.2µm to 4.2µm using 0.18µm imager design rules, then to 3.2µm using 0.15µm imager design rules. These pixels support 1.3-megapixel, 2.0-megapixel, and 3.1-megapixel CMOS image sensors for digital still cameral (DSC) applications at 3.3V, respectively. The 4TC pixels are all based on technology shrinks of Micron's 2P3M imager process [1], and each of the technology nodes report excellent CMOS imager low-noise, high-sensitivity, low-lag, and low-light performance, matching that of state-of-the-art charged-coupled device (CCD) imagers. We have put a model in place to provide the predictive performance of smaller pixels, and then use that model to discuss performance expectations down to 2.0µm pixels. With the combination of imager design rules, pixel architecture, and process technology tailored for CMOS imagers, we see no fundamental reason that CMOS imagers should not be able to continue matching CCD performance as pixel sizes shrink.

Introduction

For DSC applications, a high-performance, low-noise imager with excellent low-light performance is required. There have been several papers that discuss technology and device scaling issues as applied to CMOS imagers [2–4]. A figure of merit for imager low-light performance is the signal-to-noise ratio (SNR) at exposures less than 1.0 lux-s. In November 2002, we developed a 1.3-megapixel imager with a 5.2µm pixel optimized for CMOS imager performance that matched CCD low-light (sub-0.1 lux-s) imager performance using 0.18µm design rules tailored for CMOS imager performance. In February 2002, we developed a 2.0-megapixel imager with a 4.2µm pixel using the same 0.18µm process technology but with a slight extension of the 0.18µm design rules to improve the photodiode fill factor [5]. Finally in December 2003, we produced a 3.1-megapixel imager with 3.2µm pixels based on 0.15µm imager design rules.

Megapixel DSC Design

Figure 1 shows a block diagram of the general DSC design architecture appropriate for all three imager designs. The default active image area is 1,280(H) x 1,024(V) with 5.2µm pixels for the 1.3-megapixel imager; 1,600(H) x 1,200(V) with 4.2µm pixels for the 2.0-megapixel imager; and 2,048(H) x 1,536(V) with 3.2µm pixels for the 3.1-megapixel imager. Each imager is designed with ½-inch optical formats at 30, 20, and 12 frames per second (fps) at full resolution for the 1.3-, 2.0-, and 3.1-megapixel imagers, respectively, and each with a 48 MHz master clock. Their reset boost/charge pump circuit allows the gate of the reset transistor to be boosted above the supply voltage so that a full 3.3V can be read into the pixel floating diffusion (FD) node. The imagers' programmable gain amplifier (PGA) located in front of the dual-channel analog-to-digital converter (ADC) is a folded cascade design with analog gain adjustable from 1 to 8. Their column sample and hold and PGA are optimized for low read noise and take advantage of a DRAM high-capacitance poly/nitride/poly capacitor process, while their dual 10-bit 48 MSPS pipelined ADC supports two channels: green1/green2 and red/blue. These designs are optimized to provide low-read noise, and supports row-wise dark-level correction to further improve noise performance.

Imager Design Rules and Array Device Issues

Over the last few years, major silicon manufacturers have begun dedicating their resources to CMOS imager development, which has accelerated the pace of the technology development in this field. In order to achieve CCD quality performance in CMOS imagers, the process and design rules must be tailored to the specific needs of the photosensitive pixel and the periphery imager design [5]. New Logic and DRAM process modules are not necessarily compatible with improving imager performance. As a result, imager products are being developed with their own unique process and design rules that are not simply copies of either a Logic or a DRAM technology. Semiconductor manufacturers are willing to dedicate a manufacturing line to an optimized imager process flow in anticipation of a substantial imager market.

Achieving state-of-the-art imager performance drives imager technology development toward solving it's own technology issues. Image sensitivity is directly proportional to the array supply voltage, V_{AA_pix}. As the design rules shrink, V_{AA_pix} must be maintained at a reasonable level, which requires that the array gate oxide remains relatively thick. To reduce power consumption, the digital logic in the periphery can operate at a lower voltage with a thinner gate oxide, using a dual-gate oxide process. The array transistor threshold voltage (V_T) does not scale: the high V_T driven by a high supply voltage is not an issue, and the I_{OFF} performance remains excellent. On the other hand, the periphery n-ch transistors supporting the high array voltages can exhibit CHC hot-electron reliability issues unless the process and transistor design rules are specifically tailored to eliminate this degradation. To achieve high quantum efficiency and low crosstalk, imagers require their own unique array well design. They also require their own modified STI process flow in order to achieve state-of-the-art dark current performance. The photodiode photosensor is a unique element requiring its own carefully optimized implants to maximize full well capacity without increasing dark current or hot-pixel defect generation. The transfer gate (TG) is a unique device similar in some aspects to the access transistor of a DRAM in that they each require their own special source and drain engineering. The floating diffusion (FD) is another specialized diffusion for imagers that requires an optimized process to reduce it's junction leakage and avoid contributing to hot-pixel defect generation.

Pixel Architecture and Process Integration

Figure 2 shows Micron's 4TC in-pixel capacitor architecture that supports the 1.3-megapixel and 2.0-megapixel designs [1]. Improved linearity is achieved by adding a low-depletion poly/nitride/poly capacitor on the low-capacitance, small-area, and low-leakage FD node. With one mask change, the conversion gain can be tuned to optimize the performance trade-off between high conversion gain and low-light performance, and low conversion gain and full well capacity. The 4TC architecture with true correlated double sampling (CDS) improves read noise performance over past 3T architectures.

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Figure 3 shows a cross section of the 3.2µm pixel from the 3.1-megapixel imager. A geometric photodiode active area (AA) fill factor of 46.7 percent is achieved. Careful placement of the row select (RS), source follower (SF), and reset transistor in the shared AA area allows an equal isolation in both the x and y directions between photodiodes. This improves fill factor, reduces crosstalk, and enables better modular transfer functioning (MTF).

To achieve CCD imager performance with the 3.2µm pixel for the 3.1-megapixel product, 0.15µm imager design rules were developed, which, coupled with a shared row pixel architecture, enabled a photodiode fill factor of 46.7 percent. Figure 4 shows the schematic of the shared row architecture in which five transistor gates are shared between two photodiodes, achieving an effective 2.5 transistors/pixel. The STI and PWell processes were modified to achieve CCD-like dark current performance. The in-pixel capacitor was enabled with a double-poly process using a DRAM nitride dielectric process module, and the photodiode process was tailored for low dark current, high quantum efficiency (QE), low off-state TG leakage, and low lag. Microlenses were optimized to focus a small spot size (1µm) hitting the center of the photodiode AA.

The 3T CMOS imager architectures cannot support shared row architectures and, therefore, do not shrink as effectively as 4T architectures. The 3T pixels do not support correlated double sampling (CDS), so their read noise is inferior to 4T pixels. Additionally, they require a contact to the photodiode that is the dominant source of dark current. These limitations make it difficult for 3T architectures to ever achieve CCD imager performance.

Characterization Results for 3 Pixel Generations

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The dark current in e/s as a function of temperature is shown in Figure 5 for all three pixels. For the 5.2µm and 4.2µm pixels, there is a single slope with an activation energy corresponding to 1.16eV. This indicates that the primary component of the photodiode dark current is diffusion current from the bulk substrate. The dark current is about 20e/s at 25°C for both sensors. The in-pixel capacitor was set to achieve a conversion gain of 33 µV/e for the 5.2µm pixel and 40 µV/e for the 4.2µm pixel. The photodiode fill factors of 39.3 percent and 37.0 percent for the 1.3- and the 2.0-megapixel sensors, respectively, correspond to leakage currents of 30 pA/cm^2 and 50 pA/cm^2 at 25°C. While this dark current remains above CCD dark current performance levels, the low-light performance for reasonable integration times is dominated by read noise. The temperature dependence of the dark current on the 3.1-megapixel sensor with the 3.2µm shared row pixel is significantly improved. The dark current of the 3.2µm pixel shows a dual slope corresponding to activation energies of 0.94eV and 0.75eV, which results in a 10 times improvement in dark current performance at 60°C. The dark current of the 3.2µm pixel is equal to 15e/s at 25°C and 360 e/s at 60°C, while the conversion gain is equal to 47.5 µV/e and a 46.7 percent fill-factor, which corresponds to a leakage current of ~50 pA/cm^2 at 25°C and 1.2 nA/cm^2 at 60°C. Three components, area, field edge, and gate edge, contribute to the photodiode dark current. From our dark current modeling, we ascribe the substantial improvement of the dark current performance of the 3.2µm pixel to be due to the reduced TG width of the shrunk shared row architecture.

Table 1 summarizes important optical-electrical characteristics for all three pixel types. Pixel capacity is about 38.4ke for the 5.2µm pixel, providing the maximum signal-to-noise ratio (SNR) of 45.8dB. The 4.2µm pixel has a 32.5ke pixel capacity and corresponding SNR of 45.1dB. Due to the shared row architecture and further optimization of the pixel structure, the 3.2µm pixel has a full well linear charge capacity of 33.0ke, which provides the maximum SNR of 45.2dB. The noise floor of the 1.3-, 2.0-, and 3.1-megapixel sensors is equal to 11, 9.5, and 7.5 equivalent electrons, respectively. The corresponding pixel dynamic ranges are equal to 70.7dB, 70.9dB, and 72.9dB.

Responsivity of green pixels is in good agreement with pixel parameters and changes from 1.9 V/(lux-s) to 0.93 V/(lux-s) with diminishing pixel sizes from 5.2µm to 3.2µm. Figure 6 shows an example of photon transfer curves for the 2.0-megapixel imager with a 4.2µm trumpet pixel at unity gain.

Figure 7 presents the QE of red, green, and blue pixels as a function of wavelength measured at f/2.8 incident light for the 3.1-megapixel imager with a 3.2µm pixel. The low stack height of the dielectric layers as well as an optimized microlens process and optimized electrical isolation provide high QE and little crosstalk for all three pixel types. Figure 8 shows maximum QE for blue, green, and red pixels for each pixel generation. As shown in the chart, QE does not drop below 44 percent (for green pixels) for the smallest pixel size. Figure 9 presents the maximum responsivity for blue, green, and red pixels. Numerical data for the responsivity correlates well with pixel size and parameters.

Micron's low-profile process produces a good angular response. Figure 10 shows the signal as a function of the angle of incidence for all three pixel types. The 3.1-megapixel imager with the 3.2µm pixels shows an improvement in angular response performance due to the continued improvement of the color filter array (CFA)/microlens process improvements as well as the improved fill factor of the shared row architecture.

A major concern with both CCD and CMOS imagers is lag performance [7,8], which becomes increasingly difficult as pixel sizes shrink and photodiode process implants increase to preserve the full well capacity of the smaller photodiode area. The photodiode implant design and process were simultaneously optimized to achieve the low-lag performance shown in Figure 11 for each pixel generation. The lag is less than 0.02 percent at 40 percent saturation and less than 1 percent at 1 percent saturation.

To compare CMOS and CCD performance, a CCD imager of a well-known major CCD manufacturer was exposed at the same number of photons/pixel. Figure 12 shows color images of the standard GretagMacbeth chart taken by both the CCD and our imager at equivalent low-light conditions and results of SNR calculations for six of the chart's white-to-black patches. To exclude signal offset uncertainty after color processing, the signal from the black patch (Sq. 6) was taken as a zero signal. A comparison was made using grey patches from Sq. 2 to Sq. 5. We found that the measured SNR of our CMOS imager at low-light conditions has reached the level of CCD performance.

Modeling Results for Future Pixel Generations

As progress is made towards deep sub-3µm pixel technology, we anticipate that four-way shared pixel architectures, which achieve an effective 1.5 transistors/pixel, will become the norm [6]. Because of the mirrored nature of this pixel architecture, achieving lag-free operation will be a challenge. Random misalignment during the operation of current steppers has the potential to contribute to FPN and PRNU.

Figure 13 shows the fill factor of pixels versus pixel size. The largest trumpet pixels using 0.18µm imager design rules show a strong reduction in fill factor as pixel size shrinks. If continued, this would severely limit full well capacity and QE due to the inability of a microlens to focus light on such a small photodiode area. At sub-4µm pixels, a shared row pixel architecture and 0.15µm imager design rules are introduced, which results in a substantial increase in

fill factor. Deep sub-3µm pixels will move to a four-way shared architecture and 0.13µm imager design rules to retain fill factor.

Table II compares the predicted imager performance parameters to the actual shown in Table I for pixels down to 3.2µm, then extends the predictive model down to 2.0µm pixels. The primary assumption of this empirically based model is that the microlens has the ability to efficiently focus light onto the photodiode area. By introducing new pixel architectures, such as trumpet, shared row, and four-way shared row, we are able to maintain a high full well charge capacity in the photodiode beyond sub-3µm pixels without any lag. Even though the full well charge capacity tends to diminish in small pixels, Micron's 4TC technology can provide a dynamic range greater than 70dB for a wide range of pixel generations. Dark current modeling consists of dividing the measured dark current into area, field edge, and gate edge components. According to pixel prediction results, the dark current at 25°C is expected to be less than 10e/s for pixels smaller than 3µm, even with no further improvements in process technology, which will certainly take place.

Color Filter Array and Microlens Technology

The CFA and microlens are both critical to pixel shrink technology. CFA technology must be able to pattern pigmented or dyed resists with no streaks and no pattern uniformity issues. The pigments must be dispersed in the resists without agglomeration to avoid PRNU issues. Any transmission non-uniformities will become more apparent with shrinking pixels, so improved materials will be needed for future imagers. The microlens must be able to focus light on an increasingly smaller photodiode area to ensure high QE and to avoid crosstalk and MTF degradation. Since the thickness of the device layers above the photodiode are not shrinking, the focal distance of the microlenses needs to remain the same, independent of the pixel size. This requires the flexibility to adjust the microlens radius independent of its size. Unlike other photo resists, the CFA and microlens materials are becoming an integral part of the device and must meet stringent requirements for long-term transmission stability under all operating conditions.

Figure 14 shows a top view and a cross section of a red, green, blue (RGB) CFA and microlens with a 2.8µm pixel pitch. In Figure 15a, we show an AFM profile of the 2.8µm microlens, along with a ray tracing simulation using the actual AFM-measured lens surface (Figure 15b). As shown, the focal point is somewhat above the photodiode surface, indicating a need for a slight curvature adjustment of the microlens. Rays passing through the periphery of the microlens have a different focal length because of the aberrations of the square cushion-type lens used, but all the incident light reaches the diode with vertical incident light. More advanced lens designs can be used to reduce aberrations and improve the angular acceptance range of incident light.

The optical limits to shrinking pixel sizes are defined by diffraction and aberrations in both the camera lens system and the microlenses. The diffraction-limited resolution of a camera lens can be described as:

$$d = 2.44 \times \lambda \times f\# \qquad (1)$$

For an f/2.8 lens, this results in a 3.76µm spot size for green light (550nm), supporting a 1.9µm pixel size within a 2x2 Bayer pattern unit made up of one red, one blue, and two green pixels. However, camera lenses are usually limited by aberrations at low f-numbers, which puts the practical limit of the pixel size around 2.2µm–2.5µm for a mass-produced lens.

As noted above, microlens efficiency is degraded by aberrations, but ultimately, the shrink limits are defined by diffraction. Aberrations can be reduced by advanced lens processing, while diffraction effects due to the limited size of the lenses themselves cannot be eliminated. As a result, the collection efficiency drops with shrinking pixel size, limiting the use of effective microlenses to pixel sizes above about 2µm. Figure 16 summarizes the optical dilemma created by pixel shrinks: decreasing photodiode size and increasing diffraction-limited focal spot size of the microlenses increase the diode fill ratio. The focal spot size of red light starts exceeding the diode size at about 2µm. Smaller pixel sizes are expected to show a rapidly decreasing QE and increasing crosstalk. Figure 17a shows a summary of electromagnetic wave simulations for pixel sizes from 5µm to 1µm. It can be seen that the microlens focusing effect becomes marginal around 2µm and is lost completely at 1µm pixel size, consistent with the considerations of Figure 16. Figure 17b illustrates the added limitations of light collection due to angular light incidence. In this example showing a 3µm microlens, an angle above 10 degrees will lead to a gradual reduction in QE and increasing crosstalk. This cut-off angle depends on the distance between the microlens and the photodiode. A small distance helps to increase the range of angles accepted and provides more flexibility for the camera lens design.

Conclusions

The physics of silicon is the same whether one is fabricating a CCD sensor or a CMOS image sensor. It should be possible to achieve the same dark current, quantum efficiency, and lag performance as long as the CMOS imager pixel design and process are tailored to achieve optimum performance. The measured read noise, lag performance, and low-light performance indicate that CMOS imagers have demonstrated their capability to achieve CCD imager performance down to 3.2µm pixels. Dark current on CMOS imagers is rapidly improving but needs some further optimization to match CCD's 30 years of technology optimization. It will become difficult to shrink pixels beyond 2.2µm due to the limitations of existing photodiode technology and fundamental diffraction limits.

Acknowledgements

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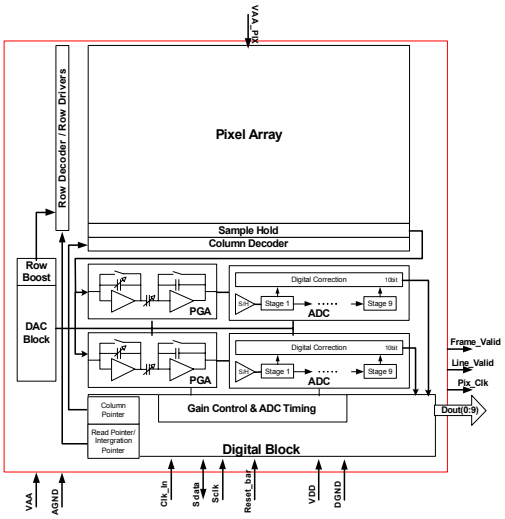


Figure 1. Structure of megapixel CMOS imager

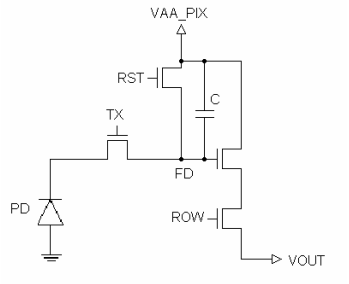


Figure 2. 4TC pixel structure

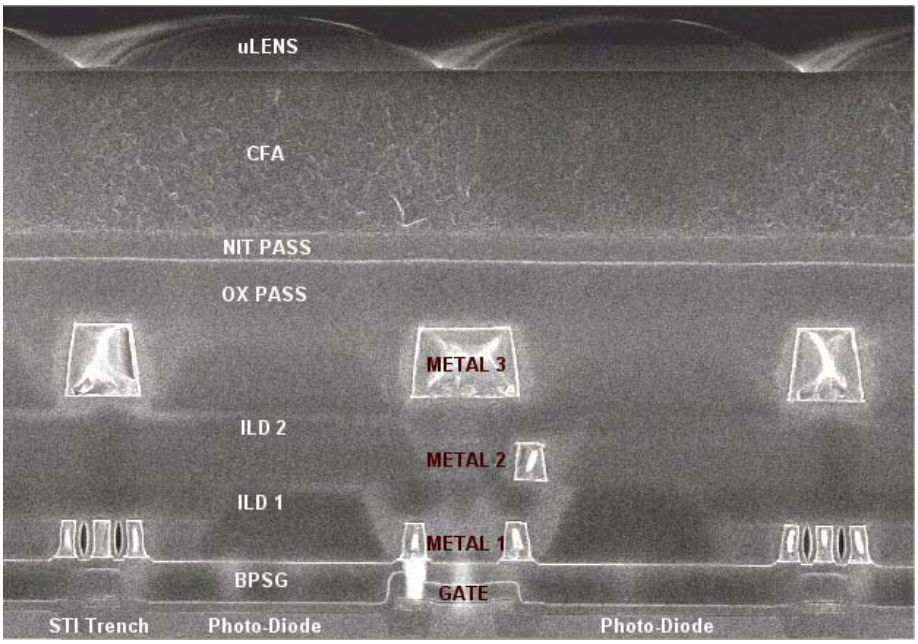


Figure 3. Cross section of 3.2µm pixel

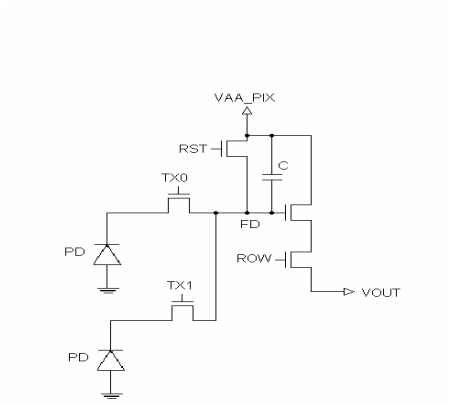


Figure 4. 4TC shared row pixel structure

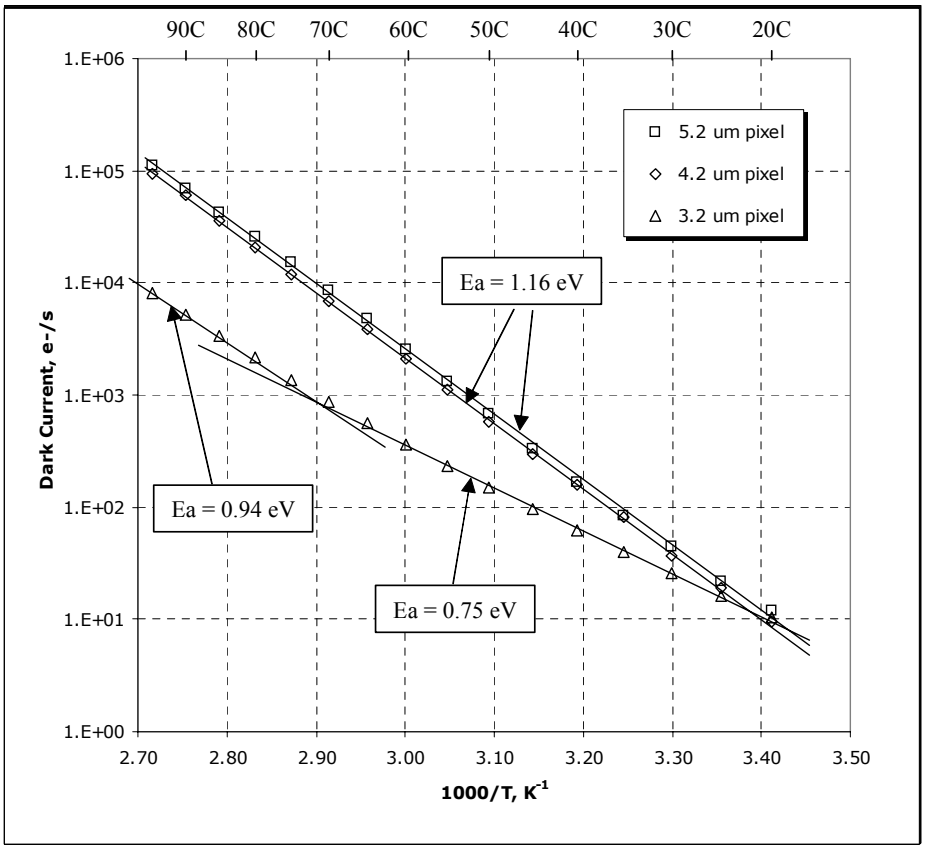


Figure 5. Dark current vs. temperature

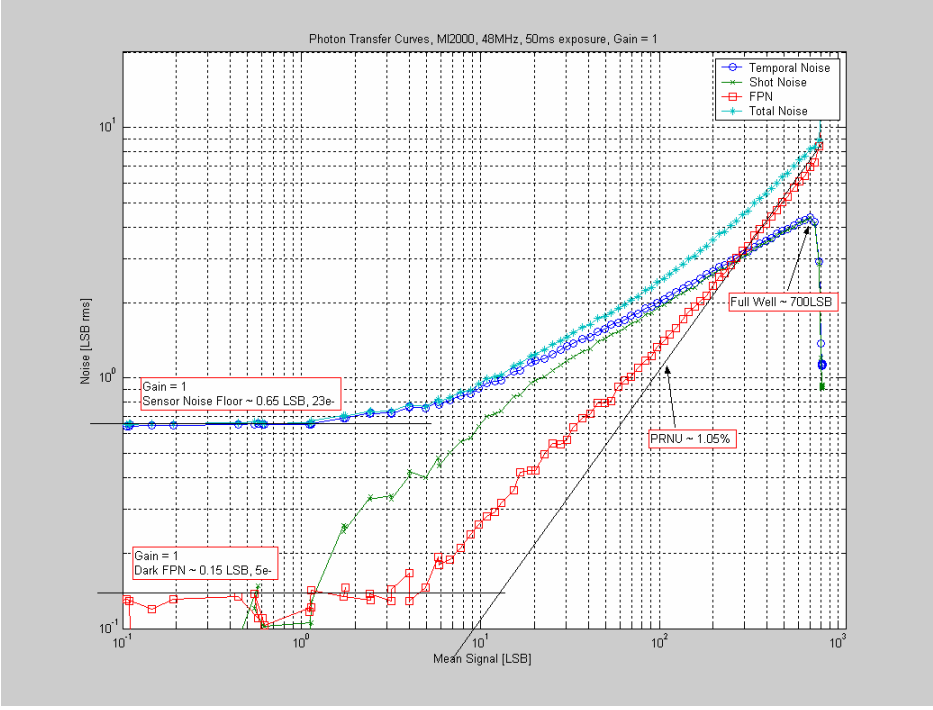


Figure 6. Photon transfer curves for 2.0-megapixel imager with 4.2µm pixel size

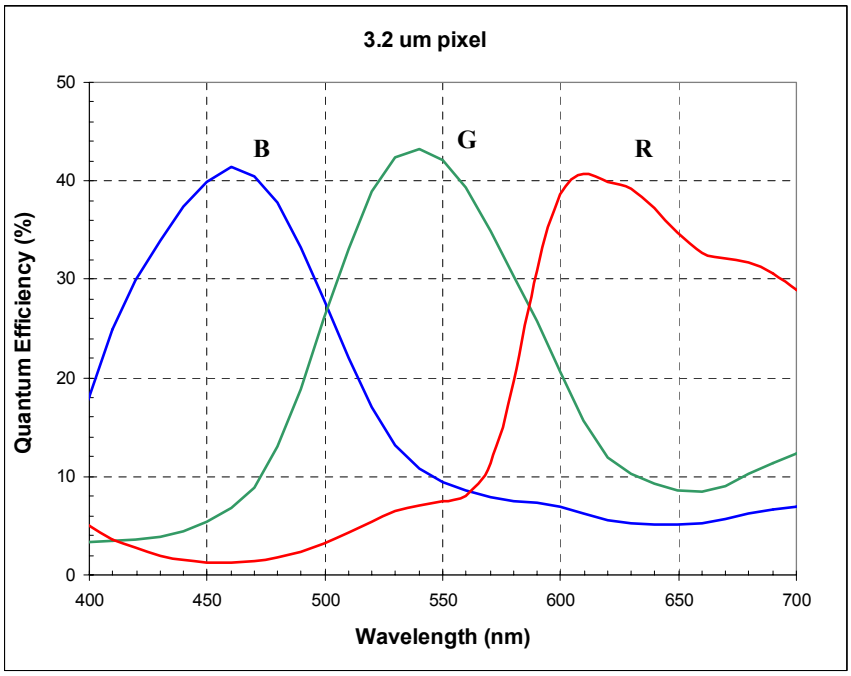


Figure 7. Quantum efficiency vs. wavelength for 3.1-megapixel imager with 3.2µm pixel size

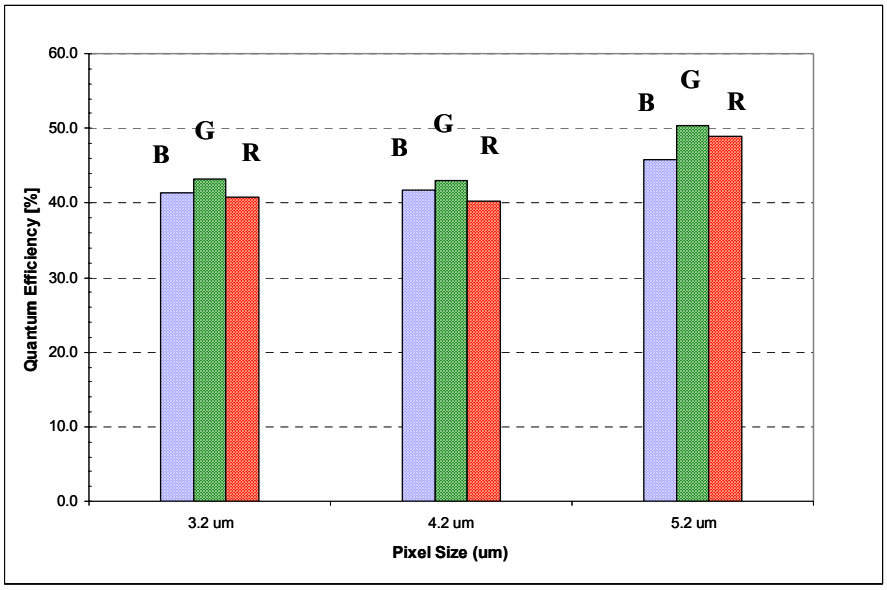


Figure 8. Maximum quantum efficiency of blue, green, and red pixels

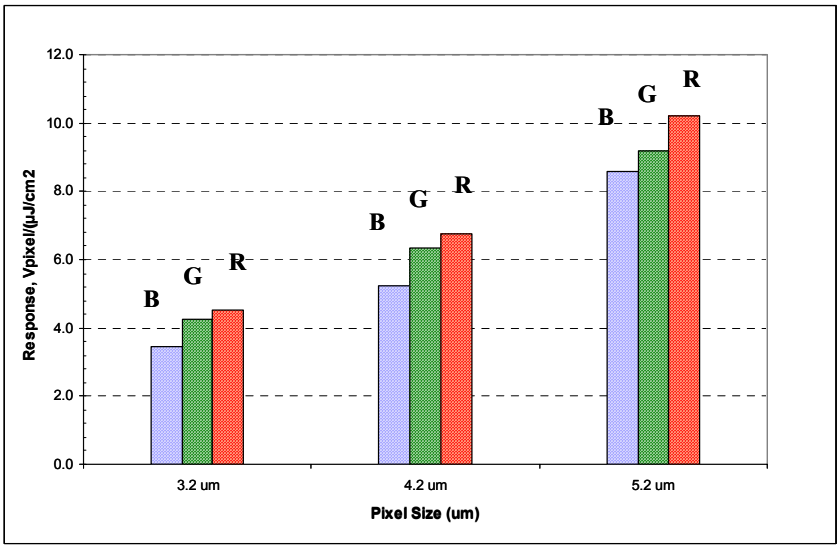


Figure 9. Maximum responsivity for blue, green, and red pixels

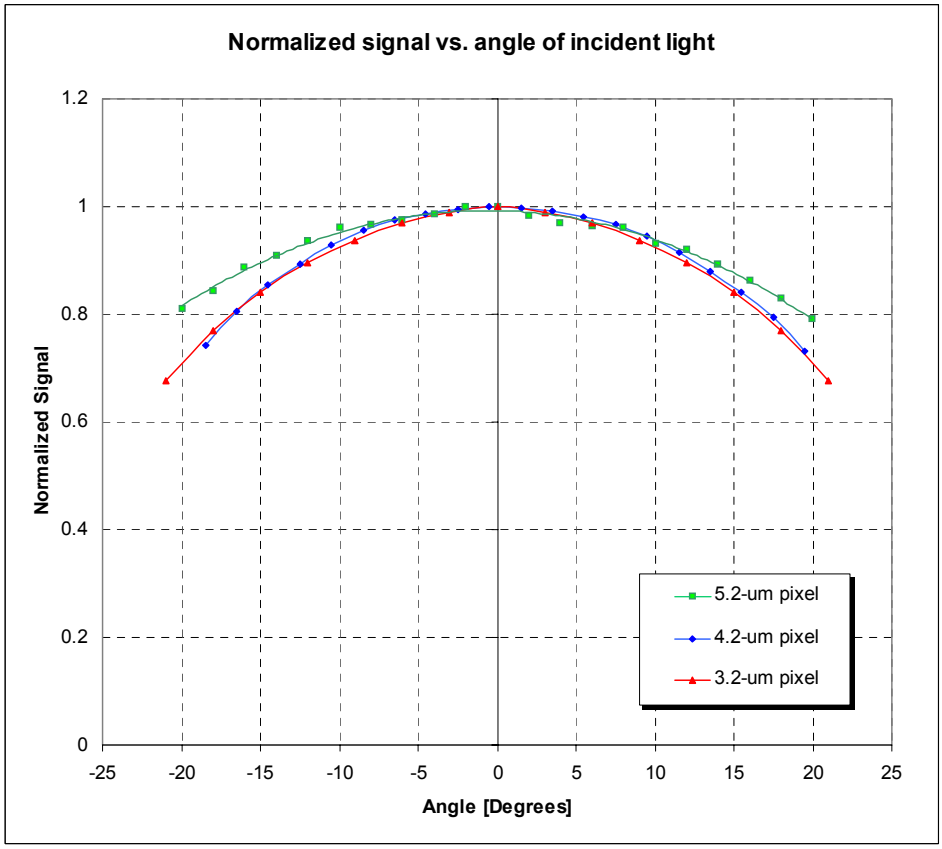


Figure 10. Angular response for all three pixel generations

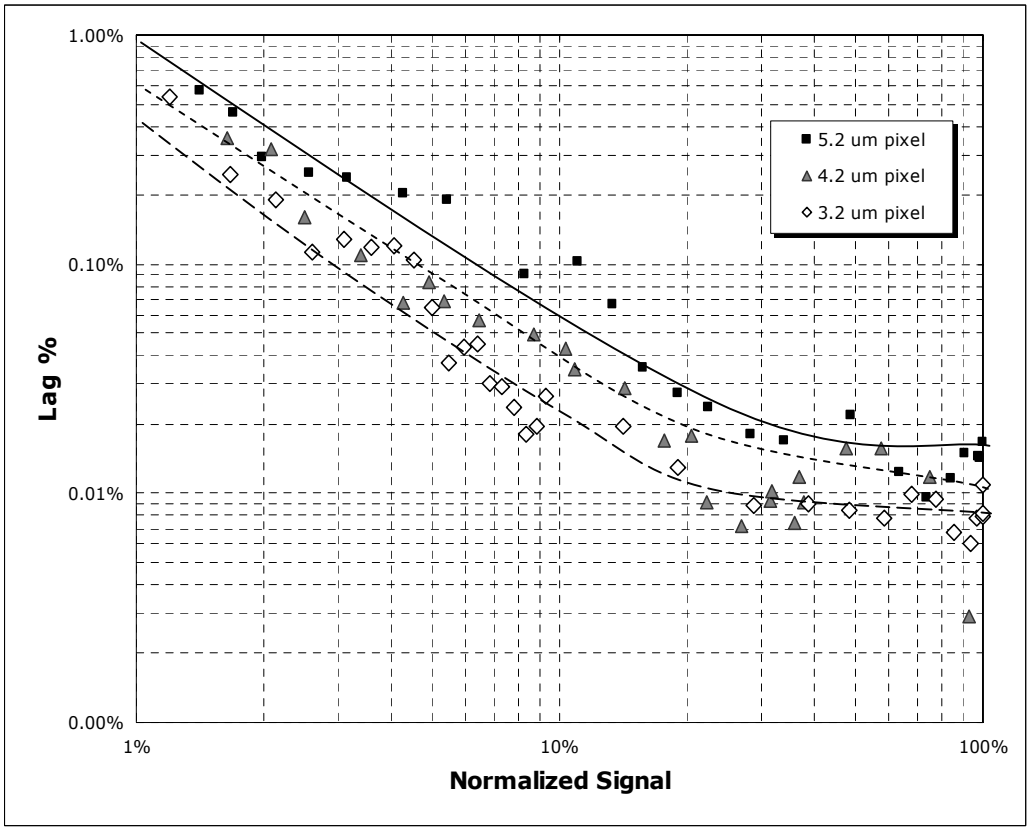
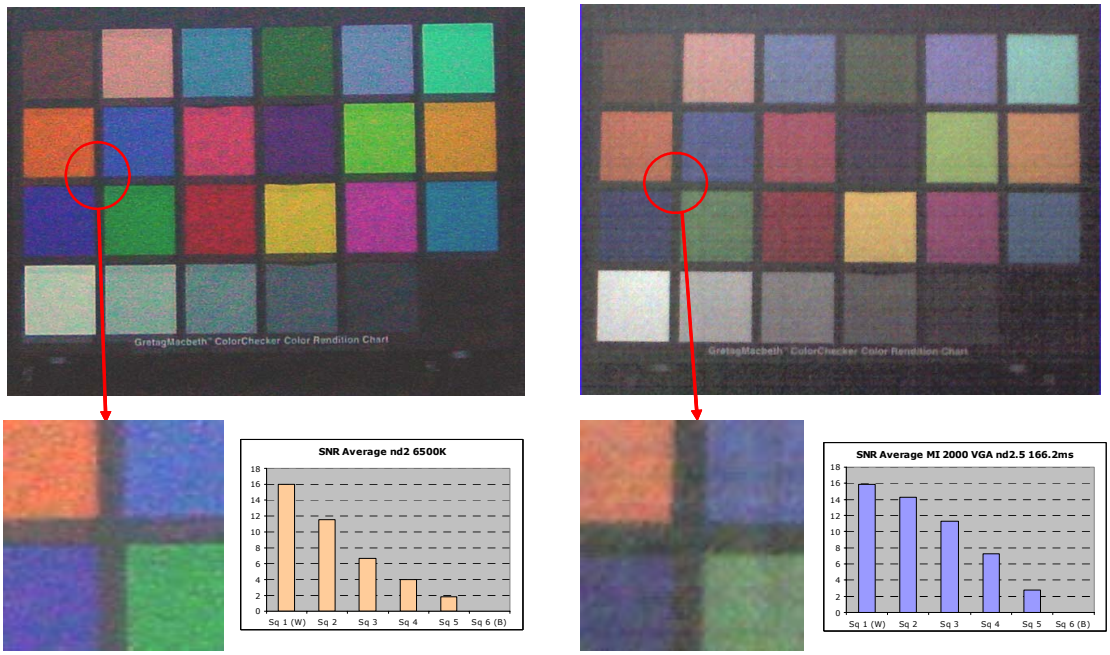


Figure 11. Lag vs. signal normalized to pixel full well capacity



CCD, F/2.8, I = 6 lux, Tint = 100ms CMOS, F/2.8, I = 2 lux, Tint = 166ms

Figure 12. Color images of GretagMacbeth chart at equivalent low-light conditions and averaged SNR across the white-to-black pattern

TABLE I. Actual pixel performance of each pixel generation.

	5.2µm pixel	4.2µm pixel	3.2µm pixel
Conversion Gain (FD), µV/e	33	39.5	47.5
Responsivity (FD), V/lux-s	1.9	1.2	0.93
Quantum efficiency	0.51	0.45	0.45
Pixel capacity at MAX of linear range, e	38,400	32,500	33,000
MAX SNR, dB	45.8	45.1	45.2
Noise floor at MAX gain, e	11	9.5	7.5
Pixel dynamic range, dB	70.9	70.7	72.9
Dark current (25°C), e/s	20	19	15
Dark current (60°C), e/s	2,500	2,100	360

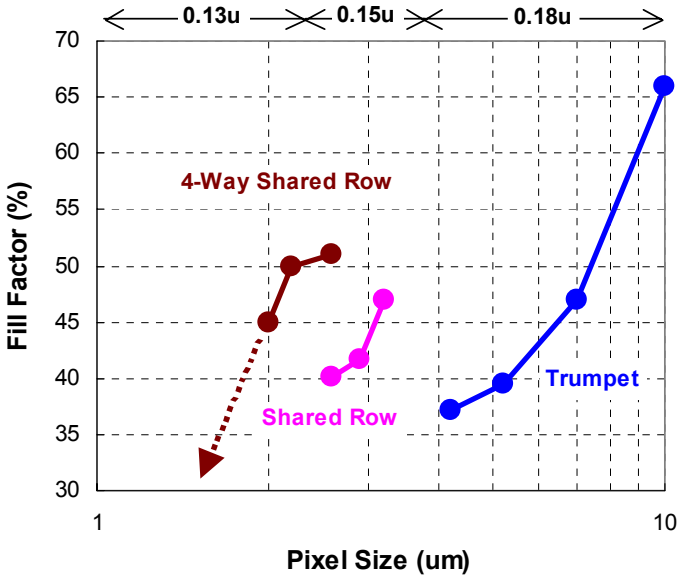


Figure 13. Fill factor vs. pixel size

TABLE II. Pixel performance prediction of each pixel generation based on an empirical model.

Pixel (µm)	Full Well (ke)	Sensitivity (ke/lux-s)	Dark current (e/s) at 25C	Dynamic Range (dB)	Max SNR (dB)
5.2	38	57	22	71	45.8
4.2	32	37	16	71	45.0
3.2	33	22	12	72	45.2
2.9	25	16.0	10	71	44.0
2.6	28	12.9	11	72	44.5
2.2	21	9.3	9	70	43.0
2.0	16	7.6	7	69	42.0

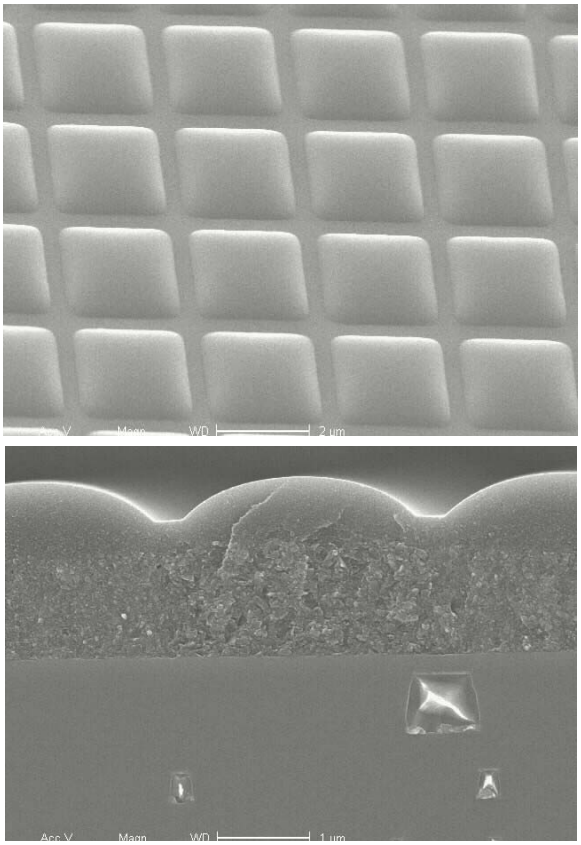


Figure 14. Cross section showing 2.8µm CFA/microlens

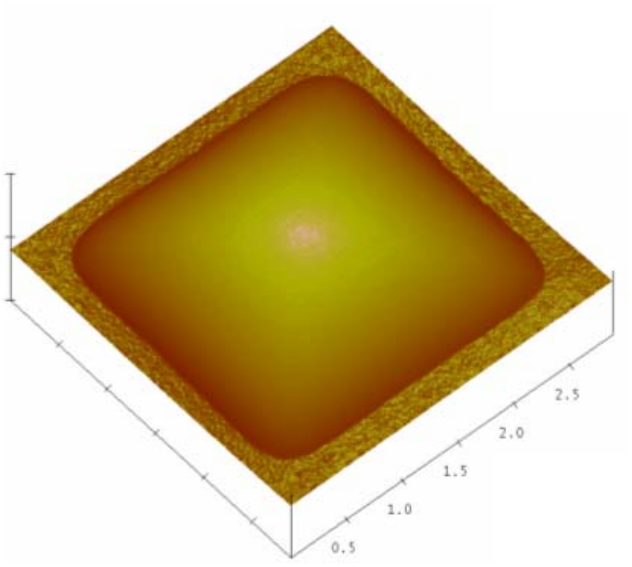


Figure 15a. AFM measurement of 2.8µm microlens

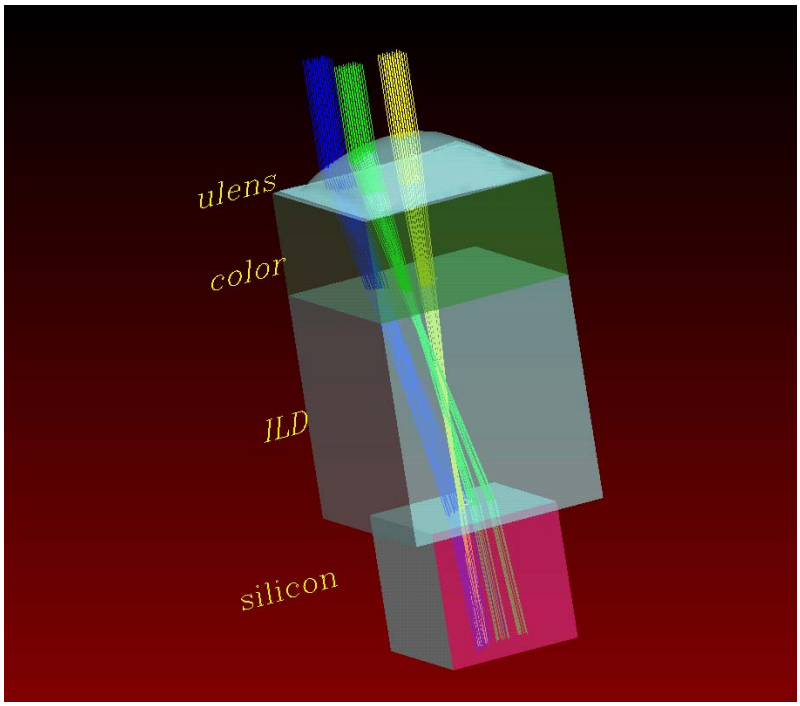


Figure 15b. Ray tracing simulation of the AFM-measured microlens shape in Fig.15a

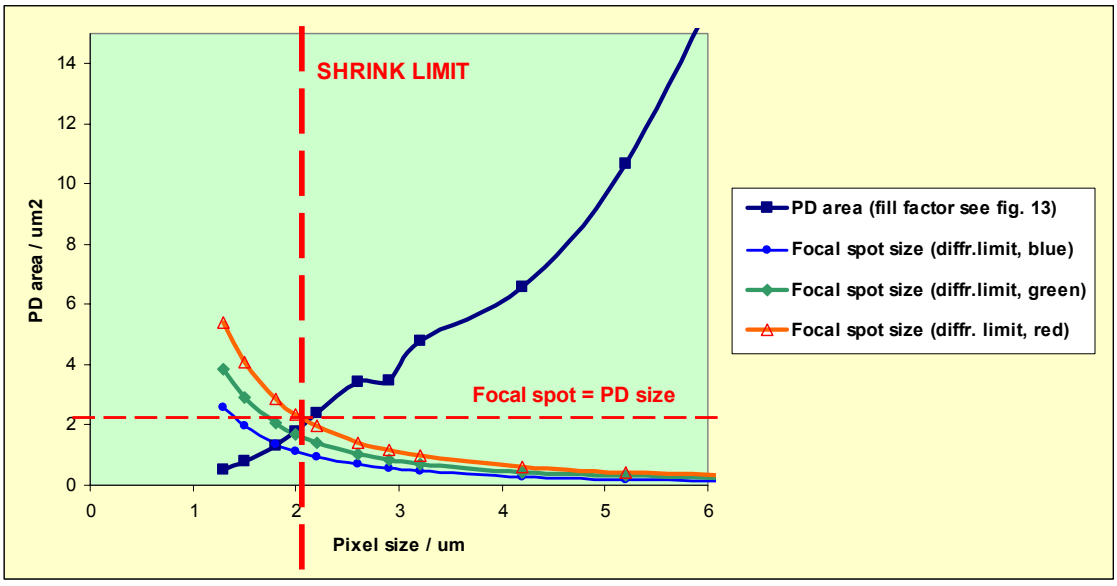


Figure 16. Diode fill ratio as a function of pixel size for diffraction limited micro-lenses

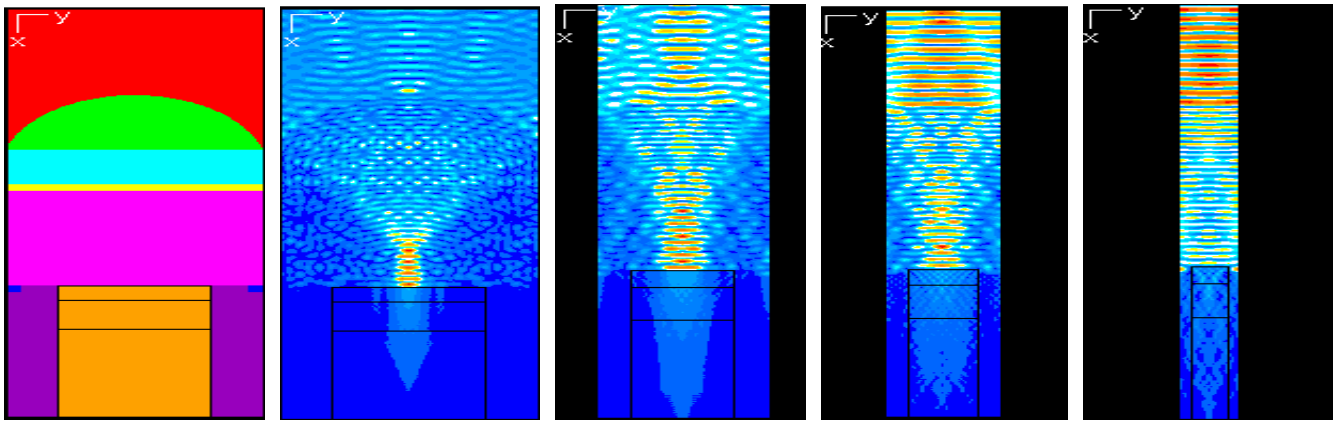


Figure 17a. Full electromagnetic simulation of microlens focusing for various pixel sizes

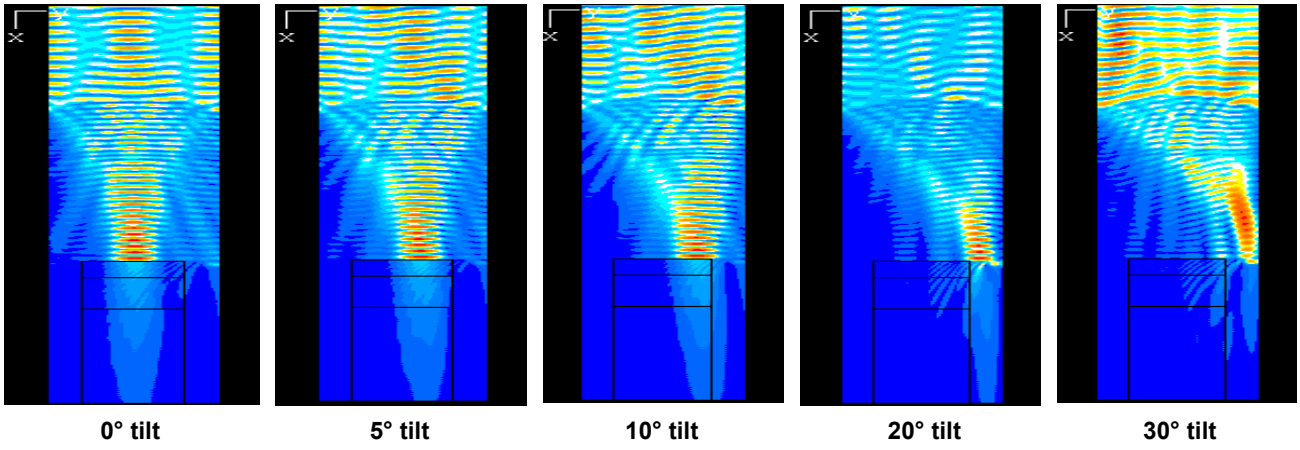


Figure 17b Electromagnetic simulation of a 3µm microlens with variable incident angle of a plane wave