Sensitivity of CMOS Based Imagers and Scaling Perspectives

Tarek Lulé, Stephan Benthien, Holger Keller, Frank Mütze, Peter Rieve, Konstantin Seibel, Michael Sommer, and Markus Böhm

***Abstract*—CMOS based imagers are beginning to compete against CCDs in many areas of the consumer market because of their system-on-a-chip capability. Sensitivity, however, is a main weakness of CMOS imagers and enhancements and deviations from standard CMOS processes are necessary to keep up sensitivity with downscaled process generations.**

In the introductory section several definitions for the sensitivity of image sensors are reviewed with regard to their potential to allow meaningful comparison of different detector structures. In the main section, the standard CMOS sensor architecture is compared to detector structures designed to improve the sensitivity, namely the photogate (PG), the pinned photodiode (PPD) and the thin film on ASIC (TFA) approach. The latter uses a vertical integration of the photodiode on top of the pixel transistors. A careful analysis of the relevant electrical, optical and technological parameters and many previously published experimental data for different imagers reveals that only the PPD and the TFA enhancements provide satisfactory sensitivity and withstand scaling down to 0.18 μ processes. Due to the higher fill factor and the higher quantum efficiency TFA provides significantly better values than PPD. The radiometric sensitivity of a 5 μm $\times$ 5 μm TFA pixel is found to amount to 11.9 V/(μJ/cm^2) for a 0.25 μm process and 27.5 V/(μJ/cm^2) for a 0.18 μm process.

***Index Terms*—Active pixel sensors, CMOS image sensors, ISO speed, PG, scaling, sensitivity, TFA.**

I. Introduction

FOR A LONG time, CCDs have been unequaled leaders in the field of electronic cameras for all kinds of applications. Over many years, this concept has been driven by an increasing market demand for ever larger pixel numbers [1] and better image quality [2] that no other technology could serve better than CCDs. However, interest in image sensors based on standard CMOS technology has increased dramatically in the past ten years [3]–[6]. CMOS based imagers offer significant advantags over CCD's such as system-on-chip capability, low power consumption and possibly lower cost. The ultimate single CMOS-chip consumer camera is expected to have a big cost advantage over conventional CCD cameras with many support ICs and discrete components. This price pressure and the expected market volume of 60 Mio. CMOS based imagers by 2002 [7] let many large players enter this emerging market [8]–[12].

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T. Lulé, S. Benthien, H. Keller, F. Mütze, P. Rieve, K. Seibel and M. Sommer are with the Silicon Vision GmbH, D-57078 Siegen, Germany (e-mail: adm@siliconvision.de).

M. Böhm is with the Silicon Vision GmbH, D-57078 Siegen, Germany, and the Institut für Halbleiterelektronik, Universität-GH Siegen, D-57068 Siegen, Germany.

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First CMOS imagers were passive pixel sensors [13] that suffered from low sensitivity and high noise [14]. With the development of small scale CMOS technology active pixel sensors (APS) became feasible [15] with improved performance due to active driving transistors in the pixels [16]. Still designers have to tackle the problem of fixed pattern noise (FPN) and temporal noise to come to levels comparable to CCDs [17]. But one of the largest problems is to get acceptable sensitivity from the CMOS structures available. Various specialized devices have been developed to increase the sensitivity without costing too much in pixel area, such as the photogate (PG) [18] and pinned photo diode (PPD) pixels [19].

Another approach to increase the imagers sensitivity is the three-dimensional (3-D) integration of the light sensitive detector on top of the pixel [20]–[22], giving the maximum sensitive area without compromising resolution. Major successes in bringing together the advantages of state of the art CMOS technology and amorphous silicon material into such vertically integrated imagers have been achieved with imagers in thin-film-on-ASIC (TFA) technology and demonstrated in [23]–[25]. A TFA sensor (Fig. 1) consists of an amorphous silicon multilayer system that is deposited on top of an application specific integrated circuit (ASIC). Thus the amorphous silicon performs the conversion of light into photocurrent while the ASIC is responsible for integration, readout and processing of the photo signal [26].

The basic properties of amorphous silicon have been discussed elsewhere [27] and shall be summarized here. Its absorption coefficient for visible light is approximately 20 times larger than that of crystalline silicon (c-Si) [28] and transient response is sufficient for most imaging applications [29]. Dark currents are comparable with c-Si at room temperature. The well developed process allows a high pixel to pixel local contrast in a cost effective process without need of lithography between pixels [30]. At the same time it is principally compatible with any CMOS ASIC process.

While CCD technology development has never stopped, CMOS sensors are gaining ground [31] especially in areas where the system integration of CMOS can be traded against the moderate image quality that is readily available, such as in toy cameras [32]. But still CCDs prevail where high resolution and sensitivity are demanded since these are the strongest points in favor of this matured technology [33] and are the reasons for its present market dominance.

After some general remarks on sensitivity in Section II, Section III investigates the dominating factors of sensitivity in more detail for the state of the art of CMOS based image sensors.

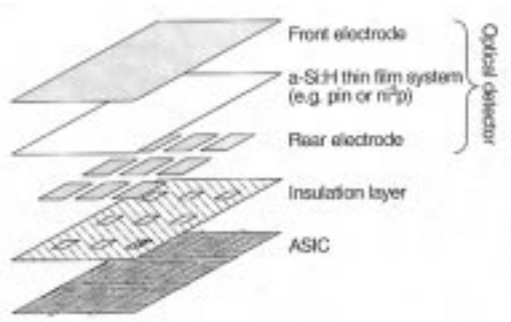

Fig. 1. Layer sequence of an image sensor in TFA technology.

One of the limiting factors for resolution and sensitivity is the acceptable total active area. Yield, die cost, and lens cost benefit from a small pixel and therefore a small die size. In order to get to the resolution standards that CCDs today dictate, CMOS sensors must use downscaled processes. The influences of downscaling on sensor performance will be discussed in Section IV.

II. General Remarks on Sensitivity

One important issue in the characterization of image sensors is sensitivity. In literature, a variety of definitions and quantities are used in order to qualify the conversion of electromagnetic radiation into electrical signals. In the following an attempt is made to standardize the specification of sensitivity.

Usually the basic transfer characteristics of a photodetector is described by its quantum efficiency $QE(\lambda)$ which depends on the wavelength λ and describes the number of electrons generated and collected per incident photon. The quantum efficiency is related to the spectral response $SR(\lambda)$ (in A/W) according to the equation

$$SR(\lambda) = \frac{\lambda q}{hc_0} \cdot QE(\lambda) \tag{1}$$

with q representing the elementary charge and hc_0 the product of Planck's constant and the vacuum speed of light. Fig. 2 compares typical quantum efficiency spectra of a c-Si photodiode [5] and an amorphous silicon (a-Si : H) based photodiode [34]. The relatively high c-Si peak quantum efficiency of 0.6 has been used for the sensitivity calculations described below, although the quantum efficiency for photodiodes realized in standard CMOS processes reported in literature is usually below 0.3 [6], [35], [36]. Due to the higher bandgap of amorphous silicon (1.7 eV) the response is concentrated to the visible, while the c-Si diode exhibits significant efficiency also in the infrared and the blue response is reduced.

The collection mechanism is different for both detector types. Since c-Si is an indirect semiconductor, the absorption coefficient is rather low in the visible range [37]. As a consequence the absorption depth extends up to several 10 μm into the semiconductor material. The deep generation profile of a c-Si photodiode requires diffusion of carriers from the bulk to the space charge region near the surface to achieve reasonable photosensitivity, thereby lowering local contrast and spatial resolution in the red and infrared.

In contrast, a-Si : H is a quasi direct semiconductor and exhibits a higher absorption coefficient in the visible [28]. In order

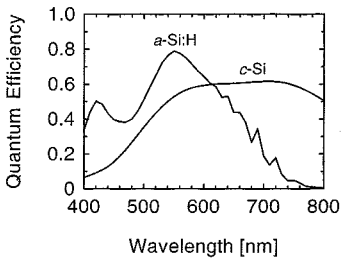

Fig. 2. Typical external quantum efficiencies of c-Si and a-Si : H photodetectors.

to absorb most of the light impinging on an a-Si : H photodetector a thin film (<1 μm) is sufficient. Photogenerated carriers are extracted as a drift current by a high electric field in a p-i-n or Schottky diode configuration.

The dark current which represents an important limitation of the dynamic range for low illumination intensity is comparable for a-Si : H and c-Si devices and amounts to 10^{-10} to 10^{-9} A/cm^2 at room temperature for both technologies [5], [26], [34], [38].

If a photodiode is exposed to a spectral power density $\Phi(\lambda)$ (in W/cm^{2}nm) the collected photocharge Q can be expressed as

$$Q = A_{\text{eff}} \cdot T_{int} \cdot \int SR(\lambda) \cdot \Phi(\lambda) \cdot d\lambda \tag{2}$$

with A_{eff} denoting the effective photoactive area of a pixel and T_{int} the integration time. Illumination is assumed to be constant during the exposure time.

The photoactive region is determined by the effective optical fill factor FF of the device that describes the portion of the pixel area A_{pix} which contributes to photosensitivity

$$FF = \frac{A_{\text{eff}}}{A_{pix}}. \tag{3}$$

The spectral response and the quantum efficiency data used in this treatise are referred to the photoactive area rather than to the complete pixel area.

The voltage swing V that is obtained from the collected photocharge is inversely proportional to the integration capacitance C_{int}, as follows:

$$V = \frac{Q}{C_{int}} = \frac{FF \cdot A_{pix} \cdot T_{int}}{C_{int}} \cdot \int SR(\lambda) \cdot \Phi(\lambda) \cdot d\lambda. \tag{4}$$

The following sensitivity considerations are all referred to the pixel input. Additional amplification in the pixel or system electronics is ignored and can be applied in all CMOS based imaging technologies. However, any circuitry creating gain reduces the effective fill factor in a CMOS pixel with the exception of the TFA arrangement.

In order to calculate the sensor sensitivity the integrated photovoltage has to be divided by the optical energy impinging on the pixel during the integration time:

$$S_W = \frac{FF \cdot A_{pix}}{C_{int}} \cdot \frac{\int SR(\lambda) \cdot \Phi(\lambda) \cdot d\lambda}{\int \Phi(\lambda) \cdot d\lambda}. \tag{5}$$

Integration extends over the relevant wavelength interval in which $SR(\lambda)$ exhibits values different from zero. The quantity defined by equation (5) is designated as radiometric sensitivity [in V/(μJ/cm^2)].

Another approach applies the photometric quantity illuminance E (in lx), which is obtained by weighting the power spectrum by the photopic sensitivity of the human eye $V_e(\lambda)$, to normalize the voltage signal

$$E = K_m \cdot \int_{380\text{ nm}}^{780\text{ nm}} V_e(\lambda) \cdot \Phi(\lambda) \cdot d\lambda \tag{6}$$

with the photometric equivalent $K_m = 683$ lx/(W/m^2). The integration extends only over the visible range from 380 to 780 nm. $V(\lambda)$ peaks at 555 nm and drops to values below 10% for wavelength smaller than 470 nm or higher than 650 nm [40]. The photometric sensitivity (in V/lxs) is expressed as

$$S_E = \frac{V}{E \cdot T_{int}} = \frac{FF \cdot A_{pix}}{C_{int} \cdot K_m} \cdot \frac{\int SR(\lambda) \cdot \Phi(\lambda) \cdot d\lambda}{\int_{380\text{ nm}}^{780\text{ nm}} V_e(\lambda) \cdot \Phi(\lambda) \cdot d\lambda}. \tag{7}$$

The use of the photometric sensitivity might lead to an overestimation of the actual sensitivity of a CMOS sensor with significant quantum efficiency in the infrared. In this case, the application of an additional infrared cutoff filter is advisable in order to get realistic values. Use of the radiometric sensitivity definition [see (5)] eliminates this problem and should be preferred.

If, for example, the CMOS imager presented in [5] is illuminated with a tungsten halogen spectrum the photometric sensitivity has been calculated to about 27 V/lxs. Changing the spectrum to daylight results in 10 V/lxs, while an additional IR cutoff filter leads to only 6 V/lxs. Using the radiometric sensitivity, the values drop from 19 V/(μJ/cm^2) for an incandescent light source to 14 V/(μJ/cm^2) for IR filtered daylight spectrum. It becomes obvious that limitation of the spectrum to the visible part causes a drop of sensitivity for c-Si based detectors. Due to the responsivity being concentrated to the visible, the radiometric sensitivity of a-Si : H photodetectors increases by changing the spectral bandwidth from a tungsten spectrum to IR filtered daylight from 4 to 11 V/(μJ/cm^2) for a 10 μm pixel.

Alternative to the integral sensitivity definitions given by (5) and (7), the sensitivity can also be defined for monochromatic illumination.

$$S_W(\lambda) = \frac{FF \cdot A_{pix}}{C_{int}} \cdot SR(\lambda) \tag{8}$$

and

$$S_E(\lambda) = \frac{FF \cdot A_{pix}}{C_{int} \cdot K_m} \cdot \frac{SR(\lambda)}{V_e(\lambda)}. \tag{9}$$

For color imagers, the relevant spectral range is definitely limited to the visible, since only this part of the spectrum can be evaluated to obtain color information. If a sensor with a significant infrared response is used, an additional IR blocking filter has to be applied in conjunction with the color filter array (CFA).

Based on the quantum efficiency data of a PPD imager with 7.8 μm pixels with color filter array [36] and the spectral response curves of a CFA filtered TFA APS with 7.0 μm pixel, the spectrally resolved sensitivity has been calculated for the RGB color channels. The data plotted in Figs. 3 and 4 reveal a higher sensitivity for the a-Si : H based detector in the monochromatic mode as well as for the three color channels. Especially in the blue channel the c-Si photodiode suffers from a reduced responsivity. Similar results can be concluded for PG pixels such as in [39].

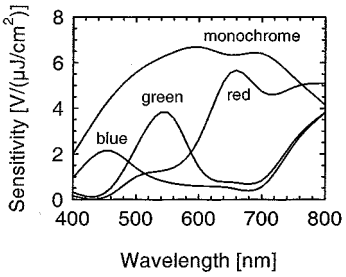

Fig. 3. Monochrome and color sensitivity of a PPD imager [36].

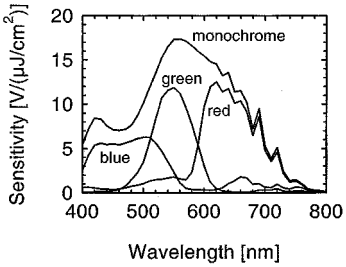

Fig. 4. Monochrome and color sensitivity of a TFA imager.

TABLE I
SENSITIVITY OF THE RED, GREEN, AND BLUE COLOR CHANNELS OF A PPD AND A TFA IMAGER

Sensitivity [V/(µJ/cm²)]	PPD [36] in 0.5µ	TFA APS in 0.8µ	TFA APS in 0.35µ
Pixel Size/µm²	7.8x7.8	10x10	7x7
Monochrome	5.5	10.9	14.2
Red	2.0	3.7	4.8
Green	1.6	3.3	4.2
Blue	1.1	3.1	4.0

In Table I, the monochromatic and color sensitivities of a PPD sensor are compared to those of two TFA arrays for daylight spectrum D65 [40]. While the TFA sensors exhibit approximately equal sensitivity in the three color channels, the values differ significantly for the PPD sensor. The unbalanced ratios for the PPD become more pronounced when incandescent illumination is used and result in an inferior signal-to-noise-ratio (SNR) of the blue channel. The low blue sensitivity limits the total SNR performance for color imagers as has been discussed already in [2], [33], [41].

The simple notation of sensitivity is not sufficient to characterize the performance of an image sensor, since noise is completely neglected. A more precise specification including all

time dependent and fixed pattern noise components is obtained by application of the ISO speed defined by ISO standard 12 232 [42]. Two criteria are defined which represent the first acceptable image and the first excellent image with an SNR of 10 and 40, respectively. The integrated illuminance required to fulfill these conditions is used to define a minimum illumination that has to be applied to ensure full sensor functionality.

In the authors' view, the ISO speed should be preferred as the main benchmark for characterization of sensitivity, since it is more related to applications and allows a direct correlation to photographic quantities. Additionally, the readout speed must be considered when comparing ISO speeds of different imagers, because at lower readout speed much lower noise levels can be achieved [43], [44].

A thorough investigation of the ISO speed of CCD sensors was published in [41]. A speed value of more than 100 000 was reported for a back-illuminated CCD due to its very low noise and virtually missing FPN though at an SNR of 10 dB and below 100 kPix/s readout rate only [45]. For the SNR $= 40$ definition, this corresponds to a speed of 970 since the sensor is mostly shot noise limited. Typical ISO speed values are around 200 as reported by Kriss for an SNR of 30 [41].

The ISO speeds for the first acceptable image of a TFA sensor [23] amount to ISO 80 and 200 with and without color filters respectively, at 14 Mpix/s readout speed, determined by fixed pattern noise rather than photon shot noise. A detailed noise analysis was performed for the noise components originating from the photodetector and the electronic circuitry [46]–[51].

Basically as a first-order approximation, the detector noise effects for c-Si and a-Si : H photodiodes can be disregarded since they are lower than the ASIC noise. Therefore comparison of the sensitivity as calculated above should allow to get an impression of the actual sensitivity of an imager and its applicability under lower light level conditions.

III. Sensitivity of Imagers

Overviews over state of the art image sensor concepts are given in detail in [31], [33], [52] or [53]. Here, only the three major CMOS pixel concepts as well as the TFA technology are reviewed with respect to sensitivity and scaling. A number of other special image sensor solutions were proposed, such as the base-stored image sensor (BASIS), charge modulation device (CMD), or static induction transistor (SIT), imagers. Since they do not offer major improvements of sensitivity or are not widespread they are not dealt here. Also, imagers with active amplification circuitry in the pixel are disregarded, since amplification can be applied to any of the following imager types.

One interesting approach "with nearly 100% FF" has been proposed by Dierickx *et al.* [55]. It tailors the substrate dopings in such a way that the photocharge that is generated in much of the substrate is redirected laterally by diffusion to a small collection diode. Theoretically all of the usually "dead" pixel regions can contribute to the sensitivity. Still, this sensor suffers from two strong loss mechanisms. A large fraction of the pixel area is covered with metal and polysilicon layers and the active transistors must be realized in a p-well where no photocharge collection can take place. This reduces the QE, especially in the critical blue part of the spectrum. Also, the structure shows a low modulation transfer function (MTF).

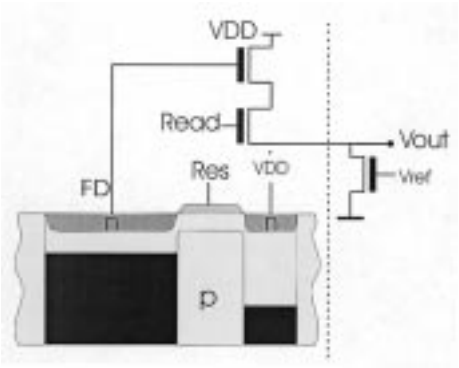

Fig. 5. Schematic diagram of a photodiode type pixel.

A. Standard Photodiode Imagers

The quasistandard for CMOS imagers, the photodiode pixel, is shown schematically along with the potential wells in Fig. 5. It contains three transistors per pixel and uses existing diodes as photodiode, e.g., the drain-substrate or well-substrate diode. The two readout transistors are shown schematically to the left of the dashed line. The reset transistor is part of the cross section.

Primarily all charge that is generated inside the depletion region is collected. Additionally, charge that is generated deeper in the substrate can diffuse due to the minority carrier concentration gradient toward the depletion region and can also be accumulated. For lower crosstalk between neighboring pixels future CMOS sensors with bulk photo diodes may have vertical overflow drains like current CCD sensors. However, these structures do not allow the diffusion of carriers from the bulk to the depletion region, thereby reducing red and IR sensitivity. Photo charges generated too close to the surface in the n-diffusion do not diffuse to the space charge region but recombine at the surface states leading to a loss of blue sensitivity. The quantum efficiency strongly depends on wavelength (Fig. 2): the deeper the collection region extends into the bulk, the further the response curve extends into the infrared. This structure is able to even collect charges by lateral diffusion as was measured for example in [54]. This mechanism increases the effective fill factor [5] and leads to a deterioration of the MTF in the red and IR spectrum [55]–[57]. Also, pixel circuitry that needs to keep small charges for longer times as, e.g., central shutter operation with short integration times are not easily possible since complete screening of photo charge is hard to accomplish [58].

Though a lot of photocurrent is gained through diffusion, the overall quantum efficiency is only medium or even poor, especially when neither the design nor the process is optimized for sensitivity [11], [59]. Metallization layers and polysilicon absorb and reflect considerable fractions of the incident light. The short wavelengths get lost due to surface recombination at the Si/SiO_2 interface. Reflection and absorption losses occur in the mostly transparent dielectric and passivation layers. So hardly any photodiode sensor can be found in the literature with a QE*FF product of more than 60% but many with less than 20%.

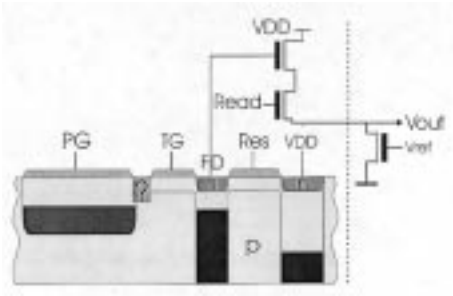

Fig. 6. Schematic diagram of a photogate type pixel.

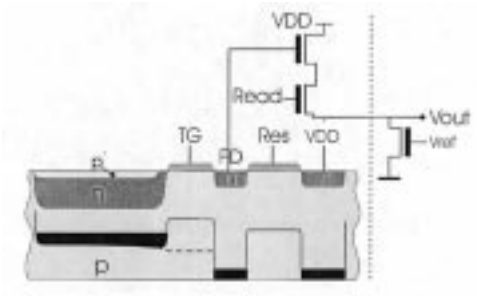

Fig. 7. Schematic diagram of a pinned photodiode pixel.

Moreover, the load capacitance of the photodiode is so large that it actually makes sense to shrink the photodiode without changing the pixel size in order to get a smaller load capacitance while still collecting photocharge through lateral diffusion, as shown by Yadid-Pecht *et al*. in [17]. Additionally, the diode capacitance is voltage dependent, which leads to a nonlinearity corresponding to a gamma larger than one. While this is positive for larger dynamic range, it makes color reproduction more difficult. As a typical value for a 14×14 μm^2 pixel in a 0.8 μ process with 60% FF the photodiode contributes around 93 fF to the total integration capacitance of 102 fF, which is equivalent to only 1.6 μV/e$^-$ conversion gain and gives a low sensitivity of 1.8 V/(μJ/cm^2). One way to improve the situation is the use of microlenses on pixels with small size photodiodes which may lead to acceptable sensitivities.

B. Photogate Imagers

A better solution to the large capacitance problem is the use of the photogate pixel (Fig. 6). It employs the operation principle of the CCD concerning integration, transport, and readout inside every single pixel [18]. During integration, the photocharge is accumulated in the potential well under the photogate PG. For readout, the complete charge can be transferred via the transmission gate TG onto the floating diffusion FD after that had been reset. So most of the photosensitive area does not contribute to the charge to voltage conversion capacitance. The resulting high conversion coefficient (e.g., 3.6 fF$\hat{=}44$ μV/e$^-$ [39]) allows for a high sensitivity. As an additional advantage this reset-transfer-readout permits true CDS (correlated double sampling) operation including subtraction of kTC noise, which becomes large for small capacitances (1 mV for the above 3.6 fF).

However, the large conversion gain is mostly lost by the low transparency of the overlying gate material. Typically, 22% transparency at 500 nm can be found for polysilicon with even lower values for blue [60]. Special transparent gates [31] have been proposed but have not been implemented in volume processes [57]. This loss in sensitivity can be compensated by increasing the size of the photogates as demonstrated in [61], [62] where 17.5 V/lxs have been achieved. But this also increases sensor cost and reduces resolution. Standard size pixels of 16 μm in 0.8 μ CMOS technology typically achieve 4 V/lxs [39]. In the region marked with the question mark in Fig. 6, the potential wells of the PG and TG need to meet. A standard CMOS process is a single gate process that does not allow two different gates to overlap [44] as is common for CCD processes. So, a coupling diffusion needs to be inserted between PG and TG [58]. This increases the effective floating capacitance during transfer resulting in lower conversion gain. It may lead to image lag and the kTC noise cannot be removed completely any more.

C. Pinned Photodiode Imagers

A more promising solution for increased sensitivity is the use of a so-called pinned photodiode as the photodetection element. Originally developed as detector with reduced dark current replacing the MOS varactor in CCDs [19], it has proved to be equally beneficial for CMOS pixels. The working principle is explained on Fig. 7. The PPD basically consists of a p$^+$np$^-$ structure where both p layers are on substrate potential (GND). As the voltage applied to the n-layer is increased, the depletion regions of both pn-junctions grow toward each other. At a certain voltage, the pinned voltage V_p, the depletion regions meet and no more majority carriers can be extracted from the device. The device is fully depleted [63]. The potential then remains fixed inside the device and cannot be increased any further. The voltage is pinned.

For light sensing operation, the PPD is initially fully depleted. During the integration phase, photogenerated majority carriers are stored in the depletion region, decreasing the potential of the PPD below V_p. For readout ,the floating diffusion FD is first reset to VDD. This reset potential may now first be read out for true CDS. Next, the transfer gate TG is opened and the complete photocharge is transferred to FD, which ensures lag-free operation [64]. The complete transfer takes place if the voltage on FD remains above the pinning voltage while the PPD operates below this voltage.

The greatest benefit of this structure lies in the complete charge transfer from a large area, large capacitance diode into the small floating diode capacitance. The second advantage is the separation of the charge collection region away from the silicon surface into the bulk through the top p$^+$ layer, equivalent to a buried channel CCD structure [65]. This surface state pinning results in a great reduction of dark current and white point defects [66] that stem from a large density of recombination centers at the surface.

Alternatively, the transfer transistor may be left away [67]. The complete photogenerated charge is then collected in FD already during integration. On the positive side pixel complexity is reduced and fill factor and sensitivity increase. Also V_p can be made very low since the PPD does not need to operate below V_p. On the other hand, kTC noise cannot be removed any more.

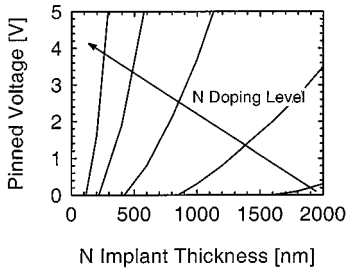

Fig. 8. Thickness dependence the pinned voltage of a PPD for n doping levels of 1×10^{15}, 3×10^{15}, 1×10^{16}, 3×10^{16}, 1×10^{17} cm^{-3}. The values are calculated for fixed concentrations of the p$^-$ substrate and the top p$^+$ implant of 10^{15} and 10^{19} cm^{-3}, respectively.

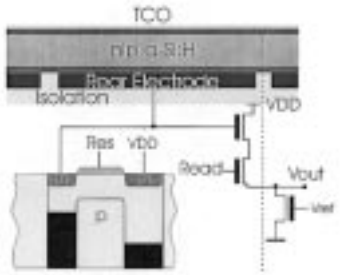

Fig. 9. Schematic diagram of a TFA pixel.

Fill factor and sensitivity may also be increased by use of microlenses which yields a total sensitivity of e.g. 5.5 V/(μJ/cm^2) [36].

In order to investigate the voltage pinning, the PPD is assumed to consist of a one-dimensional (1-D) p$^+$np$^-$-diode with the depletion width w_n inside the n-layer

$$w_n = \sqrt{\frac{2 \cdot \varepsilon_0 \cdot \varepsilon_r}{q} \cdot (V_{bi} - V_n) \cdot \frac{N_A}{N_D} \cdot \frac{1}{N_A + N_D}} \qquad (10)$$

where

N_A and N_D doping concentrations;
V_n voltage applied to the n-layer;
V_{bi} built-in voltage.

V_p is the potential of the n-region where the widths of both depletion regions w_{np^-} and w_{np^+} together amount to the total width of the n-layer, as follows:

$$V_p = V_n|_{w_{\mathrm{np}^-} + w_{\mathrm{np}^+} = w_{\mathrm{n}}}. \qquad (11)$$

Two–dimensional semiconductor simulations with the device simulator MEDICI showed that the depletion regions actually do not grow together uniformly but in a beak shape. Still, the pinning voltage derived from the simplified assumptions above match well with the simulation results. Fig. 8 shows V_p over the width of the n-region for various doping levels.

For a given target value of V_p, one can choose from various combinations of depth and doping. However, for higher doping concentration the depth window becomes very narrow and V_p strongly depends on the n-depth. So depth and doping levels must be tightly controlled to ensure sufficient headroom above and below V_p for device operation. Since three doping levels must be superimposed, the starting doping level of the substrate must be moderate which comes with larger scale processes or twin well processes [9]. These measures add complexity and cost to the CMOS process and the process deviates from the main stream standard. The implementation of a PPD process by at least one large semiconductor company [36] may indicate that the cost for the two extra mask steps necessary for the PPD [35] do not represent a road block to economic realization if market demand is there as Wong pointed out already in [60].

PG and PPD both offer charge transfer from a large collection device to a small FD. But PPDs have much higher quantum efficiencies and need fewer control signals to be wired into the pixel. This gives the PPD concept extra advantages over the PG alternative leading to higher sensitivities. Also, the reduction of leakage currents through surface pinning is automatically included in the PPD but not in the PG concept. However, the PPD module which lies at the core of the process has to be adapted to every new process generation.

D. TFA Imagers

The principle elements of a TFA pixel are shown semistructurally in Fig. 9. The photodiode consists of a rear electrode, an amorphous silicon diode and a transparent conductive oxide (TCO) front electrode. The important issue is the deposition of the photodiode on top of the ASIC. Thus the whole pixel area is available for the photodiode, resulting in an effective fill factor of 100%. In praxis the rear electrodes are spaced, which may lead to loss of photogenerated charge in the gap due to the short carrier lifetime. But as long as the fields remain strong enough, photocurrent is also collected from these regions which justifies the statement of 100% FF [68]. This has been verified experimentally with subpixel resolution measurements. In a 4 μm gap of a 1.5 μm thick diode the collection drops by less than 10% [50].

The local contrast of a TFA imager has been measured and is higher than 86 dB although the a-Si : H layer is not patterned.

There are no further layers on top of the photodiode that may obstruct the light penetration such as further metallization, polysilicon, and dielectrics, as in sensors with the diode in the bulk. The reflection losses are minimized by optimization of thickness of the TCO layer. The typical quantum efficiency is around 60% in most of the visible range peaking at 80% as shown in Fig. 2. This delivers approximately 1 fA of photocurrent per μm^2 diode area at 1 lx daylight illumination. Generally, the choice of material, detector structure, and spectral response of the overlaying detector can be tailored according to the application. For example the blue and UV or the NIR response is enhanced by use of amorphous silicon-carbon [69] or silicon-germanium alloys [70]. Moreover, a color sensor has been realized in TFA technology based on a thin-film system where the diode detects the three primary colors in each pixel [25]. Usually, however, color filter arrays are added on top of the detector.

A typical TFA sensor [23] in 0.8 μm CMOS technology has 10×10 μm pixel size and though the sensing capacitance C_{FD} is 20 fF large, equivalent to 8 μV/e$^-$, it reaches 8 V/(μJ/cm^2) or 3.1 V/lxs. Beside the floating diffusion and the readout gate, the TFA pixel's sensing capacitance is increased by the intrinsic diode capacitance and the parasitic wiring capacitance including the capacitance between the rear electrode and underlying metal

TABLE II
TECHNOLOGY PARAMETERS FOR DIFFERENT PROCESS GENERATIONS

Process	0.8µ	0.5µ	0.35µ	0.25µ	0.18µ	0.1µ
Supply Voltage [V]	5 – 3.3	5 – 3.3	5 – 3.3	2.5 – 1.8	1.8 – 1.5	1.2 – 0.9
Interconnect Levels	2	2 – 3	4 – 5	5 – 6	6 – 7	8 – 9
Substrate Doping [cm^{-3}]	8 x 10^{16}	1.2 x 10^{17}	2.5 x 10^{17}	3.4 x 10^{17}	5 x 10^{17}	1 x 10^{18}
D/S - Junction Depth [nm]	350 – 450	300 – 400	200 – 300	50 – 100	36 – 72	20 – 40
Depletion Region [µm]	0.71	0.57	0.39	0.24	0.19	0.1
Mobility [cm^2/Vs]	825	715	550	485	425	345
Life Time [µs]	3.6	2.3	1.1	0.8	0.6	0.3
Diffusion Length [µm]	88	68	41	33	25	15

layers. Both counteract the advantage of excellent fill factor and quantum efficiency and therefore need to be kept small.

The totally depleted a-Si : H photodiode exhibits an approximately constant capacitance for reverse bias operation [71], thus providing a linear charge to voltage transfer characteristic. A standard diode of 1.5 μm thickness has a capacitance of $c_{D0} = 0.085$ fF/μm^2, which yields an intrinsic sensitivity of

$$S_{W0} = \frac{S_0}{c_{D0}} = 30 \cdot \frac{V}{\mu \mathrm{J/cm}^2}. \tag{12}$$

The diode capacitance may be lowered by increasing the thickness of the intrinsic layer or by reducing the rear electrode area. With increasing diode thickness, the dark current will rise [72] imposing a limit on that measure. The rear electrode may be shrunk without degrading carrier collection as long as the electric field exeeds approximately 5×10^3 V/cm [73]. Also the field distribution and therefore the collection behavior depends on the potential difference between neighboring diodes. A good tradeoff between the above mentioned factors is the use of a ring-shaped rear electrode that provides good collection throughout the diode and still permits reduction of capacitance.

A major advantage of TFA is the 3-D integration. This allows for the implementation of more complexity into every pixel while automatically keeping the size and sensitivity of the diode large; this is in contrast to a CMOS design where active circuitry and photodetection elements compete for the pixel area.

The manufacturability of amorphous silicon layer systems is demonstrated for well established products, for example in the fields of active matrix addressed LCDs and thin-film solar cells.

IV. IMPACT OF SCALING ON SENSITIVITY—GENERAL TRENDS

A. Overview

Further decrease in pixel size much beyond 5×5 μm^2 has been considered not to be of much interest because of camera lens diffraction issues [74]. But since in a common Bayer patterned RGB color sensor 2×2 pixels define an effective color pixel, further downscaling of single pixels may be useful to fit one effective color pixel into the optical lens resolution limit. Several approaches with CCD and CMOS pixel dimensions of less than 5×5 μm^2 can be found in recent publications [75]–[78], demonstrating that CMOS imagers will benefit from further structure downscaling in terms of reducing pixel size and increasing imager resolution. So pixel sizes below 5×5 μm^2 can be expected for all imager types as opposed to the assumption Wong made in [60].

The use of silicon-on-insulator (SOI) technology for image sensors was described by Wong in [60]. However, PPD structures in SOI technology may be impossible due to the small silicon layer thickness. But in contrast to former assumptions, the current SIA Roadmap expects bulk and epi-wafer to remain available beside SOI in the future [79].

CMOS processes with structure sizes of 0.25 μm and beyond will offer silicided drain/source structures as a standard. Due to their small sheet resistance, silicided diffusions can be used for interconnection purposes. This reduces the amount of interlayer contacts in dense designs, shrinking the pixel layout size further. Additionally, the silicidation protects the shallow diffusion from punch through. To avoid a loss of transmission and hence a loss of sensitivity, it becomes necessary to use silicide blocking features for an optical window in the photosensitive area that must be available in the processes.

The predicted supply voltage downscaling (Table II) will lead to a reduction of usable signal range and together with increased noise components will limit the overall dynamic range. Sources of detrimentally high leakage currents generating shot noise and flooding the pixel are discussed by Wong (e.g., dark current, PN junction tunneling current, transistor off current, gate oxide leakage and hot-carrier effects).

Due to the downscaling of the effective integration capacitance within the pixel the kTC noise will become more and more important. A 3×3 μm^2 PPD pixel in 0.18 μm technology with an overall sense capacitance of 1.8 fF will cause a kTC noise of about 1.6 mV. Assuming an analog supply voltage of 1.8 V and an ADC with 12 Bit effective resolution the kTC noise will exceed 2 LSB, limiting system performance. Being able to eliminate both kTC and 1/f noise, real correlated double sampling on chip will become inevitable. Other novel circuit techniques have been proposed in the literature that can be employed with certain limitations where true CDS is not available as in TFA or photodiode pixels. Examples are the weak reset [80] or active reset circuitry per pixel [81].

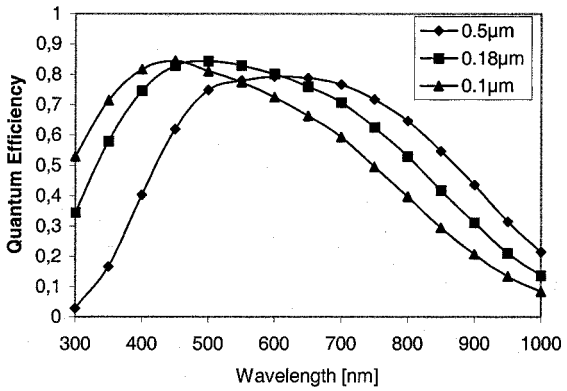

Fig. 10. Internal carrier collection efficiency under scaling trends.

B. Scaling Effects on Diffusion Photo Current

As Wong [60] points out the diffusion collection behavior is modified through the reduction of mobility and life time with increasing doping levels. Under strong absorption conditions where the absorption coefficient $\alpha(\lambda)$ and the diffusion length L_n both are much smaller than the width of the substrate the photocurrent density through diffusion in the substrate can be derived, e.g., from Yang [82] as

$$j_{Ph} = \frac{q \cdot \Phi_S}{1 + \dfrac{1}{\alpha(\lambda) \cdot L_n}} \tag{13}$$

where Φ_S is the photon flux entering the neutral p-substrate region. Further effects on spectral sensitivity result from the shallower drain/source diffusion and the shrinkage of the depletion widths. With a simplified model for the surface recombination loss, the quantum efficiency for the light entering the silicon can be calculated for different process generations. Technology parameters are taken from [79] and shown in Table II.

Fig. 10 demonstrates that the scaling effect on diffusion collection efficiency works in favor of CMOS imagers. The influence on mobility and lifetime are not very strong so the loss of sensitivity in the infrared range is not very pronounced. On the other hand, the shallower diffusions promote the collection of the blue light that enters the silicon material. That improves performance for visible light applications, especially for color sensors, as was shown above. This scaling behavior directly applies to photodiode, PG and PPD imagers while in TFA collection in the bulk is of no importance. It must be noted, however, that the losses caused by the overlying layers must be included which reduce the total QE considerably.

V. Impact of Scaling on Imager Sensitivities

A. Standard Photodiode Imagers

An average value for the scaling of a photodiode pixel size is $14^*\lambda$ where λ is the minimum process feature size [83]. The lens diffraction limit of 5 μm has been reached with the 0.35 μm process. The increased number of routing levels leads to an increasing thickness of the layer system on top of the diode which aggravates the problems of absorption, reflection, diffraction, or even light guidance into far away pixels. Also, the light that passes trough the color filters will spread over many pixels, rendering color separation difficult, as the filter moves far away from the photodiode. The accuracy requirements of microlenses become very strict as the sensitive spot in the pixels becomes smaller and moves further away from the lens. The same applies to PPD and PG pixels.

Below 0.35 μm, only processes that allow blocking of silicide layers on diffusions can be employed. Workarounds like field oxide windows into the substrate as proposed by Wong [10] cannot fully compensate the drawback of silicidation. Generally, the shrinkage of capacitances does not sufficiently compensate for the reduction of sensitive area. In fact, the area specific capacitance c_{D0} increases due to increased doping concentrations which automatically reduces the sensitivity. So with a given fill factor overall sensitivity remains low as calculated in Table III. Examples for small scale process imagers are presented in [12], [38].

B. Pinned Photodiode Imagers

As mentioned before, PPD pixels without transmission gates can be expected to scale nearly like photodiode pixels but are not favored as they do not allow true CDS. The extra complexity of the transfer gate is generally accepted and leads to slightly larger pixels with $16^*\lambda$ as a rule of thumb. As slight increases in pixel size pay off with strong increases in sensitivity downscaling may not be followed too closely but for example with $20^*\lambda$ proportionality.

The necessary process add-ons need to be realized for every new technology node. These include salicide blocking for acceptable transparency and two extra implantation steps for the p^+np^- structure based on a twin well process with reduced substrate doping. The reduction of supply voltage increases the challenge to reach a well controlled and reproducible pinned voltage that leaves enough head room during integration and readout.

C. Photogate Imagers

Average photogate pixels scale with $20^*\lambda$ due to the larger number of active devices and wirings per pixel. The 5 μm pixel size limit will therefore be reached with 0.25 μm technology. Salicidation on gate material is likely to become widespread for 0.25 μm and below, which forbids photogate pixels. While silicide blocking on diffusions is beneficial for building IO cells, no benefit to salicide blocking on transistor gates, except for PG pixels, is known to the authors. Metal gates with virtually no transparency are expected to be reintroduced for very advanced process generations which are useless for PG sensors [79].

D. CCDs

Permanent pixel size shrinkage does not leave CCD technology unaffected. According to Kriss, ISO speed of CCDs scales down linearly with pixel area [41]. Pixel sizes below 5 μm are customary [84], [85] and still reach fill factors above 80% though this number includes areas covered by polysilicon layers. Readout conversion gain has not increased much (e.g., 15 $\mu V/e^-$ [77]) partly due to the high bandwidth and readout speed demands which are a consequence of the single charge

TABLE III
SCALING TRENDS OF IMPORTANT CMOS SENSOR PARAMETERS FOR STANDARD PHOTODIODE (STD.), PPD, AND TFA SENSORS AND A TFA SENSOR WITH MINIMUM REAR ELECTRODE (MIN)

Technology	0.8µ			0.35µ			0.25µ			0.18µ					
Sensor Type	Std.	PPD	TFA	Std.	PPD	TFA	Std.	PPD	TFA	Std.	PPD	TFA	Min.	PPD	TFA
A_{pix} [µm²]	14x14	14x14	14x14	7x7	7x7	7x7	5x5	5x5	5x5	5x5	5x5	5x5	5x5	3x3	3x3
FF [%]	60	60	100	60	60	100	60	60	100	80	80	100	100	44.4	100
A_{sia} [µm²]	117.6	117.6	196	29.4	29.4	49	15	15	25	20	20	25	25	4	9
C_{ox} [fF]	5.75	7.19	5.75	2.7	3.4	2.7	1.87	2.14	1.87	0.65	0.83	0.65	0.65	0.83	0.65
C_{gate} [fF]	2.06	2.06	2.06	1.1	1.1	1.1	0.67	0.67	0.67	0.48	0.48	0.48	0.48	0.48	0.48
C_{par} [fF]	1	1	—	0.6	0.6	—	0.6	0.6	—	0.5	0.5	—	—	0.5	—
C_{dio} [fF]	93.4	—	12	37.2	—	4.3	37.7	—	2.5	23.7	—	2.5	1	—	~1.6
C_{FD} [fF]	102.2	10.3	19.8	41.6	5.1	8.1	40.8	3.41	5	25.3	1.81	3.6	2.13	1.81	2.73
q/C [µV/e⁻]	1.5	15.5	8.1	3.8	31.4	19.8	3.9	46.9	32	6.4	89	45	75	89	59
S [V/(µJcm⁻²)]	1.8	17.7	23.2	1.1	8.9	14.2	0.57	6.8	11.9	1.2	17.1	16.3	27.5	3.4	7.7

to voltage conversion stage per array. Thus, the gap between CMOS and CCD in terms of sensitivity is diminishing and is expected to close for future high performance multimegapixel sensors. What remains is the absence of dark FPN and the much lower dark current- and photo-FPN (as low as 0.25% [41]) that CCDs achieve by virtue of their readout mechanism and maturity. This still provides a great advantage for the overall performance while system integration remains basically inaccessible for CCDs.

E. TFA Imagers

Due to the 3-D integration, scaling of TFA imagers can go as fast as $12.5^*\lambda$ since no extra space for a photodiode is needed in the pixel. But similar to the PPD increases in pixel size improve sensitivity overproportionally which can be expected to be exploited giving an approximate $14^*\lambda$ scaling. The increasing number of routing levels will distort the aspect ratio: a detector of 3 to 4 μm in size will be placed 5 to 10 μm above the active circuitry whereas current sensors have 10 μm size photodiodes 4 μm above the silicon. This trend affects the parasitic capacitances occurring at interconnects that run from the substrate up to the rear electrode. Coupling between these interconnects ultimately deteriorates the MTF and may degrade color separation. Coupling capacitances to inter- and intrapixel wires increase the capacitive load and therefore lower the sensitivity. These parasitic components will predominate the TFA specific sensing capacitance in future. Currently, the rear electrode delivers the largest contributions.

Presently, insulators with dielectric constants of 3.5 to 4 are mostly employed. This value is expected to be pushed below 2.0 not far from now which alleviates the capacitive coupling effects. Optical problems with smear of color pattern over many photodiodes will not occur since the detector is directly beneath the color filter, on top of all other layers. Microlenses play no role due to the inherent 100% FF.

Overall, the optical problems that come in due to the high stack of dielectric layers for the crystalline silicon detector types is traded against capacitive coupling problems for the TFA solution. In the first case, the signal has to be passed optically through the dielectric layers, in the second case, electrically. Both ways, signals couple to neighboring pixels and may suffer from loss but the electrical effects are weaker and easier to compensate or to allow for, e.g., in the color correction algorithms.

TFA easily goes with every new process generation without regard of the optical properties of the ASIC. Advantages of silicides, salicides, SOI, and metal gates can be fully exploited. Amplifiers, arithmetics, or other complex pixel architectures especially profit from the 3-D integration like kTC noise reduction that will become necessary. Sensors with 17 transistors and two capacitors per pixel [24] can be implemented in a 5 μm pixel at the 100 nm node with unaffected sensitivity due to the FF of 100%.

VI. COMPARISON OF IMAGER TYPES

Table III compares standard CMOS three transistor pixels without (Std.) and with enhancements through PPD or TFA with regard to the effective integration capacitance, conversion gain, and resulting sensitivity for given technologies. Technological parameters are derived from actual processes of different vendors. Pixel dimensions (A_{pix}) assume a moderate scaling between 16 to 20 times the minimum structure size, providing an increased sensitivity and allowing all sensors types to fit into the same pixel area. The effective integration capacitance C_{FD} consists of the diode diffusion of the reset transistor C_{diff}, the readout gate C_{gate}, parasitic wiring capacitances C_{par} and, except for PPD pixels, the photodiode capacitance C_{dio}. For TFA sensors, the parasitic capacitances are included in the diode capacitance.

The sensitivity is calculated as an effective value at the pixel readout node C_{FD} without any pre- or post-amplification being applied. It depends on effective integration capacitance, pixel area and fill factor.

$$S_W(\lambda) = FF \cdot A_{pix} \cdot \frac{SR(\lambda)}{C_{FD}}. \tag{14}$$

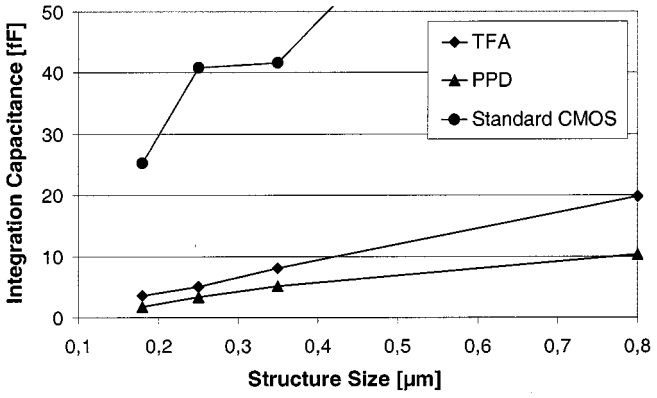

Fig. 11. Downscaling of integration capacitances.

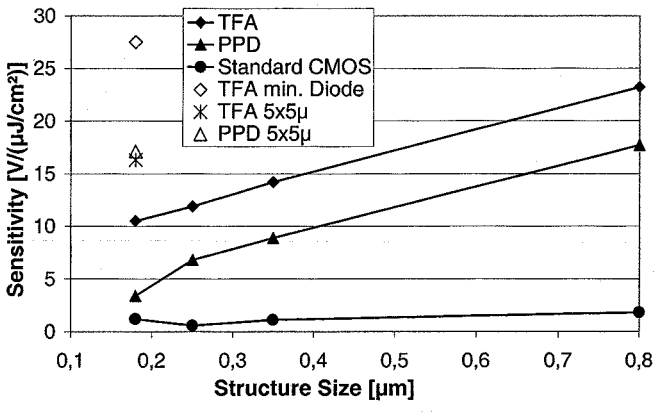

Fig. 12. Downscaling of sensitivity with pixel options.

This formula is used to scale the sensitivities starting from a given sensitivity in a certain technology generation. For the standard photodiode pixel (Std.), a QE of 45% is assumed based on an average of good sensors in the literature. These numbers may in fact be improvable when reaching higher QE and by using smaller size detectors with higher effective FF due to lateral collection as noted above, the general trend, however, remains. For the PPD the data of [9] are taken and scaled according to the formula above while the TFA data are based on [23]. For the scaling formula (14) fill factor is assumed to have linear influence though lateral diffusion in bulk technologies give relatively larger sensitivity for smaller fill factors. This might overestimate the sensitivities of PPD and Std. imagers in downscaled processes. The PG type is not included since the PPD offers better performance at similar functionality. For the 0.18 μ node extra options listed include use of minimum TFA rear electrodes and shrinking down pixel size to 3×3 μm.

Fig. 11 depicts the total integration capacitance C_{FD} versus the minimum CMOS structure size. While standard CMOS structures suffer from high area junction capacitances due to their large effective diffusion area, PPD and TFA values are by a factor of ten lower, containing only small contributions from C_{diff}. Both PPD and TFA type pixels benefit from downscaling CMOS structure size despite of technology related increasing area capacitances. PPD starts with a significantly lower value due to the suppressed diode capacitance, while TFA gets additional advantages by scaling down the diode size at constant area capacitance. When using minimum rear electrodes (Min.) as discussed above, the TFA diode related portion of the total capacitance drops to 15% for a 5×5 μm^2 pixel in 0.18 μ technology.

The plot of sensitivity from Table III in Fig. 12 shows that the sensitivity of a standard CMOS pixel is always low due to the large integration capacitance as depicted in Fig. 11. PPD and TFA pixel sensitivities are scaled down both due to the loss of pixel area. Due to high FF and QE, TFA provides higher values despite higher integration capacitances. Only in the case of the 0.18 μ process with large pixel size 5×5 μm^2 (e.g., for b/w applications), PPD pixels shows slightly better performance than TFA. However, with smaller size rear electrodes (Min.) TFA performs again better.

VII. Summary and Conclusions

In this paper, the definition of sensitivity is reviewed and use of the radiometric unit in V/(μJ/cm^2) is proposed rather than the photometric sensitivity in V/lx s. At the same time, the illumination spectrum is very important and must be given for good comparability. This is especially important for sensors aiming at color applications where IR cutoff filters are indispensable. For a more general benchmark which also includes all temporal and fixed pattern noise, the ISO speed according to ISO standard 12 232 is to be preferred. It is adequate for a benchmark between all kinds of image sensors for visible light, provided that the readout speed is stated along with the ISO value.

Image sensors based on standard CMOS technology are gaining ground against CCDs, especially as the processes scale down further and special technological enhancements and new designs keep breaking performance barriers. While smaller scale processes provide the basis for megapixel sensors, sensitivity enhancements are necessary. Techniques as the PG-, PPD- or TFA-technology address this issue. Among the crystalline silicon detectors, the PPD provides the maximum performance at moderate extra cost. But it can be outperformed by amorphous silicon diodes in TFA technology due to its 100% FF and 80% peak QE for green light, particularly if capacitance reduction is pursued consistently.

While scaling effects that increase leakage current or reduce dynamic range affect c-Si and a-Si : H equally, only TFA imagers are immune against negative scaling impacts on sensitivity such as salicidation or SOI. Special process enhancements are necessary to keep sensitivity of c-Si detectors acceptable under scaling. For PPD imaging modules, salicidation blocking, PPD implantation and optionally microlenses are necessary. These process modules need to be adapted to every new process generation while the TFA backend process is likely to be adaptable to any new chip generation with only minor fine tuning. In the future, the sensitivity of all investigated imager types will diminish with scaling since the photoactive region shrinks very quickly. If pixel size is always shrunk with the feature sizes, then TFA will remain to be the best option of the technologies known in literature today with regard to sensitivity.

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Tarek Lulé was born in Kabul, Afghanistan, in 1969. He received the undergraduate degree in physics from the University of Siegen, Germany, in 1990 and the M. Phil. degree in microelectronics from the Cambridge University, U.K., in 1992.

From 1993 to 1997, he was a Research Assistant at the Institute of Semiconductor Electronics, University of Siegen, involved in the design and characterization of new types of TFA image sensors with very high dynamic ranges. Since 1997, he is with Silicon Vision GmbH, Siegen, Germany, where he is heading the automotive vision group.

Stephan Benthien was born in Lübeck, Germany, in 1957. He received the Dipl.-Ing. degree in electrical engineering from the University of Siegen, Germany, in 1994.

From 1994 to 1997, he was a Research Assistant at the Institute of Semiconductor Electronics, University of Siegen, Germany, where he worked on the design and characterization of new types of TFA image sensors with very high dynamic range. Since 1997, he has been with Silicon Vision GmbH, Siegen, where he is Head of the consumer products group.

Holger Keller was born in 1967. He received the Dipl.-Ing. degree in electrical engineering from the University of Siegen, Germany, in 1994. In the same year, he joined the Institute for Semiconductor Electronics at the University Siegen, Germany, as a Designer of TFA image sensors.

Since 1997, he is with Silicon Vision GmbH, Siegen, Gemany, where he is engaged in the development of new types of image sensors.

Frank Mütze was born in Hattingen, Germany, in 1970. He received the Dipl.-Ing. degree in electrical engineering from the University of Siegen, Germany, in 1998.

He joined the Institute for Semiconductor Electronics, University of Siegen, where he was responsible for the design of TFA UV image sensors. Since he joined Silicon Vision GmbH, Siegen, in 1998, he has been engaged in the development of radiation hard image sensors and thin-film memory devices.

Peter Rieve was born in Waldbröl, Germany, in 1968. He received the Dipl.-Ing. and Dr.-Ing. degrees in electrical engineering from the University of Siegen, Germany, in 1994 and 2000, respectively.

From 1994 to 1997, he was a Research Engineer at the Institute for Semiconductor Electronics, University of Siegen. He worked in the field of TFA color imaging and focused on the development of spectrally selective optoelectronic sensors based on amorphous silicon. Since 1997, he has been with Silicon Vision GmbH, where he is heading the R&D department.

Konstantin Seibel was born in Krasnojarsk, Russia, in 1959. He received the Dipl.-Phys. degree in physics from the University of Novosibirsk, Russia, in 1980.

He has been in the semiconductor industry for 15 years. In 1997, he joined the Institute for Semiconductor Electronics, University Siegen, Germany, where he studied the noise of amorphous silicon p-i-n diodes. Since 1998, he has been with Silicon Vision GmbH, Siegen, Germany, where he is engaged in the development of thin-film devices for TFA technology.

Michael Sommer was born in Werdohl, Germany, in 1967. He received the Dipl.-Ing. degree in electrical engineering from the University of Siegen, Germany, in 1993.

From 1993 to 1997, he was a Research Assistant at the Institute of Semiconductor Electronics, University of Siegen, where he worked on the design and characterization of new types of TFA image sensors with very high dynamic range. Since 1997, he has been with Silicon Vision GmbH, Siegen, where he is engaged in the development of linear image sensors and multispectral diode based color imagers.

Markus Böhm was born in Gundersheim, Germany, in 1953. He received the Dipl.-Ing. and the Dr.-Ing. degrees in electrical engineering from Technical University Berlin, Germany, in 1979 and 1983, respectively.

In 1984 and 1985, he was a Visiting Scientist with the Department of Electrical Engineering, University of Delaware, Newark. In 1985, he joined Chronar Corporation, Princeton, NJ. Since 1989, he has been a Professor at the University of Siegen, Germany, where he is Head of the Institute for Semiconductor Electronics. His research interests focus on thin-film technology, novel imaging devices, and photovoltaics. He is a co-founder of Silicon Vision GmbH, Siegen.