Vignesh Balaji

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Research Interests

Architectural Support for Irregular workloads (focus on Graph Processing), Synchronization Optimizations for multi-threaded workloads, and Cache Coherence protocols

Education

2015 -   **Carnegie Mellon University, Pittsburgh**
PhD in Electrical and Computer Engineering
Advisor: Brandon Lucia
Field: Computer Architecture

2011-2015   **Birla Institute of Technology and Science (BITS) Pilani, India**
B.E. (Hons.) in Electronics and Instrumentation
Thesis: *Design of a resource tracker for a runtime reconfigurable coprocessor*
GPA: 9.34/10 (Department Rank: 1)

Research Experience

Sep 2015 - Present   **Carnegie Mellon University**
Graduate Research Assistant
My research focuses on improving the efficiency of irregular memory access workloads (with a focus on graph processing applications). We are exploring both software optimizations and architectural extensions that leverage structural properties of real-world input graphs to improve the cache locality and bandwith utilization of graph applications.

Jan 2015 - May 2015   **Indian Institute of Science (IISc), Bangalore**
Project Assistant
My undergraduate thesis was on the design of a resource availability tracker that was used to decide the appropriate kernel to be scheduled on a runtime-reconfigurable coprocessor (RE-DEFINE).

Professional Experience

May 2019 - Aug 2019   **Intel Labs, Santa Clara**
Summer Intern
Explored optimizations for streaming tensor factorization workloads by leveraging properties of real-world input tensors.

May 2018 - Aug 2018   **Nvidia Architecture Research Group (ARG), Massachusetts**
Summer Intern
Worked on developing analytical models for an accelerator (targeting graph processing and sparse linear algebra) and understanding the trade-off space for on-chip buffer management on the accelerator.

May 2014 - **Aug 2014**	**IBM Semiconductor Research and Development Centre (SRDC), Bangalore** *Summer Intern* Worked on exploring the feasibility of Tunnel Field Effect Transistors (TFETs) as a replacement technology for CMOS transistors.
May 2013 - **Aug 2013**	**Indira Gandhi Centre for Atomic Research (IGCAR), Kalpakkam** *Summer Intern* Worked on designing a SoC-based system to detect the health of an electrochemical hydrogen sensor deployed in the Fast Breeder Test Reactor.

Publications

- **Combining Data Duplication and Graph Reordering to Accelerate Parallel Graph Processing**
  Vignesh Balaji, Brandon Lucia
  Paper in International Symposium on High-Performance Parallel and Distributed Computing (HPDC) 2019

- **When is Graph Reordering an Optimization?**
  Vignesh Balaji, Brandon Lucia
  Paper in IEEE International Symposium on Workload Characterization (IISWC) 2018
  (Best Paper Award)

- **Flexible Support for Fast Parallel Commutative Updates**
  Vignesh Balaji, Dhruva Tirumala, Brandon Lucia
  (ArXiv 2017)

- **An Architecture and Programming Model for Accelerating Parallel Commutative Computations via Privatization**
  Vignesh Balaji, Dhruva Tirumala, Brandon Lucia
  Poster presented as part of PPoPP 2017

- **Intermittent Computing: Challenges and Opportunities**
  Brandon Lucia, *Vignesh Balaji*, Alexei Colin, Kiwan Maeng, Emily Ruppel
  Paper in Summit on Advances in Programming Languages (SNAPL) 2017

- **Overcoming the Data-flow Limit on Parallelism with Structural Approximation**
  Vignesh Balaji, Brandon Lucia, Radu Marculescu
  Paper presented in Workshop on Approximate Computing (WAX) 2016, co-located with ASP-LOS 2016

Relevant Coursework

- **Computer Architecture** (18-740, Fall 2015)
- **Energy Aware Computing** (18-743, Fall 2015)
- **Machine Learning** (10-701, Spring 2016)
- **Optimizing Compilers for Modern Architectures** (10-701, Spring 2016)
- **Advanced and Distributed Operating Systems** (15-712, Fall 2016)
- **Networks in the Real World** (18-755, Fall 2016)
- **Parallel Computer Architecture** (18-742, Spring 2017)

Honors

- **Deans Fellowship, Carnegie Mellon University** 2015
- **Merit Scholarship, BITS Pilani** 2013 & 2014

Service

- **Shadow Program Committee:** ASPLOS 2018

Skills

- **Languages:** C++, C, Python, MATLAB
- **Tools/Simulators:** Pin, Sniper, Gem5, perf, Intel VTune, Intel PCM, PAPI