CBCS SCHEME

USN

BCS302

Third Semester B.E./B.Tech. Degree Examination, June/July 2024
Digital Design and Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

			M	L	C
		Module – 1			
Q.1	**a.**	Reduce the following Boolean expressions to the minimum number of literals. i) $x(x' + y)$ ii) $x + x'y$ iii) $(x + y)(x + y')$ iv) $xy + x'z + yz$ v) $(x + y)(x' + z)(y + z)$	**10**	**L3**	**CO1**
	b.	Determine the minimum SOP form using Karnaugh Map $F = A'B'C' + B'CD' + A'BCD' + AB'C'$.	**10**	**L3**	**CO1**
		OR			
Q.2	**a.**	Simplify the Boolean function $F(w, x, y, z) = \Sigma(1, 3, 7, 11, 15)$ which has the don't care conditions $d(w, x, y, z) = \Sigma(0, 2, 5)$	**10**	**L3**	**CO1**
	b.	Simplify and implement the following Boolean function using NAND gates $F(x, y, z) = (1, 2, 3, 4, 5, 7)$.	**10**	**L3**	**CO1**
		Module – 2			
Q.3	**a.**	Implement the design of combinational circuit BCD and excess 3 code converter.	**10**	**L2**	**CO2**
	b	Implement full adder circuit using 3:8 decoders.	**10**	**L2**	**CO2**
		OR			
Q.4	**a.**	With Truth table and K-map simplification, implement the full adder with basic gates and using two half adders an OR gate.	**10**	**L2**	**CO2**
	b.	Realize the Boolean function using 8:1 multiplexer $F(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$.	**10**	**L2**	**CO2**
		Module – 3			
Q.5	**a.**	Explain Bus structure with diagram, explain how different peripherals connected to the bus.	**10**	**L2**	**CO3**
	b.	Explain in detail about the word alignment of a machine (microprocessor based systems) what is the consecutive addresses of aligned words for 16, 32 and 64 bit word length of the machine? Give consecutive address for each of the following specified above.	**10**	**L2**	**CO3**
		OR			
Q.6	**a.**	Write a note on : i) Register Transfer Notation (RTN) ii) Assembly Language Notation.	**10**	**L2**	**CO3**

	b.	Illustrate an indexed addressing mode with a assembly language program to find the sum of the Test 1, Test 2 and Test 3 scores of the N number of students.	10	L2	CO3
		Module – 4			
Q.7	a.	Explain Hardware interrupt, enabling/disabling of interrupts and sequence of events in handling interrupt request from a single device.	10	L2	CO4
	b.	Explain memory mapped I/O and I/O interface for an input device with a diagram.	10	L2	CO4
		OR			
Q.8	a.	Describe DMA with its register and controllers.	10	L2	CO4
	b.	Explain the effect of size, cost and speed in memory Hierarchy.	10	L2	CO4
		Module – 5			
Q.9	a.	Explain the process of Fetching word from memory in processor.	10	L2	CO5
	b.	With a diagram, explain the single bus organization of the data path inside a processor.	10	L2	CO5
		OR			
Q.10	a.	Describe how an ALU perform on arithmetic and logic operation along with input gating diagrams.	10	L2	CO5
	b.	Explain the complete set of operations involved in executing the instruction Add (R_3) R^1 along with control sequence.	10	L2	CO5

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