

14/10/2020

CO Assignment -3S. FIROZA
19131A05M3
CSE-4

- 1) Represent the following decimal numbers in both binary sign/magnitude and two's complement using 16 bits: +512, -29.

Sol: +512, since it is positive, MSB bit = 0.

Signed magnitude representation :- 0000 0010 0000 0000

Since the given number is positive, ^{it is same in} the signed MS and 2's complement representation is also same.

-29, since it is negative, MSB bit = 1.

Signed magnitude representation :- 1000 0000 0001 1101.

Signed 2's complement :- 2's complement of +29

(0000 0000 0001 1101)

$$\begin{array}{r} \Rightarrow 1111 1111 1110 0010 \\ + 1 \\ \hline 1111 1111 1110 0011 \end{array}$$

\therefore Signed 2's complement representation of (-29).

$\rightarrow 1111 1111 1110 0011.$

- (2) Represent the following two's complement values in decimal: 1101011, 0101101.

Ans:-

1101011

Here MSB bit = 1, so it is a negative number. So find 2's complement of 1101011 \Rightarrow 0010100

$$\begin{array}{r} 0010100 \\ + 1 \\ \hline 0010101 \end{array}$$

magnitude :- $0010101 = 16 + 4 + 1 = 21.$

Since, it is a negative no. ; magnitude = -21.

0101101, Here MSB = 0, so, it is a positive number. So, compute the magnitude as an unsigned binary number.

$0101101 = 32 + 8 + 4 + 1 = 45$; \therefore magnitude = 45.

13) Calculate $(72530 - 13250)$ using tens complement arithmetic.

Ans:-

$$72530 - 13250.$$

$$\text{minuend} = 72530, \text{ subtrahend} = 13250.$$

(i) 10's complement of subtrahend (13250):-

$$\begin{array}{r} 99999 \\ - 13250 \\ \hline 86749 \\ + 1 \\ \hline 86750 \end{array}$$

(ii) Add this to minuend (72530)

$$\begin{array}{r} 72530 \\ + 86750 \\ \hline 159280 \end{array}$$

omit the carry

$$\therefore \text{Result} = 59280.$$

$$(iii) \therefore 72530 - 13250 = 59280.$$

14). Assume numbers are represented in 8-bit two's complement representation. Show the calculation of following:

(a) $6+13$ (b) $-6+13$ (c) $6-13$ (d) $-6-13$.

Ans:-

Add the two numbers, including their sign bits and discard any carry out of the signed position.

Note that -ve no.s must initially be in 2's complement & that if the sum obtained after the addition is -ve, it is in 2's complement form.

(a) $6+13$

$$\begin{array}{r} +6 : 0000\ 0110 \\ +13 : 0000\ 1101 \\ \hline +19 \Leftarrow 0001\ 0011 \end{array}$$

MSB is 0, So +ve no.

$$\therefore 6+13 = 19$$

(b) $-6+13$

$$\begin{array}{r} -6 : 1111\ 1010 \text{ (in 2's comp.)} \\ +13 : 0000\ 1101 \\ \hline +7 \Leftarrow 1000\ 0011 \end{array}$$

discard carry $0000\ 0111 \Rightarrow \text{MSB} = 0$, So +ve no.

$$\therefore -6+13 = 7$$

(c) $6-13$

$$\begin{array}{r} +6 : 0000\ 0110 \\ -13 : 1111\ 0011 \text{ (in 2's comp.)} \\ \hline -7 \Leftarrow 1111\ 1001 \end{array}$$

MSB is 1, So -ve no., So find 2's comp.

$$\begin{array}{r} 2's \text{ comp. of } 1111\ 1001 \\ 0000\ 0110 \\ +1 \\ \hline 0000\ 0111 \Rightarrow -7 \end{array}$$

Since, -ve $\Rightarrow -7$

$$\therefore 6-13 = -7$$

d) $-6-13$.

$-6: 1111 1010$ (in 2's comp)

$-13: 1111 0011$ (in 2's comp)

$\begin{array}{r} 111101101 \\ \downarrow \\ 11101101 \end{array}$

discard carry \rightarrow msb = 1, so -ve no.

So find 2's comp. of 11101101.

$\begin{array}{r} 00010010 \\ +1 \\ \hline 00010011 \Rightarrow 19 \end{array}$

Since -ve, -19

$\therefore -6-13 = -19$

In each of 4 cases, addition is performed including sign bits, any carry out of sign bit is discarded and -ve results are automatically in 2's complement.

15) Find the following differences using two's complement arithmetic.

Ans: (a) $111000 - 110011$

2's complement of 110011 :- $\begin{array}{r} 001100 \\ +1 \\ \hline 001101 \end{array}$

Add this to 111000 :- $\begin{array}{r} 111000 \\ 001101 \\ \hline 1000101 \end{array}$

Emit the carry.

$\therefore \text{Result} = 000101$

(b) $11001100 - 101110$

2's complement of 101110 :- $\begin{array}{r} 00110011 \\ +1 \\ \hline 00110100 \end{array}$

Add this to

2's complement of 11001100 :- $\begin{array}{r} 11010001 \\ +1 \\ \hline 11010010 \end{array}$

Add this to 11001100 :- $\begin{array}{r} 11001100 \\ 11010010 \\ \hline 10001110 \end{array}$

Emit carry.

$\therefore \text{Result} = 10011110$

(c) $1111 0000 1111 - 1100 1111 0011$

2's complement of 1100 1111 0011 :- $\begin{array}{r} 0011 0000 1100 \\ +1 \\ \hline 0011 0000 1101 \end{array}$

Add this to 1111 0000 1111 :- $\begin{array}{r} 1111 0000 1111 \\ 0011 0000 1101 \\ \hline 1001 0000 1100 \end{array}$

Emit carry

$\therefore \text{Result} = 0000 0000 1100$

$$b) 11000011 - 11101000$$

$$2's \text{ complement of } 11101000 \Rightarrow \begin{array}{r} 00010111 \\ + 1 \\ \hline 00011000 \end{array}$$

$$\text{Add this to } 11000011 \Rightarrow \begin{array}{r} 11000011 \\ 00011000 \\ \hline 11011011 \end{array}$$

No carry.

$$\therefore \text{Result} = 11011011$$

(6) Given $x = 0101$ and $y = 1010$ and in two's complement notation (i.e., $x = 5$ and $y = -6$), compute the product with Booth's algorithm.

Ans:- $x = 0101$, $y = 1010$.

$$Q = 5 = 0101, M = -6 = 1010 \text{ (2's comp. of } 0110)$$

(Multiplier) (Multiplicand)

$$A \leftarrow 0000, C \leftarrow 4, Q_{-1} \leftarrow 0.$$

M	A	Q	Q ₋₁	Operation	C
1010	0000	0101	0		
1010	0110	0101	0		
1010	0011	0010	1	$A \leftarrow A - M$	4
1010	1101	0010	1	Shift	3
1010	0110	1001	0	$A \leftarrow A + M$	3
1010	1100	1001	0	Shift	2
1010	0110	0100	1	$A \leftarrow A - M$	2
1010	0100	1001	1	Shift	1
1010	0010	0100	0	$A \leftarrow A - M$	2
1010	1100	0100	1	Shift	1
1010	1110	0010	0	$A \leftarrow A + M$	1
				Shift	0

$$\text{Result} = AQ = 11100010 = -ve$$

$$\text{Find 2's comp. } 00011101$$

$$\text{Result} = -30.$$

$$\begin{array}{r} 00011101 \\ \hline 00011110 \\ \hline \end{array}$$

$$30.$$

(*) Use the Booth algorithm to multiply 23 (multiplicand) by 29 (multiplier), where each number is represented using 6 bits.

Ans:- Given, Multiplicand (M) = 23 = 01011 and multiplier (Q) = 29 = 011101.

$A \leftarrow 000000$, $C \leftarrow 6$ (count) , $Q_{-1} \leftarrow 0$.

M	A	Q	Q_{-1}	Operation	C
01011	000000	011101	0		6
01011	101001	011101	0	$A \leftarrow A - M$	6
01011	110100	101110	1	shift	5
01011	001011	101110	1	$A \leftarrow A + M$	5
01011	000101	110111	0	shift	4
01011	101110	110111	0	$A \leftarrow A - M$	4
01011	110111	011011	1	shift	3
01011	111011	101101	1	shift	2
01011	111101	110110	1	shift	1
01011	000100	110110	1	$A \leftarrow A + M$	1
01011	000100 0010010	011011	0	shift	0

Result = $AQ =$ ~~000010011011~~
 $= 001010011011 = 667$.

(10) Explain Division restoring algorithm with an example.

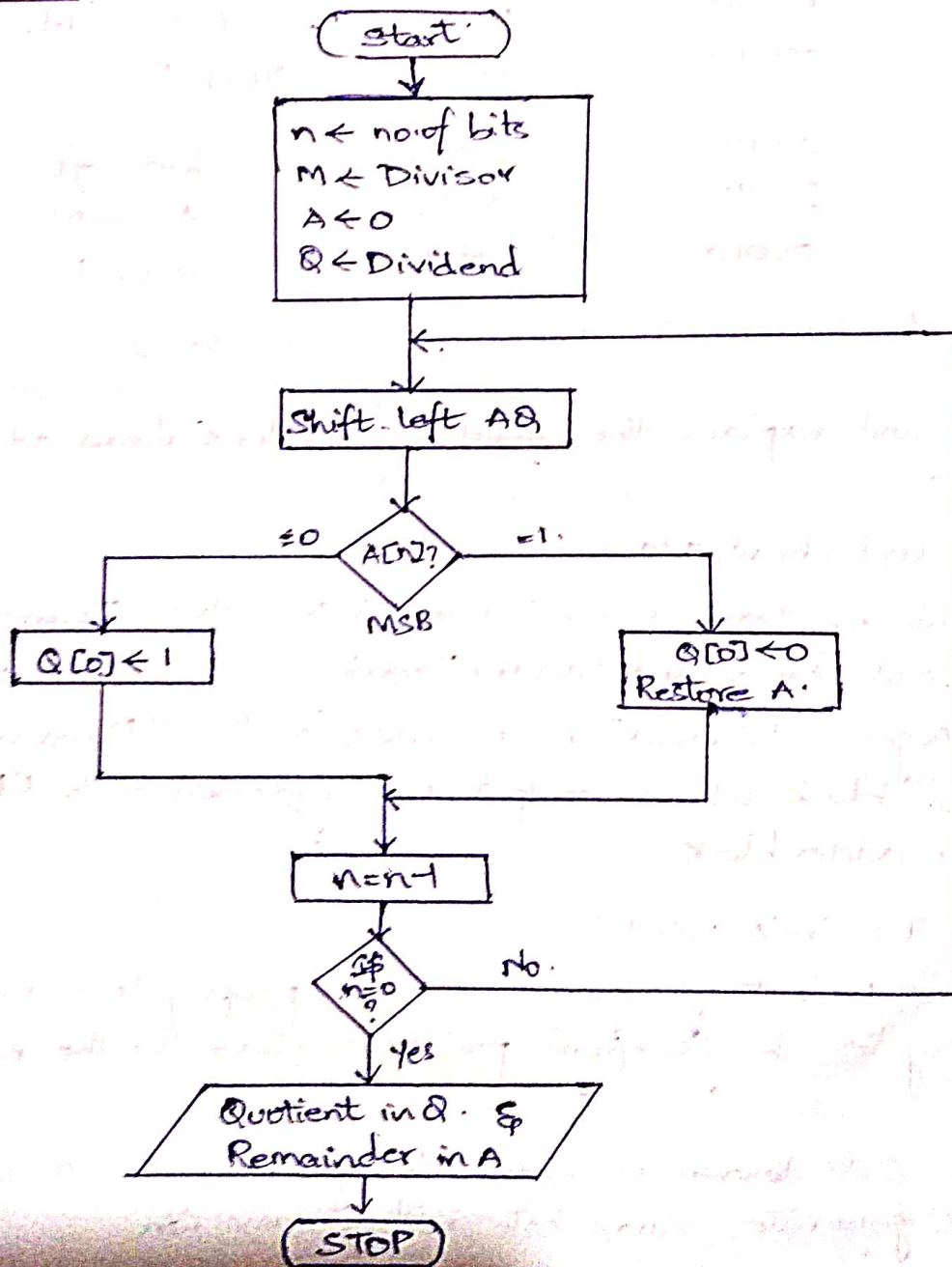
Ans:- Division Restoring Algorithm:-

A division restoring algorithm provides a quotient and a remainder when we divide two numbers.

Restoring term is due to the fact that value of register A is restored after each iteration.

Here, register Q contain quotient and register A contain remainder. Here, n-bit dividend is loaded in Q and divisor is loaded in M. Value of Register is initially kept 0 and this is the register whose value is restored during iteration due to which it is named Restoring.

Flowchart:-



Ex:- $11/3$, $Q \leftarrow 1011$, $M \leftarrow 00011$ $n = 4$.
 (Dividend) (Divisor) $A \leftarrow 00000$

n	M	A	Q	Operation
4	00011	00000	1011	Initialization
		00001	011?	Shift left AQ.
		11110	011?	$A \leftarrow A - M$
		00001	0110	$Q[0] = 0$, restore A.
3		00010	110?	Shift left AQ
		11111	110?	$A \leftarrow A - M$.
		00010	1100	$Q[0] = 0$, restore A.
2		00101	100?	Shift left AQ
		00010	100?	$A \leftarrow A - M$.
		00010	1001	$Q[0] = 1$.
1		00101	001?	Shift left
		00010	001?	$A \leftarrow A - M$
		00010	0011	$Q[0] = 1$.

Quotient = $Q = 0011 = 3$, Remainder = $A = 00010 = 2$.

(11) Draw and explain the 4-bit carry look ahead adder circuit.

Ans:- Carry Look Ahead adder:-

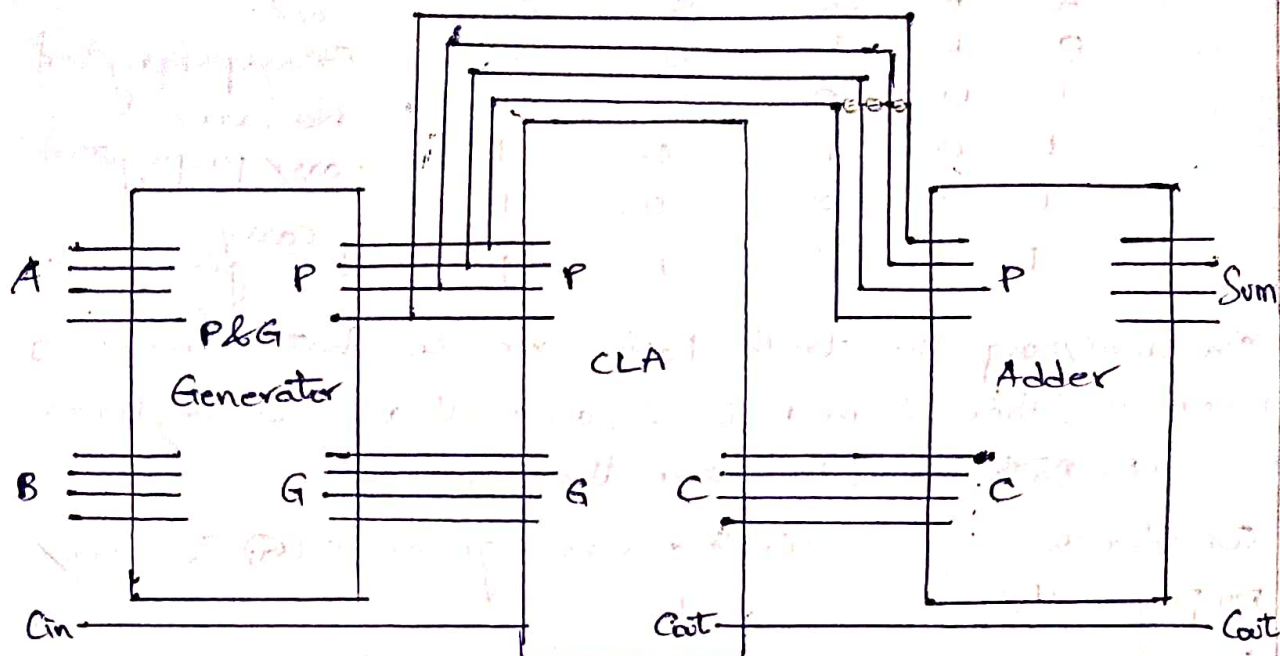
It contains three blocks:- "P and G generator", "Carry look ahead" block and "adder" block.

Input "Augend", "Addend" is provided to the "P and G generator" block whose output is connected with CLA and the adder block.

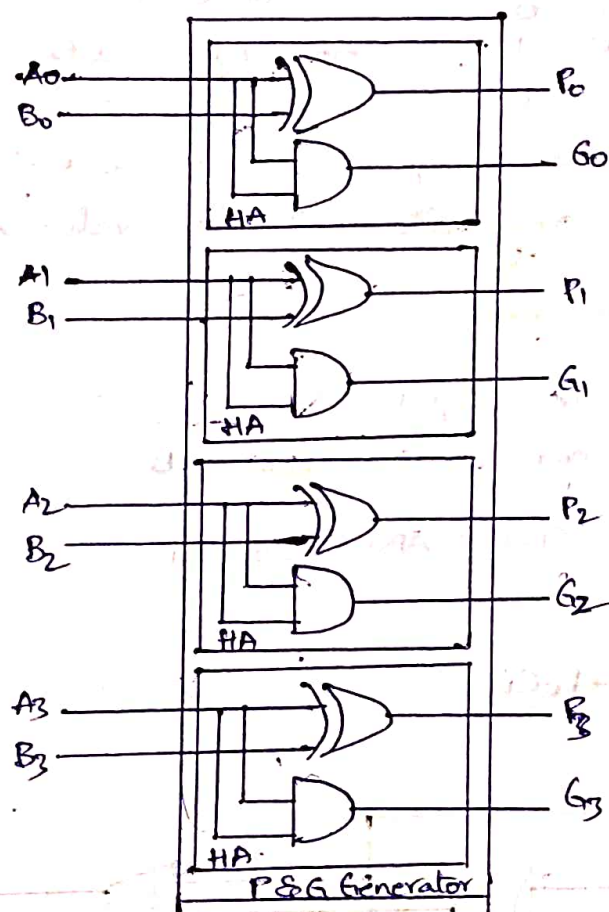
$$\text{Carry} = AB + C_{in}(A \text{ XOR } B)$$

$P = (A \text{ XOR } B)$: P is known as carry propagate, because it propagates the C_{in} from previous stage to the next stage.

$G = AB$: G is known as Carry Generate, because it can directly generate carry bit without any C_{in}



Block diagram:-



Let us consider a full adder. We have the input signals A, B and C_{in} . If we consider the addition of these three variables in every possible case, we get a truth table.

A	B	C_{in}	Sum	Carry	Condition
0	0	0	0	0	} No carry generated
0	0	1	1	0	
0	1	0	1	0	

A	B	C _{in}	S	C	Cond.
0	1	1	0	1	Carry propagated
1	0	0	1	0	No carry
1	0	1	0	1	Carry propagated
1	1	0	0	1	} carry generated.
1	1	1	1	1	

On analyzing the truth table, we see that carry is 1 when (i) either A or B is 1, as well as C_{in} is 1 (or) (ii) Both A & B have the value 1.

Consider two new variables, Carry generate (G) & Carry propagate (P).

Case (i):- Output carry is propagated, when we give an input carry. So

A	B
1	0
0	1

$$P_i = A_i \oplus B_i$$

$$A\bar{B} + \bar{A}B = A \oplus B$$

$$\therefore P_i = A_i \oplus B_i$$

Case (ii):- Output carry is generated when both inputs A and B are high, regardless of the value of C_{in}.

A	B
1	1

$$\text{So, } G_i = A_i B_i$$

For a full adder, $\text{sum} = A \oplus B \oplus C_i$

$$\text{Carry} = C_{in}(A \oplus B) + AB$$

(or)

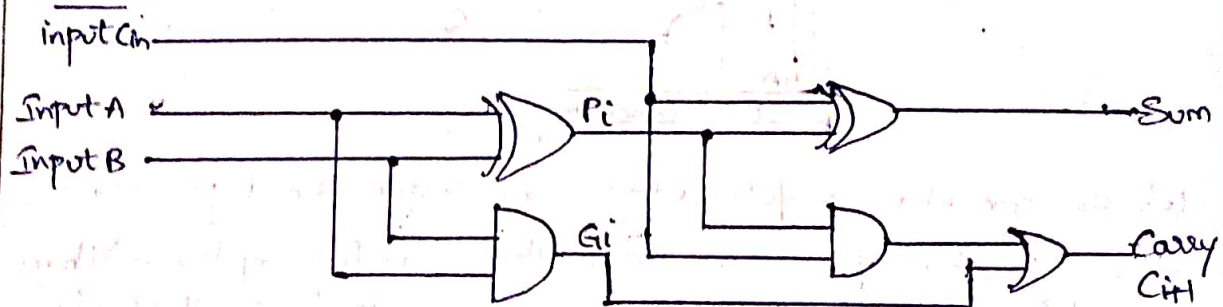
$$C_{i+1} = AB + BC_i + AC_i$$

Thus,

$$\text{Sum} = P_i \oplus C_i$$

$$\text{Carry} = G_i + P_i C_i$$

Circuit:-



We can calculate the output carry G_1, G_2, G_3 and G_4 using the above derived equations as:

$$G_1 = C_{in} \cdot P_0 + G_0.$$

$$G_2 = G_1 P_1 + G_1 = ((C_{in} P_0) + G_0) P_1 + G_1 = C_{in} P_0 P_1 + G_0 P_1 + G_1$$

$$G_3 = G_2 P_2 + G_2 = (C_{in} P_0 P_1 + G_0 P_1 + G_1) P_2 + G_2$$

$$= ((C_{in} P_0 P_1 + G_1) \cdot P_2) + G_2.$$

$$= G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_{in}.$$

$$G_4 = G_3 P_3 + G_3$$

$$= (C_{in} P_0 P_1 P_2 P_3 + P_3 P_2 P_1 G_0 + P_3 P_2 G_1 + G_2 P_3 + G_3).$$