11/03/21

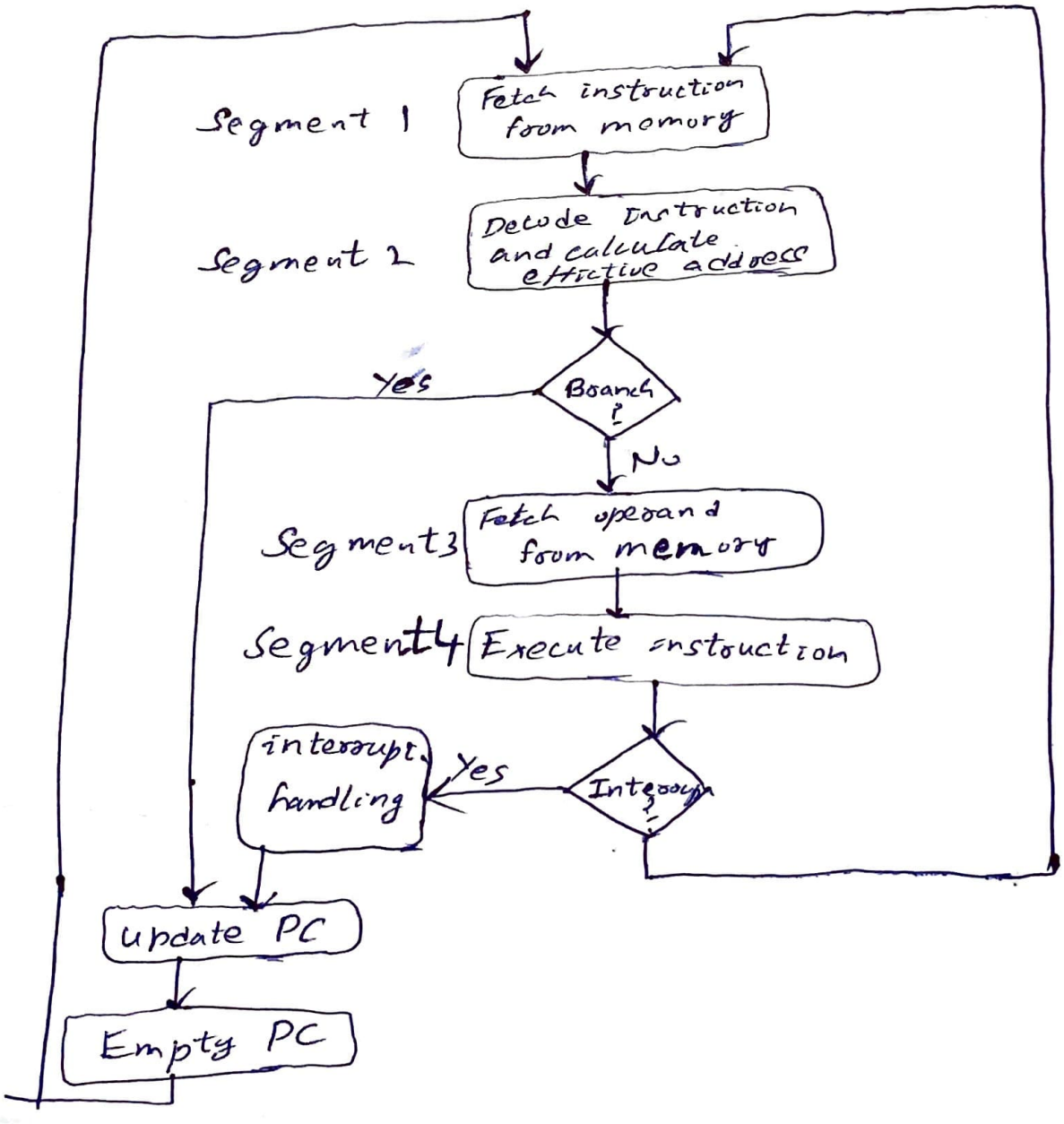
CSE-4

CO Assignment-4

A1). Aa). 4-segment instruction pipeline:

→ A four-segment instruction pipeline is the organisation of an instruction pipline will be more efficient if the instruction cycle is divided into segments of equal duration. One of the most common examples of this is a instruction pipeline.

→ It combines two or more different segments and makes it as a single one. For instance, the decod of the instruction can be combined with the calculation of the effective address into one segm



b) Vector Processing

→ There is a class of computational problems that are beyond the capabilities of the conventional computer.

→ These are characterized by the fact that they require vast number of computation and it take a conventional computer days or even weeks to complete.

→ Computers with vector processing are able to handle such instructions and they have applicat in following fields :-

i) Long range weather forecasting
ii) Petroleum exploration
iii) Image processing
iv) AI and expert system etc.

A vector of length 'n' is represented as row vector by :-

$$V = [V_1 \; V_2 \; V_3 \; V_4 \; \cdots \; V_n]$$

- The element 'V_i' of vector 'V' is written as V(I and the index I refers to a memory addre of register where the number is stored :

A 2). Asynchronous data Transfer

- In a computer system, CPU and an I/O interface are designed independently each other.
- When internal timing in each unit is independent from the other and when registers in interface and registers of CPU uses its own private clock.
- In that case the two units are said to be asynchronous to each other - CPU and I/O device must coordinate for data transfers.

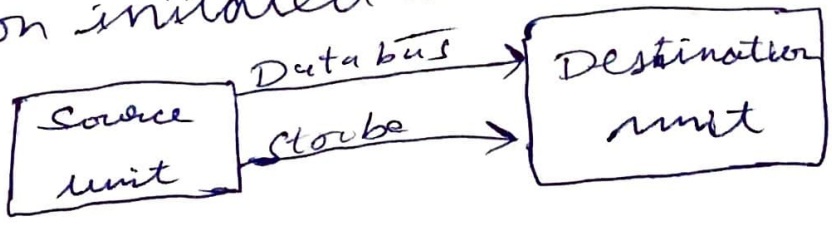
Methods used in Asynchronous data transfer

i). Strobe control:- This is one way to transfer, i.e by means of strobe pulse supplied by one of the units to indicate to the other unit when the transfer has to occur.

ii). Handshaking:- This method is used to accompa each data item being transferred with a contr signal that indicates the presence of data in the bus. The unit receiving the data item responds with another control signal to acknowledge receipt of the data

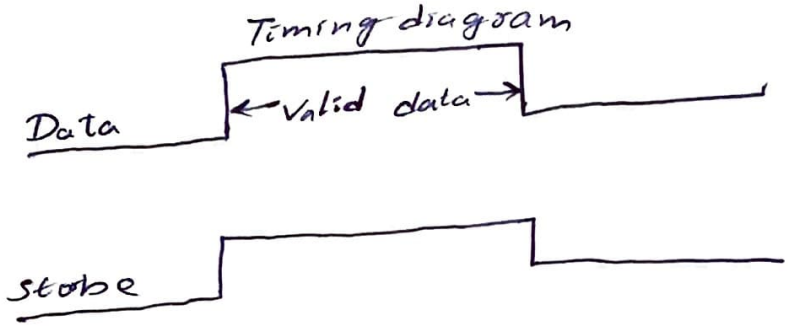
STROBE ~~CONTR~~ CONTROL

- It is a method of data transfer uses a signal control signal for each transfer. The strob may be activated by either the source unit o the destination unit.
  - Source initiated strobe
  - destination initated strobe.



Source initiated strobe

- The data bus carries the binary information from source unit to the destination unit as shown below.
- The strobe is a single line that informs the destination unit when a valid data word is available in the bus.



- The source unit 1st places the data on the bus.
- After a brief delay to ensure that data settle to a steady value, the source activities the strobe pluse.
- The information of a data bus and the strobe signal remain in the active state for a sufficient time period to allow the destination unit to receive the data.
- The source removes the data from the bus for a brief period of time after it disables its strobe pulse.

Handshaking

- In case of source initiated data transfer under strobe control method, the source unit has no way of knowing whether destination unit has received the data / not.
- Similary destination initiated transfer has no method of knowing whether the source unit

has placed the data on the data bus.

Q3). "Pipelining improves the speed of processing" Justify.

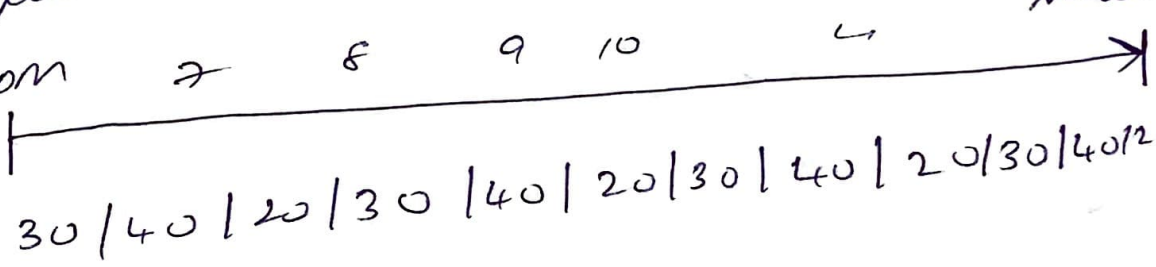
A3). Pipelining :- It is a technique of decomposing a sequential process into suboperations, with each subprocess being executed in a partial dedicated segment that operates concurrently with all other segments.

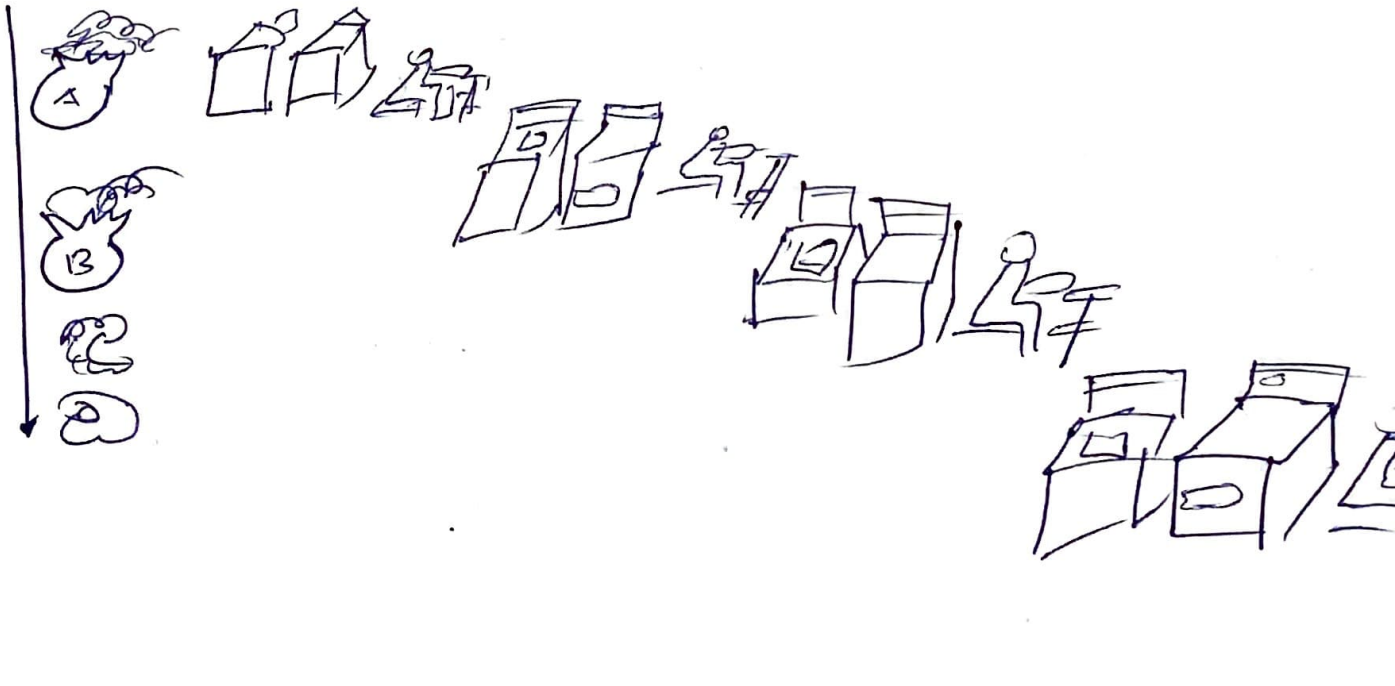
Example:- Traditional pipeline concept

Laundry example:-

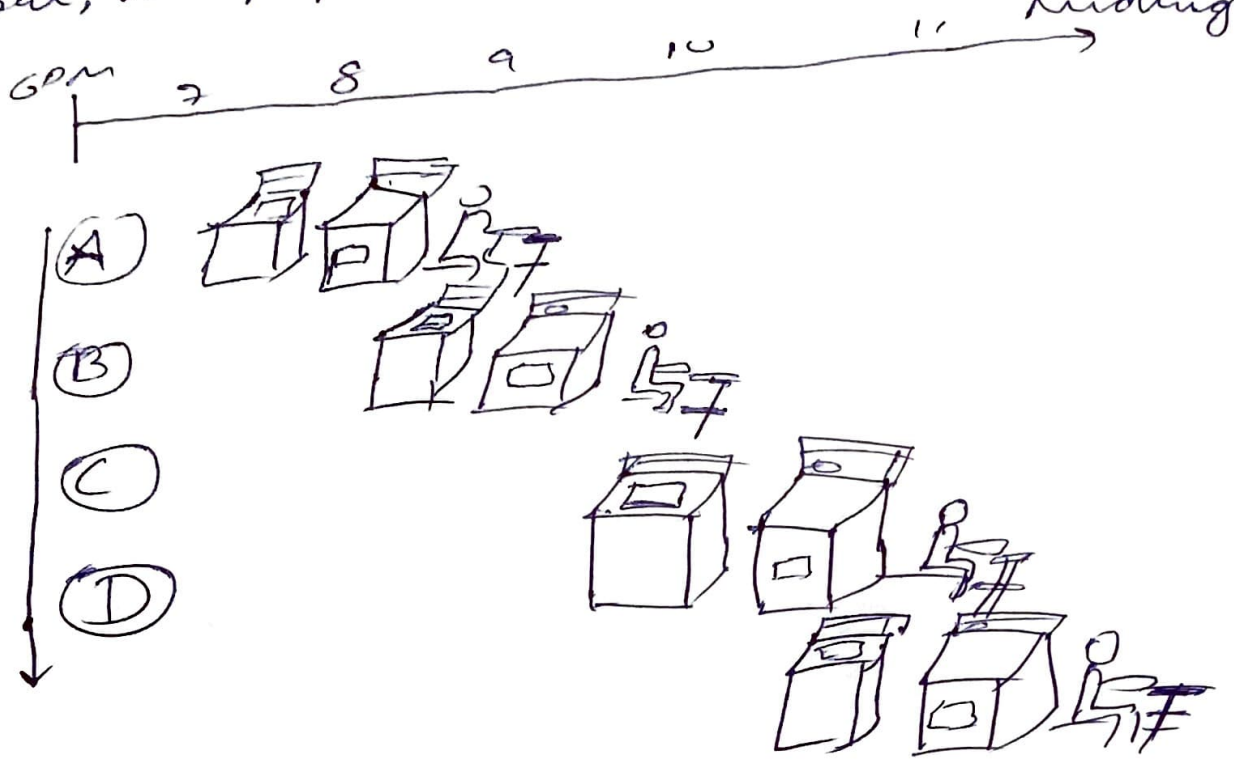
A, B, C, D each have one load of clothes to wash, dry, and fold

→ Washer takes 30 minutes
→ Folder takes 20 minutes
→ sequential laundry takes 6 hours for 4 loads





But, in pipelining concept:-

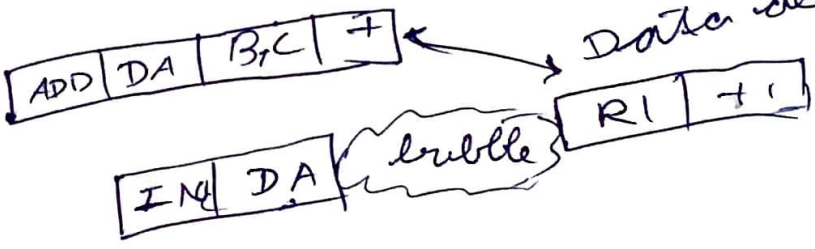


⇒ It takes 3.5 hours for 4 loads.

Hazards in pipelined:-

1). Structural hazards (Resource Conflicts)
Hardware resources required by the instructions in simultaneous overlapped execution cannot be met.

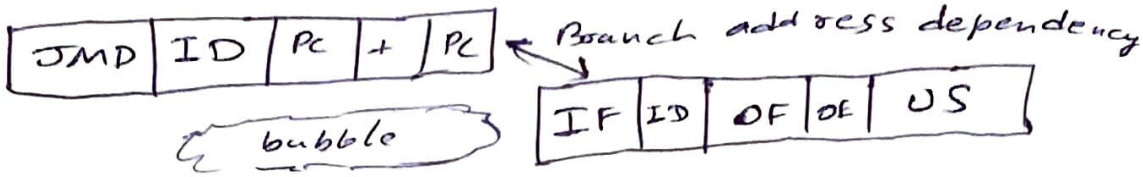
2) Data hazards (Data Dependency Conflicts)
An instruction scheduled to be executed in the pipeline requires the result of a previous instruction, which is not yet available



R1 ← B+C
R1 ← R1+1

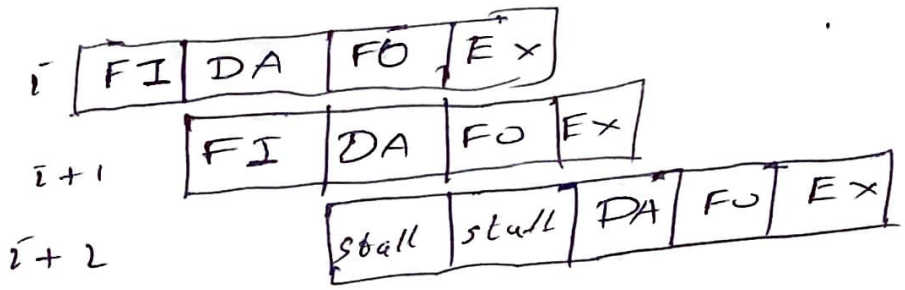
3). Control hazards

Branches and other instructions that change the "PC" make the fetch of the next instruction to be delayed.



4). Structural hazards :-

Occur when some resource has not been duplicated enough be initiated in the same clock.



) DATA Hazards :-

Occurs when the execution of an instruction depends on the results of a previous inst

ADD R1, R2, R3
SUB R4, R1, R5

Data hazards can be dealt with either hardware techniques (or) software technique

ardware Technique

Interlock
- hardware detects the data dependencies and delays the scheduling of the dependent instruction by stalling enough clock cycles.

A5) Page Fault - A page fault happens when a running program accesses a memory page that is mapped into the virtual address space, but not physical memory.

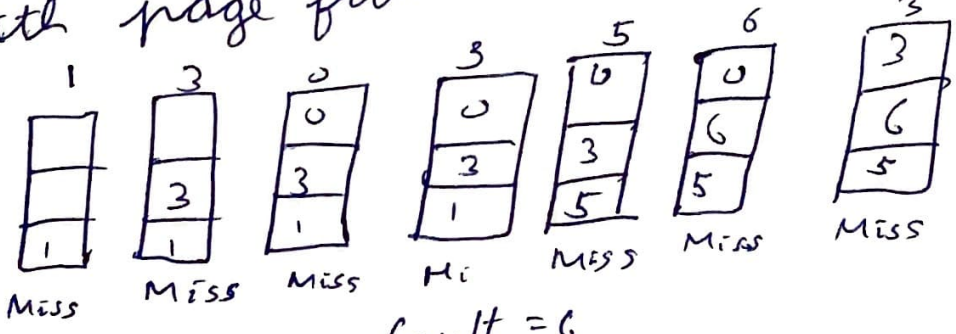
Since actual physical memory is much smaller than virtual memory, page faults happen. In case of page fault, OS might have to replace one of the existing pages with the newly needed page. Different page replacement algorithms suggest different ways to decide which page to replace. The target for all algorithms is to reduce the number of page faults.

Page fault Algorithms :-

1) First In First Out (FIFO)

The 'FIFO' and this is the simplest page replacement algorithm. In this algorithm, the OS keeps track of all pages in the memory in a queue the oldest page is in the front of the queue, the when a page needs to be replaced page in the front of the queue is selected for removal.

Ex :- Consider page reference string 1, 3, 0, 3, 5, 6 with page frames. Find number of page faults.



Total page fault = 6

Explanation:-

Initially all slots are empty, so when 1, 3, 0 came they are allcated to the empty slots ⟶ 3 page faults.

when '3' comes, it is already in memory so ⟶ 0 page faults

Then '5' comes, it is not availble in memory so it replaces the oldest page slot i.e 1 ⟶ 1 page fault.

'6' comes, it is also not available in memory so it replaces the oldest page ~~slot~~ slot i.e 3 ⟶ 1 page fault.

Finally when '3' comes it is not avaiable so it replaces '0' '1' page fault

2). Belady's anamoly :- It proves that is possible to have more page faults when increasing the number of page faults while using the FIFO page replacement algorithm, For example :- if we consider reference string 3, 2, 1, 0, 3, 2, 4, 3, 2, 1, 0, 4 and 3 slots, we get '9' total page faults, but if we increase slots to '4', we get '10' page faults.

3). Optimal page replacement :- In this algorithm pages are replaced which would not be used for the longest duration of time in the future.

4). Least recently used :- In this algorithm page will be replaced which is least recently used.