Unit - 3

Syllabus :-

Combinational Logic Design :-

Adders, Subtractors, Multiplexers, De-Multiplexers, MUX - Realization of Switching functions, Encoder, Decoder, Parity bit Generator, Code Converters, Basic PLD's :- ROM, PROM, PLA, PAL Realizations.

Logic Circuits

- **Combinational Circuit** (o/p is only depends on present i/p)
- **Sequential Circuit.** (o/p depends on present i/p as well as previous o/p)

⇒ A logic circuits for digital systems may be divided into two types - Combinational and Sequential.

=) A Combinational circuit ~~of~~ Consists of logic gates whose outputs at any-time are determined by the present Combination of inputs without regards to previous outputs.

=) Sequential circuits employ memory elements in addition to logic gates.

=) In Sequential Circuit outputs are function of the inputs and state of the memory elements. The memory elements, inturn is a function of previous o/p's or i/p's.

Example of Combinational Circuit :-

Ex-1 :- Adder.

Say, 1 + 0 = 1

Present i/p o/p.

So, o/p only depends on present i/p's.

Example of Sequential Circuit :-

Ex-1 :- Counter

Say, Count of time ~~from~~ in a clock.

Time : 00:45 (Previous o/p)
+ 1 (Present i/p)

Time : 00:46 (Present o/p)

So, o/p not only depends on present i/p's but also on previous o/p's.

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Half Adder:- (Combinational Circuit)

⇒ A Combinational Circuit the addition of two bits is called Half-Adder Circuit.

⇒ Its an binary operation of inputs (single bit each).

⇒ From the explanation of half-adder, we find this circuit needs two single binary inputs and two binary outputs (one is sum & another is Carry).

Say 'x' & 'y' are two inputs and S = Sum, C = Carry are the two outputs.

So, the truth table is →

x	y	S	C
0	0	0	0
0 ($\bar{x}$)	1 (y)	1	0
1 (x)	0 ($\bar{y}$)	1	0
1	1	0	1

So, the simplified Boolean function for the two outputs are obtained as →

* SOP form (Sum of Product) $S = \bar{x}y + x\bar{y} = x \oplus y$

$C = xy$

[** Here the equations are simple so, K-map not used, otherwise we have to use K-map to get the

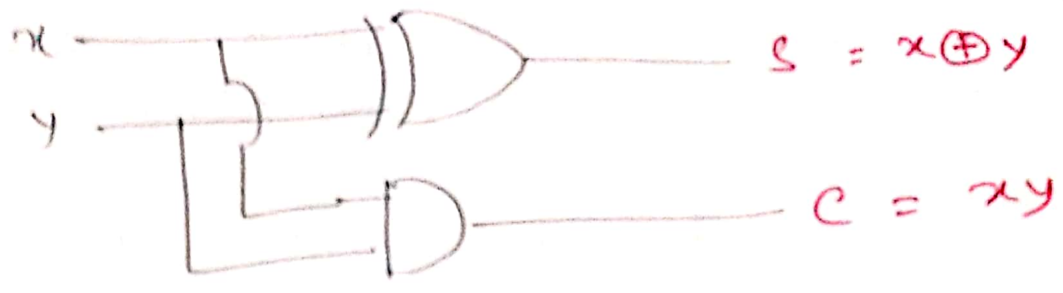
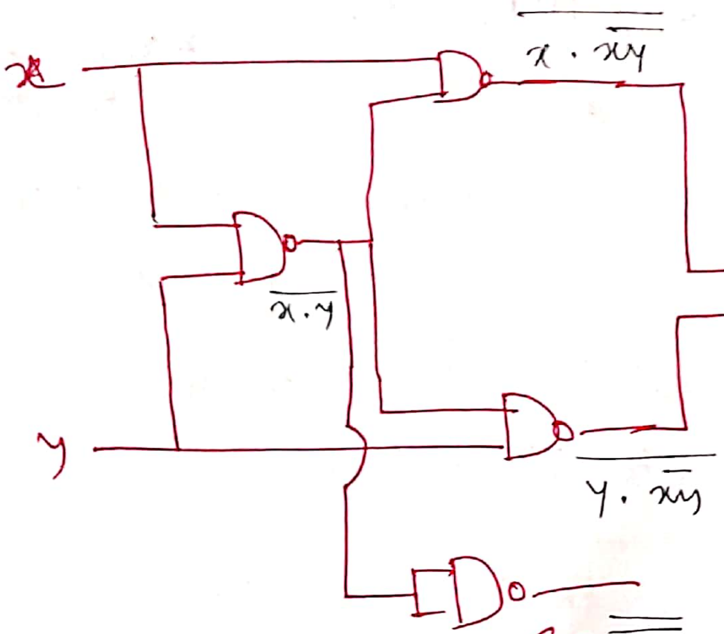


Fig - Implementation of Half-Adder Circuit

* Half Adder using NAND Gates :-



$C = \overline{\overline{x\cdot y}}$

$= xy$

* with Min^m number of NAND Gates.

$S = \overline{\overline{x\cdot\overline{xy}}\cdot\overline{y\cdot\overline{xy}}}$

$= \left(\overline{\overline{x\cdot\overline{xy}}}\right)+\left(\overline{\overline{y\cdot\overline{xy}}}\right)$

$= \left(x\cdot\overline{xy}\right)+\left(y\cdot\overline{xy}\right)$

$= x\cdot(\bar{x}+\bar{y}) + y\cdot(\bar{x}+\bar{y})$

$= (\bar{x}+\bar{y})(x+y)$

$= x\bar{y} + \bar{x}y + x\bar{x} + y\bar{y}$

$= \bar{x}y + x\bar{y} + 0 + 0$

$= x \oplus y$

$\cancel{S = \overline{x\bar{y}+\bar{x}y}}$

$= \cancel{x\bar{x}+x}$

* write in AND form of the equation.

Sol^n :- $S = x\bar{y} + \bar{x}y$

$= x\bar{y} + x\bar{x} + y\bar{y} + \bar{x}y$

$= x(\bar{x}+\bar{y}) + y(\bar{x}+\bar{y})$

$C = xy$

$= \overline{\overline{xy}}$

$\cancel{(x+y)(x}$ $= x\cdot\overline{xy} + y\cdot\overline{xy}$

$= \overline{\overline{x\cdot\overline{xy} + y\cdot\overline{xy}}}$

$= \overline{\overline{x\cdot\overline{xy}}\cdot\overline{y\cdot\overline{xy}}}$

[Back Process from Boolean Algebra & then draw the structure]

* Half Adder using NOR - Gate :-

* Expand in 'OR' form (+)

Sol :-

$$S = xy\bar{y} + \bar{x}y$$

$$= x\bar{y} + x\bar{x} + \bar{x}y + y\bar{y}$$

$$[\because x\bar{x} = 0 = y\bar{y}]$$

$$= x(\bar{x} + \bar{y}) + y(\bar{x} + \bar{y})$$

$$= (\bar{x} + \bar{y}).(x + y)$$

$$= \overline{\overline{(\bar{x} + \bar{y})} + \overline{(x + y)}}$$

$$C = xy = \overline{(\bar{x} + \bar{y})}$$