SWITCHING THEORY AND LOGIC DESIGN

UNIT-5

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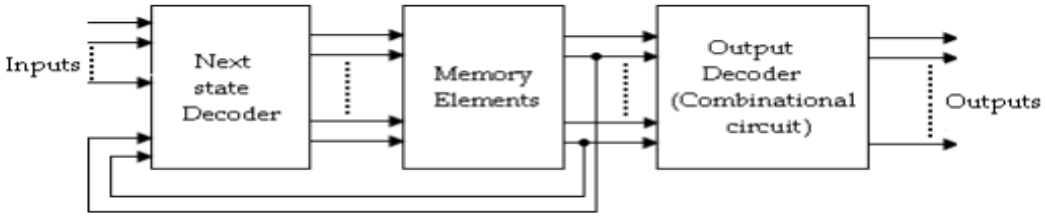
FINITE STATE MACHINES

The synchronous or clocked sequential networks are represented by two models.

- Moore model: The output depends only on the present state of the Flip-Flops.
- Mealy model: The output depends on both the present state of the Flip-Flops and on the inputs.

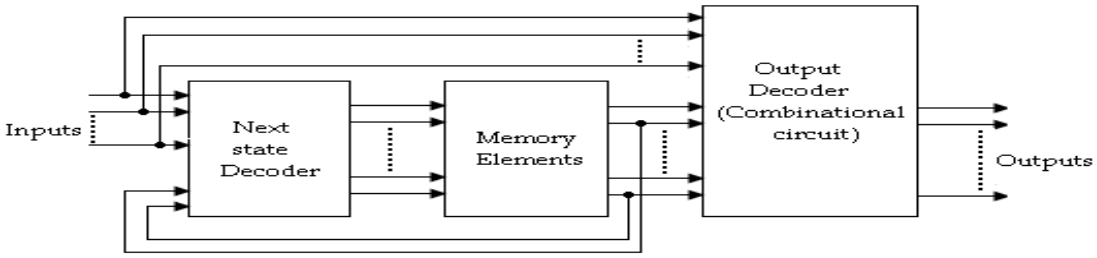
Moore model: In the Moore model, the outputs are a function of the present state of the Flip-Flops only. The output depends only on present state of Flip-Flops, it appears only after the clock pulse is applied, i.e., it varies in synchronism with the clock input.



Moore model

FINITE STATE MACHINES

Mealy model: In the Mealy model, the outputs are functions of both the present state of the Flip-Flops and inputs



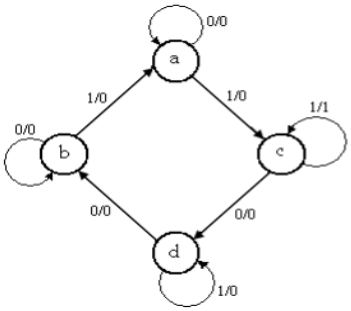
Mealy model

Difference between Moore and Mealy model

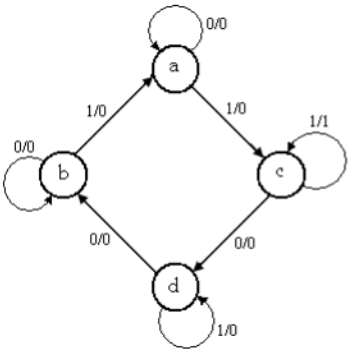
Sl.No	Moore model	Mealy model
1	Its output is a function of present state only.	Its output is a function of present state as well as present input.
2	Input changes does not affect the output.	Input changes may affect the output of the circuit.
3	It requires more number of states for implementing same function.	It requires less number of states for implementing same function.

STATE DIAGRAM

- It is a pictorial representation of a behavior of a sequential circuit.
- In the state diagram, a state is represented by a circle and the transition between states is indicated by directed lines connecting the circles. A directed line connecting a circle with circle with itself indicates that next state is same as present state. The binary number inside each circle identifies the state represented by the circle. The directed lines are labeled with two binary numbers separated by a symbol '/'. The input value that causes the state transition is labeled first and the output value during the present state is labeled after the symbol '/'.
- In case of Moore circuit, the directed lines are labeled with only one binary number representing the state of the input that causes the state transition. The output state is indicated within the circle, below the present state because output state depends only on present state and not on the input.



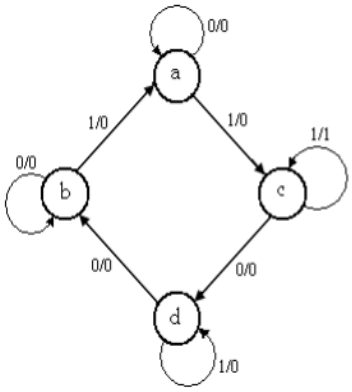
State diagram for Mealy circuit



State diagram for Mealy circuit

STATE TABLE

- It represents relationship between input, output and Flip-Flop states. It consists of three sections labeled present state, next state and output. o The present state designates the state of Flip-Flops before the occurrence of a clock pulse, and the output section gives the values of the output variables during the present state. o Both the next state and output sections have two columns representing two possible input conditions: X= 0 and X=1.

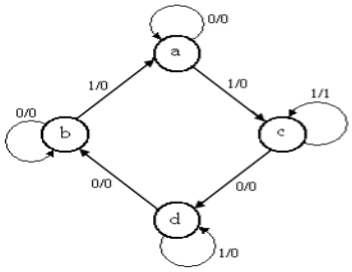


State diagram for Mealy circuit

Present state	Next state		Output	
	X= 0	X= 1	X= 0	X= 1
AB	AB	AB	Y	Y
a	a	c	0	0
b	b	a	0	0
c	d	c	0	1
d	b	d	0	0

STATE TABLE

- In case of Moore circuit, the output section has only one column since output does not depend on input. and X=1.



State diagram for Mealy circuit

Present state	Next state		Output
	X= 0	X= 1	Y
AB	AB	AB	
a	a	c	0
b	b	a	0
c	d	c	1
d	b	d	0

Successor: A's 1 successor is c and A's 0's successor is A(used in partition technique)
State Equation: It is an algebraic expression that specifies the condition for a Flip-Flop state transition. The Flip-Flops may be of any type and the logic diagram may or may not include combinational circuit gates.
State Reduction: If some states have same Next State and output then this state becomes a redundant state.This state can be removed. This process is known as State Reduction
State Assignment: In this process each state is assigned a binary value

PARTITION TECHNIQUE

- This also helps in reducing no of States
- Example:

PS	NS, Z	
	X = 0	X = 1
A	E, 0	D, 1
B	F, 0	D, 0
C	E, 0	B, 1
D	F, 0	B, 0
E	C, 0	F, 1
F	B, 0	C, 0

1. States having the same output under all input conditions can be grouped as

$$P_1 = (A, C, E)(B, D, F)$$

2. The 0- and 1-successors of (A, C, E), i.e. (E, E, C) and (D, B, F) are in the same block of P_1. 0-successors of (B, D, F), i.e. (F, F, B) are also in the same block of P_1. So, no partitioning is required, but 1-successors of (B, D, F), i.e. (D, B, C) are in different blocks of P_1. So, partition (B, D, F) into (B, D) and (F).

$$\therefore \quad P_2 = (A, C, E)(B, D)(F)$$

3. 0-successors of (A, C, E), i.e. (E, E, C) and the 0- and 1-successors of (B, D), i.e. (F, F) and (D, B) are in same blocks of P_2. So, no partitioning is required. The 1-successors of (A, C, E), i.e. (D, B, F) are in different blocks of P_2. So, partition (A, C, E) into (A, C) and (E).

$$\therefore \quad P_3 = (A, C)(E)(B, D)(F)$$

4. The 0- and 1-successors of (A, C), and (B, D) i.e. (E, E), (D, B) and (F, F), (D, B) are in the same blocks of P_3. So, no partitioning is required.

$$\therefore \quad P_4 = (A, C)(E)(B, D)(F)$$

Thus, equivalent states are

$$A = C \text{ and } B = D$$

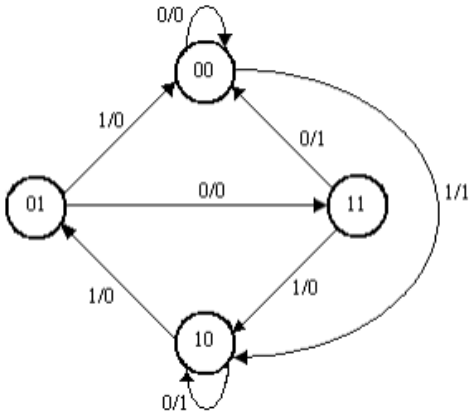
So, states C and D are redundant and can be removed. C and D can be replaced by A and B respectively in the rest of the table. The resultant minimized state table is as shown in Table

PARTITION TECHNIQUE

Reduced State Table:

PS	NS, Z	
	X = 0	X = 1
A	E, 0	B, 1
B	F, 0	B, 0
E	A, 0	F, 1
F	B, 0	A, 0

DESIGN A CIRCUIT FOR A GIVEN STATE DIAGRAM USING D FLIP-FLOP:



Present state		Next state		Output	
		X= 0	X= 1	X= 0	X= 1
A	B	AB	AB	Y	Y
0	0	00	10	0	1
0	1	11	00	0	0
1	0	10	01	1	0
1	1	00	10	1	0

State Table

DESIGN A CIRCUIT FOR A GIVEN STATE DIAGRAM USING D FLIP-FLOP:

Present state		Input	Next state		Flip-Flop Inputs		Output
A	B	X	A	B	D_A	D_B	Y
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	1
0	1	0	1	1	1	1	0
0	1	1	0	0	0	0	0
1	0	0	1	0	1	0	1
1	0	1	0	1	0	1	0
1	1	0	0	0	0	0	1
1	1	1	1	0	1	0	0

Circuit excitation table

K-map Simplification:

For Flip-flop A

A \ BX	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$D_A = A'B'X + A'BX' + ABX + AB'X'$

$= A \oplus (B \oplus x)$

For Flip-flop B

A \ BX	00	01	11	10
0	0	0	0	1
1	0	1	0	0

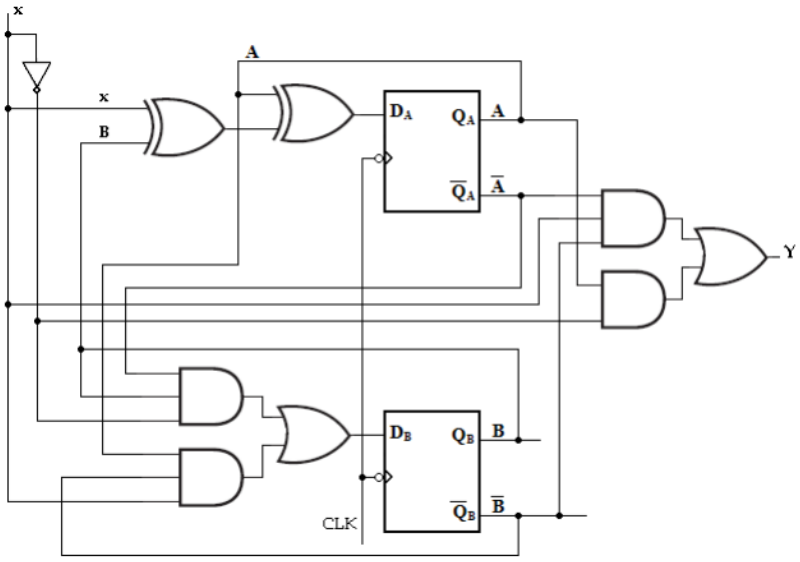
$D_B = A'BX' + AB'X$

For Output

A \ BX	00	01	11	10
0	0	1	0	0
1	1	0	0	1

$Y = A'B'X + AX'$

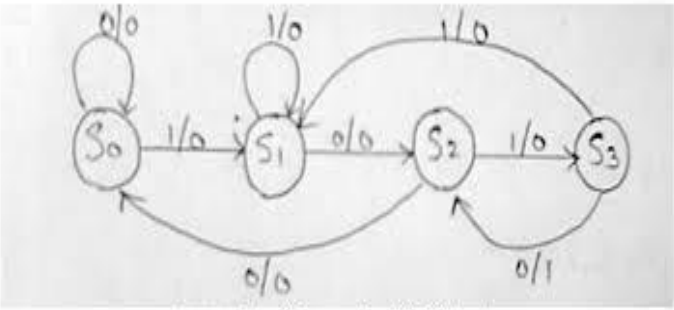
DESIGN A CIRCUIT FOR A GIVEN STATE DIAGRAM USING D FLIP-FLOP:



Logic diagram of given sequential circuit using D Flip-Flop

DESIGN A SEQUENCE DETECTOR TO DETECT SEQUENCE 1010 FOR MEALY TYPE

- First draw the state diagram to detect the Sequence 1010(consider overlapping).
- When the Sequence is completed the output will be 1.
- After drawing State diagram the design procedure is same as explained in slides 9 to 11.
- First State table, Excitation table, Boolean Expressions, Logic diagram



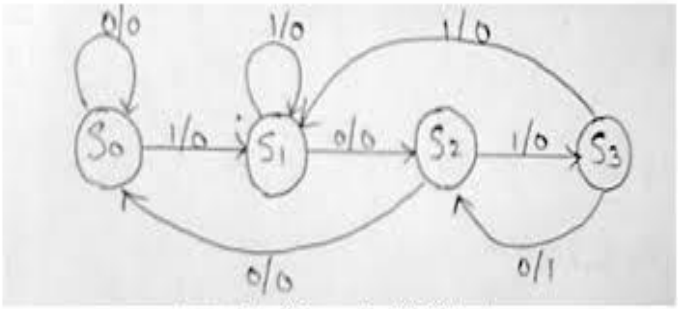
State diagram for 1010 detector

Here
S_0=00
S_1=01
S_2=10
S_3=11
After that repeat the same procedure mentioned in slides 9 to 11

DESIGN A SEQUENCE DETECTOR TO DETECT SEQUENCE 1010 FOR MEALY TYPE

- When S_0=0 we have to wait in the same state with output =0 and if S_0=1 we move to S_1 with output =0
- When S_1=0 we move to S_1 with output =0 and if S_0=1 have to wait in the same state with output =0
- When S_2=0 we move to S_0 as the sequence is wasted with output =0 if S_2=1 we move to S_3 with output =0
- When S_3=0 we move to S_2 as the sequence is completed as it is overlapping and output =1 as sequence is completed and if S_3=1 we move to S_1 as it is overlapping and output =0

(If you have doubts look into this video design procedure is present here https://www.youtube.com/watch?v=k8xxGSkJUhY for non overlapping and overlapping sequence)



State diagram for 1010 detector

After State Assignment, repeat the same procedure mentioned in slides 9 to 11

QUESTIONS:

- Design a Sequence Detector to detect the sequence 1011 for Mealy type using D-flip-flop.
- Design a Binary Serial Adder for Moore Type.
- Draw the state diagram of JK Flip-flop
- Reduce the following State Table using Partition Technique.

PS	NS, Z	
	X = 0	X = 1
A	C, 0	F, 0
B	D, 1	F, 0
C	E, 0	B, 0
D	B, 1	E, 0
E	D, 0	B, 0
F	D, 1	B, 0

THANK YOU