COMPUTER ORGANIZATION

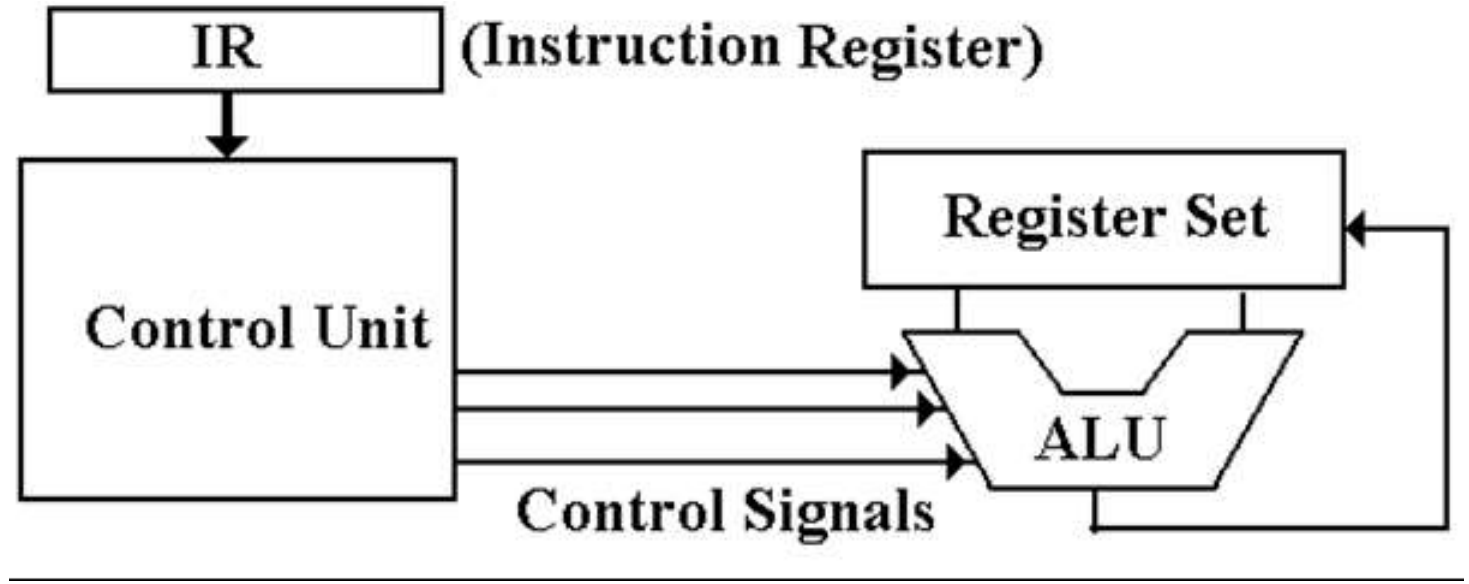
B.TECH III SEM

CSE-4

N SANTOSHI
ASSISTANT PROFESSOR
DEPARTMENT OF ECE

CONTROL UNIT

- CPU is partitioned into Arithmetic Logic Unit (ALU) and Control Unit (CU).
- The function of control unit is to generate relevant timing and control signals to all operations in the computer.
- It controls the flow of data between the processor and memory and peripherals



There are two methods to implement the control unit:

- **Hardwired:** The control signals are generated as an output of a set of basic logic gates, the input of which derives from the binary bits in the Instruction Register.
- **Microprogrammed:** The control signals are generated by a microprogram that is stored in Control Read Only Memory.
- The Hardwired and Microprogrammed control unit generates the **control signals to** fetch and execute instructions.

Hardwired Control Unit

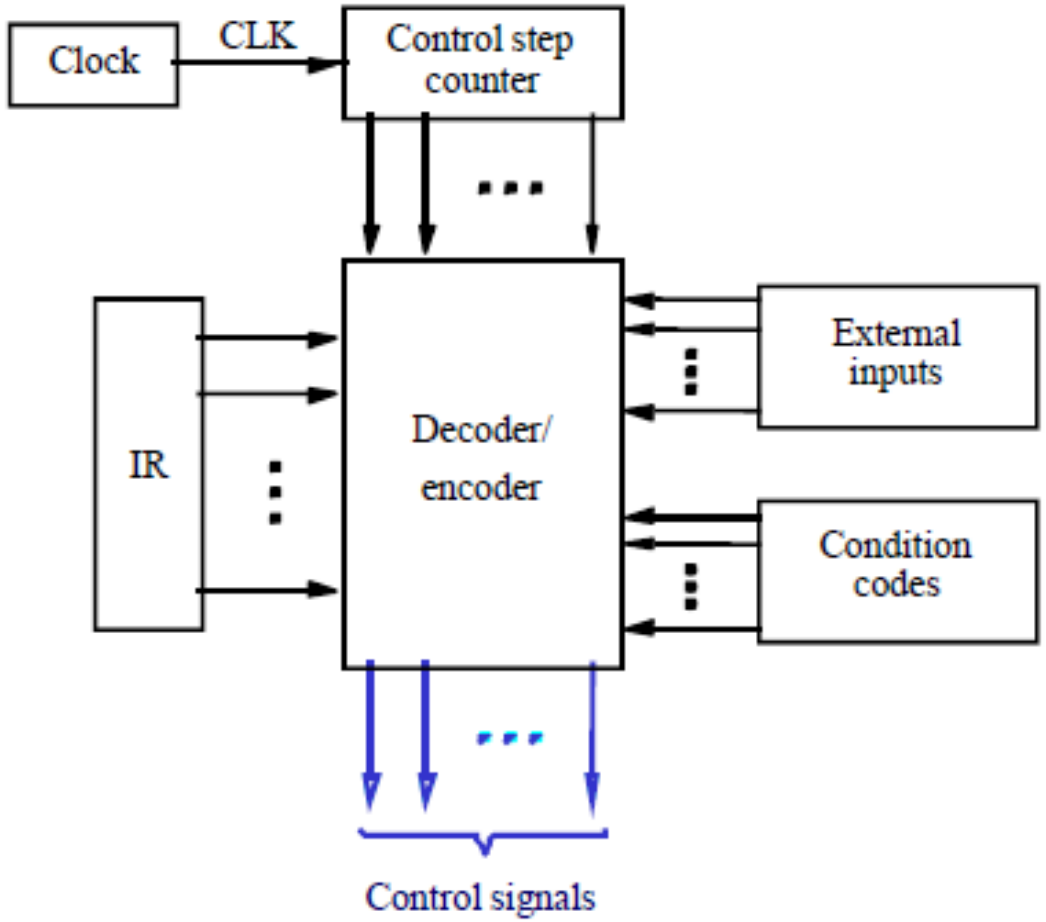
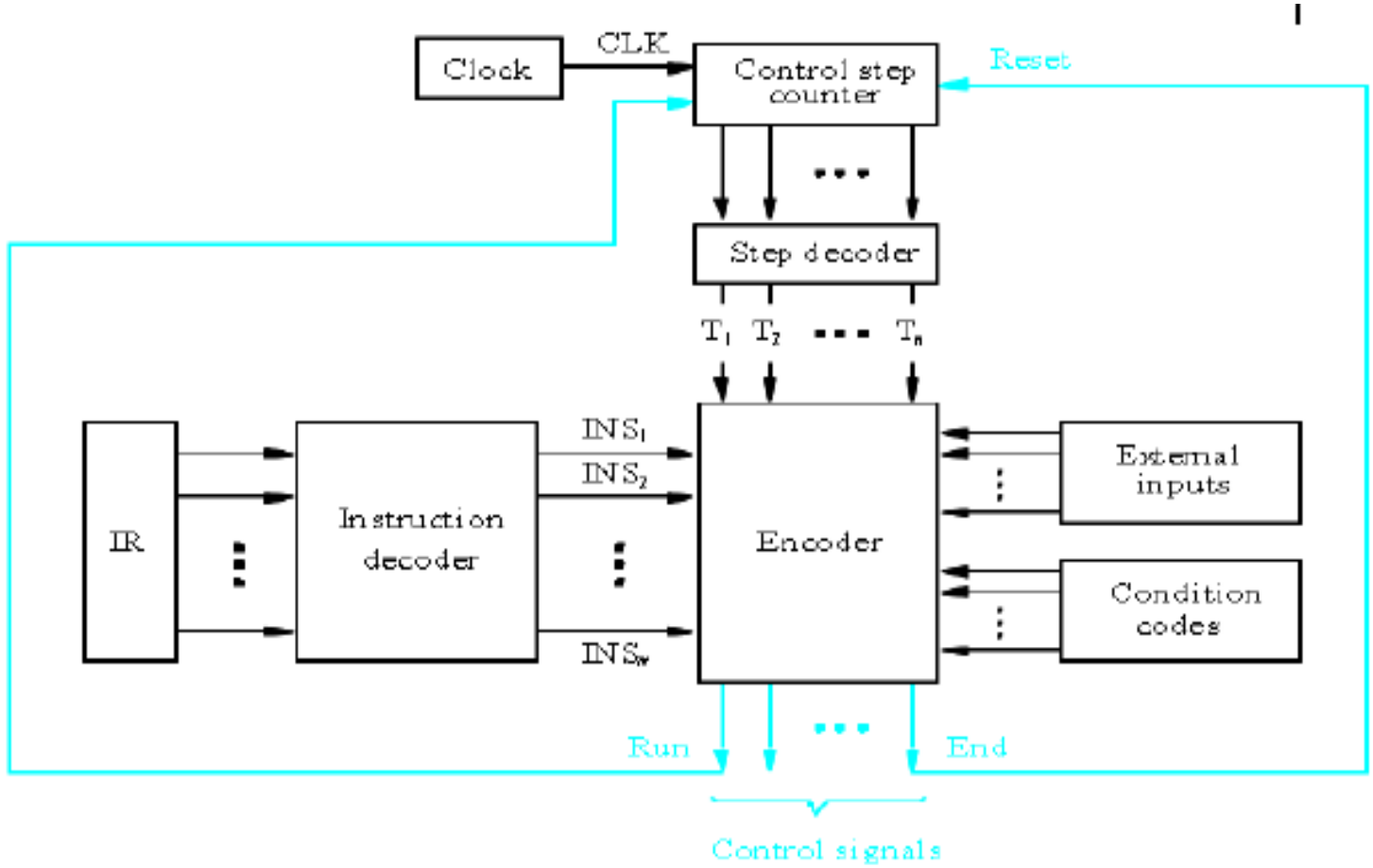


Figure 7.10 Control unit organization.

Hardwired Control Unit

- The decoder/encoder is a combinational circuit that generates a set of required control signals.
- A control step counter is used to keep track of the control steps.
- Each count of this counter corresponds to one control step.
- The required control signals are determined by the following information:
    1. contents of the control step counter
    2. contents of IR register
    3. contents of the condition code flags
    4. External input signals, like MFC and interrupt request.

Detailed Block Description



Detailed Block Description

- The step decoder generate a separate clock signal for each step, or time slot, in the control sequence.
- The instruction decoder decodes the instruction loaded in IR.
- The output of the instruction decoder consists of a separate line for each of the ‘m’ machine instruction.
- According to the code in the IR, only one line amongst all output lines of decoder is set to 1 and all other lines are set to 0.
- The input signals to encoder are combined to generate the individual control signals like add, read, etc.
- The End signal starts the a new instruction fetch cycle by resetting the control step counter to its starting value.
- When run=1, the counter to be incremented by one at the end of every clock cycle.
- When run=0, the counter stops counting and this is needed whenever the WMFC signal is activated.

Hardwired Control Unit

- Advantages of Hardwired Control Unit:

  1. Fast because control signals are generated by combinational circuits.

  2. The delay in generation of control signals depends upon the number of gates.

- Disadvantages of Hardwired Control Unit:

  1. More the control signals required by CPU, more complex will be the design of control unit.

  2. No Flexibility. Modification in control signal is very difficult i.e. it requires rearranging of wires in the hardware circuit.

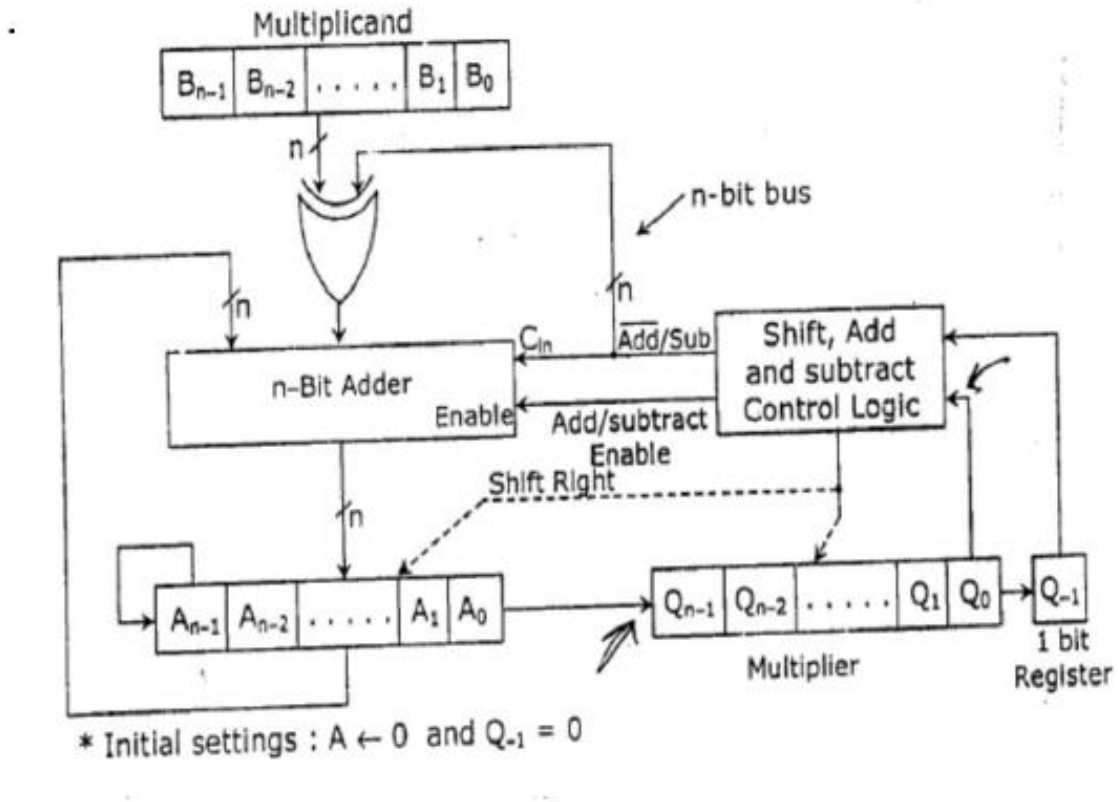
  3. Difficult to add new feature in existing design of control unit.

Hardwired Control Unit Design Methods

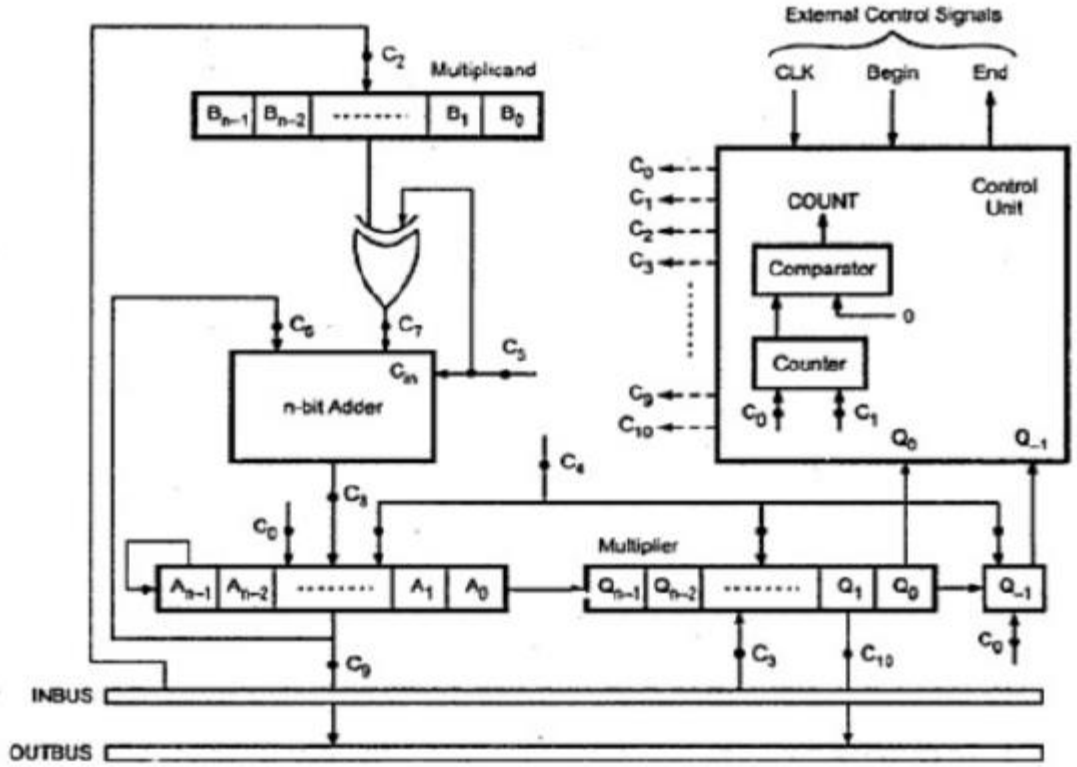
1. State-table Method
2. Delay-element Method: Uses clocked delay element (D-Flip Flop)
3. Sequence-counter Method: Uses counter for timing purposes
4. PLA Method: Uses programmable logic array

Hardwired Control Unit Design Methods (cont.)

- Let us consider 2's complement multiplier control circuit for illustration.



Hardwired Control Unit Design Methods (cont.)



Multiplier control circuit with control signals

Hardwired Control Unit Design Methods (cont.)

Control signal	Operation controlled
C_0	Clear A, Q_{-1} and count ← n
C_1	Decrement count
C_2	Transfer word on INBUS to B
C_3	Transfer word on INBUS to Q
C_4	Shift right register A, Q and Q_{-1}
C_5	2's complement multiplicand
C_6	Transfer A to left input of adder
C_7	Transfer B to right input of adder
C_8	Transfer adder output to A
C_9	Transfer A to OUTBUS
C_{10}	Transfer Q to OUTBUS

Control signals for 2's complement multiplier

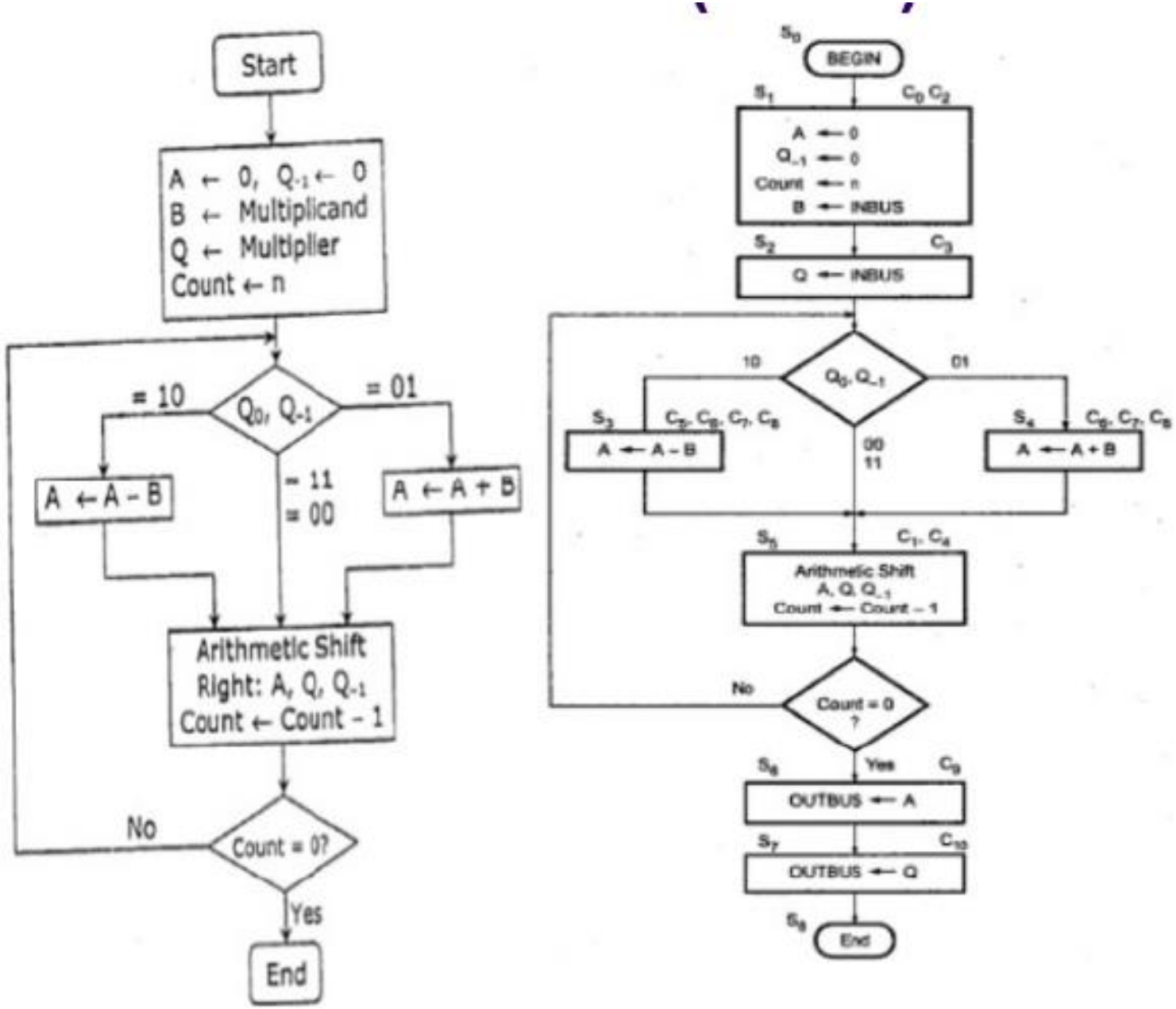
State-table Method

- Classical method of sequential circuit design.
- Attempts to minimize the amount of hardware.
- It starts with the construction of state transition table. In every state the control unit generates a set of control signals.
- Control unit transmits from one state to another state depending on its:
  1. Current state
  2. Input to the controller

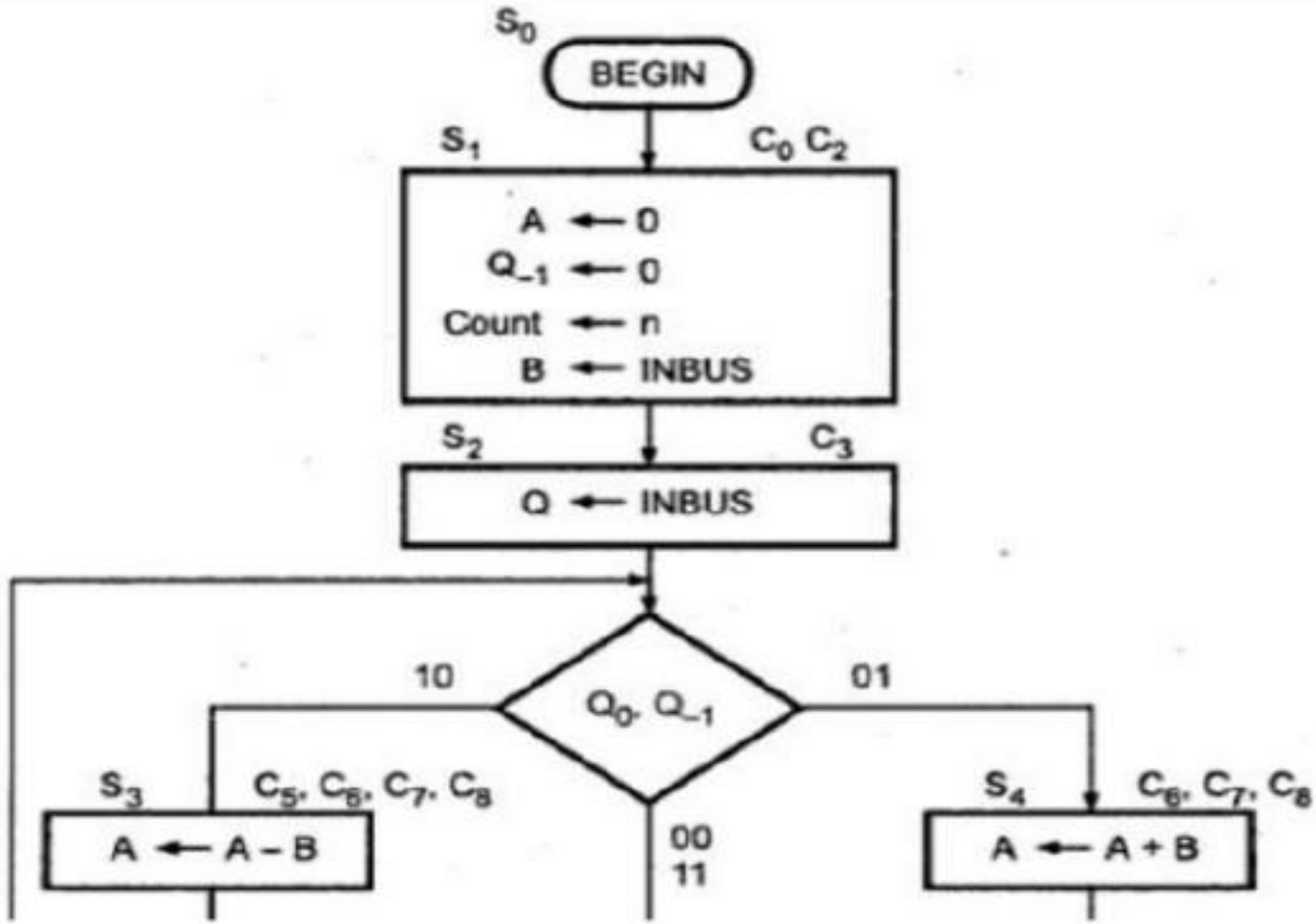
- State Assignment: States are assigned as S1,S2,S3…;each such assignment specifies a particular state of the controller at the specific time step. State table derived from state assignment

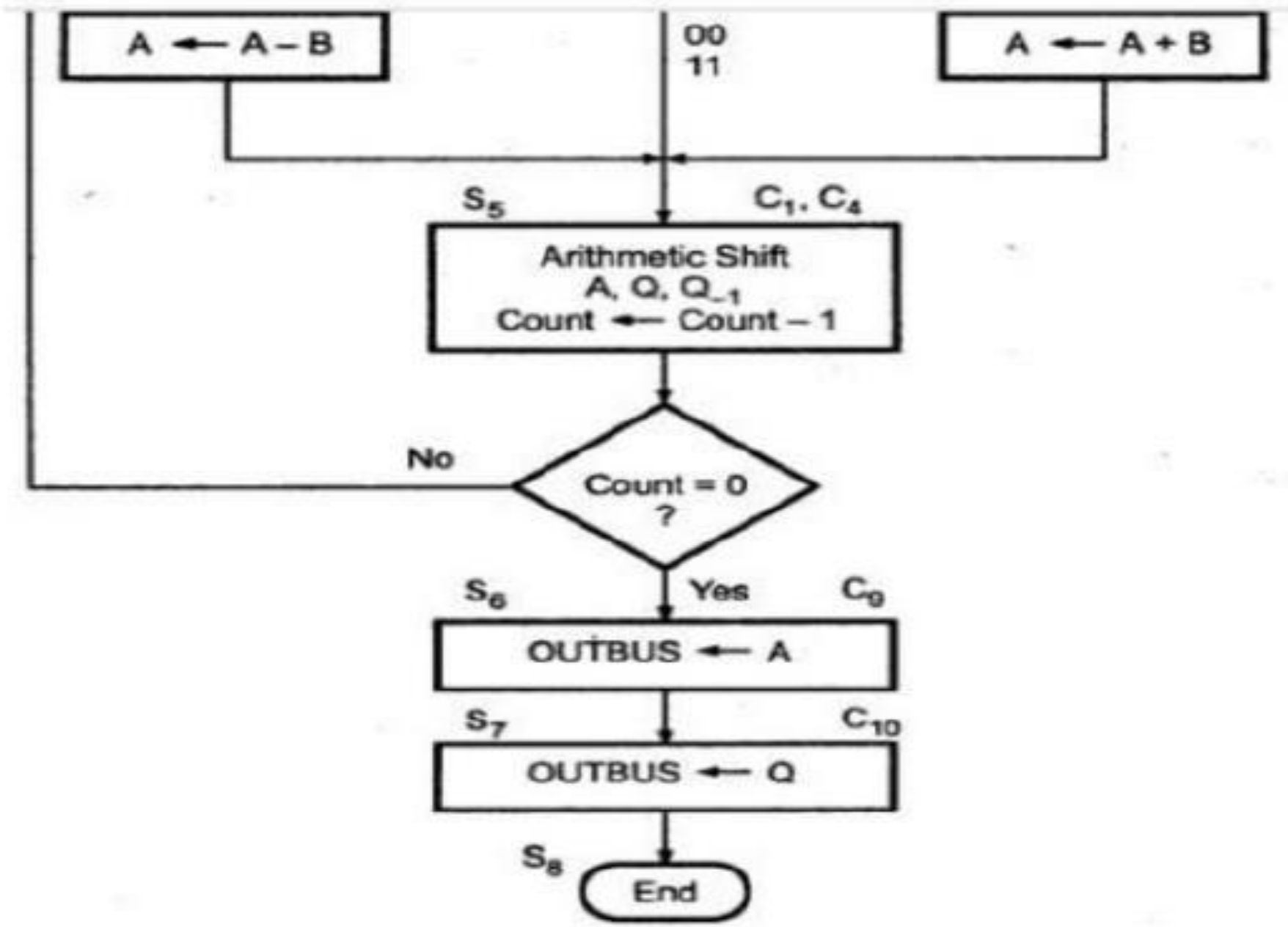
2’s complement multiplier

- State table construction is necessary.
- Associate a state with every micro-operation block giving nine states from S0 through S8.
- There are four primary input signals BEGIN, COUNT, Q0 and Q-1, so sixteen possible input combinations.
- Each entry in the table indicates next state followed by list of control signals that are activated.



Flowchart for 2's complement multiplication


S_0
BEGIN
S_1
C_0 C_2
A ← 0
Q_{-1} ← 0
Count ← n
B ← INBUS
S_2
C_3
Q ← INBUS
10
Q_0, Q_{-1}
01
00
11
S_3
C_5, C_6, C_7, C_8
A ← A – B
S_4
C_6, C_7, C_8
A ← A + B


A ← A – B
00
11
A ← A + B
S5
C1, C4
Arithmetic Shift
A, Q, Q-1
Count ← Count – 1
No
Count = 0
?
S6
Yes
C9
OUTBUS ← A
S7
C10
OUTBUS ← Q
S8
End

Inputs				States								
BEGIN	COUNT	Q_0	Q_{-1}	S_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
0 0		0 0		S_0	S_2, C_0 C_2	S_5, C_3			S_5, C_1, C_4			
0 0		0 1		S_0	S_2, C_0 C_2	S_4, C_3		S_5, C_6 C_7, C_8	S_4, C_1, C_4			
0 1		0 0		S_0	S_2, C_0 C_2	S_3, C_3	S_5, C_5 C_6, C_7 C_8		S_3, C_1 C_4			
0 1		0 1		S_0	S_2, C_0 C_2	S_5, C_3			S_5, C_1 C_4			
0 0		1 0		S_0	S_2, C_0 C_2				S_6, C_1 C_4	S_7, C_9	S_8, C_{10}	S_0, END
0 0			1 1	S_0	S_2, C_0 C_2				S_6, C_1 C_4	S_7, C_9	S_8, C_{10}	S_0, END
0 1			1 0	S_0	S_2, C_0 C_2				S_6, C_1, C_4	S_7, C_9	S_8, C_{10}	S_0, END

State table for multiplier control unit

0 0 1 1	S_0	S_2, C_0 C_2				S_6, C_1 C_4	S_7, C_9	S_8, C_{10}	S_0, END
0 1 1 0	S_0	S_2, C_0 C_2				S_6, C_1, C_4	S_7, C_9	S_8, C_{10}	S_0, END
0 1 1 1	S_0	S_2, C_0 C_2				S_6, C_1 C_4	S_7, C_9	S_8, C_{10}	S_0, END
1 0 0 0	S_1								
1 0 0 1	S_1								
1 1 0 0	S_1								
1 1 0 1	S_1								
1 0 1 0	S_1								
1 0 1 1	S_1								
1 1 1 0	S_1								
1 1 1 1	S_1								

State table for multiplier control unit (cont.)