4.16.6 Design of an SOP Circuit to Detect the Decimal Numbers 5 through 12 in a 4-bit Gray Code Input

The input to the SOP circuit is a 4-bit Gray code. Let the input Gray code be *ABCD*. There are 16 possible combinations of 4-bit Gray code. All of them are valid and hence there are no don't cares.

The truth table of the SOP circuit is shown in Figure 4.38a. Looking at the truth table of the SOP circuit, we observe that the output is 1 for the input combinations corresponding to minterms 7, 5, 4, 12, 13, 15, 14, and 10 (i.e. corresponding to the Gray code of decimal numbers 5, 6, 7, 8, 9, 10, 11 and 12). So the expression for the output is

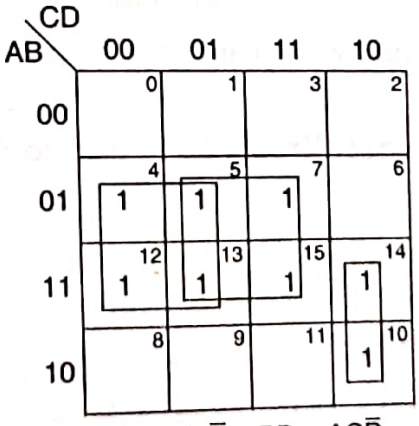
$$f = \Sigma\, m(7, 5, 4, 12, 13, 15, 14, 10) = \Sigma\, m(4, 5, 7, 10, 12, 13, 14, 15)$$

The K-map for f, its minimization, the minimal expression obtained from it and its realization in NAND logic are shown in Figures 4.38b and c respectively.

$$f_{min} = B\overline{C} + BD + AC\overline{D} = \overline{\overline{B\overline{C}} \cdot \overline{BD} \cdot \overline{AC\overline{D}}}$$

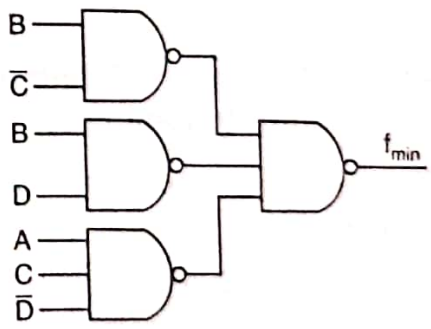
Decimal number	4-bit Gray code A	B	C	D	Output f
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	1	0
3	0	0	1	0	0
4	0	1	1	0	0
5	0	1	1	1	1
6	0	1	0	1	1
7	0	1	0	0	1
8	1	1	0	0	1
9	1	1	0	1	1
10	1	1	1	1	1
11	1	1	1	0	1
12	1	0	1	0	1
13	1	0	1	1	0
14	1	0	0	1	0
15	1	0	0	0	0

(a) Truth table



$f_{min} = B\overline{C} + BD + AC\overline{D}$

(b) K-map



(c) NAND logic

Figure 4.38 Truth table, K-map and logic diagram for the SOP circuit.

4.17 PARITY BIT GENERATORS/CHECKERS

Exclusive-OR functions are very useful in systems requiring error detection and correction codes. Binary data, when transmitted and processed, is susceptible to noise that can alter its 1s to 0s and 0s to 1s. To detect such errors, an additional bit called the *parity bit* is added to the data bits and the word containing the data bits and the parity bit is transmitted. At the receiving end the number of 1s in the word received are counted and the error, if any, is detected. This parity check, however, detects only single bit errors.

The circuit that generates the parity bit in the transmitter is called a parity generator. The circuit that checks the parity in the receiver is called a parity checker.

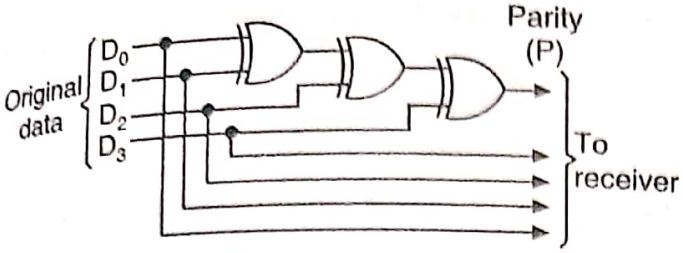
A parity bit, a 0 or a 1 is attached to the data bits such that the total number of 1s in the word is even for even parity and odd for odd parity. The parity bit can be attached to the code group either at the beginning or at the end depending on system design. A given system operates with either even or odd parity but not both. So, a word always contains either an even or an odd number of 1s.

At the receiving end, if the word received has an even number of 1s in the odd parity system or an odd number of 1s in the even parity system, it implies that an error has occurred.

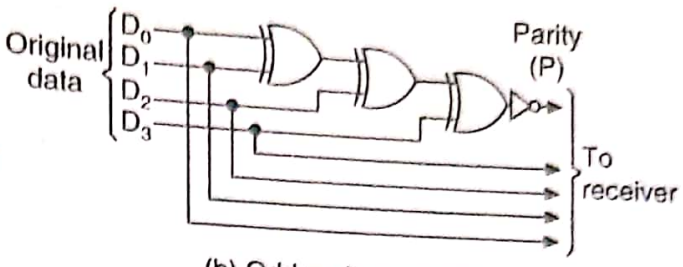
In order to check or generate the proper parity bit in a given code word, the basic principle used is, "the modulo sum of an even number of 1s is always a 0 and the modulo sum of an odd number of 1s is always a 1". Therefore, in order to check for an error, all the bits in the received word are added. If the modulo sum is a 0 for an odd parity system or a 1 for an even parity system, an error is detected.

To generate an even parity bit, the four data bits are added using three X-OR gates. The sum bit will be the parity bit. Figure 4.50a shows the logic diagram of an even parity generator.

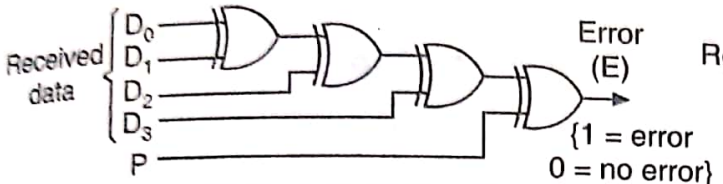
To generate an odd parity bit, the four data bits are added using three X-OR gates and the sum bit is inverted. Figure 4.50b shows the logic diagram of an odd parity generator. Figures 4.50c and d show an even bit parity checker and an odd parity checker, respectively. Also, Figure 4.50e shows the logic symbol of IC 74180, a 9-bit parity generator/checker. Figure 4.50f gives the truth table operation of this IC. This device can be used to check for odd or even parity in a 9-bit code (8 data bits and one parity bit), or it can be used to generate a 9-bit odd or even parity code.



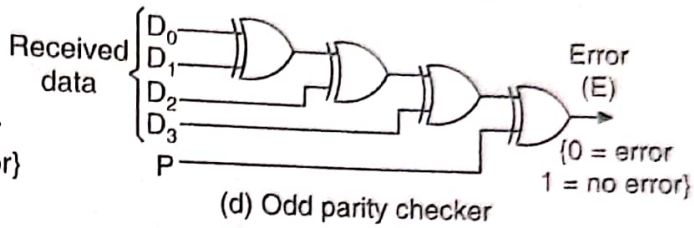
(a) Even parity generator



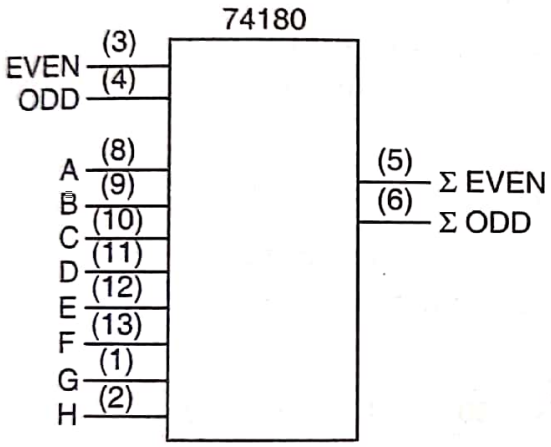
(b) Odd parity generator



(c) Even parity checker



(d) Odd parity checker



(e) Logic symbol of IC 74180

Σ of 1s at A through H	Inputs		Outputs	
	Even	Odd	Σ Even	Σ Odd
Even	1	0	1	0
Odd	1	0	0	1
Even	0	1	0	1
Odd	0	1	1	0
X	1	1	0	0
X	0	0	1	1

(f) Truth table of IC 74180 (X = don't care)

Figure 4.50 Parity bit generator/checker.