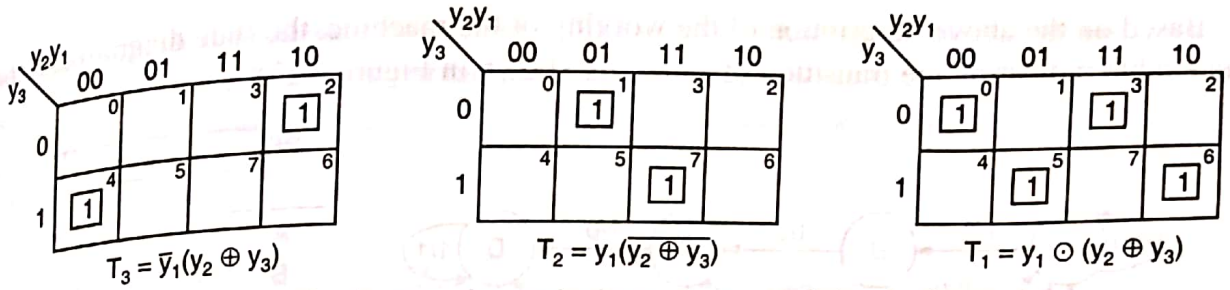


Figure 6.176 K-maps for excitations when x is ANDed with clock.

EXAMPLE 6.24 A long sequence of pulses enters a 2-input 2-output synchronous sequential circuit which is required to produce an output z = 1, whenever the sequence 1111 occurs. Overlapping sequences are accepted. For example, if the input is 01011111, the required output is 00000011. Design the circuit.

Solution

Step 1. *Word statement of the problem:* The block diagram of the 2-input, 2-output synchronous sequential circuit (sequence detector) with one input terminal and one output terminal is shown in Figure 6.177. The sequence detector has to detect and produce an output 1 whenever the sequence 1111 occurs. Overlapping sequences are accepted.

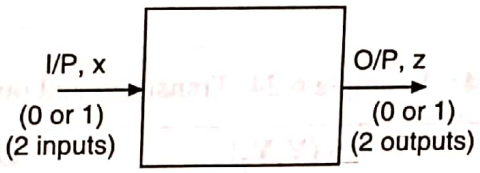
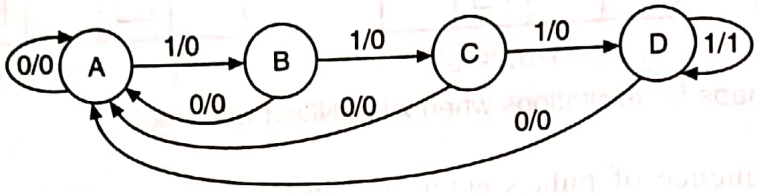


Figure 6.177 Example 6.24: Block diagram of a 2-input 2-output synchronous sequential machine.

Steps 2 *and* 3. *State diagram and state table:* Let the machine be initially in state A. While at A the first bit received may be a 0 or a 1. If it is a 0, it is invalid, so it will not start the detection process and so it will remain at A itself and outputs a 0. If the first bit is a 1, it is valid and so the detection process starts and the machine goes to next state B and outputs a 0. While at B the next bit received may be a 0 or a 1. If the second bit is a 0, the first two bits become 10 which is not a part of the valid sequence and so the detection has to start afresh. So machine goes back to A the starting state and outputs a 0. If the second bit is a 1, the first two bits become 11 which is a part of the valid sequence. So machine goes to next state C and outputs a 0. While at C, the machine may receive the next bit as a 0 or a 1. If the third bit is a 0, the sequence becomes 110 which is not a part of the valid sequence. So machine will output a 0 and goes to the initial state A. If the third bit is a 1, the sequence becomes 111 which is a part of the valid sequence. So the machine goes to the next state D and outputs a 0. While at D, the machine may receive the next bit as a 0 or a 1. If the fourth bit is a 0, the sequence becomes 1110, which is not valid and so the machine outputs a 0 and goes to state A. If the fourth bit is a 1, the four bits become 1111 which is a valid sequence. The machine outputs a 1 and remains at D itself because overlapping is permitted. It can utilize the second, third and fourth bits, i.e. 111 and continue the detection process. So if the fifth bit is a 0, the last four bits become 1110, so it will output a 0 and goes to state A. If the fifth bit is a 1, the last four bits become 1111, so it will output a 1 and remain at D itself and so on.

Based on the above description of the working of the machine, the state diagram and the state table indicating the transition of states are shown in Figure 6.178.



(a) State diagram

PS	NS, z	
	x = 0	x = 1
A	A, 0	B, 0
B	A, 0	C, 0
C	A, 0	D, 0
D	A, 0	D, 1

(b) State table

Figure 6.178 Example 6.24: Sequence (1111) detector.

Step 4. *Reduced standard form state table:* The machine is already in this form. So no need to do anything.

Step 5. *State assignment and transition and output table:* The state assignment is arbitrary. There are four states. So, two state variables are needed, which can give a maximum of four states. Therefore, there are no invalid states. Let the states be assigned as A → 00, B → 01, C → 10, and D → 11. With this state assignment, the transition and output table is as shown in Table 6.24.

Table 6.24 Example 6.24: Transition and output table

PS		NS (Y_1Y_2)		Output, z	
y_1	y_2	x = 0	x = 1	x = 0	x = 1
0	0	0 0	0 1	0	0
0	1	0 0	1 0	0	0
1	0	0 0	1 1	0	0
1	1	0 0	1 1	0	1

Step 6. *Choose type of flip-flops and form the excitation table:* Let us say D flip-flops are used as memory elements. With D flip-flops as memory elements the excitation table is as shown in Table 6.25.

Table 6.25 Example 6.24: Excitation table

PS		I/P	NS		I/P to FF		O/P
y_1	y_2	x	Y_1	Y_2	D_1	D_2	z
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0
0	1	0	0	0	0	0	0
0	1	1	1	0	1	0	0
1	0	0	0	0	0	0	0
1	0	1	1	1	1	1	0
1	1	0	0	0	0	0	1
1	1	1	1	1	1	1	

Step 7. K-maps and minimal expressions: The minimal expressions for excitations of FFs of the sequential circuit in terms of the present state variables y_1, y_2 and input x are obtained using K-maps as shown in Figure 6.179. From the excitation table the output z is given by $z = y_1 y_2 x$.

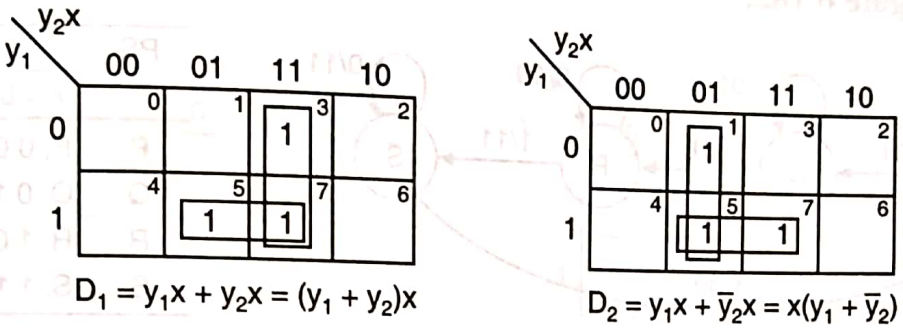


Figure 6.179 Example 6.24: K-maps for the sequence (1111) detector using D flip-flops.

Step 8. Implementation: The logic diagram of the sequence detector based on those minimal expressions is shown in Figure 6.180.

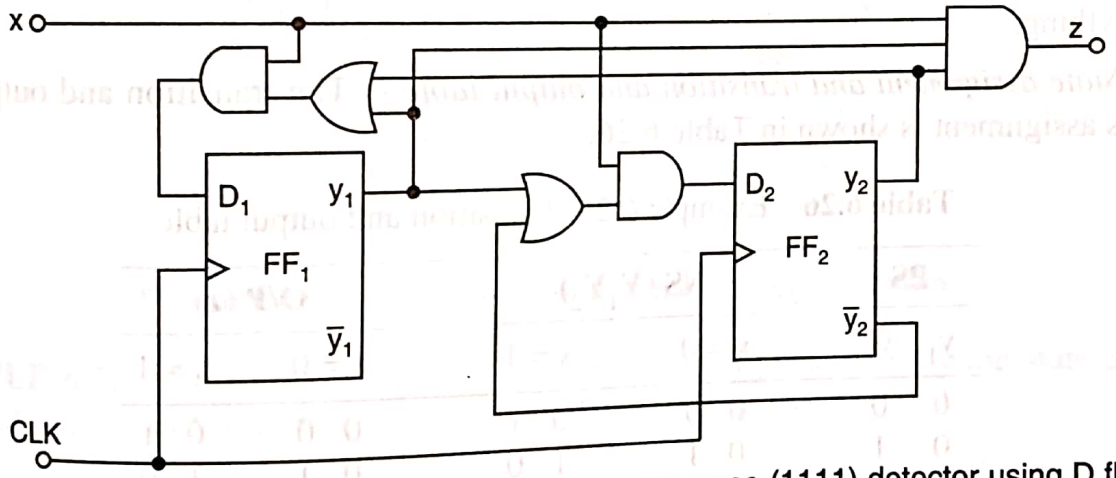


Figure 6.180 Example 6.24: Logic diagram of the sequence (1111) detector using D flip-flops.