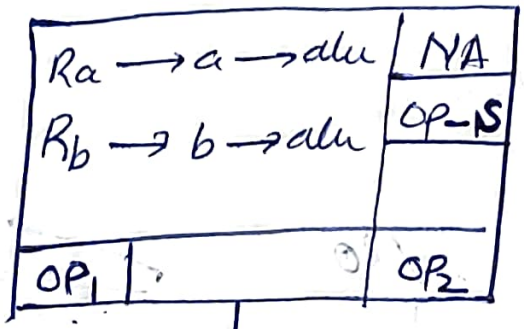
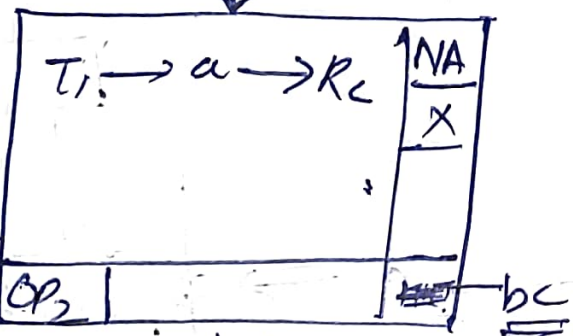
ADD

NDU :

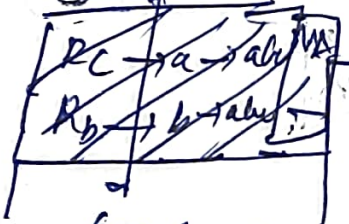
ADL





K=1

K=0

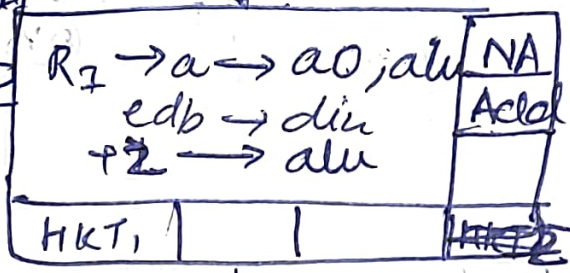


OP1 (K=1)

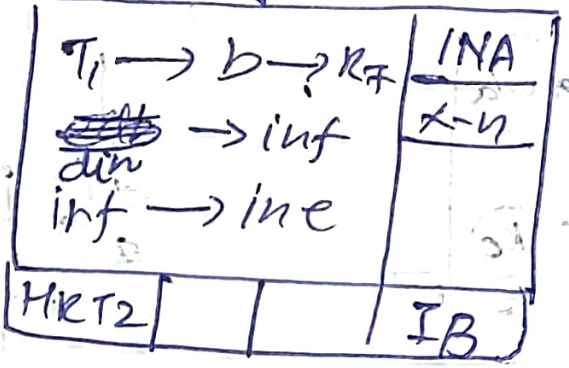
OP2 (K=1)

HKT1

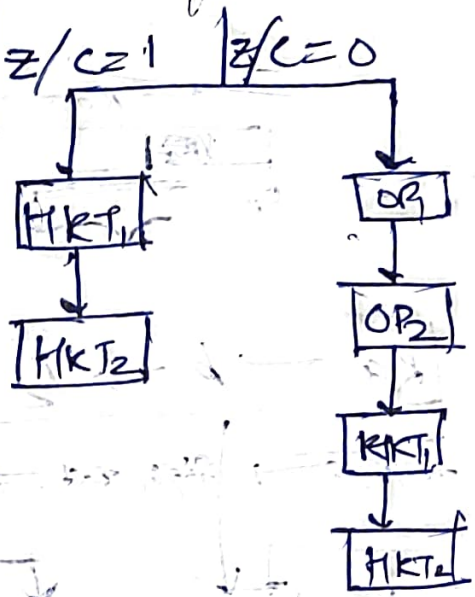
HKT



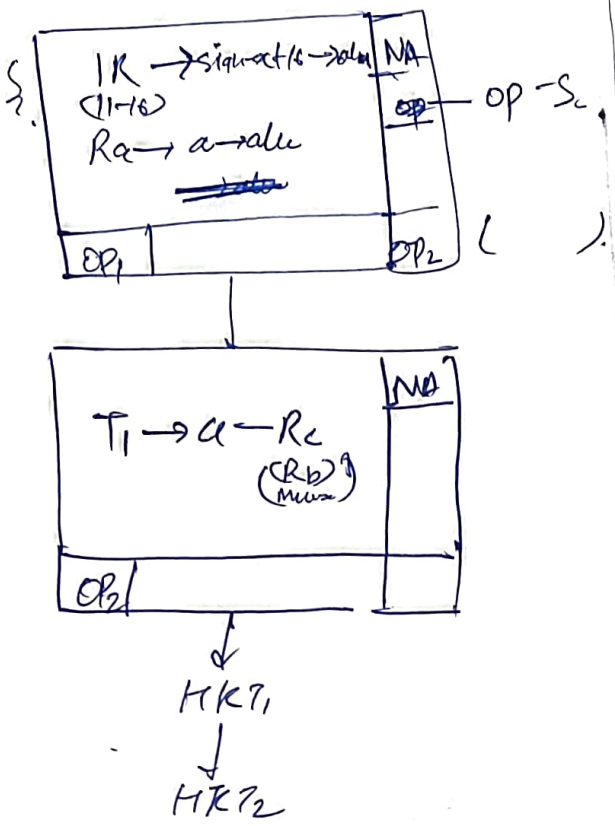
HKT2



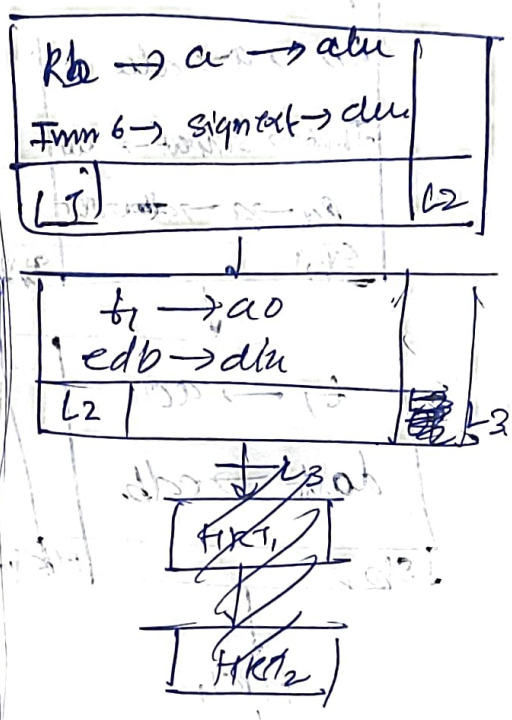
ADC / NDC
ADZ / NDZ



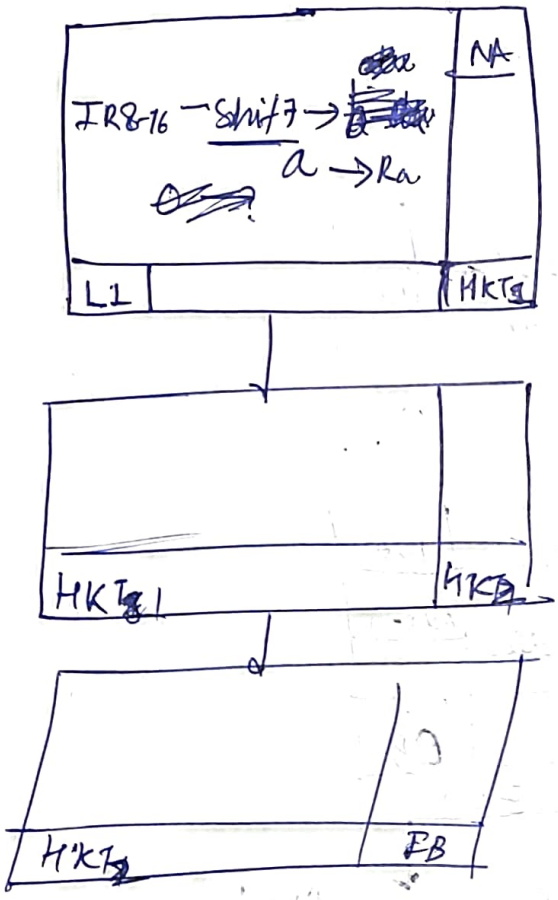
ADI

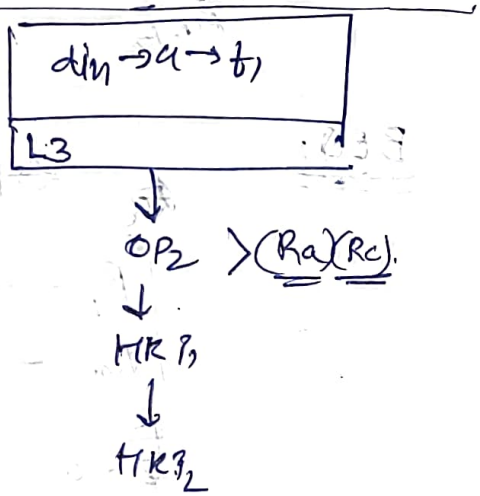

IR → sign-ext 16 → alu
(11-16)
Ra → a → alu
NA
op
op - Sc
OP1
OP2
T1 → a → Rc
(Rb)
Mux
NA
OP2
HKT1
HKT2

LW


Rb → a → alu
Imm 6 → sign ext → alu
L1
L2
t1 → a0
edb → din
L2
L3
L3
HKT1
HKT2

LHI


IR8-16 → Shift 7 →
a → Ra
NA
L1
HKT1
HKT1
HKT2
HKT2
FB


din → a → t1
L3
OP2 > (Ra)(Rc).
HKT1
HKT2

~~E~~ SW

Rb → a → dlu	
Imb → sign ext → dlu	
Ra → a → ~~dlu~~ dout	
SW1	SW2

↓

t1 → a0	
dout → edb	
SW2	HKT1

↓

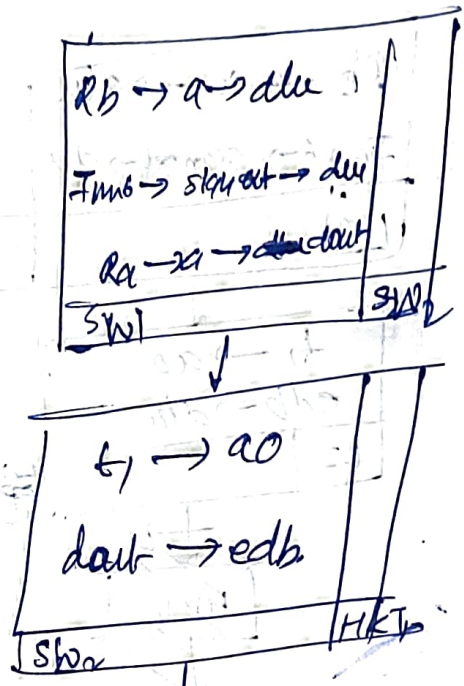
HKT1

↓

HKT2

BEQ:

~~Ra~~ ~~01~~



~~RB → b → dlu~~	~~add~~
~~Ra → a → dlu~~	
~~Z = 0~~	

RB → b → dlu	NA
Ra → a → dlu	Add-n
B1	CB

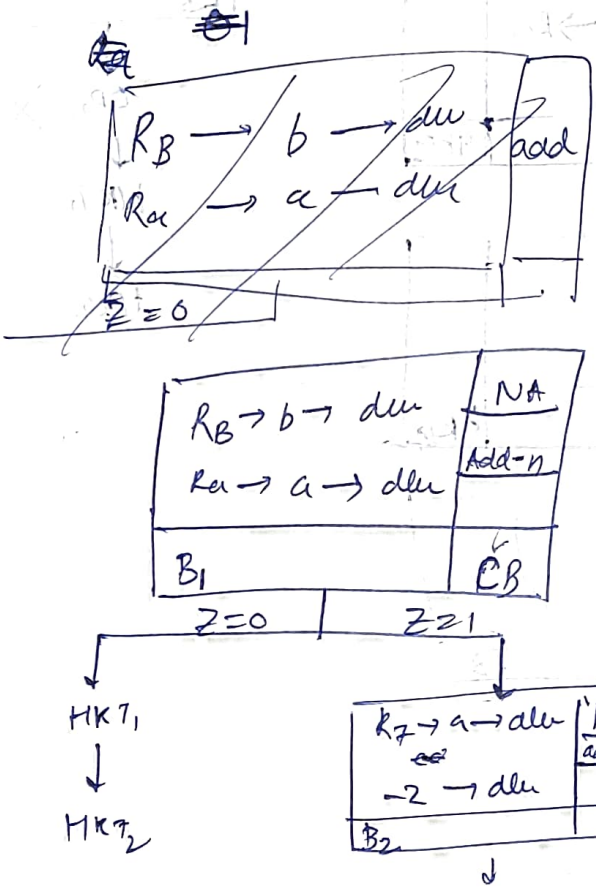
Z=0 | Z=1

↓ HKT1

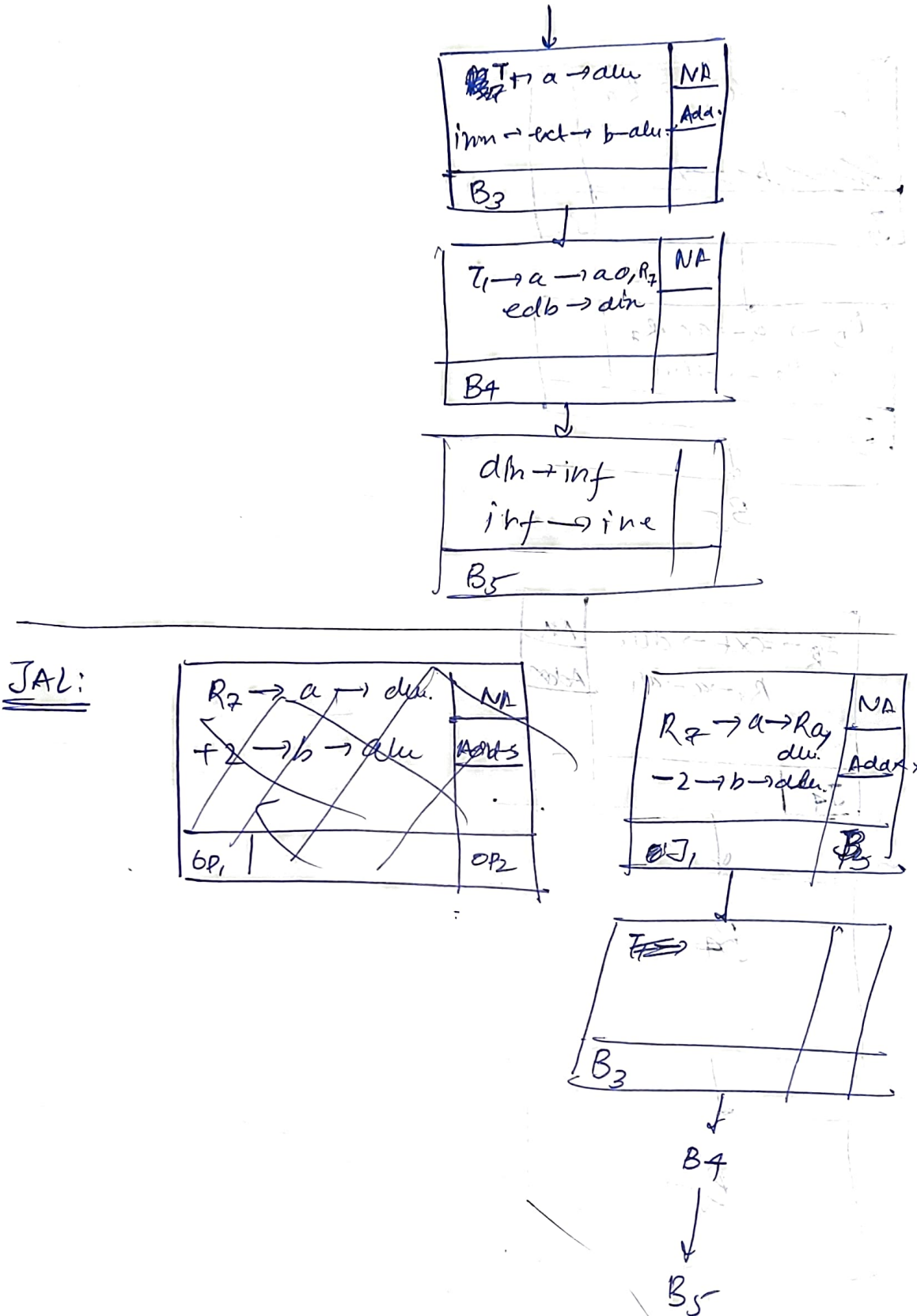
↓

HKT2

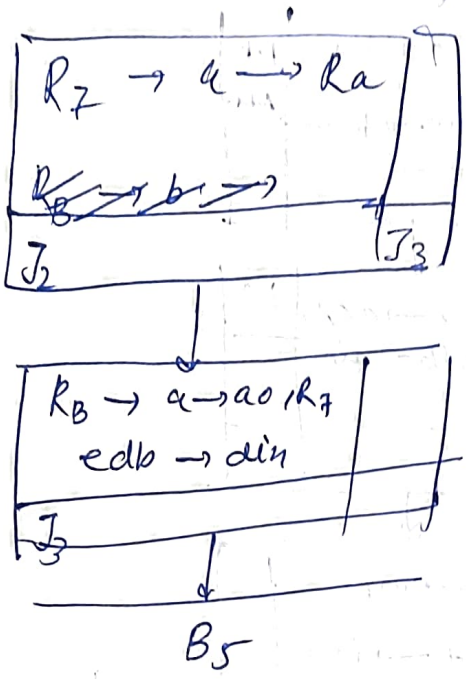
R7 → a → dlu	NA
~~ad~~	add-n
-2 → dlu	
B2	



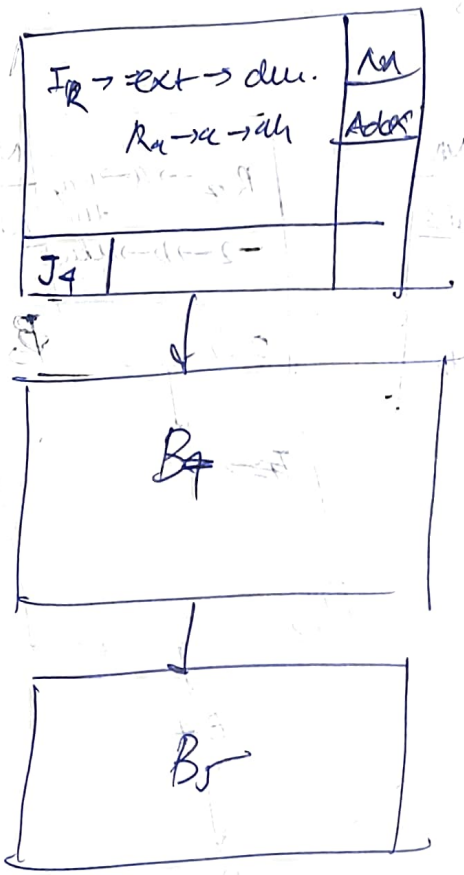
↓


T → a → alu
NA
imm → ext → b-alu
Add.
B3
T1 → a → a0, R7
edb → dtn
NA
B4
dtn → inf
inf → ine
B5
JAL:
R7 → a → alu.
NA
+2 → b → alu
Adds
OP1
OP2
R7 → a → Ra
alu.
NA
-2 → b → alu
Add
B5
B3
B4
B5

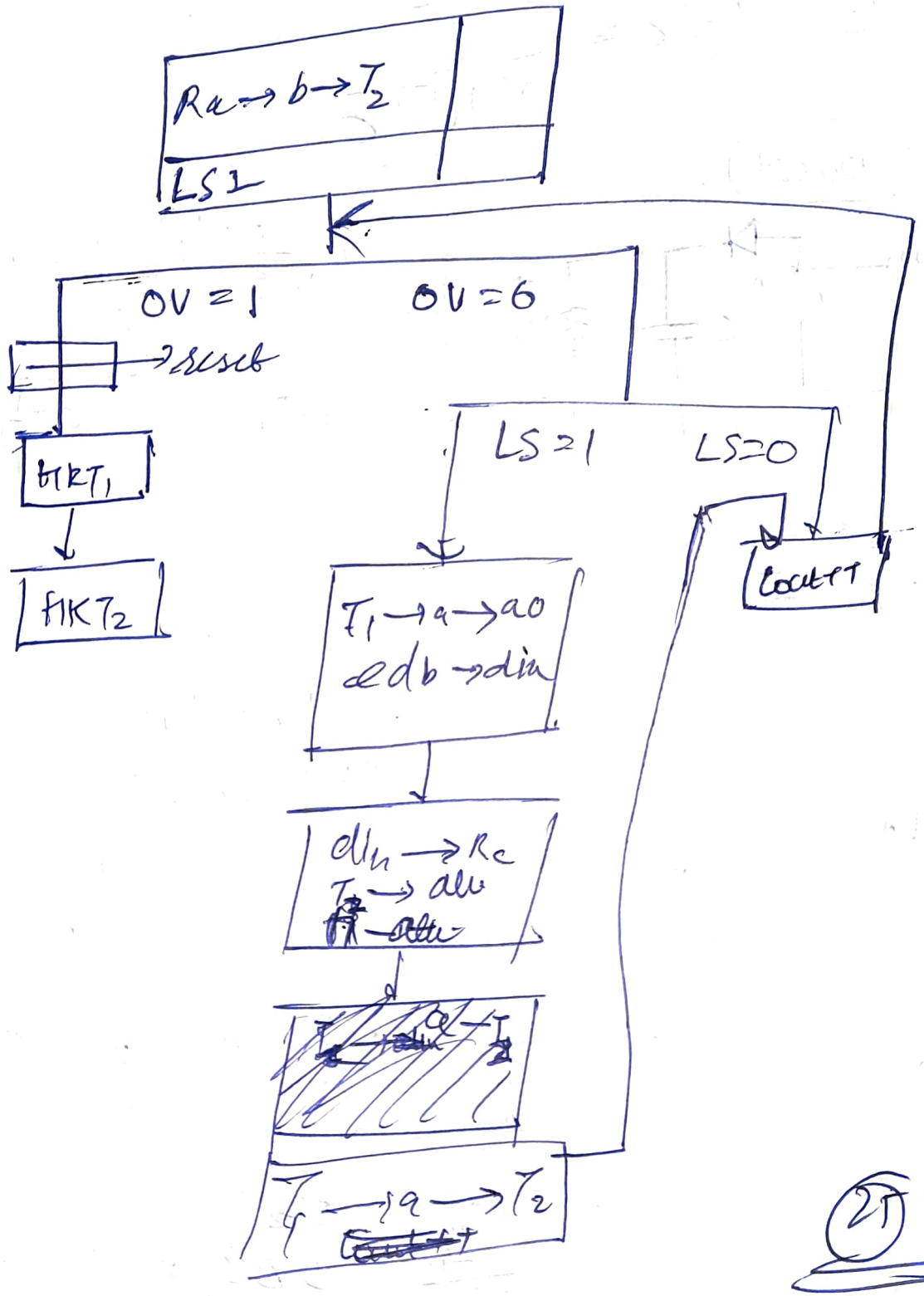
JLR.


R_7 → a → Ra
R_B → b →
J_2
J_3
R_B → a → a0 / R_7
edb → din
J_5
B_5

JRI:

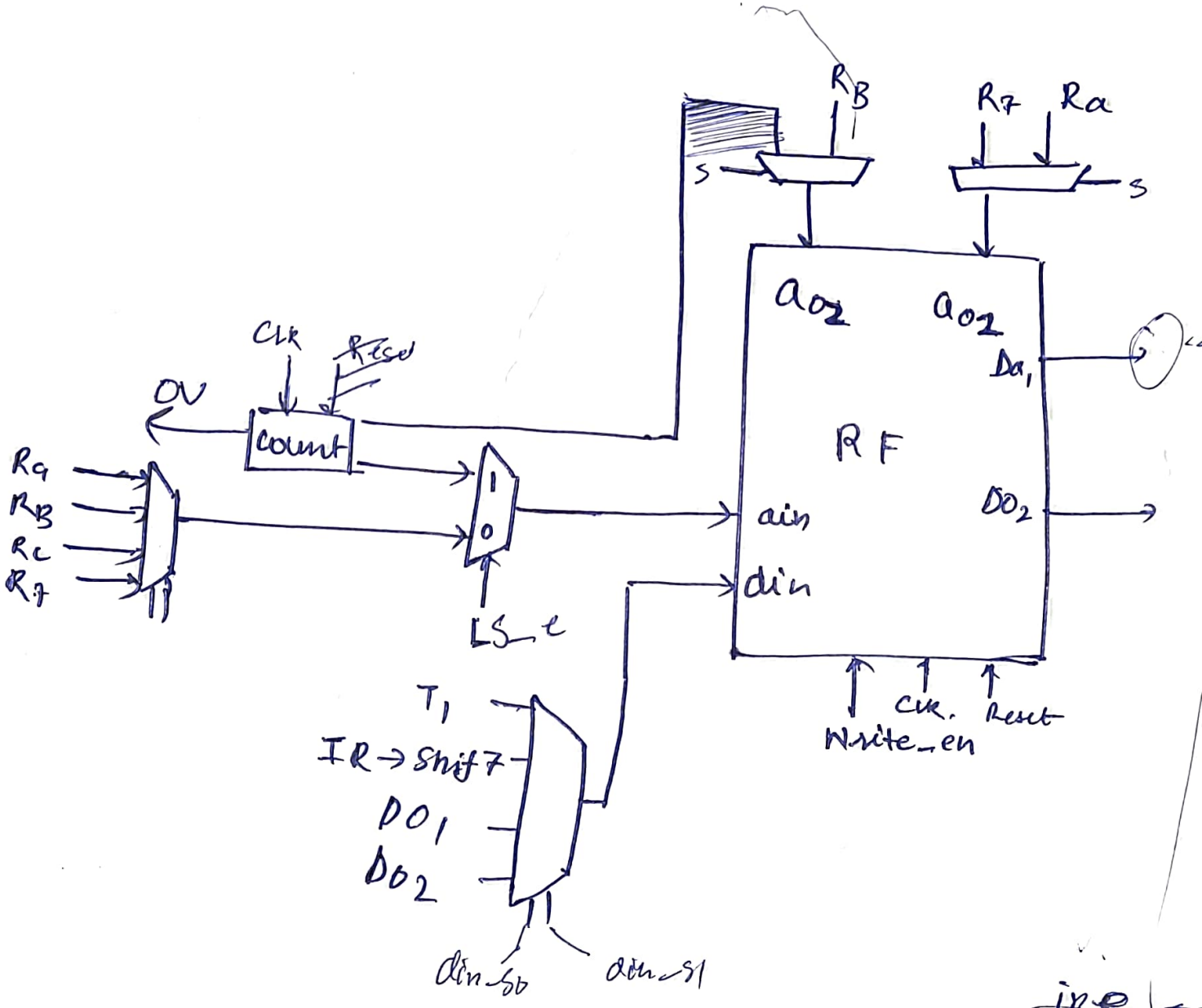

I_R → ext → dm.
R_a → a → ah
Adar
J_4
B_4
B_5

LM:

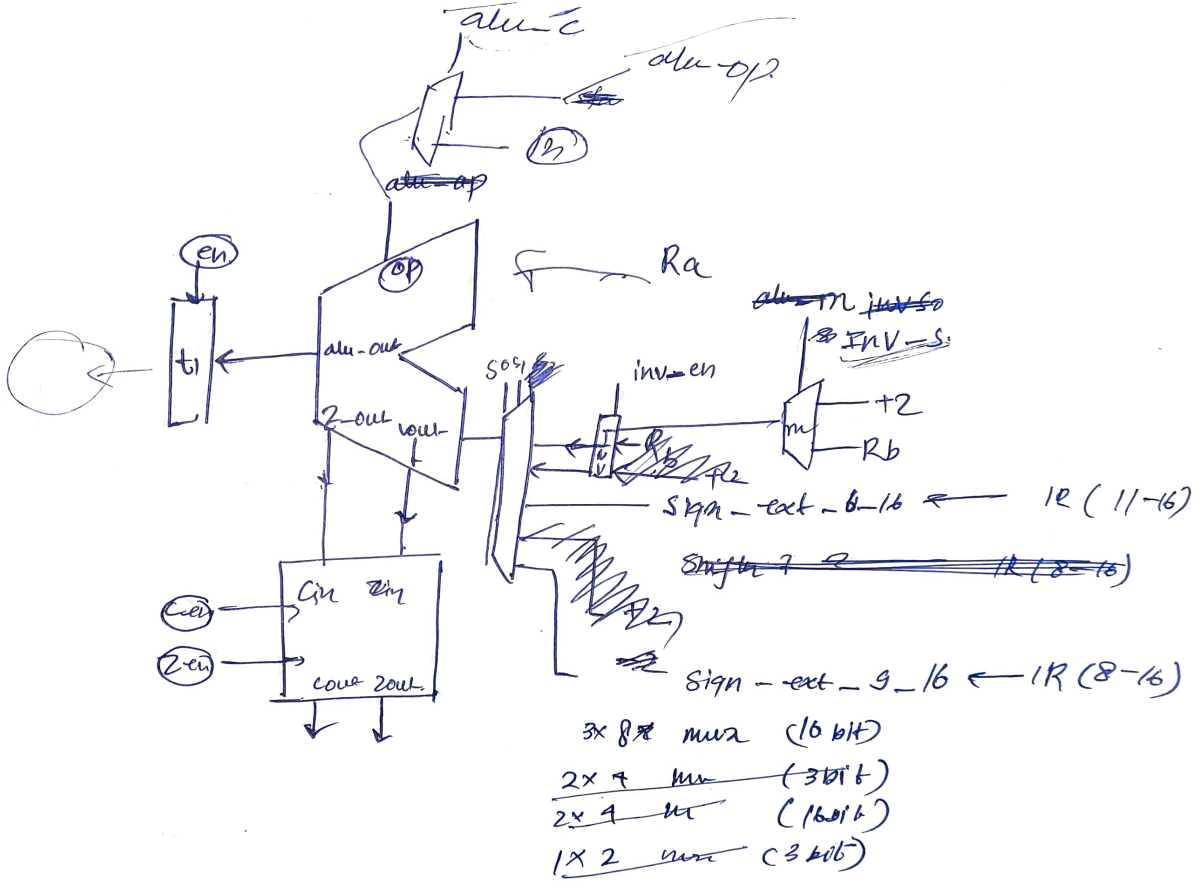


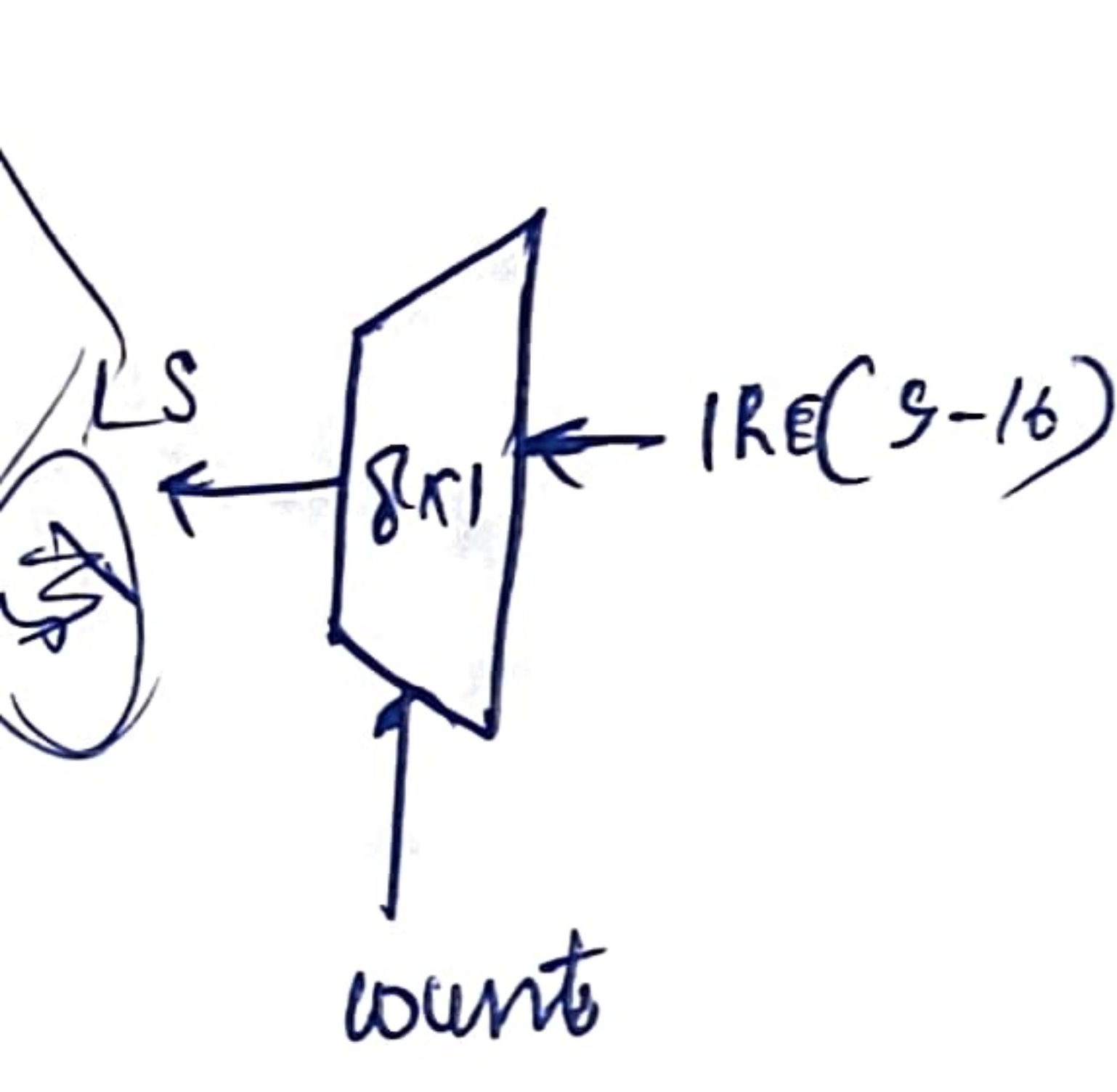
Ra → b → T2
LS1
OV = 1
OV = 0
reset
HKT1
HKT2
LS = 1
LS = 0
T1 → a → a0
edb → din
din → Rc
T2 → alu
T1 → a → T2

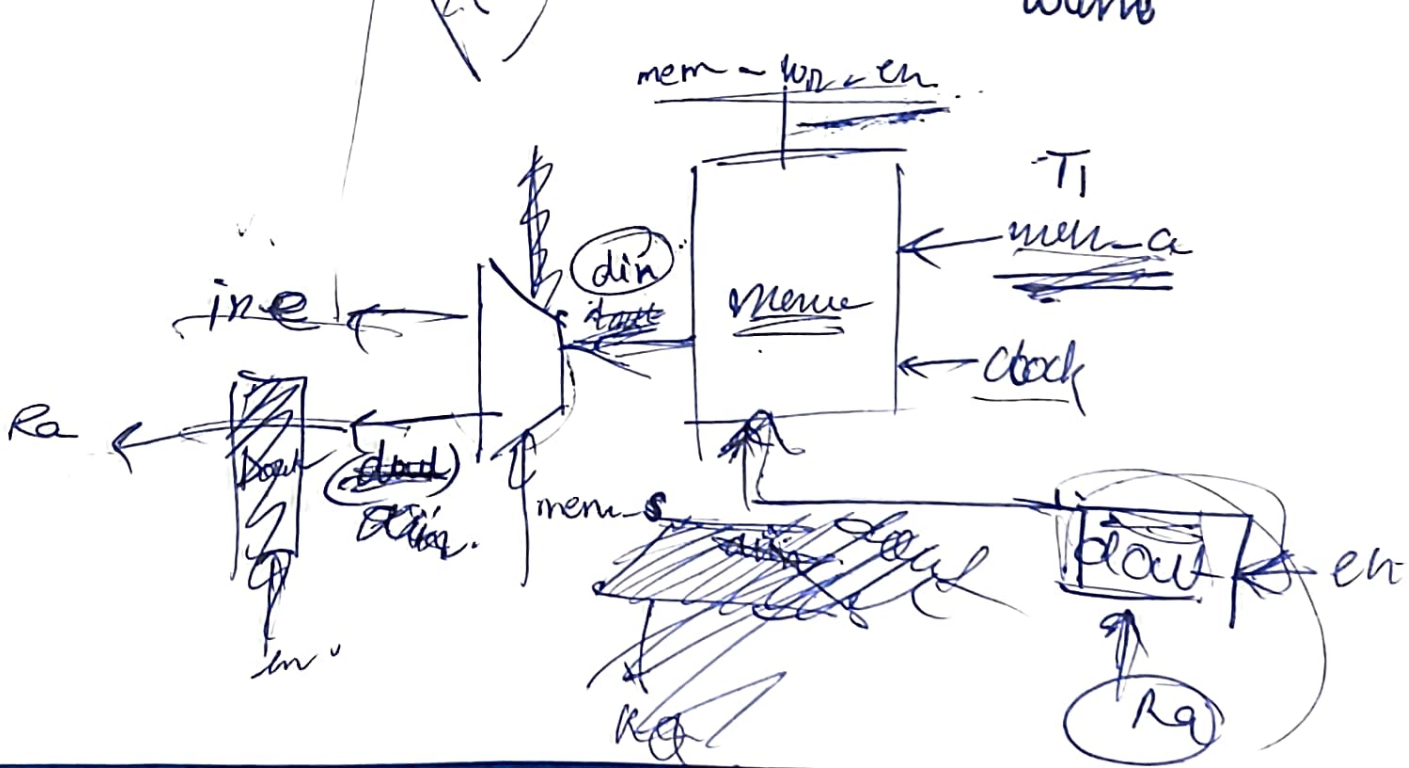
Ra Cmend — RF



RB
R7
Ra
S
S
a02
a02
Da1
RF
DO2
ain
din
Clk
Reset
0V
count
Ra
RB
Rc
R7
1
0
LS_e
T1
IR → Shift7
DO1
DO2
din_s0
din_s1
Write_en
Clk.
Reset


alu_c
alu_op
alu_op
en
op
Ra
t1
alu_out
2_out
sos1
inv_en
INV_S
+2
Rb
sign_ext_6_16 ← IR (11-16)
Cin
Zin
Cen
Zen
cout
2out
sign_ext_9_16 ← IR (8-16)
3x 8 mux (16 bit)
2x 4 mux (3 bit)
2x 4 mux (16 bit)
1x 2 mux (3 bit)


S
8x1
IR(9-16)
counts


mem_wr_en
T1
mem_a
din
ine
mem
clock
Ra
dout
mem_s
dout
en
Ra