15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Instruction	Note
0		rs				rd			0	0	0	0	0	0	0	mov	segment reg?
0				[7:0]					0	0	0	1	0	0	0	int	
0			-			0	0	0	0	0	1	0	0	0	0	sei	enable irq
0			-			0	0	1	0	0	1	0	0	0	0	cli	disable irq
0			-			0	1	0	0	0	1	0	0	0	0	sec	set carry
0			-			0	1	1	0	0	1	0	0	0	0	clc	clear carry
0			-			1	0	0	0	0	1	0	0	0	0	clv	clear overflow
0				…						…			0	0	0	**unused*14**	
0				…					1	1	1	1	0	0	0	emulation	break, halt, etc
0		rs				rd			0	0	0	0	0	0	1	add	
0		rs				rd			0	0	0	1	0	0	1	sub	
0		rs				rd			0	0	1	0	0	0	1	addc	
0		rs				rd			0	0	1	1	0	0	1	subb	
0		rs				rd			0	1	0	0	0	0	1	and	
0		rs				rd			0	1	0	1	0	0	1	or	
0		rs				rd			0	1	1	0	0	0	1	xor	
0		rs				rd			0	1	1	1	0	0	1	shl	
0		rs				rd			1	0	0	0	0	0	1	asr	
0		rs				rd			1	0	0	1	0	0	1	lsr	
0		rs				rd			1	0	1	0	0	0	1	cmp	
0		rs				rd			1	0	1	1	0	0	1	**unused**	
0		rs				rd			1	1	0	0	0	0	1	**unused**	
0		rs				rd			1	1	0	1	0	0	1	**unused**	
0		rs				rd			1	1	1	0	0	0	1	**unused**	
0		rs				rd			1	1	1	1	0	0	1	**unused**	
0		-				rd			-	0	0	0	0	1	0	not	
0		-				rd			0	0	0	1	0	1	0	neg	
0		-				rd			1	0	0	1	0	1	0	negb	
0	-		[2:1]			rd			[0]	0	1	0	0	1	0	shli	
0	-		[2:1]			rd			[0]	0	1	1	0	1	0	asri	
0	-		[2:1]			rd			[0]	1	0	0	0	1	0	lsri	
0		[4:1]				rd			[0]	1	0	1	0	1	0	andi	
0		[4:1]				rd			[0]	1	1	0	0	1	0	ori	
0		[4:1]				rd			[0]	1	1	1	0	1	0	xori	
0				[7:0]						rd			0	1	1	addi	
0				[7:0]						r1			1	0	0	cmpi	
0				[7:0]						rd			1	0	1	loadi	
0				[7:0]					lr		as		1	1	0	call	register relative
0				[7:0]					0	0	0	0	1	1	1	jmp	
0				[7:0]					0	0	0	1	1	1	1	br.eq	
0				[7:0]					0	0	1	0	1	1	1	br.ne	
0				[7:0]					0	0	1	1	1	1	1	br.lt	
0				[7:0]					0	1	0	0	1	1	1	br.ge	
0				[7:0]					0	1	0	1	1	1	1	br.lts	
0				[7:0]					0	1	1	0	1	1	1	br.ges	
0				…					0	1	1	1	1	1	1	**unused**	
0				[7:0]					1	-	lr		1	1	1	call	pc relative
1				[7:0]						rd			as		0	load	
1				[7:0]						rd			as		1	store	