SL Unit 2 – Computer Organization

Quiz 2

Question 1			
Objectives:	2.1.12	Exam Reference:	Nov-15 3

Construct a truth table for the following Boolean expression.

`(A and B) nor C` [3]

*Award **[3]** for completely correct table.*
*Award **[2]** if only 6 or 7 rows are correct.*
*Award **[1]** if only 4 or 5 rows are correct.*
*Award **[0]** otherwise*, or if table does not contain 8 rows.

A	B	C	(A AND B) NOR C
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Question 2			
Objectives:	2.1.10	Exam Reference:	May-16 9

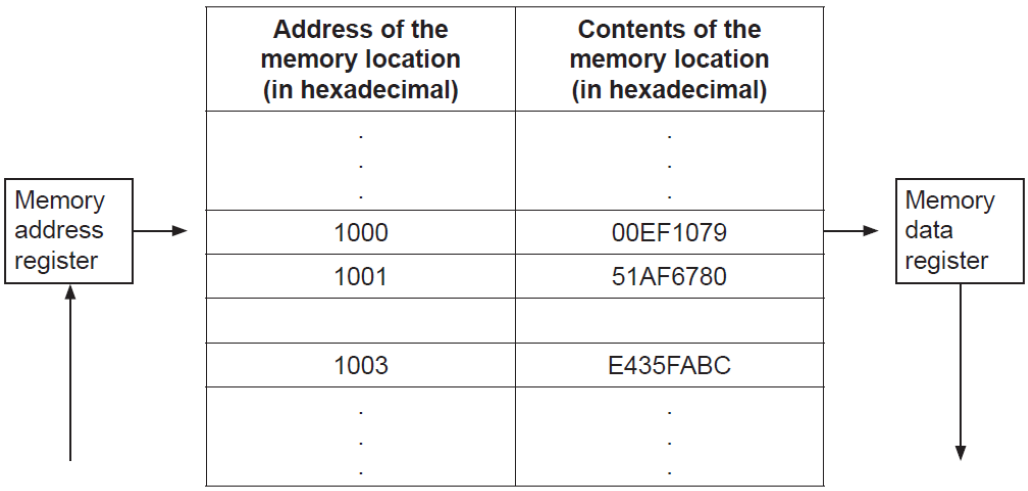
In an 8-bit register, state the binary representation of the hexadecimal number *3B*. [2]

*Award **[1]** for correct 111011.*
*Award **[1]** for using two leading zeroes for the 8-bit register.*

00111011;

Question 3			
Objectives:	2.1.1, 2.1.6,2.1.9	Exam Reference:	Nov-15 8

The following diagram shows the structure of the random access memory (RAM).



Address of the memory location (in hexadecimal)	Contents of the memory location (in hexadecimal)
. . .	. . .
1000	00EF1079
1001	51AF6780
1003	E435FABC
. . .	. . .

(a) Calculate the number of bits in each memory location. [1]

32

(b) Calculate the number of bytes in each address. [1]

2

(c) Outline the function of the:

(i) memory address register [2]

*Award up to **[2 max]**.*
MAR is a register in the CPU;
Loaded with the address of the next instruction/data;
To be taken from the RAM;

(ii) memory data register. [2]

*Award up to **[2 max]**.*
MDR is a register in the CPU;
Holding the data which is most recently;
Taken from RAM

(d) (i) Identify two functions of the operating system. [2]

*Award up to **[2 max]**.*
Resource allocation;
Memory management;
Interrupt handling; **[2]**
Etc.

(ii) State where the operating system is held when the computer is turned off. [1]

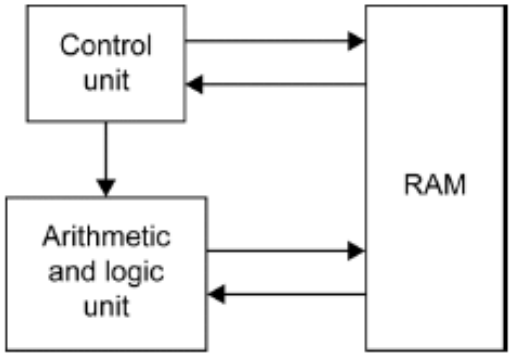
*Award up to **[2 max]**.*
Resource allocation;
Memory management;
Interrupt handling; **[2]**
Etc.

The machine instruction cycle refers to the retrieval of an instruction from the RAM, and subsequently decoding, executing and storing the result.

(e) (i) Construct a diagram to illustrate the structure of a central processing unit (CPU), clearly showing the flow of data within the CPU. [4]

*Award up to **[4 max]** for any acceptable diagram.*
*Award **[1]** for each unit **x3**, **[1]** for showing the flow of data.*

Example answer:



(ii) Identify the part of the CPU which performs decoding. [1]

Control Unit