Hardware

PCB

For the chip tester, two PCBs are needed in this project. One which is called B2 has been designed for the virtual designs to be loaded in a slave FPGA. The other is called B1 that is developed as an interface for those real chips are about to be tested. Both PCBs are two layers board and designed by using Allegro 16.3 PCB designer tools. The dimensions of B1 and B2 are 98.93 mm* 68.5 mm and 81.28 mm * 68.33 mm and the minimum wire size is 8mm.

I. B1 (DUT testing board)

1. DUT

The superchip under test has the following specific features:

+16 separate design sites
+24 digital input pins [A0..A23], shared between all design sites;
+24 digital output pins [Q0..Q23], shared between all design sites;
+16 separate VDD pins, one dedicated to each design site;
+1 global GND pin for all design sites and infrastructure circuitry;
+1 global VDD pin to power the site buffers and I/O pad ring;
+68-pin JLCC package (with 2 unused pins).

The chip is interfaced with the PCB by a 68WAY PLCC socket. The power is supplied by the 3.3V VDD from the DE2 board. The GND is also connected to the DE2 GND.
The shared I/Os are connected to the powered design site, and disconnected from the other design sites. Hence a controllable power switch is designed with a 4-16 decoder and an integrated power switch array. The Q1 is the output of a ring oscillator. The frequency can be digitally tested by the general I/O. However, to examine the analog properties of this output, an analog part including a buffer, 3rd order Butterworth filter and ADC with their own power supply is also designed.

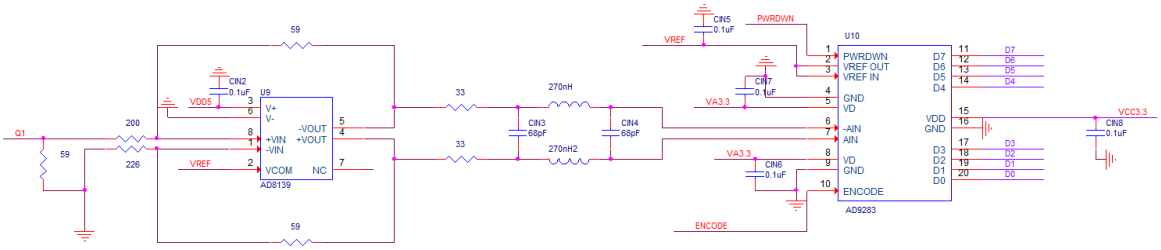
2. Digital part

A. Decoder
Although there are 16 design sites to be selected, the data can be shrunk down to 4 bit to save space of the test vector and metadata, since only one site is selected at a time. The decoder we used is 74HC4514, a 4-to-16 line decoder with latch. The input and output are active high.

B. Switch array
The switch array consists of four TPS2095 quad power-distribution switches. One could simply use a CMOS to realize a switch. However, with thermal sense, current limit and charge pump, the TPS2095 switches are more reliable, stable, smooth (minimum switching current surges) and relatively compact in scale. The operation of a switch is simple: when EN pin is asserted, the OUT pin offers the power with the same voltage in

the IN pin. Otherwise the OUT pin is disconnected from the input power. In one TPS2095 chip there are 4 such switches, the EN pins of which are all active high.

3. Analog part



A. Buffer

An AD8139 differential ADC driver is used as the front buffer of the ADC. It is an ultralow noise, high performance differential amplifier with rail to rail output from Analog Devices. The designed gain of the buffer is 0.295, and the differential gain is approximately 0.14.

B. ADC

The 8-bit, 100MSPS ADC is used to convert the analog signal. The encode clock is the clock from the DE2 board (100MHz by default). A power-down function select is also connected to the FPGA for shutting down the ADC when it's not in use. The ADC signal wires should be placed far away from the other wires for minimum interference; and they should also be placed parallel to each other to have similar length for better signal integrity. However, since the pin density is too high of the HSMC connector we used, it is inevitable that the ADC wires are closed to the other wires. The ADC is placed on the other side of the PCB board for a better result.

C. Butterworth Filter

To minimize the high frequency noise, a third-order low pass Butterworth filter is designed. With three poles, the attenuation is -60dB/decade on signals higher than the cut-off frequency. The filter topology used here is balanced ladder topology. Automatic design tool Elsie is used for designing the parameters of the RCI circuit. The cut-off frequency is 40MHz.

D. Separate power supplies

The buffer and ADC are separately powered from the other parts of the board. The AD8139's power ranges from 5V to 12V, and the ADC ranges from 2.7V to 3.6V. Two low dropout regulators (LDP), ADP3335 and ADP3333 are used to offer 5V and 3.3V voltages respectively. The supply voltage of these two LDP ranges from 2.6V to 12V. Their load currents are up to 500mA and 300mA respectively.

II. B2 (Virtual design board)

When started designing the B2 board for slave FPGA, the Altera Power Estimator is used for early power estimation calculations. Assume that an almost full usage of the FPGA, which means 90% of all of logic blocks/cells, 90% of multipliers and 90% of memory elements, as well as 64 I/O pins. The clock rate was assumed to be 100MHz. In case of the toggle rates, two figures are assumed here. One set is 12.5% on every net as a maximum toggle rate for the device while the other is 30% which is a huge and unlikely to be realistic in the worst-case power consumption situation.

Ambient temperature was taken as 25 degrees and no heat sink was assumed in the calculations, and no air flow (still air).

The power consumption result for 12.5% toggle rate:
-Logic: 0.235 W
-RAM: 0.009 W
-DSP: 0.032W
-I/O: 0.023 W
-PLL: 0.016 W
-Clock: 0.135W
-P_static: 0.123W
Total: around 0.574 W

For 30% toggle rate the main change is the change in Logic power consumption, therefore consumption of Logic is 0.565 W and the in total is now 0.905 W.

Translate these into power supply current requirements. For 12.5% toggle rate:
-Icc (int) (1.2V) 0.352A
-Icc (A) (2.5V) 0.036A
-Icc (d) (1.2V) 0.014A
-Icc (IO) (3.3V) 0.013A

For 30% toggle rate main change is Icc (int) changes to 0.627A.

The current consumption the main board provides is 1.5A in 3.3V power supply when 50% usage of the FPGA, which is sufficient for both cases since only 20% usage occupied in this project.

1. Slave FPGA

Slave FPGA is the core chip of the virtual design board. It can be used for programing designs when they are going to be tested. An Altera Cyclone III FPGA will be implemented as the slave FPGA.

Cyclone III (EP3C25E144) belongs to Cyclone III device family. With densities ranging from about 5,000 to 200,000 logic elements (LEs) and 0.5Mb to 8Mb of memory for less than ¼V of static power consumption, cyclone III devices makes it easier to meet the power budget.[1](Cyclone III device handbook, Volume 1)

The reason for choosing Cyclone III is their lowest power, high functionality with the lowest cost. 144 pins are enough for this design. I/O pins on the Cyclone III are grouped together into I/O banks, and each bank has a separate power bus. There are eight I/O banks, as shown in Figure 1. (Cyclone III device handbook, Volume 1) All single-ended I/O standards are supported in all banks except HSTL-12 Class II which is only supported in column banks. The same case can be found in all differential I/O standards.

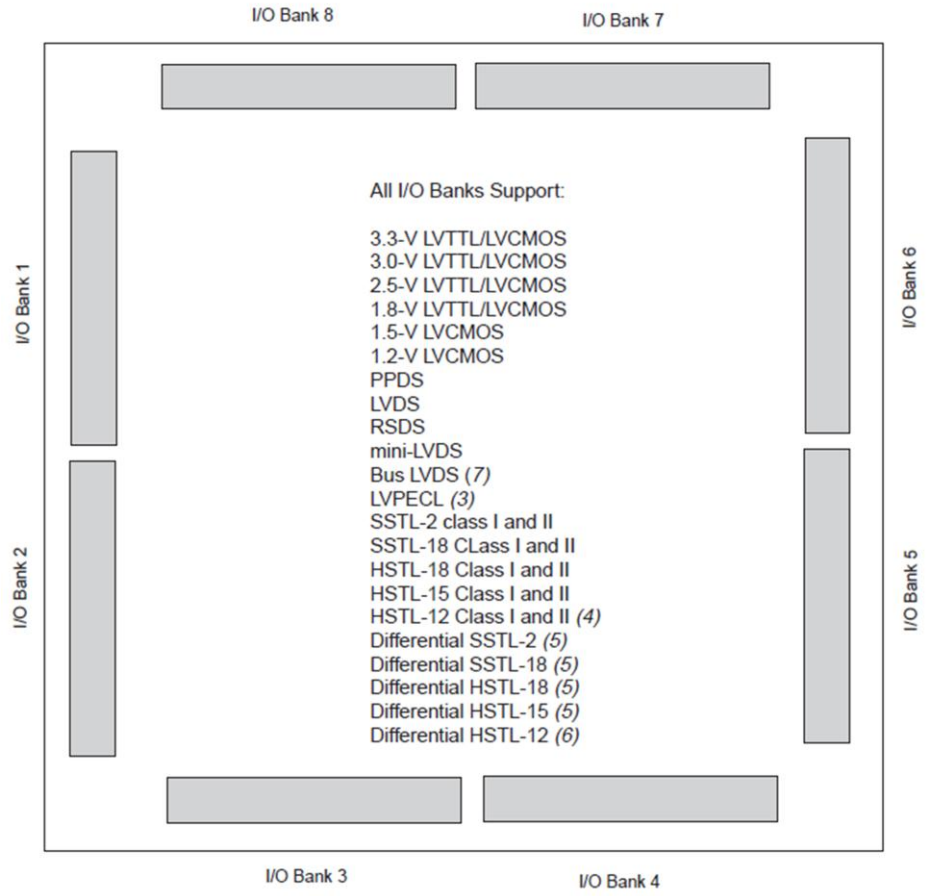


Figure 1

Each I/O banks of Cyclone III has a VREF bus to accommodate voltage-referenced I/O standards. Connect the VREF pin of each group to the appropriate voltage. In this design three voltage levels, which VCCIO=3.3V, VCCINT= 1.2V and VCCA=2.5V, are necessary. Proper bypassing and decoupling technique for the power pins is very important for reliable design operation. In this case, additional decoupling capacitance is needed. The VCCINT, VCCIO and ground pins should add as many as 0.2uF power-supply decoupling capacitors as possible. So 0.01uF capacitor for VCCIO and 0.1uF for VCCINT seems to be appropriate. Note that all the capacitors should be place close enough to the power pins.

In regard of the Cyclone III configuration, the Cyclone II device uses SRAM cells to store configuration data. EP3C25E144 can only be configured in Fast Active serial (AS) mode.

Configuration data is loaded into Cyclone III at each DCLK cycle. As soon as the device receives all data, the device releases the open-drain CONF_DONE pin, which is pulled high

by an external 10-$K\Omega$ pull-up resistor. The CONF_DONE pin transits low-to-high to indicate that configuration is complete and initialization of the device can begin. The CONF-DONE pin must have a 10-$K\Omega$ pull-up resistor for initialization.

Pulling the nCONFIG pin low can begin reconfiguration and this pin must be low for at least 500ns. The Cyclone III device is reset when nCONFIG is pulled low. Meanwhile, the device will pulls nSTATUS and CONF_DONE low and I/O pins are tri_stated. When nCONFIG returns to high and nSTATUS is released, reconfiguration begins.

The clock source for initialization is either a 10-MHz (typical) internal oscillator or an optional CLK pin. In this situation, an external oscillator (A TXC-50MHz oscillator is going to be introduced later) will be implemented as the clock source. The required clock for initialization in Cyclone III is 3,185 and the maximum CLUK frequency is 133MHz.

The configuration mode is selected by driving the MSEL pins either low or high. The MSEL pins can be powered by VCCIO and GN D. For AS mode, MSEL [1] should be pulled up by connecting to VCCIO. MSEL [0] and MESL [2] are pulled down by connecting to GND. The MESL pins have 9-$K\Omega$ internal pull-down resistors that are always active.

The maximum active master frequency for Cyclone III is 30MHz typically and device only work with serial configuration devices that support up to 40MHz.

In AS mode, Cyclone III reads the configuration data providing by serial configuration (A Spansion SPI Flash is going to be introduced later) via a serial interface. The serial configuration device controls the configuration interface.

There are four pins on the serial configuration devices:
-Serial clock input (DCLK)
-serial data output (DATA)
-As data output (ASDI)
-Active-low chip select (nCS)

Connect these four pins to Cyclone III device pins, as shown in Figure 2.

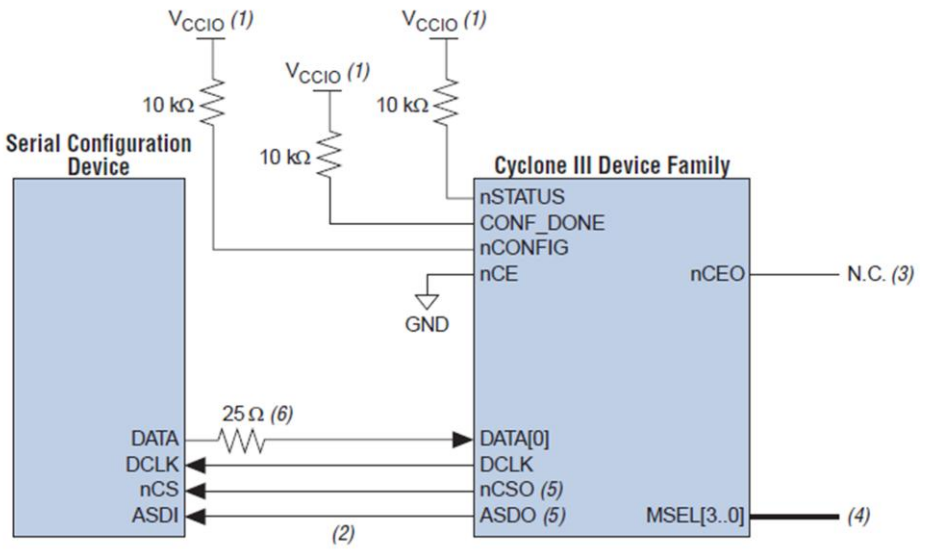


Figure 2

A 25Ω series resistor must connect a between serial configuration device and the Cyclone III device at the near end of the serial configuration device for DATA [0] when configure the Cyclone III device in the AS mode. The 25Ω resistor works to minimize the driver impedance mismatch with the board trace and reduce the overshoot seen at the Cyclone III device input pin DATA [0].

The maximum trace length between Cyclone III device and the serial configuration device, in another words, the DCLK, DATA [0], NCSO and ADSO pins, must less than 10 inches. In the B1 PCB designing, only 8mils is used.

Cyclone III device uses a 40MHz internal oscillator to generate DCLK to controls the entire configuration cycle and provide timing for the serial interface.

By driving the nCSO output pin low, which connect to nCS pin of the configuration device, the Cyclone III device enables the configuration device. DCLK and DATA [1] pins are used to send operation commands and read address signals to the serial configuration device. The configuration device sends data on DATA pin which connects to the DATA [0] pin of the Cyclone III device. After all the configuration bits are received, cyclone III releases the open-drain CONF_DONE pin with a 10-$K\Omega$ pull-up resistor. The CONF_DONE pin must have an external 10-$K\Omega$ resistor for the device to initialize.

2. Serial Configuration Device

Cyclone III FPGAs are programmable logic devices used for basic logic functions, chip-to-chip connectivity, signal processing, and embedded processing. They can be programmed and configured by a microprocessor, JTAG port, or directly bay a serial PROM or flash. Spansion SPI (Serial Peripheral Interface) flash S25FL064K can configure the FPGA easily at power-up. [2] (SPANSION, Connecting Spansion SPI Serial Flash to Configure Altera FPGAs, revision 4, November 16, 2011).

The three stages of the configuration cycle are power-on reset, configuration, and initialization. When the FPGA enters power-on rest (POR), it drives the nSTATUS signal low to indicate it is busy, drives the CONF_DONE signal low to indicate the configuration has not been completed, and tri-states all I/O pins. All pins will be released after POR.

The DCLK generated by the FPGA device control the configuration data transferring. The CONF_DONE pin will be released with pulling high by an external pull-up resistor after all configuration data is transferred to the FPGA. The FPGA enters user mode after internal initialization.

The SPI is a simple four-pin synchronous interface protocol which enables a master device and one or more slave devices to intercommunicate. Four signal wires are:
-Master Out Slave In (MOSI) signal generated by the master (data to slave)
-Master In Slave Out (MISO) signal generated by the slave (data to master)
-Serial Clock (SCK) signal generated by the master to synchronize data transfers
- Slave Select (SS) signal generated by master to select individual slave devices (also known as Chip Select (CS) or Chip Enable (CE))

Figure 3 displays a simple block diagram of the connection between FPGA and SPI flash, as well as the HSMC header and JTAG programming the SPI flash from a host PC.

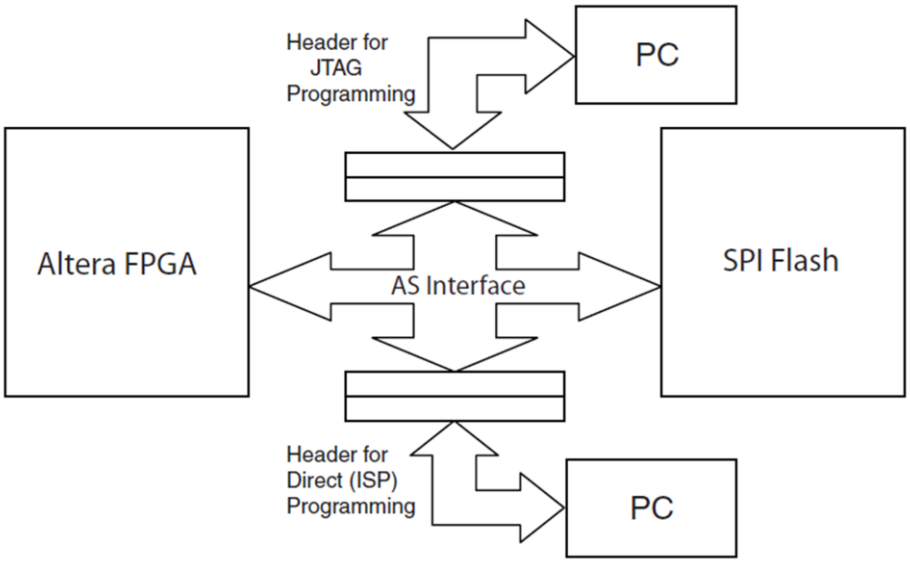


Figure 3

Figure 4 displays the details of the connection between SPI flash and FPGA. According to the introduction of Cyclone III, we can acquire the whole routing of FPGA, SPI flash and the HSMC header (A Samtec ASP header will be introduced later).

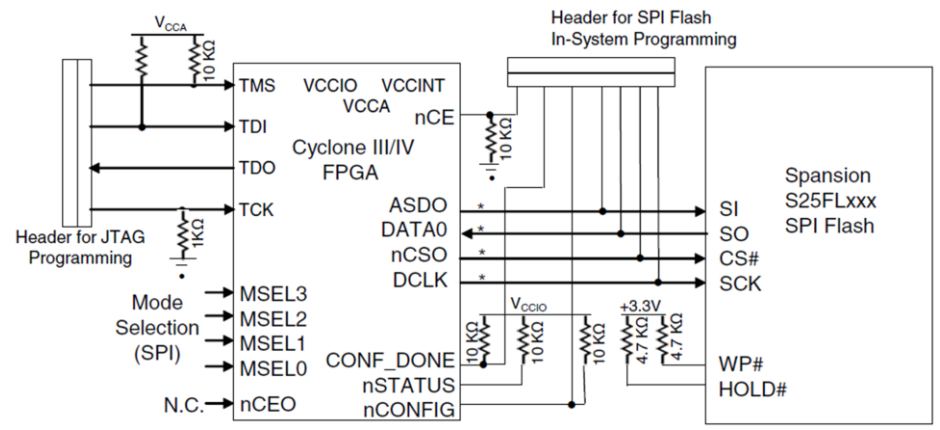


Figure 4

The TMS, TDI, TDO and TCK pins of Cyclone III device are used to operating in the IEEE Std. 1149.1 BST. The TDO pin is powered by VCCIO (3.3V). TDI and TMS are powered by VCCA (2.5V).

The header for JTAG and the header for SPI Flash In-system is use the same HSMC header with 172 pins which is quite enough for these two headers.

3. External Oscillator

As mentioned in the Cyclone III part, an external oscillator is needed as the clock source to provide certain frequency for the FPGA. A 50MHz oscillator of TXC will be implemented. The typical clock frequency for Cyclone III device is 30HMz and the maximum is 40MHz. The TXC DEL04 oscillator is a sealed clock crystal oscillator unit with high precision characteristic covering up to wide frequency range (1 to 170 MHz), which is appropriate for the FPGA. The supply voltage range is 1.8V ~5V. [3] (TXC, Oscillators 7 X 5 mm SMD CMOS CXO 7W SERIES, datasheet)

4. Voltage Regulator

The B2 board needs at least three different voltage levels, as mentioned before, VCCIO=3.3V, VCCINT= 1.2V and VCCA=2.5V. The external power source is provided by the main FPGA DE2-115 board at 3.3V. Hence two voltage regulators are used to transfer 3.3V into 1.2V and 2.5V.

- 1.2V Voltage Regulator LD1117

  The LD111712 is a low drop voltage regulator able to provide up to 800mA of output current, available in adjustable version ($V_{REF} = 1.25V$). The device is supplied in DPAK surface mount package optimize the thermal characteristics even offering a relevant space saving effect. A very common 10 μF minimum capacitor is needed for stability. [4] (ST, LD1117xx datasheet, Adjustable and fixed low drop positive voltage regulator, revision 31, 13-Feb-2012)

Figure 5 is the application circuit for 1.2V output.

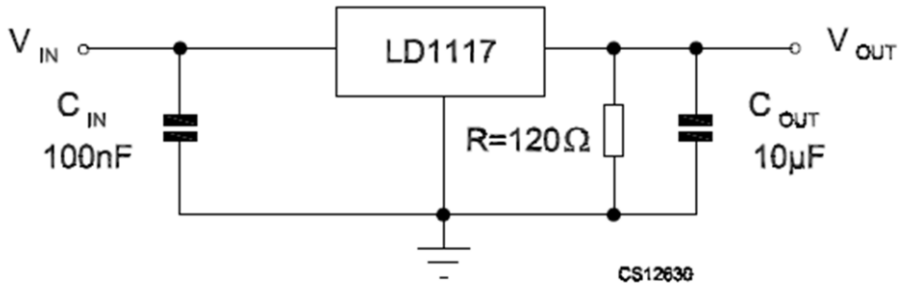


Figure 5

- 2.5 Voltage Regulator TPS78225

The TPS78228 is a low dropout linear voltage regulator designed by TI. The enable pin (EN) is compatible with standard CMOS logic while the low drop output is stable with any capacitor greater than $1\mu F$. The device requires minimal board space for miniaturized packaging and potentially small output capacitor. [5] (TI, TPS782 datasheet, 150mA, Ultra-low Quiescent Current, Low-Dropout Linear Regulator, 2008.9)

The enable pin is active high and is compatible with standard and low-voltage CMOS levels. Therefore if the shutdown capacitor is not necessary, enable pin can connect to the IN pin as shown on Figure 6.

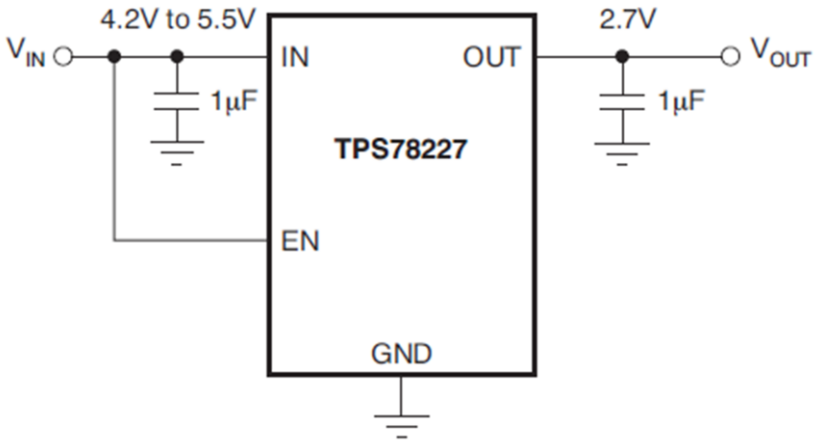


Figure 6

Both current for voltage regulators are linear. They maintain when the toggle rate is changed. For example, 0.352A at 1.2V are still 0.352A at 3.3V.

5. HSMC Header

The Altera High Speed Mezzanine Card (HSMC) specification defines the electrical and mechanical properties of the HSMC adapter inter face for FPGA-based motherboards. The

HSMC connector is based on the Samtec 0.5mm pitch, surface-mount QTH/QSH family of connectors. [6] (ALTERA, High Speed Mezzanine Card specification, revision 17, 2009.6). Two versions can are used in FPGA board. ASP-122953-01 Socket for the host boards and ASP-122952-01 Header for Mezzanine Cards (slave boards).

Figure 7 is the diagram for HSMC header. The clock-data-recovery differential signals in Bank 1 are the highest frequency signals. Signals between the HSMC connector and the host board FPGA device are intended to be D/C coupled. The JTAG, a system management bus (SMBus), and clock signals are also dedicated in Bank 1. In banks 2 and Bank 3, there are main CMOS/LVDS interface signals, including LVDS/COMS clocks, as well as both 12-V and 3.3-V power pins.

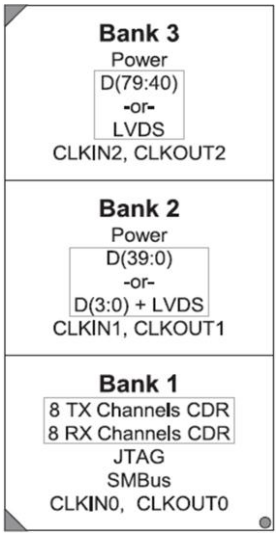


Figure 7

The host board is any board with an FPGA connected to one or more HSMC interface. In this project it is DE2-115 developed board. The interconnect I/O pins available on the HSMC connector can have all possible I/O standard and logic features that can be supported by the host FPGA since FPGAs are configurable devices. However basically they are limited by the wire types on the board.

The HSMC connectors provided the interface between host and slave boards. The ‘header’ part (ASP-122952-01) on slave board plugs into the ‘socket’ part on the host board. The host board provides +12V DC and +3.3V DC power to the slave board via the HSMC connector. In addition to power and clock signals, the host board provides access to JTAG, high speed serial I/O, and single-ended or differential I/O via the HSMC connector.

The HSMC connector has a total of 172 pins, including 121 signal pins (120 signal pins + 1 PSNTn pin), 39 power pins, and 12 ground pins. The ground pins are much larger than the power pins and are located between the two rows of signal and power pins. Figure 8 is the modules for HSMC connectors.

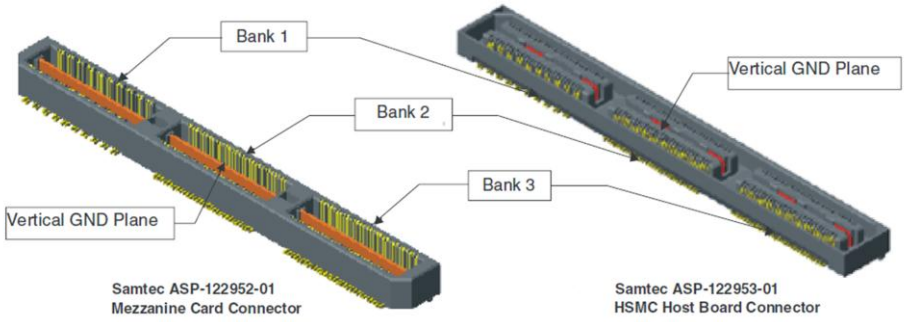


Figure 8

The ASP-122952-01 header provides 160 total pins and 12 ground plane connection pins down the center. Bank1 has 40 pins with every third pin removed. Bank 2 and 3 have 60 pins each as no pins are removed. Host boards provide transceivers to Bank 1 which is not used in this project. Single-ended signals are provided to Bank 2 and 3. Typically, the single-ended signals are capable of differential signalling such as LVDS.

The JTAG signals are intended to connect to dedicated JTAG pins on the host FPGA and be part of the JTAG chain. The JTAG signals TCK, TMS and TDI are intended to be output from host board while JTAG TDO should be the input to host board as Figure 4 before.

Appendix

Table 1 is the pin-outs for the HSMC header on B1 board.

Pin Number	Pin Name
39	ENCODE
48	A0
50	A1
54	A2
56	A3
60	A4
62	A5
66	A6
68	A7
72	A8
74	A9
78	A10
80	A11
96	A12
98	A13
102	A14
104	A15
108	A16
110	A17
114	A18
116	A19
120	A20
122	A21
126	A22
128	A23
132	Q0
134	Q1
138	Q2
140	Q3
144	Q4
146	Q5
150	Q6
152	Q7
156	Q8
158	Q9
157	Q10
155	Q11
151	D0
149	D1
145	D2
143	D3
139	D4
137	D5
133	D6
131	D7
127	Q12
125	Q13
121	Q14
119	Q15

115	Q16
113	Q17
109	Q18
107	Q19
103	Q20
101	Q21
97	Q22
95	Q23
91	SEL1
89	SEL2
85	SEL3
83	SEL4
79	PWRDWN
45	VCCIO
51	VCCIO
57	VCCIO
63	VCCIO
69	VCCIO
75	VCCIO
81	VCCIO
87	VCCIO
93	VCCIO
99	VCCIO
105	VCCIO
111	VCCIO
117	VCCIO
123	VCCIO
129	VCCIO
135	VCCIO
141	VCCIO
147	VCCIO
153	VCCIO
159	VCCIO
161	GND
162	GND
163	GND
164	GND
165	GND
166	GND
167	GND
168	GND
169	GND
170	GND
171	GND
172	GND

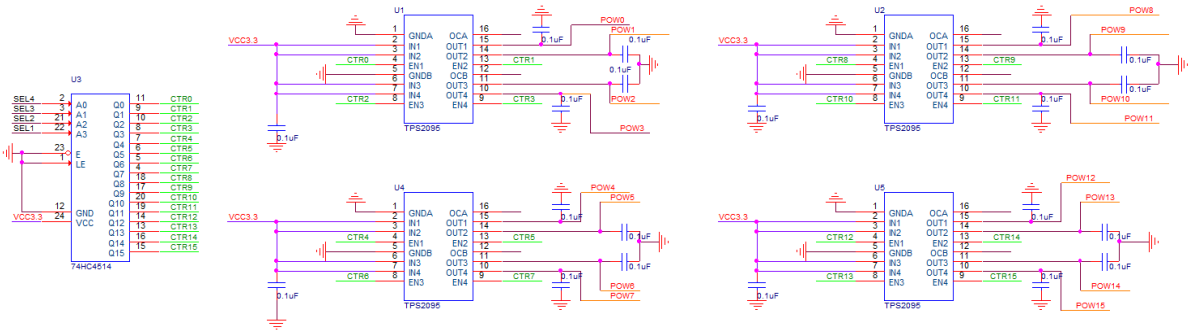
Table 2 is the pin-outs for the HSMC header on B2 board.

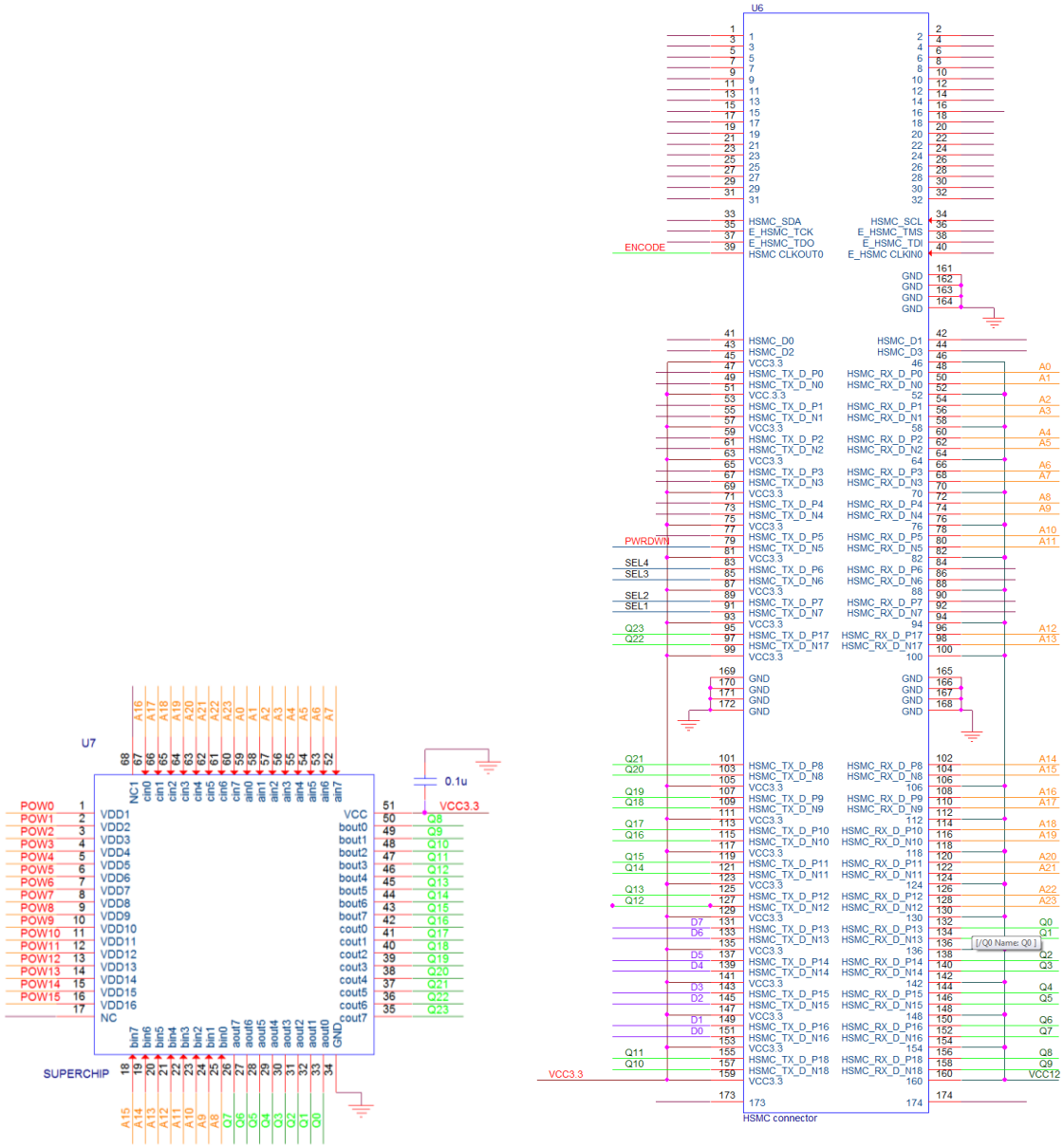
Pin Number	Pin Name
35	TCK
36	TMS

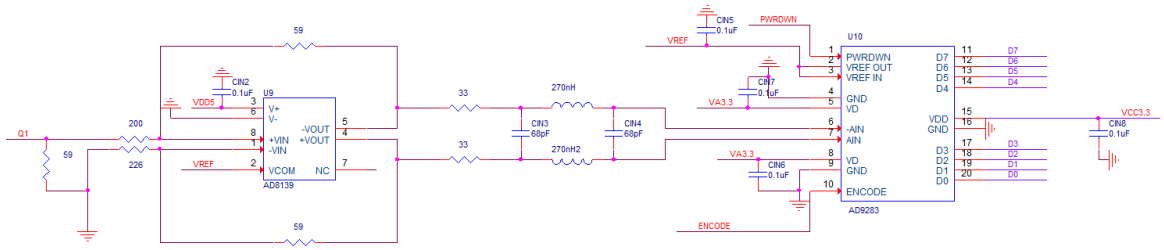
37	TDO
38	TDI
39	Ded_Clock
41	CONF_DONE
42	nSTATUS
43	nCONFIG
44	nCE
48	IO1
50	IO2
54	IO3
56	IO4
60	IO5
62	IO6
66	IO7
68	IO8
72	IO9
74	IO10
78	IO11
80	IO12
84	MOSI
86	MISO
90	nCS
92	SCK
96	IO13
98	IO14
102	IO15
104	IO16
108	IO17
110	IO18
114	IO19
116	IO20
120	IO21
122	IO22
126	IO23
128	IO24
132	IO25
134	IO26
138	IO27
140	IO28
144	IO29
146	IO30
150	IO31
152	IO32
156	IO33
158	IO34
157	IO35
155	IO36
151	IO37
149	IO38
145	IO39
143	IO40
139	IO41
137	IO42

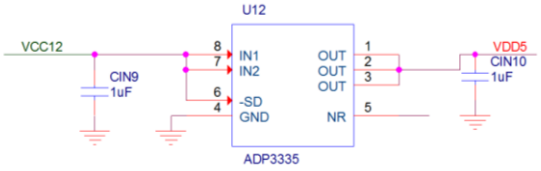
133	IO43
131	IO44
127	IO45
125	IO46
121	IO47
119	IO48
115	IO49
113	IO50
109	IO51
107	IO52
103	IO53
101	IO54
97	IO55
95	IO56
91	IO57
89	IO58
85	IO59
83	IO60
79	IO61
77	IO62
73	IO63
45	VCCIO
51	VCCIO
57	VCCIO
63	VCCIO
69	VCCIO
75	VCCIO
81	VCCIO
87	VCCIO
93	VCCIO
99	VCCIO
105	VCCIO
111	VCCIO
117	VCCIO
123	VCCIO
129	VCCIO
135	VCCIO
141	VCCIO
147	VCCIO
153	VCCIO
159	VCCIO
161	GND
162	GND
163	GND
164	GND
165	GND
166	GND
167	GND
168	GND
169	GND
170	GND
171	GND
172	GND

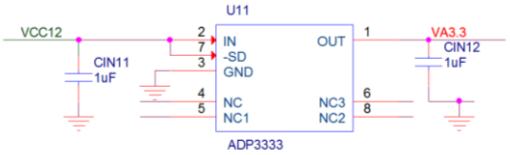
3. Schematic and PCB for B1

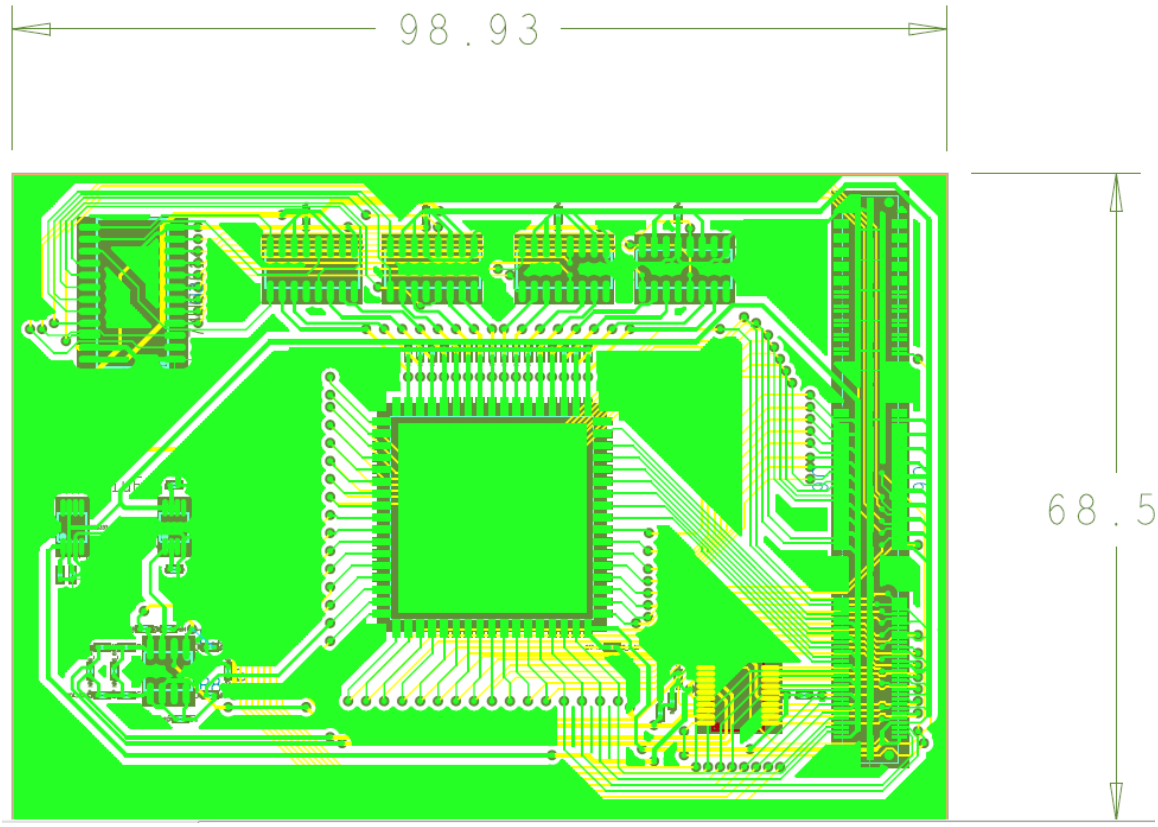




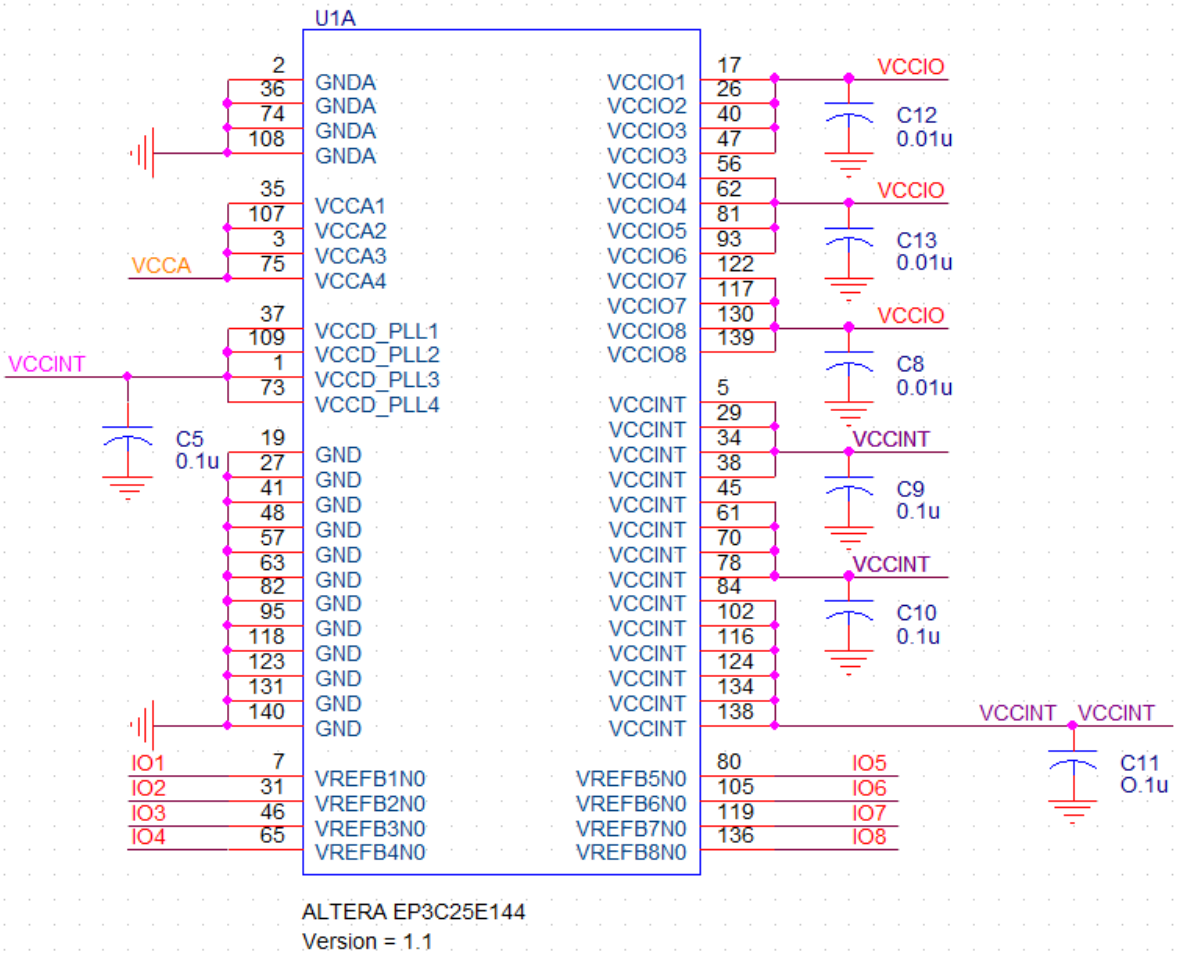


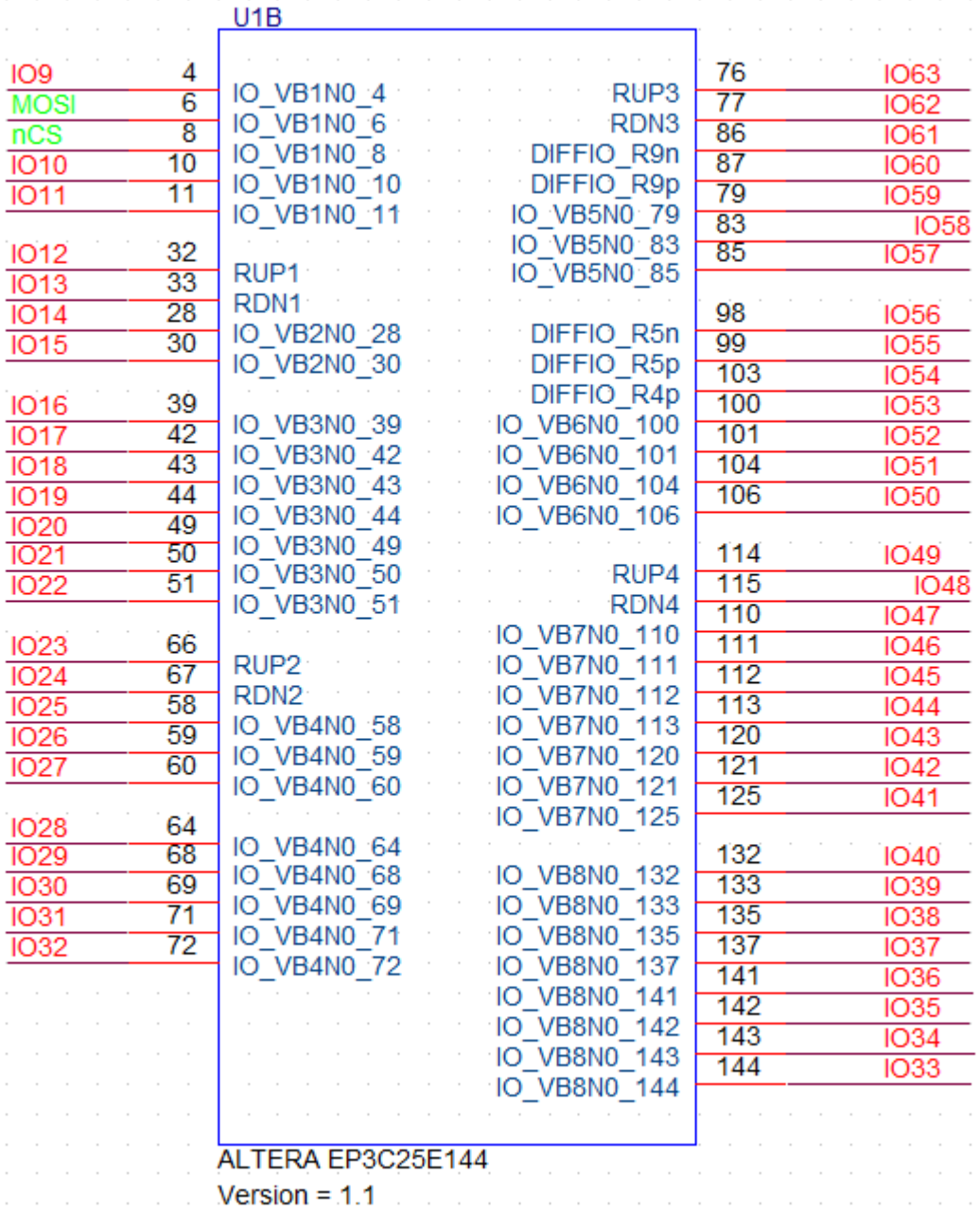


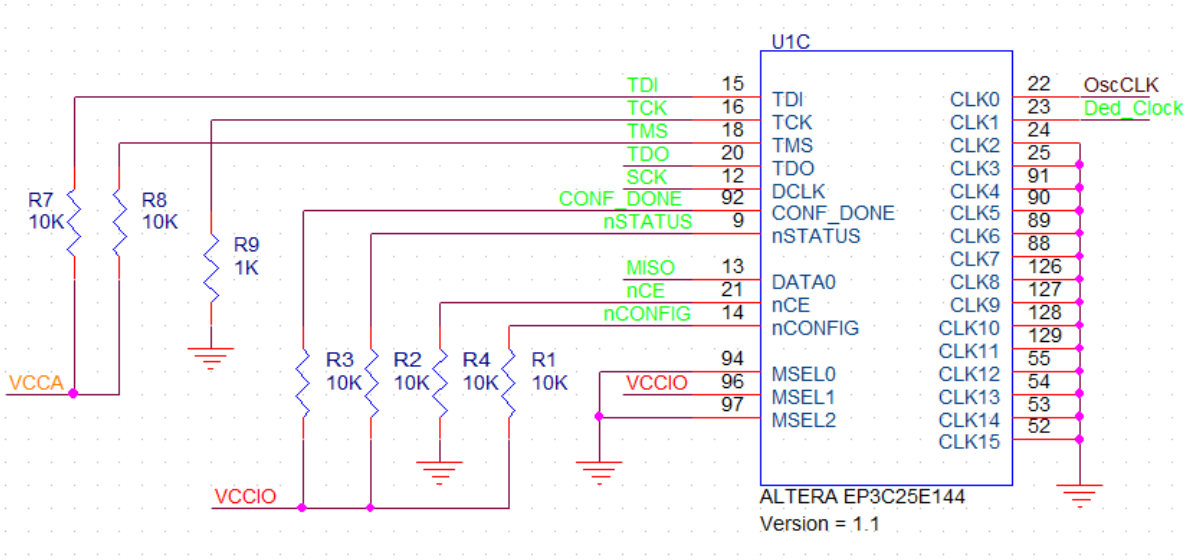


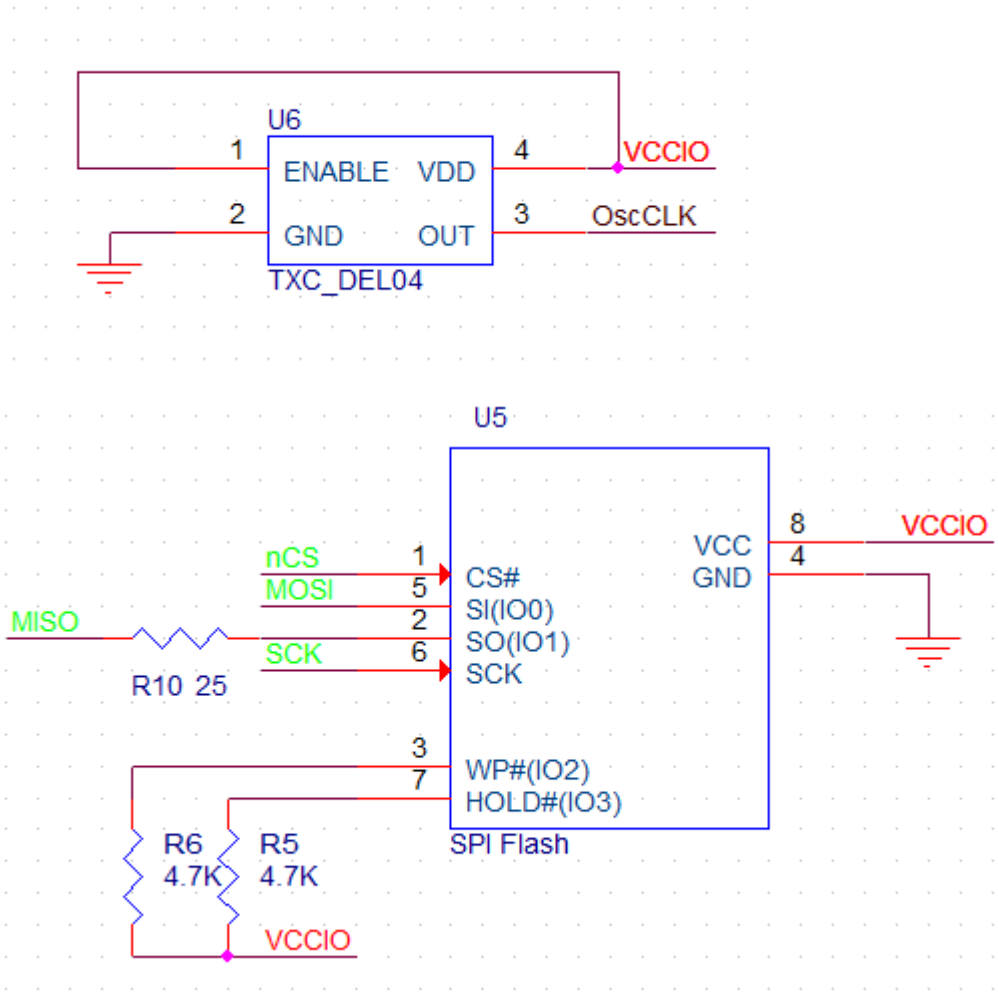


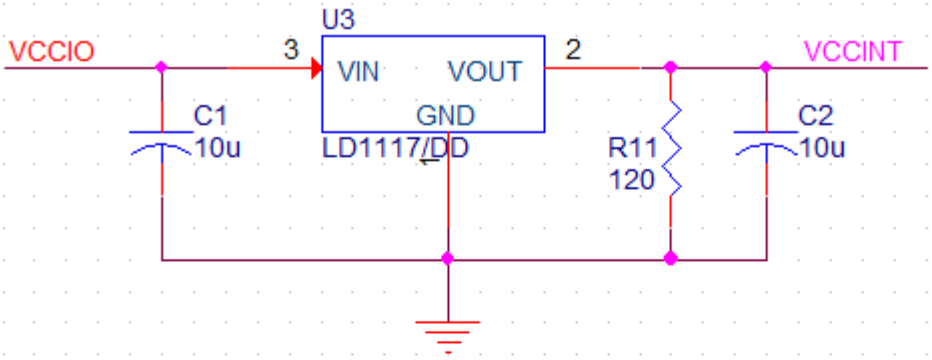
4. Schematic and PCB for B2

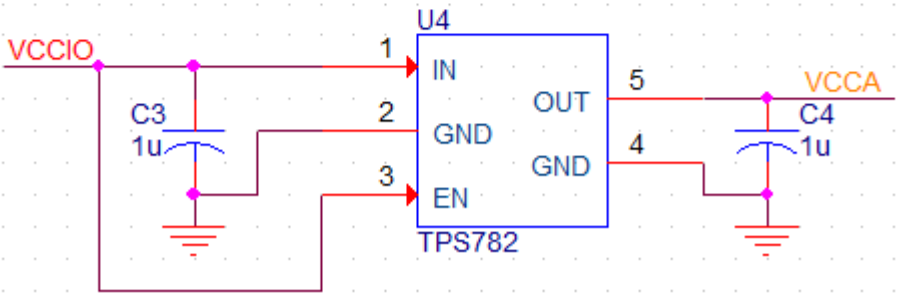

U1A
2
36
74
108
GNDA
GNDA
GNDA
GNDA
35
107
3
75
VCCA1
VCCA2
VCCA3
VCCA4
VCCA
37
109
1
73
VCCD_PLL1
VCCD_PLL2
VCCD_PLL3
VCCD_PLL4
VCCINT
C5
0.1u
19
27
41
48
57
63
82
95
118
123
131
140
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
IO1
IO2
IO3
IO4
7
31
46
65
VREFB1N0
VREFB2N0
VREFB3N0
VREFB4N0
VCCIO1
VCCIO2
VCCIO3
VCCIO3
VCCIO4
VCCIO4
VCCIO5
VCCIO6
VCCIO7
VCCIO7
VCCIO8
VCCIO8
VCCINT
VCCINT
VCCINT
VCCINT
VCCINT
VCCINT
VCCINT
VCCINT
VCCINT
VCCINT
VCCINT
VCCINT
VREFB5N0
VREFB6N0
VREFB7N0
VREFB8N0
17
26
40
47
56
62
81
93
122
117
130
139
5
29
34
38
45
61
70
78
84
102
116
124
134
138
80
105
119
136
IO5
IO6
IO7
IO8
VCCIO
C12
0.01u
VCCIO
C13
0.01u
VCCIO
C8
0.01u
VCCINT
C9
0.1u
VCCINT
C10
0.1u
VCCINT
VCCINT
C11
O.1u
ALTERA EP3C25E144
Version = 1.1

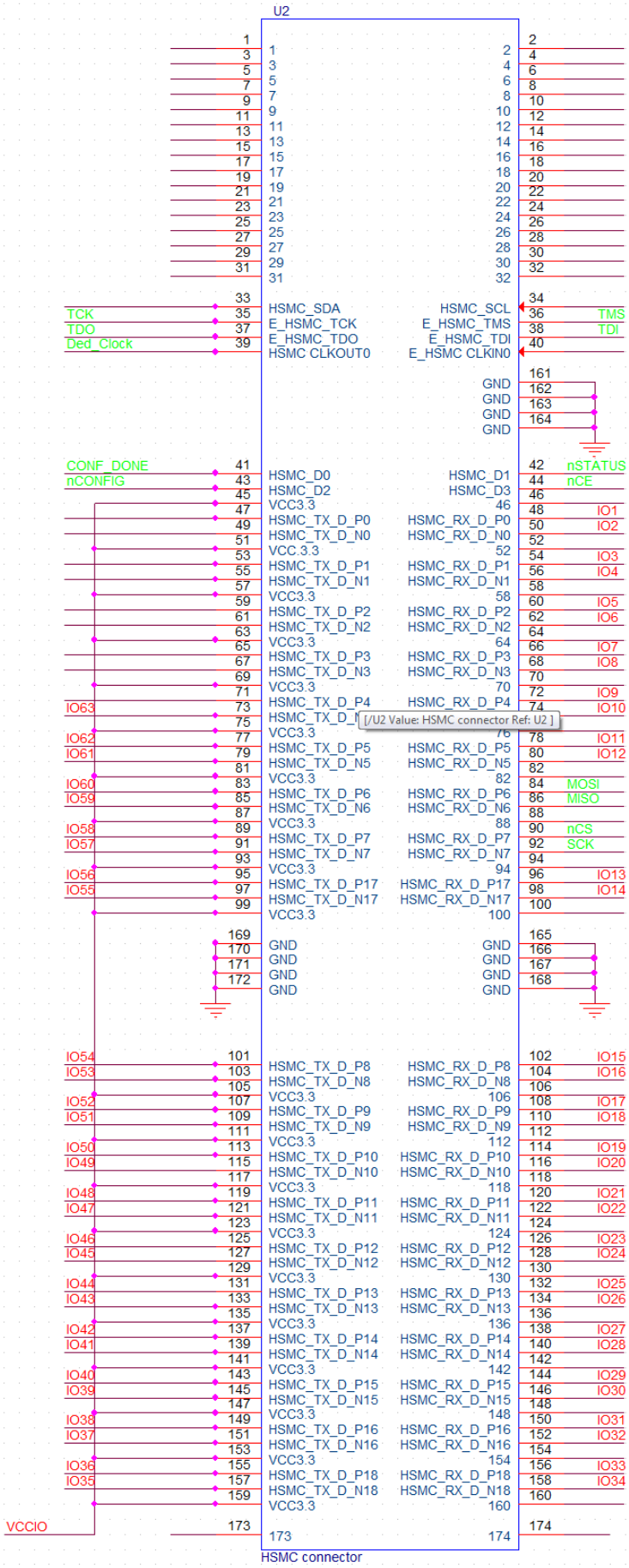

U1B
IO9 4
MOSI 6
nCS 8
IO10 10
IO11 11
IO12 32
IO13 33
IO14 28
IO15 30
IO16 39
IO17 42
IO18 43
IO19 44
IO20 49
IO21 50
IO22 51
IO23 66
IO24 67
IO25 58
IO26 59
IO27 60
IO28 64
IO29 68
IO30 69
IO31 71
IO32 72
IO_VB1N0_4
IO_VB1N0_6
IO_VB1N0_8
IO_VB1N0_10
IO_VB1N0_11
RUP1
RDN1
IO_VB2N0_28
IO_VB2N0_30
IO_VB3N0_39
IO_VB3N0_42
IO_VB3N0_43
IO_VB3N0_44
IO_VB3N0_49
IO_VB3N0_50
IO_VB3N0_51
RUP2
RDN2
IO_VB4N0_58
IO_VB4N0_59
IO_VB4N0_60
IO_VB4N0_64
IO_VB4N0_68
IO_VB4N0_69
IO_VB4N0_71
IO_VB4N0_72
RUP3
RDN3
DIFFIO_R9n
DIFFIO_R9p
IO_VB5N0_79
IO_VB5N0_83
IO_VB5N0_85
DIFFIO_R5n
DIFFIO_R5p
DIFFIO_R4p
IO_VB6N0_100
IO_VB6N0_101
IO_VB6N0_104
IO_VB6N0_106
RUP4
RDN4
IO_VB7N0_110
IO_VB7N0_111
IO_VB7N0_112
IO_VB7N0_113
IO_VB7N0_120
IO_VB7N0_121
IO_VB7N0_125
IO_VB8N0_132
IO_VB8N0_133
IO_VB8N0_135
IO_VB8N0_137
IO_VB8N0_141
IO_VB8N0_142
IO_VB8N0_143
IO_VB8N0_144
76 IO63
77 IO62
86 IO61
87 IO60
79 IO59
83 IO58
85 IO57
98 IO56
99 IO55
103 IO54
100 IO53
101 IO52
104 IO51
106 IO50
114 IO49
115 IO48
110 IO47
111 IO46
112 IO45
113 IO44
120 IO43
121 IO42
125 IO41
132 IO40
133 IO39
135 IO38
137 IO37
141 IO36
142 IO35
143 IO34
144 IO33
ALTERA EP3C25E144
Version = 1.1

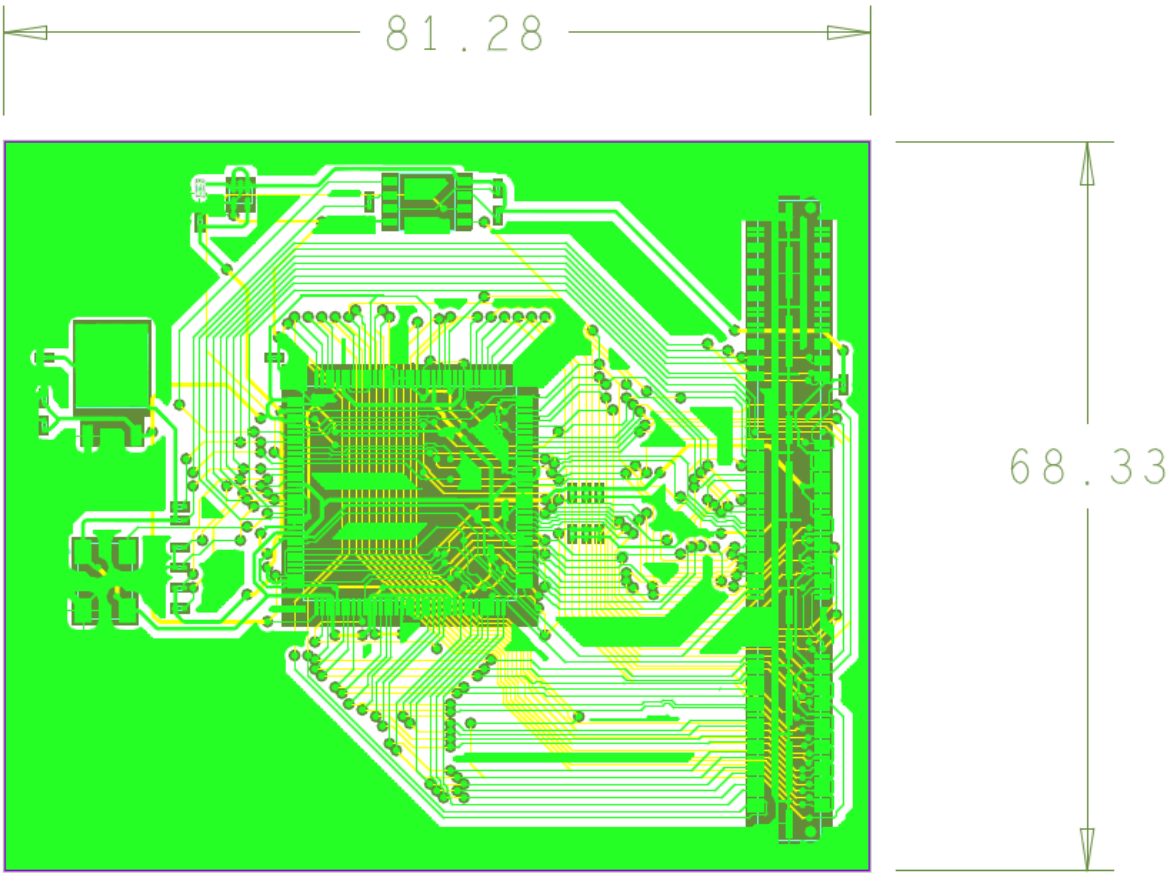

U1C
TDI
TCK
TMS
TDO
SCK
CONF_DONE
nSTATUS
MISO
nCE
nCONFIG
MSEL0
MSEL1
MSEL2
15
16
18
20
12
92
9
13
21
14
94
96
97
TDI
TCK
TMS
TDO
DCLK
CONF_DONE
nSTATUS
DATA0
nCE
nCONFIG
MSEL0
MSEL1
MSEL2
CLK0
CLK1
CLK2
CLK3
CLK4
CLK5
CLK6
CLK7
CLK8
CLK9
CLK10
CLK11
CLK12
CLK13
CLK14
CLK15
22
23
24
25
91
90
89
88
126
127
128
129
55
54
53
52
OscCLK
Ded_Clock
R7
10K
R8
10K
R9
1K
R3
10K
R2
10K
R4
10K
R1
10K
VCCA
VCCIO
VCCIO
ALTERA EP3C25E144
Version = 1.1


U6
1
ENABLE
VDD
4
VCCIO
2
GND
OUT
3
OscCLK
TXC_DEL04
U5
nCS
1
CS#
MOSI
5
SI(IO0)
MISO
2
SO(IO1)
SCK
6
SCK
R10 25
VCC
8
VCCIO
GND
4
3
WP#(IO2)
7
HOLD#(IO3)
R6
4.7K
R5
4.7K
SPI Flash
VCCIO


U3
VCCIO
3
VIN
VOUT
2
VCCINT
C1
10u
GND
LD1117/DD
R11
120
C2
10u


U4
VCCIO
1
IN
OUT
5
VCCA
C3
1u
2
GND
C4
1u
4
GND
3
EN
TPS782


U2
HSMC connector
HSMC_SDA
HSMC_SCL
E_HSMC_TCK
E_HSMC_TMS
E_HSMC_TDO
E_HSMC_TDI
HSMC CLKOUT0
E_HSMC CLKIN0
TCK
TDO
Ded_Clock
TMS
TDI
GND
VCC3.3
VCC.3.3
HSMC_D0
HSMC_D1
HSMC_D2
HSMC_D3
CONF_DONE
nCONFIG
nSTATUS
nCE
HSMC_TX_D_P0
HSMC_RX_D_P0
HSMC_TX_D_N0
HSMC_RX_D_N0
HSMC_TX_D_P1
HSMC_RX_D_P1
HSMC_TX_D_N1
HSMC_RX_D_N1
HSMC_TX_D_P2
HSMC_RX_D_P2
HSMC_TX_D_N2
HSMC_RX_D_N2
HSMC_TX_D_P3
HSMC_RX_D_P3
HSMC_TX_D_N3
HSMC_RX_D_N3
HSMC_TX_D_P4
HSMC_RX_D_P4
HSMC_TX_D_P5
HSMC_RX_D_P5
HSMC_TX_D_N5
HSMC_RX_D_N5
HSMC_TX_D_P6
HSMC_RX_D_P6
HSMC_TX_D_N6
HSMC_RX_D_N6
HSMC_TX_D_P7
HSMC_RX_D_P7
HSMC_TX_D_N7
HSMC_RX_D_N7
HSMC_TX_D_P17
HSMC_RX_D_P17
HSMC_TX_D_N17
HSMC_RX_D_N17
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
IO10
IO11
IO12
IO13
IO14
IO15
IO16
IO17
IO18
IO19
IO20
IO21
IO22
IO23
IO24
IO25
IO26
IO27
IO28
IO29
IO30
IO31
IO32
IO33
IO34
IO35
IO36
IO37
IO38
IO39
IO40
IO41
IO42
IO43
IO44
IO45
IO46
IO47
IO48
IO49
IO50
IO51
IO52
IO53
IO54
IO55
IO56
IO57
IO58
IO59
IO60
IO61
IO62
IO63
MOSI
MISO
nCS
SCK
VCCIO
[/U2 Value: HSMC connector Ref: U2]


81.28
68.33