

UNIVERSITY OF SOUTHAMPTON
Faculty of Engineering, Science and Mathematics

A group design project report submitted for the award of
Master of Engineering

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Examiner:

ELEC6027 VLSI Group Design Project
Team I
Southampton Superchip Automated Tester
by

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UNIVERSITY OF SOUTHAMPTON

ABSTRACT

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List of Symbols

w The weight vector

Acknowledgements

Thanks to no one.

To ...

Chapter 1

Introduction

1.1 Aim and Background

Nano (get started)

mention: D2, Superchip, stuff

1.2 DE2 Board Overview

Nano (get started)

1.3 System Overview

Pavlos (get started)

see slides

Chapter 2

Hardware

2.1 Hardware Overview

The hardware part consists of two main blocks: NIOS System on Programmable Controller and the Tester.

The *NIOS SoPC* coordinates the whole system, writing the data from SD Card into the SRAM for the Tester to read the data from it; retrieving the result that the Tester writes

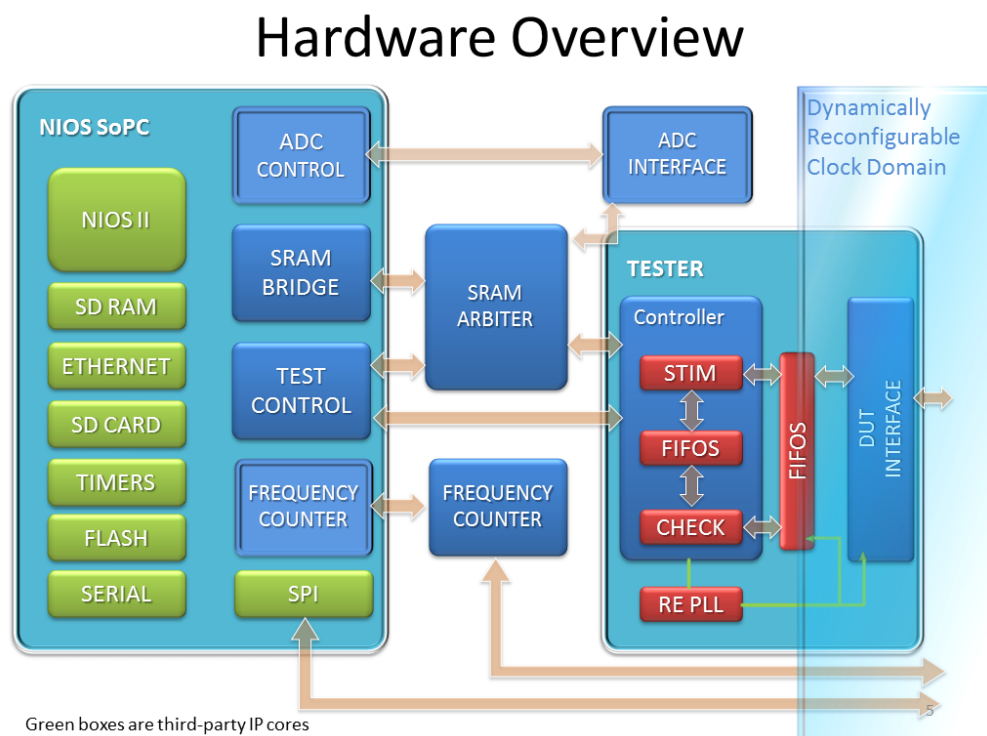


FIGURE 2.1: Hardware Overview.

back to the SRAM and sending the data to the backend for archiving and reviewing for the users. Its tasks include:

- coordinate the data from multiple sources (SRAM, SD Card, Flash, Serial connection, SPI bus, Ethernet, etc.)
- control the testing process (which is executed by the Tester, frequency counter and ADC)
- send results to the backend
- user interface

The *SRAM arbiter* is the interface between the SoPC, tester and the SRAM by Avalon Memory Mapped Interface (Avalon-MM). It handles the SRAM read and write requests from SoPC and tester.

The *Tester* contains several HDL blocks which are responsible for the testing process.

- read the command, request and test vector from SRAM
- generate the test input signals for every pin of the DUT
- monitor the output pins of the DUT and write the result into the memory when the it is valid
- offer a dynamically reconfigurable clock for the DUT and its relative interface

The purpose of the *frequency counter* and the *ADC* is that there is a designated pin on the chip which is the output of a ring oscillator. It is preferable that not only the frequency of this clock output is tested, but that the output waveform is also monitored.

2.2 PCB (interface board)

For the chip tester, two PCBs are needed in this project. One which is called *B2* has been designed for the virtual designs to be loaded in a slave FPGA. The other is called *B1* that is developed as an interface for those real chips are about to be tested. Both PCBs are two layers board and designed by using Allegro 16.3 PCB designer tools. The dimensions of *B1* and *B2* are $98.93mm * 68.5mm$ and $81.28mm * 68.33mm$ and the minimum wire size is $8mm$.

2.2.1 B1 (DUT testing board)

2.2.1.1 DUT

The superchip under test has the following specific features:

- 6 separate design sites
- 24 digital input pins [$A0 \dots A23$], shared between all design sites;
- 4 digital output pins [$Q0 \dots Q23$], shared between all design sites;
- 16 separate VDD pins, one dedicated to each design site;
- 1 global GND pin for all design sites and infrastructure circuitry;
- 1 global VDD pin to power the site buffers and I/O pad ring;
- 68-pin JLCC package (with 2 unused pins).

The chip is interfaced with the PCB by a 68WAY PLCC socket. The power is supplied by the 3.3V VDD from the DE2 board. The GND is also connected to the DE2 GND.

The shared I/Os are connected to the powered design site, and disconnected from the other design sites. Hence a controllable power switch is designed with a 4-16 decoder and an integrated power switch array. The $Q1$ is the output of a ring oscillator. The frequency can be digitally tested by the general I/O. However, to examine the analog properties of this output, an analog part including a buffer, 3rd order Butterworth filter and ADC with their own power supply is also designed.

2.2.1.2 Digital Part

Decoder Although there are 16 design sites to be selected, the data can be shrunk down to 4 bits to save space of the test vector and metadata, since only one site is selected at a time. The decoder we used is 74HC4514, a 4 – to – 16 line decoder with latch. The input and output are active high.

Switch Array The switch array consists of four *TPS2095* quad power-distribution switches. One could simply use a CMOS to realize a switch. However, with thermal sense, current limit and charge pump, the *TPS2095* switches are more reliable, stable, smooth (minimum switching current surges) and relatively compact in scale. The operation of a switch is simple: when EN pin is asserted, the OUT pin offers the power with the same voltage in the IN pin. Otherwise the OUT pin is disconnected from the input power. In one *TPS2095* chip there are 4 such switches, the EN pins of which are all active high.

2.2.2 B2 (Virtual design board)

2.2.2.1 Slave FPGA

Slave FPGA is the core chip of the virtual design board. It can be used for programming designs when they are going to be tested. An Altera Cyclone III FPGA will be implemented as the slave FPGA.

Cyclone III (*EP3C25E144*) belongs to Cyclone III device family. With densities ranging from about 5,000 to 200,000 logic elements (LEs) and 0.5Mb to 8Mb of memory for less than $\frac{1}{4}V$ of static power consumption, Cyclone III devices makes it easier to meet the power budget ([Altera Corporation, 2011](#)).

The reason for choosing Cyclone III is their lowest power, high functionality with the lowest cost. 144 pins are enough for this design. I/O pins on the Cyclone III are grouped together into I/O banks, and each bank has a separate power bus. There are eight I/O banks, as shown in [Figure 1](#) ([Altera Corporation, 2011](#)). All single-ended I/O standards are supported in all banks except HSTL-12 Class II which is only supported in column banks. The same case can be found in all differential I/O standards.

Each I/O banks of Cyclone III has a VREF bus to accommodate voltage-referenced I/O standards. Connect the VREF pin of each group to the appropriate voltage. In this design three voltage levels, which $VCCIO = 3.3V$, $VCCINT = 1.2V$ and $VCCA = 2.5V$, are necessary. Proper bypassing and decoupling technique for the power pins is very important for reliable design operation. In this case, additional decoupling capacitance is needed. The VCCINT, VCCIO and ground pins should add as many as $0.2\mu F$ power-supply decoupling capacitors as possible. So $0.01\mu F$ capacitor for VCCIO and $0.1\mu F$ for VCCINT seems to be appropriate. Note that all the capacitors should be place close enough to the power pins.

In regard of the Cyclone III configuration, the Cyclone II device uses SRAM cells to store configuration data. *EP3C25E144* can only be configured in Fast Active serial (AS) mode.

Configuration data is loaded into Cyclone III at each DCLK cycle. As soon as the device receives all data, the device releases the open-drain CONF_DONE pin, which is pulled high by an external 10k pull-up resistor. The CONF_DONE pin transits low-to-high to indicate that configuration is complete and initialization of the device can begin. The CONF_DONE pin must have a 10k pull-up resistor for initialization.

Pulling the nCONFIG pin low can begin reconfiguration and this pin must be low for at least $500ns$. The Cyclone III device is reset when nCONFIG is pulled low. Meanwhile, the device will pull nSTATUS and CONF_DONE low and I/O pins are tri-stated. When nCONFIG returns to high and nSTATUS is released, reconfiguration begins.

The clock source for initialization is either a $10MHz$ (typical) internal oscillator or an optional CLK pin. In this situation, an external oscillator (A $TXC-50MHz$ oscillator is going to be introduced later) will be implemented as the clock source. The required clock for initialization in Cyclone III is 3,185 and the maximum CLK frequency is $133MHz$.

The configuration mode is selected by driving the MSEL pins either low or high. The MSEL pins can be powered by VCCIO and GND. For AS mode, MSEL [1] should be pulled up by connecting to VCCIO. MSEL [0] and MSEL [2] are pulled down by connecting to GND. The MSEL pins have 9 internal pull-down resistors that are always active.

The maximum active master frequency for Cyclone III is $30MHz$ typically and device only work with serial configuration devices that support up to $40MHz$.

In AS mode, Cyclone III reads the configuration data providing by serial configuration (A Spansion SPI Flash is going to be introduced later) via a serial interface. The serial configuration device controls the configuration interface.

There are four pins on the serial configuration devices:

- Serial clock input (DCLK)
- serial data output (DATA)
- As data output (ASDI)
- Active-low chip select (nCS)

Connect these four pins to Cyclone III device pins, as shown in **Figure 2.**

A 25Ω series resistor must connect a between serial configuration device and the Cyclone III device at the near end of the serial configuration device for DATA [0] when configure the Cyclone III device in the AS mode. The 25Ω resistor works to minimize the driver impedance mismatch with the board trace and reduce the overshoot seen at the Cyclone III device input pin DATA [0].

The maximum trace length between Cyclone III device and the serial configuration device, in another words, the CLK, DATA [0], NCSO and ADSO pins, must less than $10in$. In the B1 PCB designing, only $8mm$ is used.

Cyclone III device uses a $40MHz$ internal oscillator to generate DCLK to controls the entire configuration cycle and provide timing for the serial interface.

By driving the nCSO output pin low, which connect to nCS pin of the configuration device, the Cyclone III device enables the configuration device. DCLK and DATA [1] pins are used to send operation commands and read address signals to the serial configuration device. The configuration device sends data on DATA pin which connects to

the DATA [0] pin of the Cyclone III device. After all the configuration bits are received, cyclone III releases the open-drain CONF_DONE pin with a 10Ω pull-up resistor. The CONF_DONE pin must have an external 10Ω resistor for the device to initialize.

2.2.2.2 Serial Configuration Device

Cyclone III FPGAs are programmable logic devices used for basic logic functions, chip-to-chip connectivity, signal processing, and embedded processing. They can be programmed and configured by a microprocessor, JTAG port, or directly by a serial PROM or flash. Spansion SPI (Serial Peripheral Interface) flash *S25FL064K* can configure the FPGA easily at power-up ([Spansion, 2011](#)).

The three stages of the configuration cycle are power-on reset, configuration, and initialization. When the FPGA enters power-on reset (POR), it drives the nSTATUS signal low to indicate it is busy, drives the CONF_DONE signal low to indicate the configuration has not been completed, and tri-states all I/O pins. All pins will be released after POR.

The DCLK generated by the FPGA device controls the configuration data transferring. The CONF_DONE pin will be released with pulling high by an external pull-up resistor after all configuration data is transferred to the FPGA. The FPGA enters user mode after internal initialization.

The SPI is a simple four-pin synchronous interface protocol which enables a master device and one or more slave devices to intercommunicate. Four signal wires are:

- Master Out Slave In (MOSI) signal generated by the master (data to slave)
- Master In Slave Out (MISO) signal generated by the slave (data to master)
- Serial Clock (SCK) signal generated by the master to synchronize data transfers
- Slave Select (SS) signal generated by master to select individual slave devices (also known as Chip Select (CS) or Chip Enable (CE))

Figure 3 displays a simple block diagram of the connection between FPGA and SPI flash, as well as the HSMC header and JTAG programming the SPI flash from a host PC.

Figure 4 displays the details of the connection between SPI flash and FPGA. According to the introduction of Cyclone III, we can acquire the whole routing of FPGA, SPI flash and the HSMC header (A Samtec ASP header will be introduced later).

The TMS, TDI, TDO and TCK pins of Cyclone III device are used to operating in the IEEE Std. 1149.1 JTAG. The TDO pin is powered by VCCIO (3.3V). TDI and TMS are powered by VCCA (2.5V).

The header for JTAG and the header for SPI Flash In-system is use the same HSMC header with 172 pins which is quite enough for these two headers.

2.2.2.3 External Oscillator

As mentioned in the Cyclone III part, an external oscillator is needed as the clock source to provide certain frequency for the FPGA. A $50MHz$ oscillator of TXC will be implemented. The typical clock frequency for Cyclone III device is $30MHz$ and the maximum is $40MHz$. The TXC DEL04 oscillator is a sealed clock crystal oscillator unit with high precision characteristic covering up to wide frequency range ($1MHz$ to $170MHz$), which is appropriate for the FPGA. The supply voltage range is $1.8V \sim 5V$ (TXC).

2.2.2.4 Voltage Regulator

The B2 board needs at least three different voltage levels, as mentioned before, $VCCIO = 3.3V$, $VCCINT = 1.2V$ and $VCCA = 2.5V$. The external power source is provided by the main FPGA DE2-115 board at $3.3V$. Hence two voltage regulators are used to transfer $3.3V$ into $1.2V$ and $2.5V$.

1.2V Voltage Regulator LD1117 The LD111712 is a low drop voltage regulator able to provide up to $800mA$ of output current, available in adjustable version (). The device is supplied in DPAK surface mount package optimize the thermal characteristics even offering a relevant space saving effect. A very common 10 minimum capacitor is needed for stability (ST Microelectronics, 2012).

Figure 5 is the application circuit for $1.2V$ output.

2.5V Voltage Regulator TPS78225 The TPS78228 is a low dropout linear voltage regulator designed by TI. The enable pin (EN) is compatible with standard CMOS logic while the low drop output is stable with any capacitor greater than 1. The device requires minimal board space for miniaturized packaging and potentially small output capacitor (Texas Instruments, 2008).

The enable pin is active high and is compatible with standard and low-voltage CMOS levels. Therefore if the shutdown capacitor is not necessary, enable pin can connect to the IN pin as shown on Figure 6.

2.2.2.5 HSMC Header

The Altera High Speed Mezzanine Card (HSMC) specification defines the electrical and mechanical properties of the HSMC adapter interface for FPGA-based motherboards. The HSMC connector is based on the Samtec 0.5mm pitch, surface-mount *QTH/QSH* family of connectors ([Altera Corporation, 2009](#)). Two versions can be used in FPGA board. *ASP – 122953 – 01* Socket for the host boards and *ASP – 122952 – 01* Header for Mezzanine Cards (slave boards).

Figure 7 is the diagram for HSMC header. The clock-data-recovery differential signals in Bank 1 are the highest frequency signals. Signals between the HSMC connector and the host board FPGA device are intended to be D/C coupled. The JTAG, a system management bus (SMBus), and clock signals are also dedicated in Bank 1. In banks 2 and Bank 3, there are main CMOS/LVDS interface signals, including LVDS/COMS clocks, as well as both 12V and 3.3V power pins.

The host board is any board with an FPGA connected to one or more HSMC interface. In this project it is *DE2 – 115* development board. The interconnect I/O pins available on the HSMC connector can have all possible I/O standard and logic features that can be supported by the host FPGA since FPGAs are configurable devices. However basically they are limited by the wire types on the board.

The HSMC connectors provided the interface between host and slave boards. The “header” part (*ASP – 122952 – 01*) on slave board plugs into the “socket” part on the host board. The host board provides +12V DC and +3.3V DC power to the slave board via the HSMC connector. In addition to power and clock signals, the host board provides access to JTAG, high speed serial I/O, and single-ended or differential I/O via the HSMC connector.

The HSMC connector has a total of 172 pins, including 121 signal pins (120 signal pins + 1 PSNTn pin), 39 power pins, and 12 ground pins. The ground pins are much larger than the power pins and are located between the two rows of signal and power pins.

Figure 7 is the modules for HSMC connectors.

The *ASP – 122952 – 01* header provides 160 total pins and 12 ground plane connection pins down the center. Bank 1 has 40 pins with every third pin removed. Bank 2 and 3 have 60 pins each as no pins are removed. Host boards provide transceivers to Bank 1 which is not used in this project. Single-ended signals are provided to Bank 2 and 3. Typically, the single-ended signals are capable of differential signalling such as LVDS.

The JTAG signals are intended to connect to dedicated JTAG pins on the host FPGA and be part of the JTAG chain. The JTAG signals TCK, TMS and TDI are intended to be output from host board while JTAG TDO should be the input to host board as **Figure 4** before.

Tables [A.1](#) and [A.2](#) in the appendix show the pin-outs for the HSMC header on B1 and B2 boards, respectively.

2.3 Chip Tester (Verilog Module)

Joey (and a bit Alex)

mention: reconfigurable clock domain, synchronizing DC FIFOs

- test controller
- mem_if
- stim
- check
- dut_if (and its pipeline)
- reconfigurable PLL

2.4 SRAM Arbiter (sram_arb_sync.v)

Pavlos

Chapter 3

SoPC

3.1 Overview

Alex

- Altera-provided Peripherals
- Nios II core
- Avalon-MM bus (at least the signals we use)

3.2 SRAM_bridge

Alex

3.3 test_runner

Alex

3.4 Frequency Counter

3.4.1 Overview and Specification

The frequency counter module of the Superchip tester is connected to the oscillator found in the superchip designs, to measure its output frequency.

According to specification for the academic year 2011 – 12, the ring oscillators found in the teams' superchip designs have a basic frequency of $1MHz$ and an offset frequency of the teams' ID number multiplied by $250kHz$ ([The University of Southampton, 2011](#)). For 16 teams, the frequency range would be $1250kHz - 5000kHz$.

3.4.2 Functionality

Since the clock of the FPGA is significantly faster than the oscillator frequency, the frequency counter designed for this project counts the number of the oscillator signal edges over a given number of FPGA clock cycles. The frequency counter consists of three modules, a $24-to-1$ multiplexer, the measurement module and a control module. When the frequency counter is enabled, the processor provides it with the required number of clock cycles. The counter starts counting the rising edges of the input signal and after it stops counting, once the specified number of clock cycles has been reached, it raises an interrupt signal for the data to be read from the processor. While the active-low *nReset* signal is enabled, the counter ceases all function and all registers and outputs are nulled.

Multiplexer The purpose of the multiplexer is to connect the measurement module to the correct pin of the chip under test, to achieve better reconfigurability. In order to provide compatibility of the design with chips whose oscillator output can be different, the multiplexer is connected to all design outputs and only connects the one specified by the processor to the measurement module.

Measurement Module The measurement module of the frequency counter provides the main functionality of the design, measuring the number of input signal periods over a specified time. This module is provided with the target number of clock cycles and the input signal (to be measured). In order to maintain signal integrity, since the input signal is effectively crossing a clock domain, the design contains a synchroniser stage, to synchronise the input signal with the FPGA clock. When the module is enabled, the edge counter increments its value on every rising edge of the input signal. Once the module has gone through the required clock cycles, it stops counting input signal periods and an *count_overflow* flag is raised.

Control Module The frequency counter control module handles the communication and the input setup data from the processor, as well as the the output data from the measurement module. It provides an Avalon Memory Mapped slave interface for communication with the NIOS II processor as well as an Avalon Interrupt signal interface (*IRQ*) and a *busy* signal.

Before starting the frequency measurement procedure the NIOS core writes data to the frequency counter, to specify parameters such as the duration of the measurement. When the *write* signal in the Avalon interface is active, the register specified on the address bus is written with the data on the data bus.

The internal *enable* signal to start the process is activated by the controller when a dedicated register is written with a unity value and kept high for a single clock cycle. As long as the frequency counter is enabled and counts periods of the input wave, the controller keeps the *busy* signal high to inform the NIOS II core that it is processing.

The data stored on the registers of the controller are kept steady and provided to the other modules of the frequency counter. Once the measurement module is done and the *done* flag is enabled, the controller stores the count value to the relevant register and raises the *irq* signal to the processor.

Following an interrupt request, the processor starts reading values from the registers of the frequency counter module. When the *read* signal in the Avalon interface is active, the module outputs the data on the register specified on the address bus to the processor. Meanwhile, when data is read from the registers, the *readdatavalid* signal is high as well. When the data contained in the registers is read after a calculation procedure and an interrupt request to the processor, the *irq* signal is cleared.

3.5 ADC

The ADC interface provides an Avalon MM interface, with the same input and output signalling as the frequency counter. Reading from and writing to the registers involves the same signals as the ones discussed in the frequency counter.

Chapter 4

Embedded Software

4.1 Bootloader and Operating System

Alex

- u-boot
- uClinux (w Linux 3.3)

4.2 Drivers

Alex

- fcounter
- test_runner (and arbiter)
- adc
- Character LCD driver
- sram_access (not really driver, simply memory mapped)

4.3 confrd

Alex

- parser, lcd, api access, hardware access, ...

4.4 SPI Flash Configuration

Romel

4.5 Configuration File Format

Alex (get started)

Chapter 5

Backend Software

5.1 Overview

Romel

5.2 API

Romel

5.3 “Server” (Sinatra stuff, database, etc)

Romel

5.4 E-Mails

Romel

5.5 Remote Reconfiguration

Romel

5.6 User Interface

In order to provide an interface between the Superchip Tester, the database and the user, a webpage has been set up to provide the required functionality. The website provides access to the results database, but also allows the user to upload configuration files for the device.

The design of the webpage is based on a website template found on [CSS Templates](#), altered to provide a look and functionality suitable for interface to the chip tester.

The webpage is laid out in a user-friendly and simple manner, with a navigation bar at the top of the page through which the user can browse the pages of the chip tester interface, clearly displaying which page the user is currently on. The four entries in the navigation bar are *Overview*, *Admin*, *Log Entries* and *Upload Files*. In the main part of the screen, the content of the current view is displayed.

The first navigation option, *Overview*, takes the user to an overview of the database where the superchip test results are stored. The table contains seven columns, displaying the number of the team, the date when the test was run and the relevant academic year, the result of the test, the date and time when the entry was updated and whether the design was virtual or actual.

Clicking on the result of an entry takes the user to a more detailed view of that specific run. In this view the user can also see the measured frequency of the oscillator of the design and the name of the design. If the design has failed the test, clicking on the failed result of the test takes the user to another view, where they can monitor the failed test in more detail. This page provides information on the failed test, to help identify the reason of the failure. In specific, the user can see information about the test run, including the input vector to the design and a comparison between the expected and the actual result.

The second option of the navigation bar, *Admin* prompts the user to enter their administrator credentials and takes them to the administrator view page. From this page, an administrator can reset the database, e-mail the results to a specified e-mail address, go to a detailed view of the database or add a new administrator to the system.

more stuff about manage database

Choosing the third option on the navigation bar, *Log Entries*, take the user to yet another webpage that I can't explain what it does.

The last option of the navigation bar, *Upload Files* allows the user to upload a configuration file to the server. The user is asked to enter their e-mail and their team number and a file to upload.

Chapter 6

Some other yet-unnamed section

6.1 Detailed resource usage on FPGA

stuff.

6.2 Rough bill of materials (or more like, cost of each board)

more stuff.

Appendix A

Pinout Tables

| Pin Number | Pin Name | Pin Number | Pin Name | Pin Number | Pin Name |
|------------|----------|------------|----------|------------|----------|
| 39 | ENCODE | 48 | A0 | 50 | A1 |
| 54 | A2 | 56 | A3 | 60 | A4 |
| 62 | A5 | 66 | A6 | 68 | A7 |
| 72 | A8 | 74 | A9 | 78 | A10 |
| 80 | A11 | 96 | A12 | 98 | A13 |
| 102 | A14 | 104 | A15 | 108 | A16 |
| 110 | A17 | 114 | A18 | 116 | A19 |
| 120 | A20 | 122 | A21 | 126 | A22 |
| 128 | A23 | 132 | Q0 | 134 | Q1 |
| 138 | Q2 | 140 | Q3 | 144 | Q4 |
| 146 | Q5 | 150 | Q6 | 152 | Q7 |
| 156 | Q8 | 158 | Q9 | 157 | Q10 |
| 155 | Q11 | 151 | D0 | 149 | D1 |
| 145 | D2 | 143 | D3 | 139 | D4 |
| 137 | D5 | 133 | D6 | 131 | D7 |
| 127 | Q12 | 125 | Q13 | 121 | Q14 |
| 119 | Q15 | 115 | Q16 | 113 | Q17 |
| 109 | Q18 | 107 | Q19 | 103 | Q20 |
| 101 | Q21 | 97 | Q22 | 95 | Q23 |
| 91 | SEL1 | 89 | SEL2 | 85 | SEL3 |
| 83 | SEL4 | 79 | PWRDWN | 45 | VCCIO |
| 51 | VCCIO | 57 | VCCIO | 63 | VCCIO |
| 69 | VCCIO | 75 | VCCIO | 81 | VCCIO |
| 87 | VCCIO | 93 | VCCIO | 99 | VCCIO |
| 105 | VCCIO | 111 | VCCIO | 117 | VCCIO |
| 123 | VCCIO | 129 | VCCIO | 135 | VCCIO |
| 141 | VCCIO | 147 | VCCIO | 153 | VCCIO |
| 159 | VCCIO | 161 | GND | 162 | GND |
| 163 | GND | 164 | GND | 165 | GND |
| 166 | GND | 167 | GND | 168 | GND |
| 169 | GND | 170 | GND | 171 | GND |
| | | 172 | GND | | |

TABLE A.1: Pin-outs for the HSMC header on B1 board.

| Pin Number | Pin Name | Pin Number | Pin Name | Pin Number | Pin Name |
|------------|----------|------------|-----------|------------|-----------|
| 35 | TCK | 36 | TMS | 37 | TDO |
| 38 | TDI | 39 | Ded_Clock | 41 | CONF_DONE |
| 42 | nSTATUS | 43 | nCONFIG | 44 | nCE |
| 48 | IO1 | 50 | IO2 | 54 | IO3 |
| 56 | IO4 | 60 | IO5 | 62 | IO6 |
| 66 | IO7 | 68 | IO8 | 72 | IO9 |
| 74 | IO10 | 78 | IO11 | 80 | IO12 |
| 84 | MOSI | 86 | MISO | 90 | nCS |
| 92 | SCK | 96 | IO13 | 98 | IO14 |
| 102 | IO15 | 104 | IO16 | 108 | IO17 |
| 110 | IO18 | 114 | IO19 | 116 | IO20 |
| 120 | IO21 | 122 | IO22 | 126 | IO23 |
| 128 | IO24 | 132 | IO25 | 134 | IO26 |
| 138 | IO27 | 140 | IO28 | 144 | IO29 |
| 146 | IO30 | 150 | IO31 | 152 | IO32 |
| 156 | IO33 | 158 | IO34 | 157 | IO35 |
| 155 | IO36 | 151 | IO37 | 149 | IO38 |
| 145 | IO39 | 143 | IO40 | 139 | IO41 |
| 137 | IO42 | 133 | IO43 | 131 | IO44 |
| 127 | IO45 | 125 | IO46 | 121 | IO47 |
| 119 | IO48 | 115 | IO49 | 113 | IO50 |
| 109 | IO51 | 107 | IO52 | 103 | IO53 |
| 101 | IO54 | 97 | IO55 | 95 | IO56 |
| 91 | IO57 | 89 | IO58 | 85 | IO59 |
| 83 | IO60 | 79 | IO61 | 77 | IO62 |
| 73 | IO63 | 45 | VCCIO | 51 | VCCIO |
| 57 | VCCIO | 63 | VCCIO | 69 | VCCIO |
| 75 | VCCIO | 81 | VCCIO | 87 | VCCIO |
| 93 | VCCIO | 99 | VCCIO | 105 | VCCIO |
| 111 | VCCIO | 117 | VCCIO | 123 | VCCIO |
| 129 | VCCIO | 135 | VCCIO | 141 | VCCIO |
| 147 | VCCIO | 153 | VCCIO | 159 | VCCIO |
| 161 | GND | 162 | GND | 163 | GND |
| 164 | GND | 165 | GND | 166 | GND |
| 167 | GND | 168 | GND | 169 | GND |
| 170 | GND | 171 | GND | 172 | GND |

TABLE A.2: Pin-outs for the HSMC header on B2 board.

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