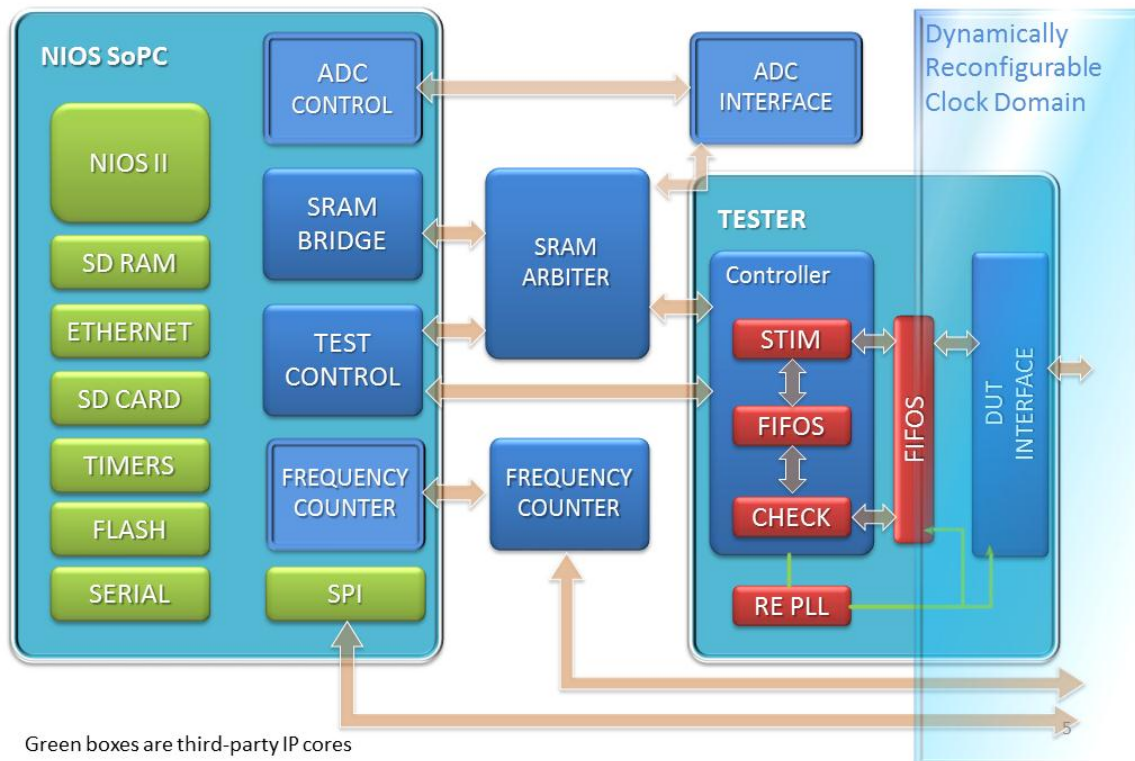


Hardware Overview



The hardware part consists of two main blocks: NIOS System on Programmable Controller and the Tester.

The NIOS SoPC coordinates the whole system, writing the data from SD Card into the SRAM for the Tester to read the data from it; retrieving the result that the Tester writes back to the SRAM and sending the data to the backend for archiving and reviewing for the users. Its tasks include:

- +coordinate the data from multiple sources (SRAM, SD Card, Flash, Serial connection, SPI bus, Ethernet, etc.)
- +control the testing process (which is executed by the Tester, frequency counter and ADC)
- +send results to the backend
- +user interface

SRAM Arbitrator

The SRAM arbitrator is the interface between the SoPC, tester and the SRAM by Avalon Memory Mapped Interface (Avalon-MM). It handles the SRAM read and write requests from SoPC and tester.

The Tester contains several HDL blocks which are responsible for the testing process.

- +read the command, request and test vector from SRAM

- +generate the test input signals for every pin of the DUT

- +monitor the output pins of the DUT and write the result into the memory when the it is valid

- +offer a dynamically reconfigurable clock for the DUT and its relative interface

ADC, Frequency Counter

The purpose of the frequency counter and the ADC is that there is a designated pin on the chip which is the output of a ring oscillator. It is preferable that not only the frequency of this clock output is tested, but that the output waveform is also monitored.