

# Fast and Robust Phase Estimation Algorithm for Heavily Distorted Grid Conditions

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**Abstract**—This paper proposes a fast and robust phase estimation algorithm (PEA), a counterpart of the phase-locked loop (PLL), for heavily distorted grid conditions. The PEA, named as the WLSE-PEA, consists of the moving average filter (MAF), the weighted least squares estimation (WLSE), the frequency-locked loop (FLL), and the zero crossing detection (ZCD). The MAF can eliminate all the odd-order harmonics in the distorted grid voltages. The WLSE is employed to estimate the fundamental positive-sequence component. The combination of the ZCD and the FLL enables the WLSE-PEA to be adaptive to frequency deviations. Compared with some advanced phase-locked loops, the proposed WLSE-PEA has a faster response. Also, it is robust to common grid disturbances including three-phase unbalances, dc offsets, harmonics, phase jumps, and voltage sags. Simulation and experimental results have verified the effectiveness and advantages of the WLSE-PEA.

**Index Terms**—Grid synchronization, moving average filter (MAF), phase estimation algorithm (PEA), phase-locked loop (PLL), weighted least squares estimation (WLSE).

## I. INTRODUCTION

FAST and robust estimation of the fundamental positive-sequence (FPS) and fundamental negative-sequence (FNS) components from the grid voltage is a crucial issue for the synchronization and advanced operation of the grid-connected power converters. For example, many countries have released the grid codes, one of which requires that the converter should stay connected to the grid and inject active and reactive power (PQ) into the grid even under grid faults [1]–[3]. The dynamic performance and the power quality of the power converter system depend highly on the characteristics of the FPS and FNS detection module [4], [5]. The FPS component is also critical for the islanding detection [6], [7]. Moreover, the future microgrid which is made up of multiple power converters allows both islanded and interconnected operation and requires soft

transitions during reconnection. The FPS detection is important for the performance of the system under such operation requirements [8]–[9].

Generally, the FPS detector should be able to reject all the disturbances in the grid voltages, including phase jumps, voltage sags, harmonics, unbalance and dc offset [10]. In three-phase systems, the synchronous reference frame phase-locked loop (SRF-PLL) [11] is the classical solution for the FPS detection. The performance of the SRF-PLL is satisfactory under ideal grid conditions. However, its bandwidth has to be tuned too narrow to be acceptable for three-phase unbalance rejection [12]. For operation under unbalanced grid condition, many advanced PLLs have been proposed. A representative is the dual second order generalized integrator PLL (DSOGI-PLL) [13] based on the sinusoidal integrator. Other solutions include the three-phase enhanced PLL [14] based on adaptive filtering, and the decoupled double synchronous reference frame PLL [15] based on a decoupling network. Although all of them can work properly under the unbalanced condition, the steady-state error exists in the detected FPS component when the grid voltage is heavily distorted with harmonics [16].

The adaptive notch filter based PLL [17] has been proposed to mitigate harmonics distortions. Unfortunately, its dynamic response is slower than the SRF-PLL due to the need for harmonics mitigation. Another solution for the harmonics elimination is the moving average filter-based PLL (MAF-PLL) [18], [19]. The disadvantages of the MAF-PLL with in-loop filters are the narrow open-loop bandwidth and slow dynamic response [20]. In [21], the MAF is innovatively placed outside the control loop as a prefiltering stage, which greatly reduces the settling time, achieving outstanding response speed as well as filtering ability. In [22], arctangent function is employed over the grid voltages in the  $\alpha\beta$  coordinate, and the MAF is implemented to completely eliminate distortions to achieve fast and accurate FPS and FNS detection. In [23] and [24], the dynamics of the MAF-PLL have been improved by adding phase-lead compensator, and incorporating a special proportional component, respectively. However, the settling time of the improved MAF-PLLs is still longer than one cycle under distorted grid conditions in [23] and [24]. Furthermore, the dc offset, which possibly appears in the grid voltage signal caused by the sensor saturation, A/D conversion error or grid faults [25], [26], is not considered in [23]. Some solutions have good dc offset rejection ability and improved dynamics under harmonics distortions including the hybrid PLL (HPLL) [27] and the enhanced generalized delayed signal cancellation PLL (EGDSC-PLL) [28].

Another technique for the FPS detection is weighted least squares estimation (WLSE)-based phase estimation algorithm

Manuscript received October 9, 2015; revised December 29, 2015 and April 8, 2016; accepted May 1, 2016. Date of publication June 27, 2016; date of current version October 7, 2016. This work was supported in part by the National Natural Science Foundation of China under Grant U1510208, Grant 61273045, and Grant 51361135705, in part by the National High Technology Research and Development Program of China under Grant 2012AA050217, and in part by the National Key Research and Development Program under Grant 2016YFB0900302.

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Digital Object Identifier 10.1109/TIE.2016.2585078

(PEA) [29]–[32]. Its basic idea, based on the system identification theory, is to estimate the voltage magnitude and phase angle by minimizing the squared discrepancies between observed samples and their expected values. Though the WLSE based PEA can estimate the FPS accurately and fast under ideal condition, it should sacrifice its response speed for better harmonics mitigation performance under the highly distorted grid conditions. Otherwise, the dimension of the internal matrices in the WLSE scheme has to be greatly expanded to reject harmonics disturbance, which increases the computational burden. However, usually the heavy computational burden is not acceptable for commonly used digital signal processors. Moreover, it should be noticed that the dynamics of the frequency-locked loop (FLL) in the WLSE under frequency deviations can be very slow [29], [31].

To sum up, a key issue of the FPS detector design is the conflict between filtering ability and response speed. The bandwidth of the conventional PEA/PLL always needs to be reduced to attenuate the FNS and harmonics. Therefore, few above mentioned PEAs/PLLs can not only reject all the disturbances in the grid voltages but also have the settling time less than a half of a grid cycle. Especially, most of the conventional PLLs have difficulties mitigating dc offsets because the frequency of the dc component is close to the FPS component, which makes filter design challenging. Moreover, the conflict between response speed and frequency swing exists in most of the PLLs. The fast response of the PLL under phase jump would usually cause large frequency swings due to the coupling between frequency and phase in the PLLs [33].

This work proposes a fast and robust PEA, the WLSE-PEA, for the FPS component detection. The WLSE-PEA consists of four blocks including the MAF, the WLSE, the FLL, and the zero crossing detection (ZCD). The MAF as a prefiltering stage in [21] has excellent performance and is used in this paper. On one hand, the MAF is complementary to the WLSE. The MAF can filter out all the odd-order harmonics but would have to sacrifice its settling time to one grid cycle if dc offset was taken into consideration; the WLSE can deal with only limited number of harmonics with fast dynamics due to the computational burden issue. In the proposed PEA, all the odd-order harmonics are filtered out by the MAF so that the WLSE can estimate the FPS component only considering dc offsets. Combining the two blocks greatly reduces the size of matrices and the computational burden of the WLSE. Also, the WLSE-PEA achieve the dc offsets mitigation without sacrificing its dynamics a lot. On the other hand, the ZCD is complementary to the FLL. The ZCD has faster dynamics, and less sensitivity to phase jump than the FLL; the FLL has more detecting accuracy than the ZCD. In the WLSE-PEA, the ZCD, acting as a feed-forward loop to improve the response speed, is combined with the FLL which acts as a feedback loop to improve steady-state tracking ability. Thus, good FPS estimation accuracy can be achieved in the steady state and the response speed is not compromised.

One contribution of this paper is a systematic PEA design which employs four complementary elements to effectively alleviate the conflicts existing in the conventional PLLs. According to this idea, some extended PLLs can be obtained by replacing

existing blocks with other blocks as long as they remain complementary to each other, e.g., replacing the MAF with GDSC filters, and replacing the WLSE with other stochastic filters such as the Kalman filter or even artificial neural network. The other contribution is to draw the readers' attention to the WLSE, which has potential to be a good candidate for the FPS extraction as well as the dc offsets mitigation. As the contradiction between filtering ability and dynamics has been alleviated, the WLSE-PEA is robust to almost all the disturbances, including unbalance, harmonics, dc offset, phase jump, voltage sag, and frequency fluctuation. Also, it should be noticed that the response speed of the WLSE-PLL under phase jump and voltage sag has been improved to be as fast as a half of a grid cycle approximately.

The paper is organized as follows. Section II shows the characterization of grid voltages in the  $dq$  and the  $\alpha\beta$  coordinate. Section III provides analyses of the moving average filter. Sections IV and V introduce the WLSE and the proposed WLSE-PEA, respectively. Section VI is devoted to the comparative simulation between the WLSE-PEA and some popular PLLs including the SRF-PLL, the HPLL, and the EGDSC-PLL. The experimental results are described in Section VII. Section VIII sets out the conclusion.

## II. CHARACTERIZATION OF GRID VOLTAGES

Three-phase grid voltages can be modeled as the summation of positive-, negative- and zero-sequence components. The zero-sequence component is not considered in (1) because the grid-connected power conversion systems are usually coupled to the grid by three-wire connection. It is the common case in the high-power application where low-voltage ride through and advanced control are necessary and the PLL is crucial. The FPS at the PCC is most critical for grid code fulfillment. The grid voltages can be formulated as the FPS in addition with other sequence components as

$$\begin{aligned} v_{abc} &= v_{abc}^{+1} + \sum_{\substack{n=-\infty \\ n \neq +1}}^{+\infty} v_{abc}^n \\ &= V^{+1} \begin{bmatrix} \cos(\omega t + \theta_{+1}) \\ \cos(\omega t - 2\pi/3 + \theta_{+1}) \\ \cos(\omega t + 2\pi/3 + \theta_{+1}) \end{bmatrix} \\ &\quad + \sum_{\substack{n=-\infty \\ n \neq +1}}^{+\infty} V^n \begin{bmatrix} \cos(n\omega t + \theta_n) \\ \cos(n\omega t - 2\pi/3 + \theta_n) \\ \cos(n\omega t + 2\pi/3 + \theta_n) \end{bmatrix}. \quad (1) \end{aligned}$$

The grid voltages can also be expressed on a  $dq$  rotating reference frame by using Park transformation as

$$\begin{aligned} v_{dq} &= V^{+1} \sqrt{\frac{3}{2}} \begin{bmatrix} \cos(\omega t + \theta_{+1} - \theta') \\ \sin(\omega t + \theta_{+1} - \theta') \end{bmatrix} \\ &\quad + \sum_{\substack{n=-\infty \\ n \neq +1}}^{+\infty} V^n \sqrt{\frac{3}{2}} \begin{bmatrix} \cos(n\omega t + \theta_n - \theta') \\ \sin(n\omega t + \theta_n - \theta') \end{bmatrix} \\ &= \bar{v}_{dq}^{+1} + \tilde{v}_{dq}^{+1}. \quad (2) \end{aligned}$$

In (2), if the  $dq$  coordinate rotates at fundamental frequency, i.e.,  $\theta' = \omega t$ , the FPS will be a dc signal in the coordinate and the other sequence components will be ac ripples.

On the other hand, the grid voltages can be expressed on a  $\alpha\beta$  stationary reference frame. The relation between grid voltages in the  $\alpha\beta$  coordinate and in the  $dq$  coordinate can be written as

$$v_{\alpha\beta} = \sum_{n=-\infty}^{+\infty} T^n \bar{v}_{dq}^n \quad (3)$$

where

$$T^n = \begin{bmatrix} \cos(n\omega t) & -\sin(n\omega t) \\ \sin(n\omega t) & \cos(n\omega t) \end{bmatrix}, n = 0, \pm 1, \pm 2, \dots \quad (4)$$

### III. MOVING AVERAGE FILTER

The MAF is one of the linear-phase finite-impulse response filters that can act as an ideal notch filter under certain conditions. The MAF in [21] and [22] is used in this paper. It can be easily performed by a digital controller and costs little computational burden. However, when frequency deviates from nominal value, sampling error can be large without variable sampling rate. Fortunately, a linear interpolation technique can reduce the sampling error greatly [34], [35].

In the continuous time domain, the MAF can be realized by applying the input  $x(t)$  to the operator as

$$y(t) = \frac{1}{T_w} \int_{t-T_w}^t x(\tau) d\tau \quad (5)$$

where  $T_w$  is the window length of the MAF. From (5), the transfer function of the MAF can be derived as

$$G_{\text{MAF}}(s) = \frac{1 - e^{-T_w s}}{T_w s}. \quad (6)$$

The settling time of the MAF is a window length  $T_w$  [21]. Thus, a wider window length makes the MAF have slower dynamics.

Substituting  $s = j\omega$  into (6), the magnitude and phase expressions of the MAF can be obtained as

$$G_{\text{MAF}}(j\omega) = \left| \frac{\sqrt{2 - 2\cos(\omega T_w)}}{\omega T_w} \right| \angle -\omega T_w / 2. \quad (7)$$

The MAF has a zero gain and no phase shift when  $\omega = 2k\pi/T_w$  ( $k = 1, 2, 3, \dots$ ), i.e.,  $f = k/T_w$  ( $k = 1, 2, 3, \dots$ ). Moreover, the MAF has a unity gain and no phase shift when  $\omega = 0$ . Therefore, the MAF can completely block all the harmonics, if the window length is one cycle. The Bode diagram of the MAF for different window lengths can be appreciated in Fig. 1. It can be observed that a narrower window length may indicate a poorer filtering quality, though shrinking window length can increase response speed as just mentioned. Hence, a tradeoff between filtering ability and dynamics should be made.

### IV. WEIGHTED LEAST SQUARES ESTIMATION

The WLSE mainly focuses on the FPS and the FNS extraction, i.e.,  $\theta^{+1}$ ,  $\bar{v}_{dq}^{+1}$ ,  $\theta^{-1}$ , and  $\bar{v}_{dq}^{-1}$  from the grid voltages in the  $\alpha\beta$  coordinate. Other sequence components can also be estimated

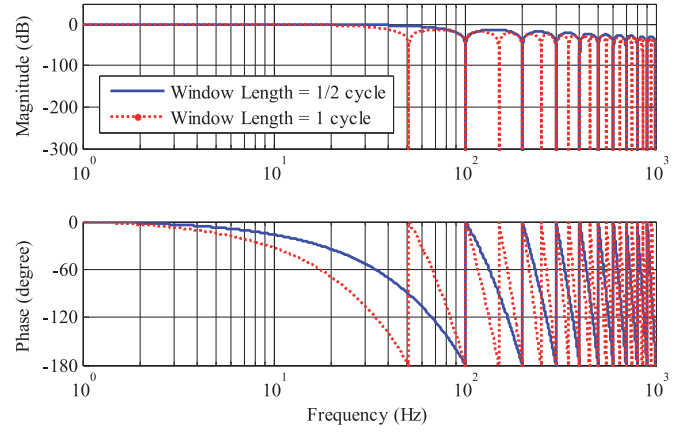


Fig. 1. Bode Diagram of the MAF for different  $T_w$ .

if necessary. The sequence components that need to be estimated in the WLSE of the proposed PEA and its extensions may vary in different harmonics contents as will be discussed in Table I in the next section. The proposed WLSE-PEA requires that the FPS and the dc offset should be included in the estimation vector  $\hat{v}_{dq}$ , which is defined as

$$\begin{aligned} \hat{v}_{dq}^T &= [\hat{v}_d^{+1} \quad \hat{v}_q^{+1} \quad \hat{v}_d^0 \quad \hat{v}_q^0] \\ &= [(\hat{v}_{dq}^{+1})^T \quad (\hat{v}_{dq}^0)^T]^T. \end{aligned} \quad (8)$$

According to (3),  $\hat{v}_{\alpha\beta}$  can be derived from  $\hat{v}_{dq}$  as

$$\begin{aligned} \hat{v}_{\alpha\beta} &= \hat{v}_{\alpha\beta}^{+1} + \hat{v}_{\alpha\beta}^0 \\ &= H \cdot \hat{v}_{dq} = [T^{+1} \quad T^0] \hat{v}_{dq}. \end{aligned} \quad (9)$$

In (9), since sequence components except the FPS and the dc offset are not estimated, they are assumed to be zero and act as disturbance to the WLSE if not completely eliminated in the previous stages.

When the WLSE is implemented on the discrete time domain,  $v_{\alpha\beta}$  is sampled regularly and  $\hat{v}_{\alpha\beta}$  is calculated at each instant  $j$  ( $j = 1, 2, 3, \dots$ ). If  $n$  samples have been obtained and the WLSE is employed to estimate  $\hat{v}_{\alpha\beta}$  of the next instant, the principle of the WLSE is to derive the optimal  $\hat{v}_{dq}$  that can minimize the cost function  $J[v_{dq}]$  as

$$J[v_{dq}] = \sum_{j=0}^n \lambda^{n-j} \|v_{\alpha\beta(j)} - \hat{v}_{\alpha\beta(j)}\|^2 \quad (10)$$

where  $v_{\alpha\beta(j)}$  and  $\hat{v}_{\alpha\beta(j)}$  stand for  $v_{\alpha\beta}$  and  $\hat{v}_{\alpha\beta}$  at instant  $j$ , respectively. In (10),  $\lambda \in (0, 1)$  is the forgetting factor. It indicates that fresh information is more important than old information and hence has larger weight. The recursive method to obtain the optimal  $\hat{v}_{dq(n+1)}$ , i.e., the estimated grid voltages in the  $dq$  coordinate at instant  $(n+1)$ , is detailed as

1) Compute the autocorrelation matrix  $R$

$$R_{(n+1)} = \lambda I + H_{(n)} \cdot P_{(n)} \cdot H_{(n)}^T. \quad (11)$$

TABLE I  
WLSE-PEA AND EXTENDED WLSE-PEAS

	Harmonics Contents	FPS estimation	FNS estimation	Rotating angle of the $dq$ coordinate in Fig. 3.	MAF $T_w$ (MAF settling time)	Sequence components in the WLSE estimation vector
WLSE-PEA	All the odd-order harmonics	✓	✗	$+\omega t$	1/2 cycle	dc, +1
Extended WLSE-PEA 1	All the odd-order harmonics	✗	✓	$-\omega t$	1/2 cycle	dc, -1
Extended WLSE-PEA 2	$\pm 3$ and $\pm 5, \pm 7, \pm 11, \pm 13 \dots$	✓	✓	$+\omega t$ and $-\omega t$	1/6 cycle * 2	dc, $\pm 1, \pm 3$
Extended WLSE-P PEA 3	$\pm 5, \pm 7, \pm 11, \pm 13 \dots$	✓	✓	$+\omega t$ and $-\omega t$	1/6 cycle * 2	dc, $\pm 1$
Extended WLSE-P PEA 4	$-5, +7, -11, +13 \dots$	✓	✓	$+\omega t$	1/6 cycle	dc, $\pm 1$

“±” indicates both positive- and negative-sequence components.

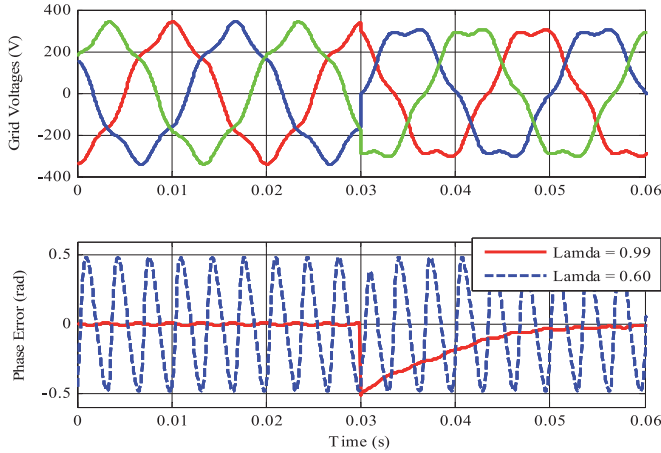


Fig. 2. Operation of the WLSE for different  $\lambda$ .

- 2) Calculate the gain matrix  $K$

$$K_{(n)} = P_{(n)} \cdot H_{(n)}^T \cdot R_{(n)}^{-1}. \quad (12)$$

- 3) Update the error covariance matrix  $P$

$$P_{(n+1)} = \lambda^{-1} \cdot (I - K_{(n)} \cdot H_{(n)}) \cdot P_{(n)}. \quad (13)$$

- 4) Obtain the estimation vector  $\hat{v}_{dq}$

$$\hat{v}_{dq(n+1)} = \hat{v}_{dq(n)} + K_{(n)} \cdot (v_{\alpha\beta(n)} - \hat{v}_{\alpha\beta(n)}). \quad (14)$$

- 5) Derive the phase angle of the FPS

$$\hat{\phi}_{(n+1)}^{+1} = \text{atan}(\hat{v}_q^{+1}, \hat{v}_d^{+1}) \quad (15)$$

$$\hat{\theta}_{(n+1)}^{+1} = \text{atan}(\hat{v}_\beta^{+1}, \hat{v}_\alpha^{+1}). \quad (16)$$

where subscript  $(n+1)$  stands for value of variables at instant  $(n+1)$ ,  $\hat{v}_{dq(-1)} = 0$  (initial value of estimated grid voltages in the  $dq$  coordinate),  $P_{(-1)} = \pi_0 I$  (initial value of the error covariance matrix  $P$ ),  $\pi_0 (> 0)$  is the initial covariance constant.

### A. Tuning of Parameters

The dynamics of the WLSE are determined by  $\pi_0$  and  $\lambda$ . A larger  $\pi_0$  means a larger  $K$  at the startup stage and a faster convergence. In the steady state,  $P$  converges to a fixed value [31]. Therefore,  $\lambda$  is responsible for the performance of the WLSE during the steady state. In Fig. 2, operation of the WLSE for the FPS estimation with different  $\lambda$  under 0.1 per unit (pu) fifth harmonic distortion can be appreciated. A phase jump (30°)

occurs at all the three phases at 0.03 s. A small  $\lambda$  such as 0.6 has a fast dynamic response but a poor filtering capability while a large  $\lambda$  close to 1 has a good filtering capability but a slow dynamic response. If certain order of harmonics is not filtered out before the WLSE and also not included in the  $\hat{v}_{dq}$ , a large  $\lambda$  is recommended for the accuracy of estimation.

### B. Frequency Adaptation

There will be a phase error in  $\theta^{+1}$  if the rotating speed of  $T^n$  does not match the frequency of grid voltages. Therefore, the WLSE in [29] uses the inherited FLL for frequency adaptation. However, the dynamics of the WLSE under frequency deviation can be very slow [29], [31]. A description of the FLL is presented below.

At the end of each instant,  $\hat{\phi}_{(n+1)}^{+1}$  in (15) is compared with  $\hat{\phi}_{(n)}^{+1}$ . A new estimation of frequency can be derived as

$$\hat{\omega}_{(n+1)}^{FLL} = \hat{\omega}_{(n)}^{FLL} + k_p (\hat{\phi}_{(n+1)}^{+1} - \hat{\phi}_{(n)}^{+1}) + k_i \hat{\phi}_{(n+1)}^{+1}. \quad (17)$$

The rotating speed of  $T^n$  should be changed correspondingly with the latest estimated frequency.

### V. PROPOSED WLSE-PEA ALGORITHM

The structure of the proposed WLSE-PEA can be appreciated in Fig. 3. First, the grid voltages are transformed into the  $dq$  coordinate using the estimated frequency. As shown in (2),  $v_{dq}$  may contain other sequence components besides the FPS. Since the  $dq$  coordinate rotates at fundamental frequency, the FPS is a dc signal. The MAF in [21] is applied to completely filter out all the odd-order harmonics. Hence, considering the analyses in Section III, the window length of the MAF is chosen to be 1/2 cycle. After the MAF stage, the filtered grid voltages still contain the FPS, and the dc component. Then, the voltages are transformed into the  $\alpha\beta$  coordinate. Finally, the WLSE uses  $v_{\alpha\beta}$ , which contains the information of the FPS, and the dc offset, to estimate  $\hat{v}_{dq}^{+1}$  and  $\hat{\phi}^{+1}$ .  $\theta^{+1}$  can be obtained by adding  $\hat{\phi}^{+1}$  with  $\theta_{srf}$  ( $\theta_{srf} = \int_0^t \omega dt$ ). Matrix  $H$  is chosen as shown in (9). Only the FPS, and the dc component need to be estimated thanks to the previous MAF stage. That is a great advantage over the traditional WLSE [31], as including many sequence components can cause complex calculation of large matrices and consequently heavy computational burden. Moreover, since the dc component is included in  $H$ , it is not considered as disturbance from the perspective of the WLSE. In Fig. 3, algebraic



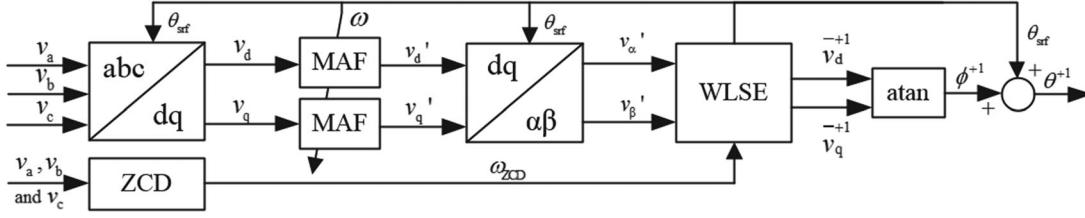


Fig. 3. Structure of the proposed WLSE-PEA.

loops exist. Unit delay can be introduced or the MAF and the synchronous reference frames can be directly fed by the ZCD with a little accuracy sacrificed.

The frequency adaptation relies on the ZCD and the FLL of the WLSE. The ZCD has a relatively fast dynamic and is insensitive to phase jump, dc offset and harmonics. However, its accuracy is limited by sampling frequency of the digital controller when noise in the grid voltage signal is properly filtered out. (The error of the ZCD can be as small as 0.01 Hz or as large as 0.2 Hz, depending on the sampling frequency.) The FLL has a poor dynamic performance but can give a precise estimation of grid frequency. They are combined to obtain an accurate steady-state estimation and a quick frequency response. If there is not fast frequency fluctuation, output frequency of the combined block  $\hat{\omega}_{(n+1)}$  will be equal to  $\hat{\omega}_{(n)}^{\text{FLL}}$  for better accuracy. If there is fast frequency fluctuation, since FLL's dynamics is slower than the ZCD's,  $\hat{\omega}_{(n)}^{\text{ZCD}}$  can better indicate the real-grid frequency. That is if  $|\hat{\omega}_{(n)}^{\text{FLL}} - \hat{\omega}_{(n)}^{\text{ZCD}}| > \varepsilon_1$ , then  $\hat{\omega}_{(n+1)}^{\text{FLL}} = \hat{\omega}_{(n)}^{\text{ZCD}} + k_p(\hat{\phi}_{(n+1)}^{+1} - \hat{\phi}_{(n)}^{+1}) + k_i\hat{\phi}_{(n+1)}^{+1}$ , and for the next  $T_\varepsilon$  second, output frequency of the combined block  $\hat{\omega}_{(n+1)}$  will be equal to  $\hat{\omega}_{(n)}^{\text{ZCD}}$ . Here, the ZCD can be considered as a feed-forward loop to improve the dynamic performance of the PEA. However, in the steady state, the frequency obtained from the ZCD may have a small error. If the sampling frequency is high, high-frequency noise in the voltage signal is small, the error will be small, such as 0.02 Hz, i.e., the discrepancy between the output frequency of the ZCD obtained from the newest two zero crossing points and that from the last two zero crossing points will be less than 0.02 Hz. Then, for the next  $T_\varepsilon$  second, output frequency of the combined block  $\hat{\omega}_{(n+1)}$  will be equal to  $\hat{\omega}_{(n)}^{\text{ZCD}}$  for possible rejection of disturbance such as phase jump. The parameters  $\varepsilon_1$  and  $T_\varepsilon$  should be chosen according to the detection error of the ZCD. The ZCD can be immune to dc offset, even-order and odd-order harmonic distortions if the time lapse of a grid cycle is detected. The ZCD can also be immune to phase jump [21] and can be used on all the three phases to boost response speed. Then, if any phase detects a frequency step, the output frequency of the ZCD will be updated immediately.

The previous descriptions of the proposed PEA in this section are for the FPS component detection under the odd-order harmonics distortion condition. Some extended WLSE-PEAs for FPS and FNS components estimation under other harmonics contents can be obtained by proper modification as shown in Table I. The FNS component detection under odd-order harmonics distortion condition can be achieved with the extended WLSE-PEA 1. To derive the extended WLSE-PEA 2, the first

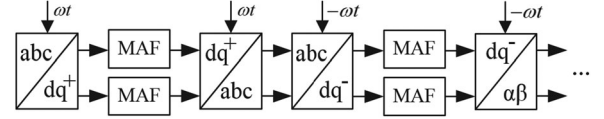


Fig. 4. Cascaded filtering stages in the extended WLSE-PEA 2 and 3.

step is to replace the MAF in Fig. 3 with the cascaded filtering stages in Fig. 4. In Fig. 4, the rotating angles of the first and the second dq coordinate are  $\omega t$  and  $-\omega t$ , respectively. The second step is to change the estimation vector from (8) to (18)

$$\begin{aligned} \hat{v}_{dq}^T &= \begin{bmatrix} \hat{v}_d^{+1} & \hat{v}_q^{+1} & \hat{v}_d^{-1} & \hat{v}_q^{-1} & \hat{v}_d^0 & \hat{v}_q^0 & \hat{v}_d^{+3} & \hat{v}_q^{+3} & \hat{v}_d^{-3} & \hat{v}_q^{-3} \end{bmatrix} \\ &= \begin{bmatrix} (\hat{v}_{dq}^{+1})^T & (\hat{v}_{dq}^{-1})^T & (\hat{v}_{dq}^0)^T & (\hat{v}_{dq}^{+3})^T & (\hat{v}_{dq}^{-3})^T \end{bmatrix}. \end{aligned} \quad (18)$$

Other extended versions of the WLSE-PEA can be obtained similarly. To some extent, the window length of the MAF indicates the settling time and the size of the estimation vector indicates computational burden. It is important to take these factors as well as harmonics contents into consideration when choosing between the WLSE-PEA and its extensions.

In the WLSE-PEA and its extended versions, the WLSE and the MAF are complementary to each other. For example, in the extended WLSE-PEA 3, the WLSE mitigates low-order distortions with fast dynamics, such as dc offsets and the FNS, while a short-window-length MAF filters out some high-order distortions as shown in Table I. They work together to reject the harmonics, the FNS, and the dc offset distortions with a fast response speed. According to this idea, some extended PEAs can be obtained as long as two blocks remain complementary to each other. For example, the MAF can be replaced with GDSC filters, and the WLSE can be replaced with other stochastic filters such as Kalman filters.

## VI. COMPARATIVE SIMULATIONS

In order to evaluate the performance of the proposed PEA, comparative simulations have been done. The benchmarks are the SRF-PLL, the HPLL [27], and the EGDSC-PLL [28]. The SRF-PLL, incorporated with two low-pass filters to enhance its filtering ability, is shown in Fig. 5. The parameters of the SRF-PLL are  $\omega_{\text{LPF}} = 100$  rad/s,  $k_p = 41.67$ ,  $k_i = 723.38$ . The SRF-PLL's phase margin and cutoff frequency are  $44.8^\circ$  and 6.64 Hz, respectively. The parameters of the HPLL and the EGDSC-PLL are tuned according to [27] and [28], i.e.,  $k_p = 94$ ,  $k_\varphi = 0.05$ ,  $T_w = 0.01$  s in the HPLL and  $k_p = 440$ ,  $k_i = 48361$ ,  $k_\varphi = 9.6875 \times 10^{-3}$ ,  $k_v = 1.665 \times 10^{-5}$  in the

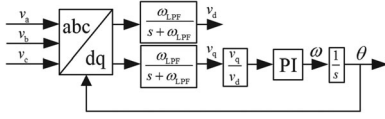


Fig. 5. Structure of the SRF-PLL.

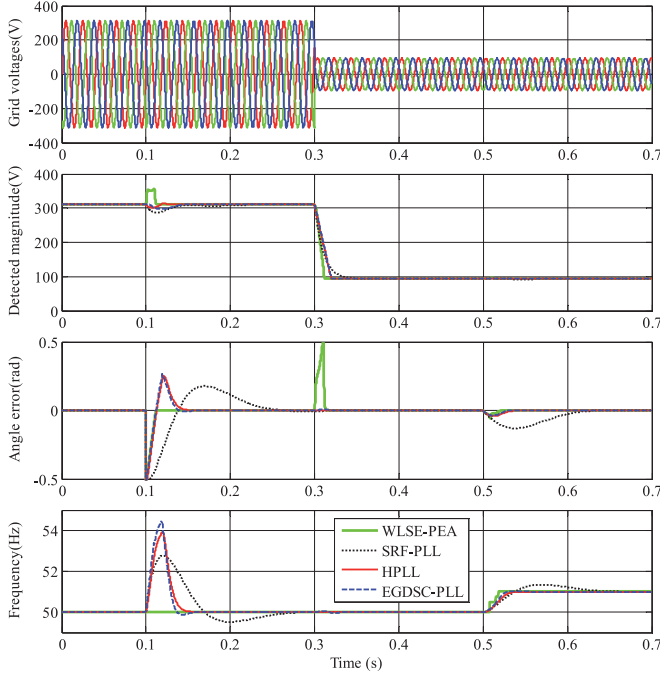


Fig. 6. Comparison of the PLLs under phase jump (0.1 s), voltage sag (0.3 s), and frequency deviation (0.5 s).

EGDSC-PLL. The parameters of the WLSE-PEA are chosen as  $T_w = 0.01$  s,  $\varepsilon_1 = 0.2$  Hz,  $T_\varepsilon = 0.012$ ,  $k_p = 30$ ,  $k_i = 5$ ,  $\lambda = 0.8$ , and  $\pi_0 = 300$ .

Several criterions have been selected for better evaluation, including the errors of detection ( $e_{\text{angle}}$ ,  $e_{\text{mag}}$ ,  $e_{\text{freq}}$ ), settling time of the phase angle ( $ts_{\text{angle}}$ ), magnitude ( $ts_{\text{mag}}$ ), and frequency ( $ts_{\text{freq}}$ ). In [21], the reference for the selection of the criterions and design of the comparative simulations is given. The settling time here is the time required for the response curve to reach and stay within certain range of the real value, i.e. 0.02 pu (6.22 V), 0.02 rad, and 0.02 Hz for magnitude, phase angle, and frequency, respectively. If the overshoot of one PLL under specific disturbance is so small that the estimations always stay in the range given above, the settling time will be recorded as “0” as can be seen in the tables below, especially Table VIII.

For all the comparative simulation cases discussed below, the initial magnitude of the three-phase rms phase-to-phase voltage is 381.05 V and the initial-phase angle is 0°. Due to limited space, the transience is not magnified. However, the comparative experiments were conducted under the same grid voltages and can be appreciated clearly in the next section.

In Fig. 6, the WLSE-PEA’s performance under phase jump, voltage sag, and frequency deviation can be appreciated. At 0.1 s, a 30° phase jump occurs on all the three phases. At 0.3 s,

TABLE II  
PERFORMANCE COMPARISON UNDER PHASE JUMP

	WLSE-PEA	SRF-PLL	HPLL	EGDSC-PLL
$e_{\text{angle}}$ (rad)	0	0	0	0
$ts_{\text{angle}}$ (s)	0.011	0.140	0.036	0.041
$e_{\text{mag}}$ (V)	0	0	0	0
$ts_{\text{mag}}$ (s)	0.011	0.036	0.033	0.014
$e_{\text{freq}}$ (Hz)	0	0	0	0
$ts_{\text{freq}}$ (s)	0	0.177	0.057	0.053

TABLE III  
PERFORMANCE COMPARISON UNDER VOLTAGE SAG

	WLSE-PEA	SRF-PLL	HPLL	EGDSC-PLL
$e_{\text{angle}}$ (rad)	0	0	0	0
$ts_{\text{angle}}$ (s)	0.012	0	0	0
$e_{\text{mag}}$ (V)	0	0	0	0
$ts_{\text{mag}}$ (s)	0.011	0.048	0.020	0.020
$e_{\text{freq}}$ (Hz)	0	0	0	0
$ts_{\text{freq}}$ (s)	0	0	0.030	0

TABLE IV  
PERFORMANCE COMPARISON UNDER FREQUENCY DEVIATION

	WLSE-PEA	SRF-PLL	HPLL	EGDSC-PLL
$e_{\text{angle}}$ (rad)	0	0	0	0
$ts_{\text{angle}}$ (s)	0.016	0.106	0.021	0.024
$e_{\text{mag}}$ (V)	0	0	0	0
$ts_{\text{mag}}$ (s)	0.014	0	0	0
$e_{\text{freq}}$ (Hz)	0	0	0	0
$ts_{\text{freq}}$ (s)	0.018	0.145	0.032	0.038

there is a three-phase voltage sag (70%). At 0.5 s, the grid frequency deviates from 50 to 51 Hz. The detailed evaluation of settling time and error can be seen in Tables II–IV. The WLSE-PEA has the shortest settling time, especially when phase jump occurs while the SRF-PLL has the slowest dynamics. The response speed of the HPLL and the EGDSC-PLL is also good compared to the SRF-PLL.

In Fig. 7, the WLSE-PEA’s performance under odd-order harmonics as well as even-order harmonics is shown. At 0.1 s, the harmonics imposed on the grid voltages include the third-order positive sequence, the third-order negative sequence, the fifth-order positive sequence, the fifth-order negative sequence, the seventh-order positive sequence, the seventh-order negative sequence, the ninth-order positive sequence, and the ninth-order negative sequence (all 0.05 pu, −30°, 70°, 45°, 50°, 30°, 30°, 40°, 60°, respectively). At 0.3 s, the grid voltages return to normal. At 0.5 s, the harmonics imposed on the grid voltages include the fourth-order negative sequence (0.01 pu, −60°), the sixth-order positive sequence (0.01 pu, 30°), and the eighth-order negative sequence (0.01 pu, 30°). According to the voltage quality standard EN 50160 for electricity distribution systems in Europe [37], even-order harmonics distortions are less severe than odd-order harmonics. Thus, less even-order harmonics are added at 0.5 s. The detailed evaluation of settling time and error

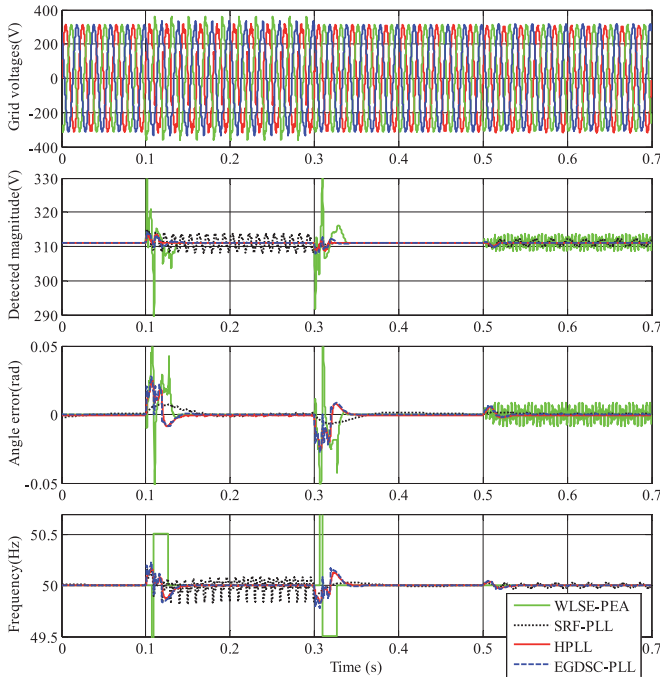


Fig. 7. Comparison of the PLLs under odd-order harmonics (0.1–0.3s) and even-order harmonics (0.5–0.7s).

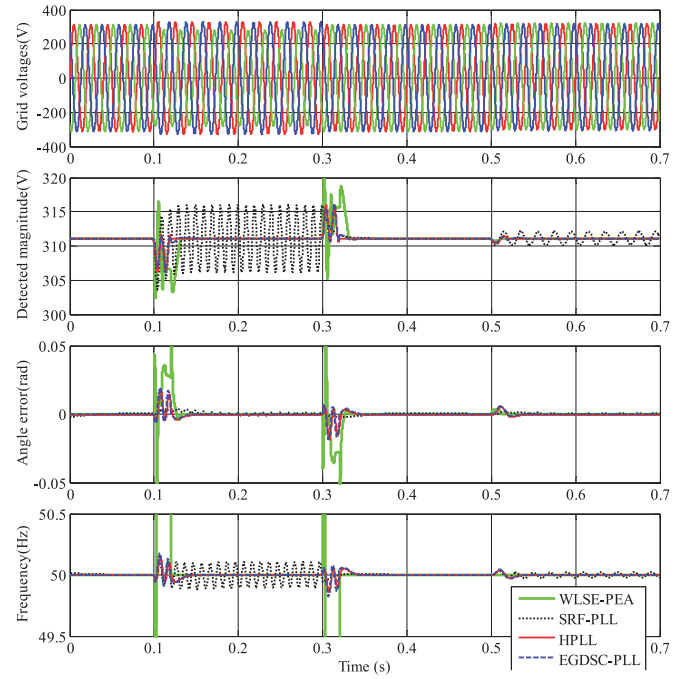


Fig. 8. Comparison of the PLLs under three-phase unbalance (0.1–0.3 s) and dc offset (0.5–0.7 s).

TABLE V  
PERFORMANCE COMPARISON UNDER ODD-ORDER HARMONICS

	WLSE-PEA	SRF-PLL	HPLL	EGDSC-PLL
$e_{\text{angle}}$ (rad)	0	<0.001	0	0
$t_{s_{\text{angle}}}$ (s)	0.025	0	0.012	0.007
$e_{\text{mag}}$ (V)	0	$\pm 3.4$	0	0
$t_{s_{\text{mag}}}$ (s)	0.010	0	0	0
$e_{\text{freq}}$ (Hz)	0	$\pm 0.16$	0	0
$t_{s_{\text{freq}}}$ (s)	0.023	N/A <sup>a</sup>	0.037	0.038

<sup>a</sup>The detected frequency in the steady state does not stay within 0.02 Hz around the real value.

TABLE VI  
PERFORMANCE COMPARISON UNDER EVEN-ORDER HARMONICS

	WLSE-PEA	SRF-PLL	HPLL	EGDSC-PLL
$e_{\text{angle}}$ (rad)	$\pm 0.008$	<0.001	0	0
$t_{s_{\text{angle}}}$ (s)	0	0	0	0
$e_{\text{mag}}$ (V)	$\pm 2.3$	$\pm 1.0$	0	0
$t_{s_{\text{mag}}}$ (s)	0	0	0	0
$e_{\text{freq}}$ (Hz)	$\pm 0.07$	$\pm 0.025$	0	0
$t_{s_{\text{freq}}}$ (s)	N/A <sup>a</sup>	N/A <sup>a</sup>	0.011	0.011

<sup>a</sup>The detected frequency in the steady state does not stay within 0.02 Hz around the real value.

can be seen in Tables V and VI. The HPLL and the EGDSC-PLL are immune to both odd-order and even-order harmonics. However, the WLSE-PEA cannot completely eliminate even-order harmonics, and errors exist in the estimations obtained from SRF-PLL under both odd-order and even-order harmonics distortions.

TABLE VII  
PERFORMANCE COMPARISON UNDER UNBALANCE

	WLSE-PEA	SRF-PLL	HPLL	EGDSC-PLL
$e_{\text{angle}}$ (rad)	0	$\pm 0.001$	0	0
$t_{s_{\text{angle}}}$ (s)	0.022	0	0.009	0.008
$e_{\text{mag}}$ (V)	0	$\pm 4.9$	0	0
$t_{s_{\text{mag}}}$ (s)	0.024	0.005	0	0
$e_{\text{freq}}$ (Hz)	0	$\pm 0.11$	0	0
$t_{s_{\text{freq}}}$ (s)	0.020	N/A <sup>a</sup>	0.034	0.034

<sup>a</sup>The detected frequency in the steady state does not stay within 0.02 Hz around the real value.

TABLE VIII  
PERFORMANCE COMPARISON UNDER DC OFFSET

	WLSE-PEA	SRF-PLL	HPLL	EGDSC-PLL
$e_{\text{angle}}$ (rad)	0	<0.001	0	0
$t_{s_{\text{angle}}}$ (s)	0	0	0	0
$e_{\text{mag}}$ (V)	0	$\pm 1.0$	0	0
$t_{s_{\text{mag}}}$ (s)	0	0	0	0
$e_{\text{freq}}$ (Hz)	0	$\pm 0.022$	0	0
$t_{s_{\text{freq}}}$ (s)	0	N/A <sup>a</sup>	0.028	0.027

<sup>a</sup>The detected frequency in the steady state does not stay within 0.02 Hz around the real value.

In Fig. 8, the performance of the WLSE-PEA under three-phase unbalance and dc offset can be appreciated. At 0.1 s, a FNS component (0.1 pu,  $-60^\circ$ ) is imposed on the grid voltages. At 0.3 s, the grid voltages return to normal. At 0.5 s, dc offsets occur on the grid voltages (phase a: 0.03 pu, phase b: 0.05 pu, phase c: 0.025 pu). The detailed evaluation of settling time and error can be seen in Tables VII and VIII. Keep in mind that when

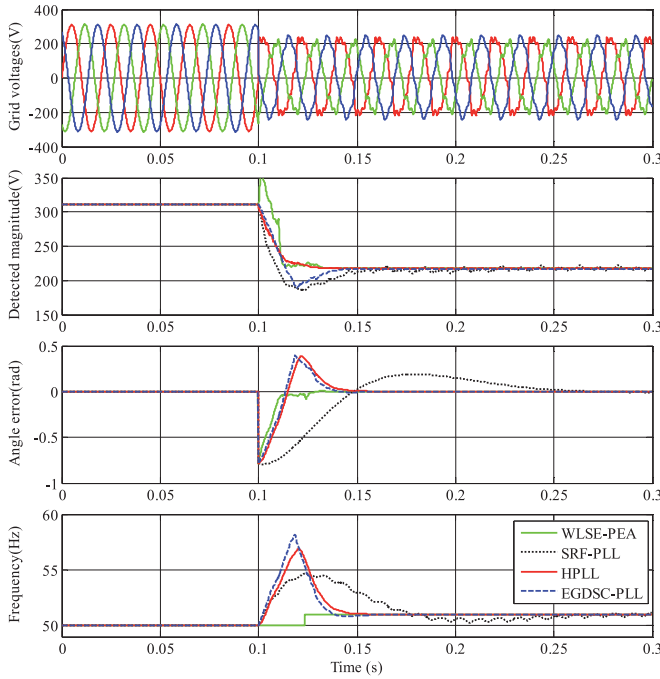


Fig. 9. Comparison of the PLLs under harsh grid conditions where three-phase unbalance, dc offset, odd-order harmonics, phase jump, voltage sag, and frequency deviation occur at the same time (0.1–0.3 s).

the detected angle, magnitude, and frequency stay within certain ranges (0.02 rad, 0.02 pu, and 0.02 Hz for angle, magnitude, and frequency, respectively) around the real value during the transience, the settling time is recorded as “0”. The WLSE-PEA, the HPLL, and the EGDSC-PLL have shown us good performance under this test. But the SRF-PLL’s estimations are inaccurate, especially under three-phase unbalance condition.

In Fig. 9, several disturbances occur at the same time to further test the FPS detection ability of the PEA. At 0.1 s, there is a phase jump (45°, on all the three phases), a voltage sag (30%, on all the three phases), and a frequency step (from 50 to 51 Hz). Meanwhile, some sequence components distort the grid voltages, including the dc offsets (phase a: 0.05 pu, phase b: 0.03 pu, phase c: 0.02 pu), the fundamental negative sequence (0.1 pu, −30°), the third-order positive sequence (0.05 pu, 40°), the third-order negative sequence (0.05 pu, 60°), the fifth-order positive sequence (0.05 pu, 45°), the seventh-order negative sequence (0.05 pu, 30°), the ninth-order positive sequence (0.05 pu, 40°), and the ninth-order negative sequence (0.05 pu, 60°). The detailed evaluation of settling time and error can be seen in Table IX. The WLSE-PEA is verified to be superior to the other three solutions according to Table IX.

The simulation results indicate that accurate estimations can be obtained from the WLSE-PEA, the HPLL, and the EGDSC-PLL under dc offsets, three-phase unbalance, and odd-order harmonics, while the SRF-PLL tuned for heavily distorted conditions shows small errors. The estimation error of the WLSE-PEA is acceptable under even-order harmonics distortion. But when the even-order harmonics distortions are serious, the HPLL, or the EGDSC-PLL can be a better choice. As to the dynamics, the

TABLE IX  
PERFORMANCE COMPARISON UNDER HARSH CONDITIONS

	WLSE-PEA	SRF-PLL	HPLL	EGDSC-PLL
$e_{\text{angle}}$ (rad)	0	<0.010	0	0
$t_{s_{\text{angle}}}$ (s)	0.025	0.148	0.038	0.043
$e_{\text{mag}}$ (V)	0	±4.1	0	0
$t_{s_{\text{mag}}}$ (s)	0.016	0.118	0.036	0.024
$e_{\text{freq}}$ (Hz)	0	±0.19	0	0
$t_{s_{\text{freq}}}$ (s)	0.023	N/A <sup>a</sup>	0.059	0.059

<sup>a</sup>The detected frequency in the steady state does not stay within 0.02 Hz around the real value.

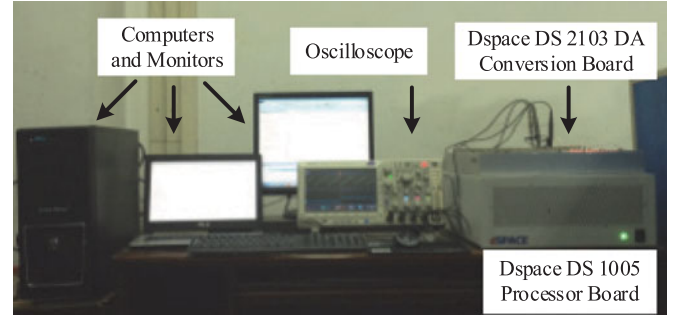


Fig. 10. Experimental setup.

WLSE-PEA is the fastest in most of the tests when phase jump, voltage sag, or frequency deviation occurs. The response speed of the HPLL and that of the EGDSC-PLL are roughly on the same level. The performance of the SRF-PLL is not satisfactory especially when phase jump or frequency deviation occurs.

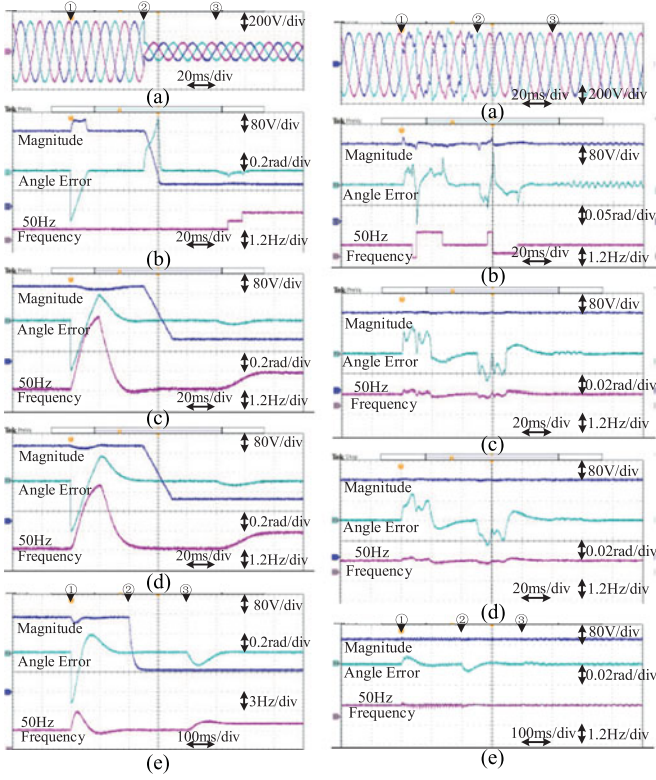
## VII. COMPARATIVE EXPERIMENTS

For better evaluation of the proposed PEA’s performance, the WLSE-PEA has been implemented on a dSPACE DS 1005 control board and the sampling frequency is 10 kHz for all the tests. All the experimental waveforms in this section are captured by the Tektronix MDO3024 mixed domain oscilloscope connected to the DS 2103 DAC board. The experimental setup can be appreciated in Fig. 10.

In this section, the tests are designed to be the same as that in the simulations to verify the WLSE-PEA’s ability of the FPS estimation and better present the transience when disturbances occur. The initial phase and magnitude of the grid voltages, the phase and, magnitude of the distortions added as well as the benchmarks are the same. Since the transience of the SRF-PLL is longer than the other three PLLs, the unit of its x-axis is longer (100ms/div or 40ms/div). The experimental results can be appreciated in Figs. 11 and 12.

In Fig. 11, the grid voltages of the comparative experiment I are the same as that in Fig. 6. The experiment results agree with the simulation results. All the four FPS detectors can estimate the magnitude, the angle, and the frequency accurately. The experiment verifies that the WLSE-PEA has the fastest dynamics and the HPLL’s and the EGDSC-PLL’s dynamics are also good compared with the SRF-PLL.





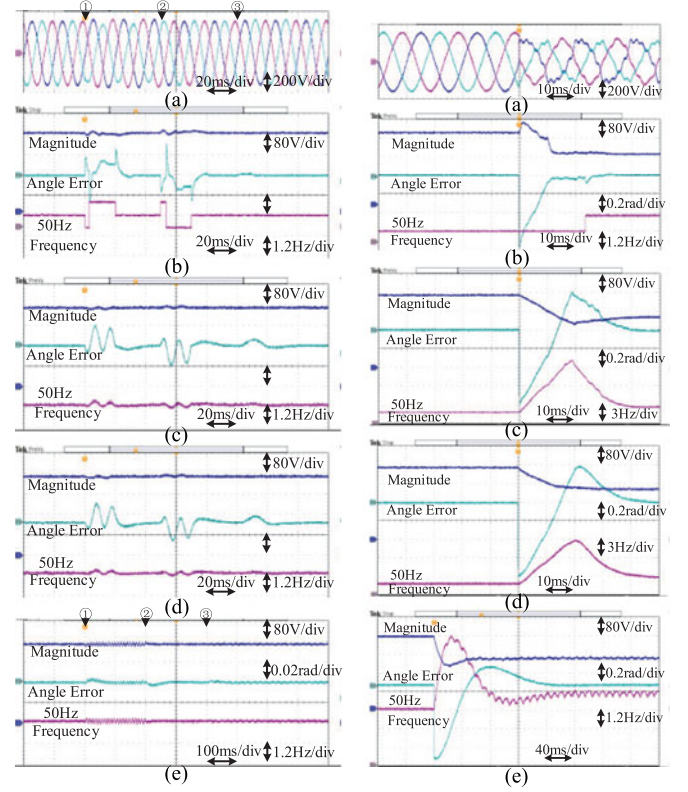
**Fig. 11.** Left: comparative experiment I, ①: phase jump, ②: voltage sag, ③: frequency deviation. Right: comparative experiment II, ①: odd-order harmonics, ②: recovery, ③: even-order harmonics. (a) Grid Voltages. (b) WLSE-PEA. (c) HPLL. (d) EGDSC-PLL. (e) SRF-PLL.

In Fig. 11, the grid voltages of the comparative experiment II are the same as that in Fig. 7. The experiment results agree with the simulation results. The experiment verifies that the HPLL and the EGDSC-PLL have better harmonics rejection ability. Also, the WLSE-PEA is immune to odd-order harmonic and shows small errors under even-order harmonics distortion.

In Fig. 12, the grid voltages of the comparative experiment III are the same as that in Fig. 8. The experiment results agree with the simulation results. The experiment verifies that all the four PLLs, except the SRF-PLL, are robust to three-phase unbalance and dc offsets.

In Fig. 12, the grid voltages of the comparative experiment IV are the same as that in Fig. 9. The experiment results agree with the simulation results. The WLSE-PEA, the HPLL, and the EGDSC-PLL are immune to the distortions added while errors exist in the SRF-PLL. The experiment verifies that the WLSE-PEA has the fastest dynamics, and the HPLL and the EGDSC-PLL have better response speed than the SRF-PLL.

The computational burden of the WLSE-PEA has been tested and compared with other advance solutions on the dSPACE hardware as shown in Table X. Since the hardware commonly used is a DSP rather than the dSPACE, the processing time in the test is normalized based on the processing time of the DSOGI-PLL [13]. As the one global cycle processing time of the DSOGI-PLL on the TMS320F28335 DSP is  $5.91 \mu\text{s}$  [38],



**Fig. 12.** Left: comparative experiment III, ①: unbalance, ②: recovery, ③: dc offset. Right: comparative experiment IV. (a) Grid Voltages. (b) WLSE-PEA. (c) HPLL. (d) EGDSC-PLL. (e) SRF-PLL.

**TABLE X**  
ONE GLOBAL CYCLE PROCESSING TIME

Methods	Time (per unit)
DSOGI-PLL	1.00
WLSE-PEA	2.20
HPLL [35]	1.64
EGDSC-PLL [36]	1.80

the computational burden of the WLSE-PEA is acceptable for practical applications.

To sum up, the WLSE-PEA has demonstrated its ability of accurately detecting the FPS component under most of the common distortions in the grid voltages with fast dynamics. The performance is better even compared with some advanced PLLs and the computational cost is acceptable.

## VIII. CONCLUSION

In this paper, a fast and robust PEA, the WLSE-PEA, has been proposed. In the algorithm, the MAF filters out all the odd-order harmonics and enables the WLSE to detect the fundamental positive-sequence component with fast dynamics. Furthermore, the ZCD and the FLL of the WLSE have been combined to improve the immunity of the detector to frequency deviations. Comparative simulations and experiments show that the WLSE-PEA has better dynamics than some PLLs and good accuracy under heavily distorted grid conditions.

## REFERENCES

- [1] J. P. Da Costa, H. Pinheiro, T. Degner, and G. Arnold, "Robust controller for DFIGs of grid-connected wind turbines," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4023–4038, Sep. 2011.
- [2] H. Geng, C. Liu, and G. Yang, "LVRT capability of DFIG-based WECS under asymmetrical grid fault condition," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2495–2509, Jun. 2013.
- [3] S. Alepuz, S. Busquets-Monge, J. Bordonau, J. A. Martinez-Velasco, C. A. Silva, J. Pontt, and J. Rodriguez, "Control strategies based on symmetrical components for grid-connected converters under voltage dips," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2162–2173, Jun. 2009.
- [4] P. Rodriguez, A. Luna, R. Teodorescu, and F. Blaabjerg, "Grid synchronization of wind turbine converters under transient grid faults using a double synchronous reference frame PLL," in *Proc. IEEE Energy 2030 Conf.*, Atlanta, GA, USA, 2008, pp. 1–8.
- [5] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1398–1409, Oct. 2006.
- [6] D. Dong, B. Wen, P. Mattavelli, D. Boroyevich, and Y. Xue, "Modeling and design of islanding detection using phase-locked loops in three-phase grid-interface power converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 4, pp. 1032–1040, Dec. 2014.
- [7] B. Yu, M. Matsui, and G. Yu, "A correlation-based islanding-detection method using current-magnitude disturbance for PV system," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2935–2943, Jul. 2011.
- [8] I. J. Balaguer, Q. Lei, S. Yang, U. Supatti, and F. Z. Peng, "Control for grid-connected and intentional islanding operations of distributed power generation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 147–157, Jan. 2011.
- [9] C. Cho, J. Jeon, J. Kim, S. Kwon, K. Park, and S. Kim, "Active synchronizing control of a microgrid," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3707–3719, Dec. 2011.
- [10] R. M. Santos Filho, P. F. Seixas, P. C. Cortizo, L. A. B. Torres, and A. F. Souza, "Comparison of three single-phase PLL algorithms for UPS applications," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2923–2932, Aug. 2008.
- [11] S. Chung, "A phase tracking system for three phase utility interface inverters," *IEEE Trans. Power Electron.*, vol. 15, no. 3, pp. 431–438, May 2000.
- [12] V. Kaura and V. Blasko, "Operation of a phase locked loop system under distorted utility conditions," *IEEE Trans. Ind. Appl.*, vol. 33, no. 1, pp. 58–63, Jan./Feb. 1997.
- [13] P. Rodriguez, R. Teodorescu, I. Candela, A. V. Timbus, M. Liserre, and F. Blaabjerg, "New positive-sequence voltage detector for grid synchronization of power converters under faulty grid conditions," in *Proc. 37th IEEE Power Electron. Spec. Conf.*, Jeju, South Korea, 2006, pp. 1–7.
- [14] M. Karimi-Ghartemani and M. R. Iravani, "A method for synchronization of power electronic converters in polluted and variable-frequency environments," *IEEE Trans. Power Syst.*, vol. 19, no. 3, pp. 1263–1270, Aug. 2004.
- [15] P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos, and D. Boroyevich, "Decoupled double synchronous reference frame PLL for power converters control," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 584–592, Mar. 2007.
- [16] A. Timbus, M. Liserre, R. Teodorescu, and F. Blaabjerg, "Synchronization methods for three phase distributed power generation systems—an overview and evaluation," in *Proc. IEEE Power Electron. Spec. Conf.*, Recife, Brazil, 2005, pp. 2474–2481.
- [17] D. Yazdani, M. Mojiri, A. Bakhshai, and G. Joos, "A fast and accurate synchronization technique for extraction of symmetrical components," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 674–684, Mar. 2009.
- [18] F. D. Freijedo, J. Doval-Gandoy, O. Lopez, and E. Acha, "Tuning of phase-locked loops for power converters under distorted utility conditions," *IEEE Trans. Ind. Appl.*, vol. 45, no. 6, pp. 2039–2047, Nov./Dec. 2009.
- [19] A. M. Salamah, S. J. Finney, and B. W. Williams, "Three-phase phase-locked loop for distorted utilities," *IET Elect. Power Appl.*, vol. 1, pp. 937–945, 2007.
- [20] A. Ghoshal and V. John, "A method to improve PLL performance under abnormal grid conditions," in *Proc. Nat. Power Electron. Conf.*, Bangalore, India, Dec. 2007, pp. 17–19.
- [21] E. Robles, S. Ceballos, J. Pou, J. Martin, J. Zaragoza, and P. Ibanez, "Variable-frequency grid-sequence detector based on a quasi-ideal low-pass filter stage and a phase-locked loop," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2552–2563, Oct. 2010.
- [22] E. Robles, J. Pou, S. Ceballos, J. Zaragoza, J. Martin, and P. Ibanez, "Frequency-adaptive stationary-reference-frame grid voltage sequence detector for distributed generation systems," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4275–4287, Sep. 2011.
- [23] S. Golestan, J. M. Guerrero, and A. Abusorrah, "MAF-PLL with phase-lead compensator," *IEEE Trans. Ind. Electron.*, vol. 62, no. 6, pp. 3891–3895, Jun. 2015.
- [24] J. Wang, J. Liang, F. Gao, L. Zhang, and Z. Wang, "A method to improve the dynamic performance of moving average filter based PLL," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5978–5990, Oct. 2015.
- [25] M. Karimi-Ghartemani, S. A. Khajehoddin, P. K. Jain, A. Bakhshai, and M. Mojiri, "Addressing DC component in PLL and notch filter algorithms," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 78–86, Jan. 2012.
- [26] S. Golestan, J. M. Guerrero, and G. B. Gharehpetian, "Five approaches to deal with problem of DC offset in phase-locked loop algorithms: design considerations and performance evaluations," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 648–661, Jan. 2016.
- [27] S. Golestan, J. M. Guerrero, A. M. Abusorrah, and Y. Al-Turki, "Hybrid synchronous/stationary reference-frame-filtering-based PLL," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 5018–5022, Aug. 2015.
- [28] S. Golestan, F. D. Freijedo, A. Vidal, A. G. Yepes, J. M. Guerrero, and J. Doval-Gandoy, "An efficient implementation of generalized delayed signal cancellation PLL," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1085–1094, Feb. 2016.
- [29] H. S. Song and K. Nam, "Instantaneous phase-angle estimation algorithm under unbalanced voltage-sag conditions," *Proc. Inst. Elect. Eng.—Gener., Transmiss. Distrib.*, vol. 147, pp. 409–415, 2000.
- [30] L. Zheng, H. Geng, and G. Yang, "Improved phase locked-loop under heavily distorted grid condition," in *Proc. 41st Annu. Conf. IEEE Ind. Electron. Soc.*, Yokohama, Japan, 2015, pp. 4778–4783.
- [31] F. D. Freijedo et al., "WLSE for fast, accurate and robust generation of references in power converter applications," in *Proc. IEEE Int. Symp. Ind. Electron.*, Bari, Italy, 2010, pp. 2946–2951.
- [32] M. Beza and M. Bongiorno, "Application of recursive least squares algorithm with variable forgetting factor for frequency component estimation in a generic input signal," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1168–1176, Mar./Apr. 2014.
- [33] M. K. Ghartemani, S. A. Khajehoddin, P. K. Jain, and A. Bakhshai, "Problems of startup and phase jumps in PLL systems," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1830–1838, Apr. 2012.
- [34] S. Golestan, M. Ramezani, J. M. Guerrero, F. D. Freijedo, and M. Monfared, "Moving average filter based phase-locked loops: Performance analysis and design guidelines," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2750–2763, Jun. 2014.
- [35] L. Wang, Q. Jiang, L. Hong, C. Zhang, and Y. Wei, "A novel phase-locked loop based on frequency detector and initial phase angle detector," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4538–4549, Oct. 2013.
- [36] F. D. Freijedo et al., "Grid-synchronization methods for power converters," in *Proc. 35th Annu. Conf. IEEE Ind. Electron. Soc.*, Porto, Portugal, 2009, pp. 522–529.
- [37] *Voltage Characteristics of Public Distribution System*, Standard EN 50160, Nov. 1999.
- [38] A. Luna, J. Rocabert, J. I. Candela, J. R. Hermoso, R. Teodorescu, F. Blaabjerg, and P. Rodriguez, "Grid voltage synchronization for distributed generation systems under grid fault conditions," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3414–3425, Jul./Aug. 2015.



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