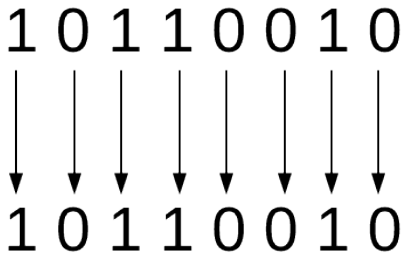
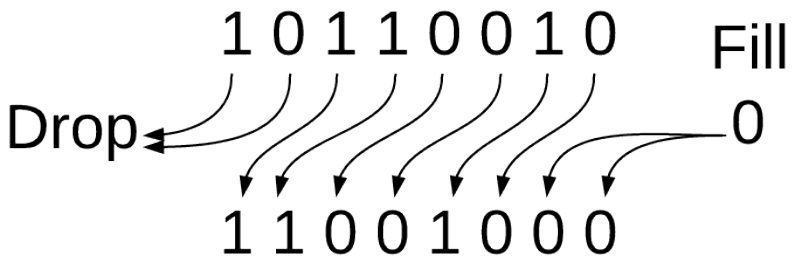
Shift Register

Shift Register



Shift Register



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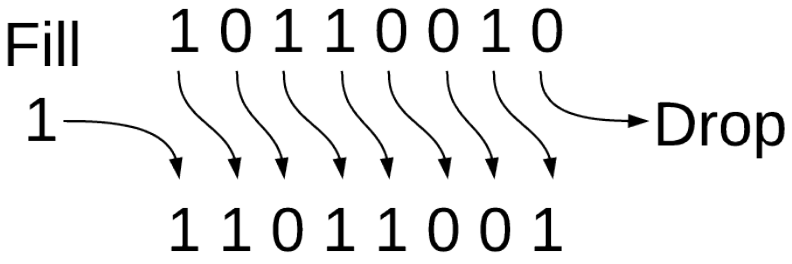

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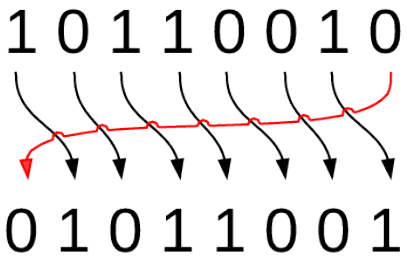
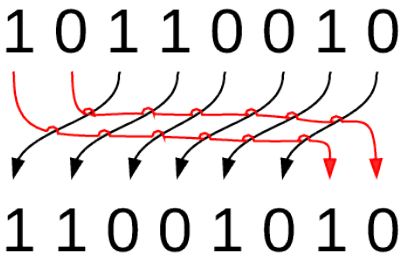
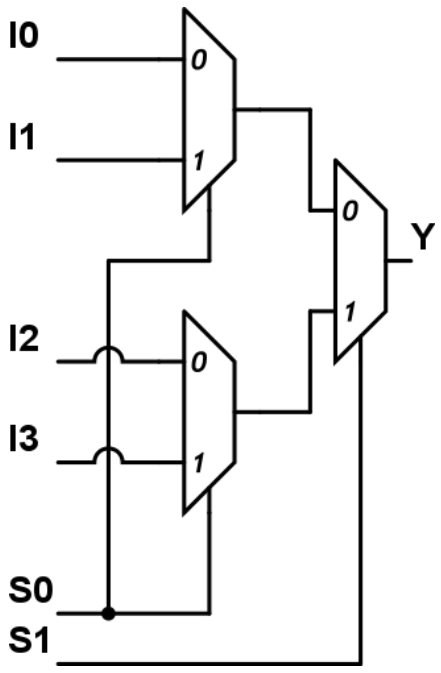


Shift Register



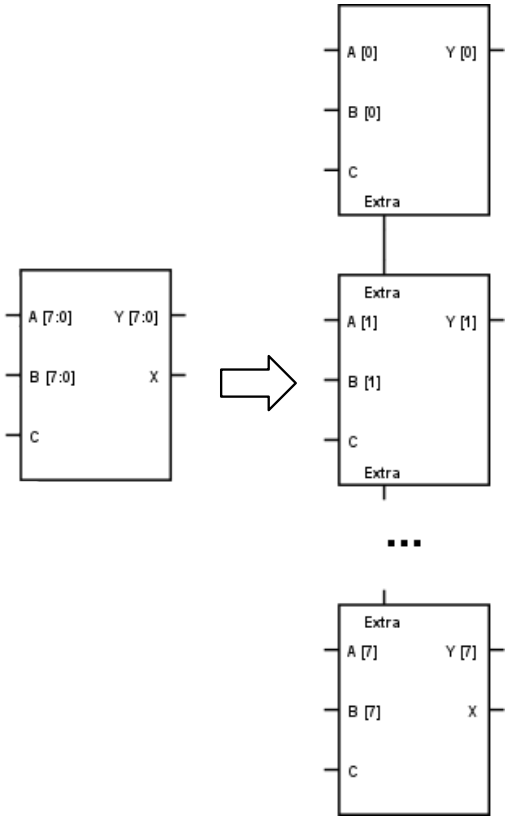
Complex Verilog Modules

MUX 4:1



Verilog Example

Bit Slice



Comparator

Comparator

A = 01011010
B = 11001110

0. 0 = 0
1. 1 = 1
2. 0 < 1
3. 1 = 1
4. 1 > 0
5. 0 = 0
6. 1 = 1
7. 0 < 1

Comparator

An	Bn	GTI	LTI	EQI	GTO	LTO	EQO
0	0						
0	0						
0	0						
0	1						
1	0						
1	1						
1	1						
1	1						

Comparator