Number Representation

Number Representation

Number Representation

Hex - Binary Conversion

Decimal to Binary

Decimal to Hex

Verilog

Verilog

Structural Design:

```
assign F = A & B;
assign Y = B | C;
```

Behavior Design:

```
always @(A or B or C)
    begin
        F = A & B;
        Y = B | C;
    end
```

Verilog Behavioral

Verilog Behavioral

Logical Operators

- !
- &&
- ||
- ==
- !=
- <
- >
- <=
- >=

Verilog Conditional

if ... else

```
if (A == 1)
    X = C;
else
    X = D;


if (A)
    X = C;
else
    X = D;
```

Verilog Conditional

```
if (A == 1)
    X = C;
else if (B == 1)
    X = D;
else
    X = E;

if ((A ==1) && (B == 1))
    X = C;
else
    X = D;
```

Verilog Conditional

```
if (A&B == 1)
    begin
        X = C;
        F = A;
    end
else
    begin
        X = D;
        F = B;
    end
```

Verilog

Verilog Number Formats

Verilog Memory

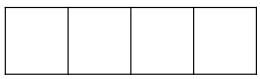
Verilog Vectors (Buses)

Verilog Vectors

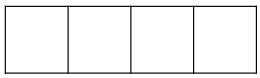
reg [3:0] A A

reg [0:3] B B

A = 4'b1010 A

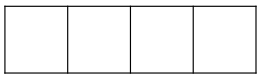


B = 4'b1010 B



Verilog Vectors

A = 4'b1010 A



Verilog Conditional

```
reg [1:0] select;

case (select)
    2'b00: F = A&B;
    2'b01: F = A|B;
    2'b10: F = A^B;
    default: F = A;
endcase
```

```
reg [1:0] select;

if (select == 2'b00)
    F = A&B;
else if (select == 2'b01)
    F = A|B;
else if (select == 2'b10)
    F = A^B;
else
    F = A;
```

Verilog Loops

for loop

```
reg [3:0] count;

for (count = 0; count < 4'b1111; count = count+1)
    begin
        ...
    end
```

while loop

```
while (A == 0)
    begin
        ...
    end
```