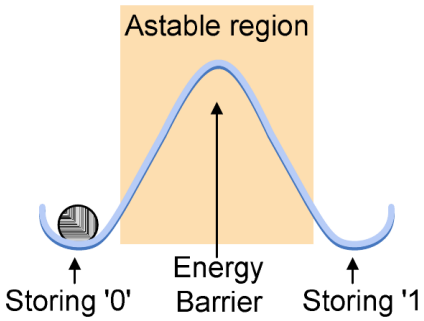
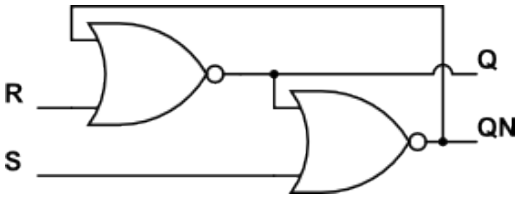
Digital Memory Circuits

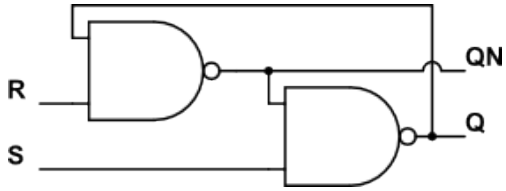
State Stability



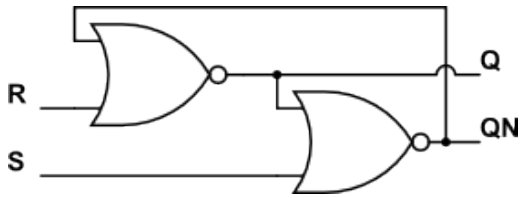
Basic Memory Cell

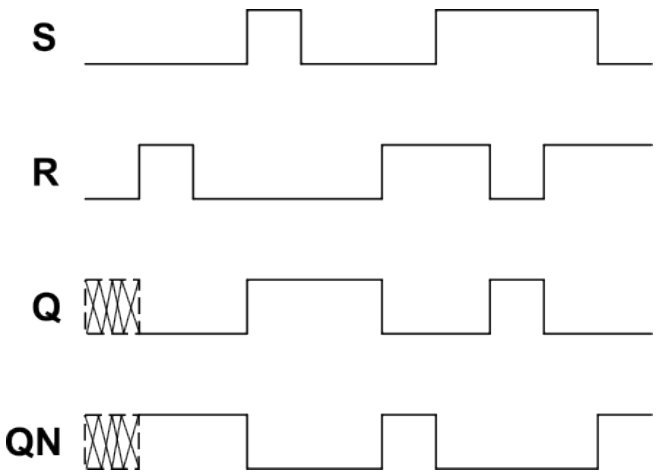
Inputs	Outputs



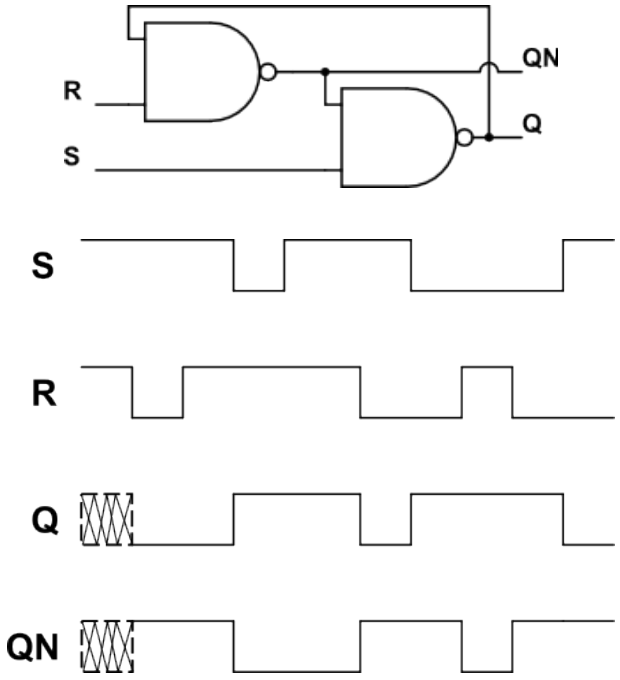


SR NOR Cell





SR NAND Cell



Basic Memory Cell

NOR Memory Cell

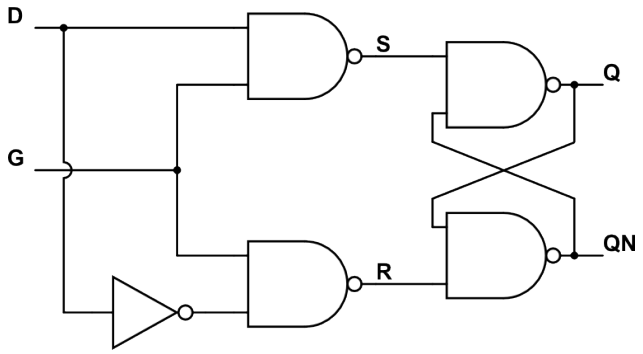
S	R	Q	QN
0	0		
0	1		
1	0		
1	1		

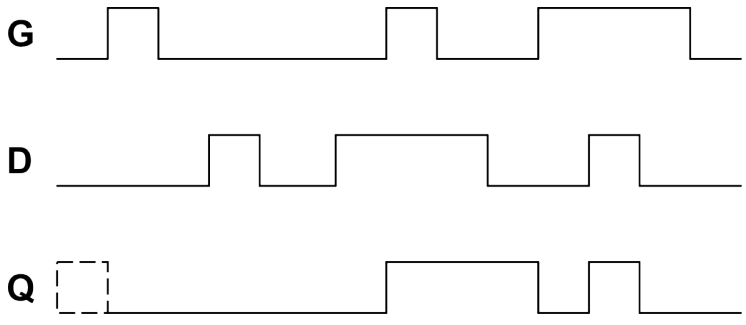
NAND Memory Cell

S	R	Q	QN
0	0		
0	1		
1	0		
1	1		

D-Latch

D-Latch





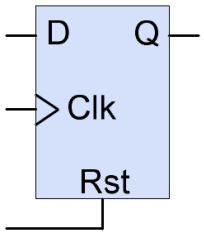
D-Latch

D - Memory Cell

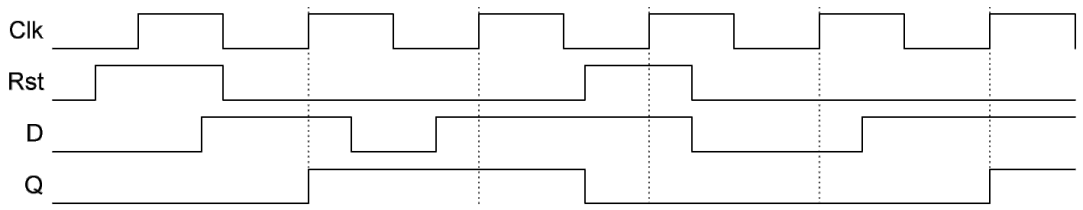
Latch vs Flip Flop

Reset Input

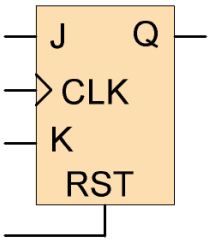
D - Flip Flop (DFF)



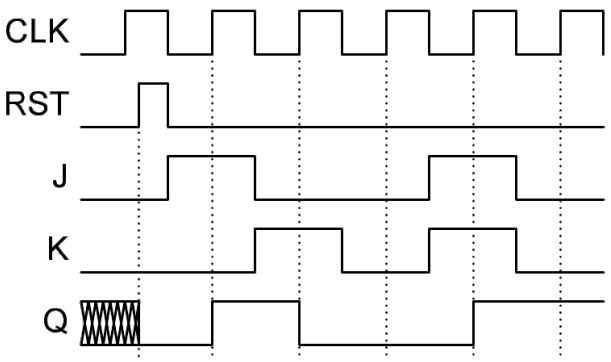
D	Q



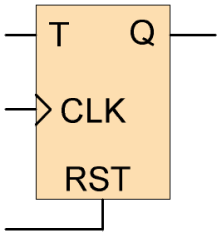
JK - Flip Flop



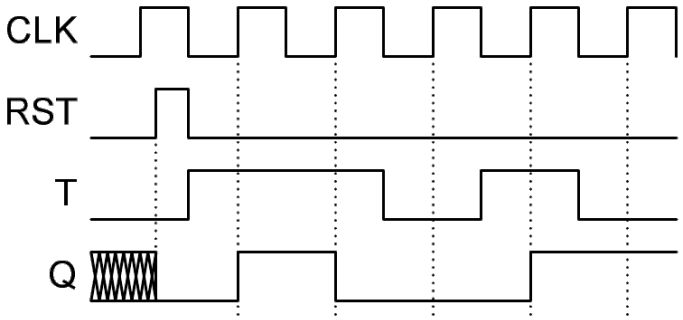
J K	Q



T - Flip Flop



T	Q



Registers