## **XOR** Function

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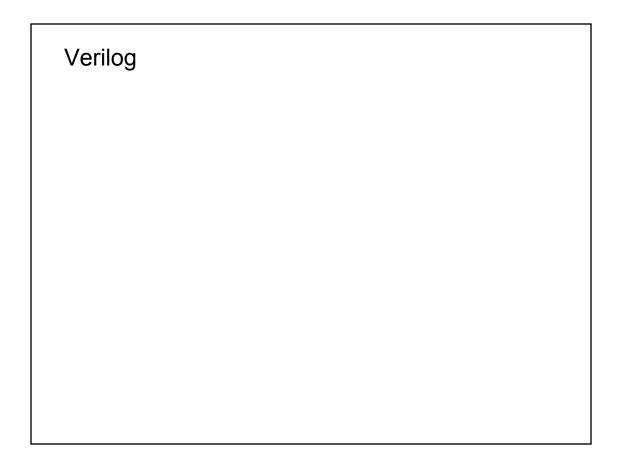
**XOR** Function

Control	Α	F
0	0	
0	1	
1	0	
1	1	

Nexys4 Board

Handriana Dasiera kafana FDOA
Hardware Design before FPGA
Hardware Design with FPGA

Digital Circuits	
g	
Hardware Description Language	



## Verilog

```
module module_name(
    input variable_name,
    input variable_name,
    output variable_name,
    output variable_name,
    );
endmodule
```

Verilog		
Verilog		

Bitwise Operators:

- ~
- &
- |
- ^

	X = A B F = X D	F = X D X = A B	X <= A B F <= X D	assign X = A B assign F = X D
A = 0 B = 0 D = 0				
A = 1				
B = 1				
B = 0				
A = 0				