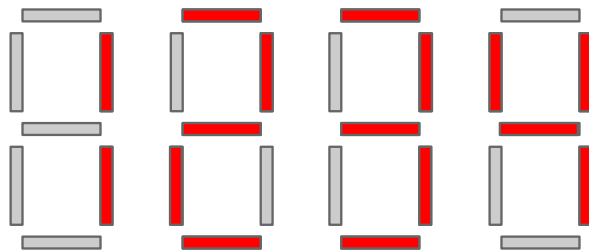# Nexys3 7 Segment LED

7 Segment LED

Display 1234 on Seven Segment

```verilog
reg [1:0] digit  = 2'b00;  // only 2 bits, initialize to 2'b00

always @( Refresh_Rate ) // 240+ Hz input
    begin
        case (digit)
            00: // display 4 at digit 0
            01: // display 3 at digit 1
            10: // display 2 at digit 2
            11: // display 1 at digit 3
        endcase
        digit = digit + 1;
    end
```