"Real World" Digital Circuits

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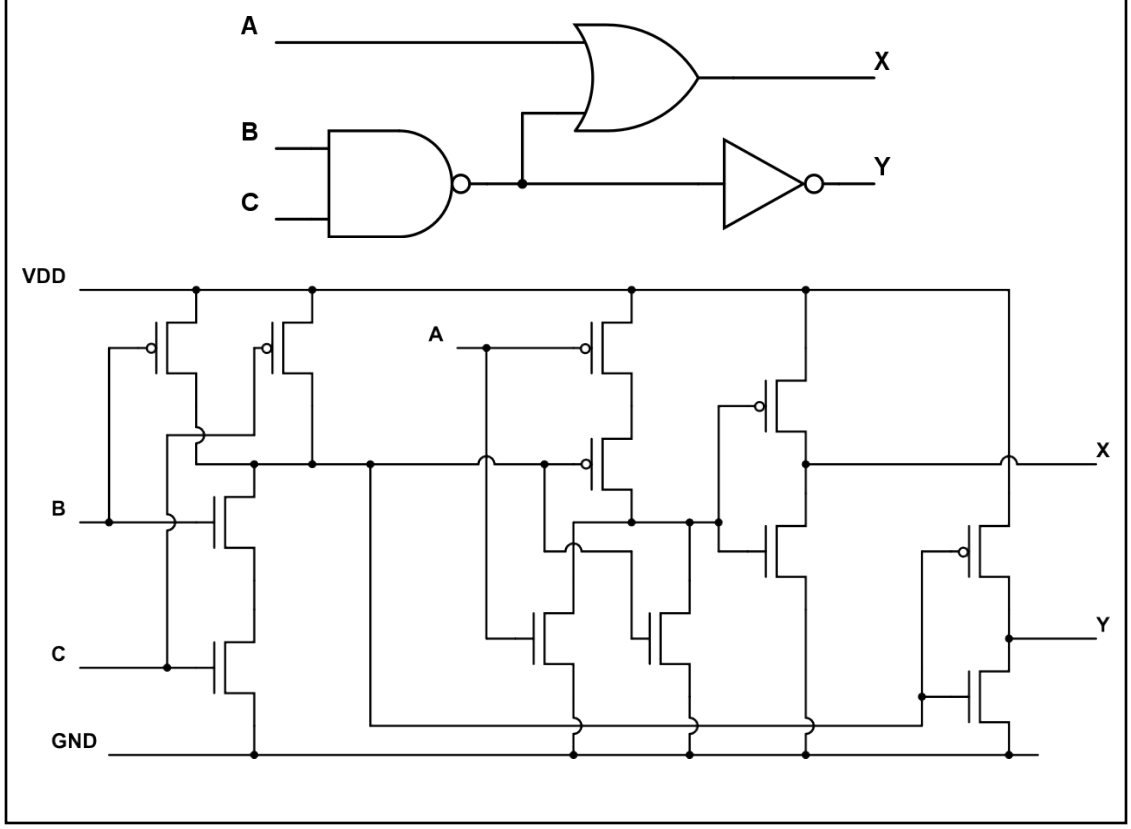
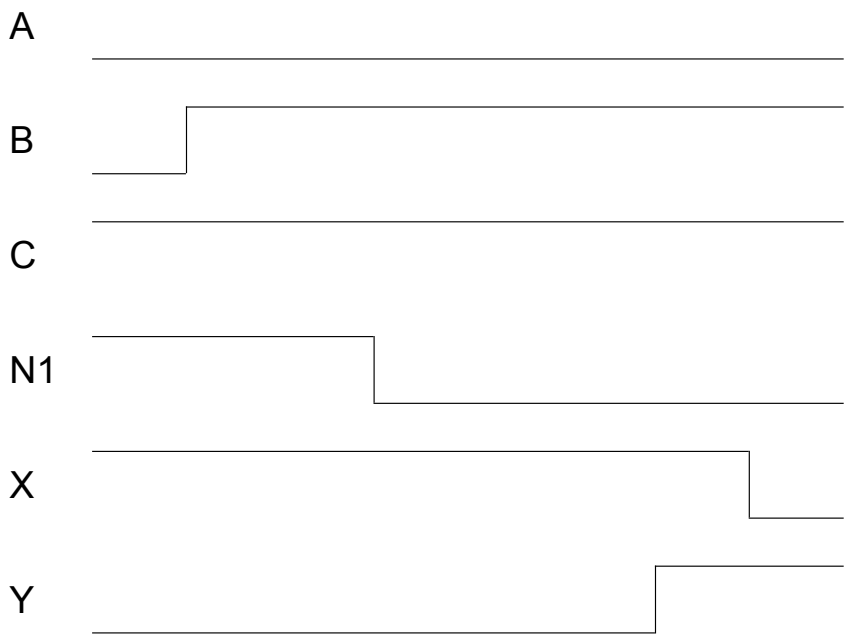
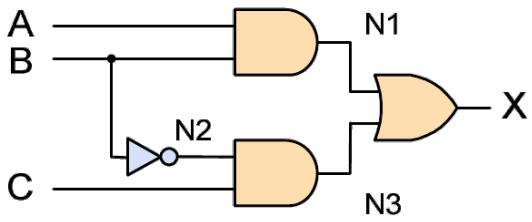
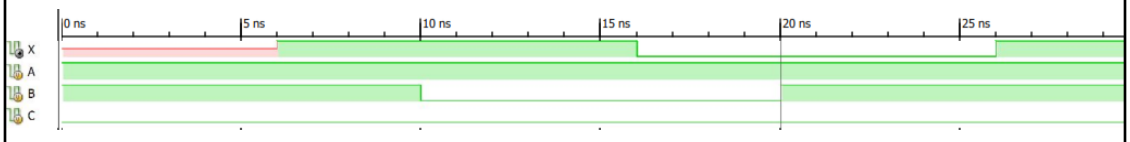




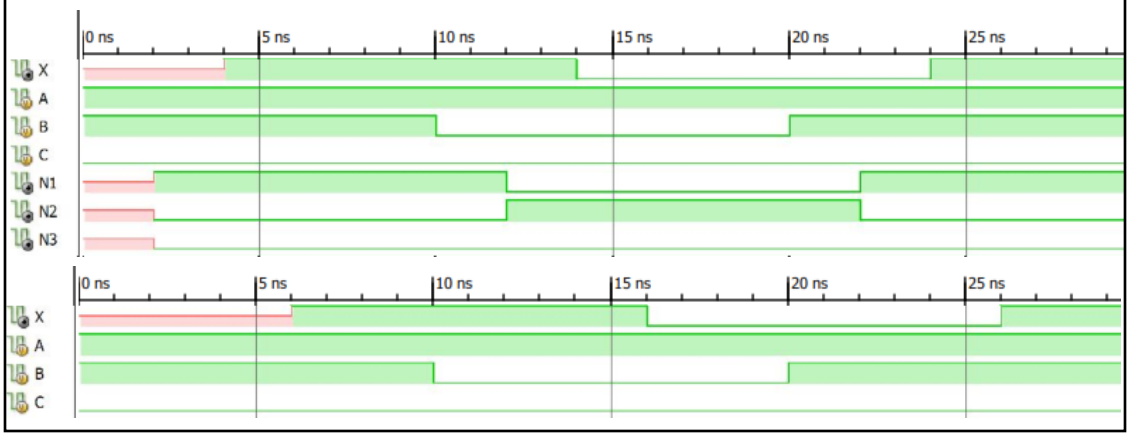
Simulating Propagation Delays

Pre-route Simulation



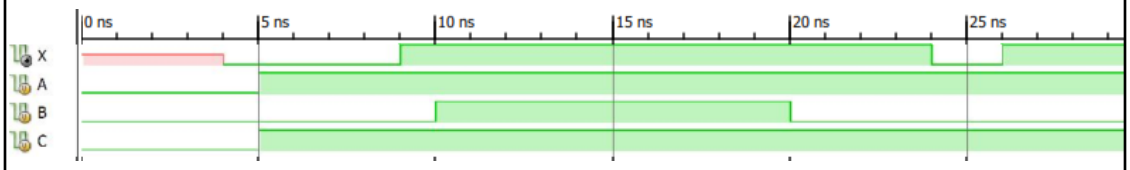


Pre-route Simulation



Glitches

Glitches



Glitches

A \ BC	0 0	0 1	1 1	1 0
0	0	1	0	0
1	0	1	1	1

Glitches

AB \ CD	00	01	11	10
00	0	1	0	0
01	0	1	1	1
11	0	0	1	1
10	0	0	0	0

AB \ CD	00	01	11	10
00	0	1	0	0
01	1	1	1	1
11	0	0	1	0
10	0	0	0	0

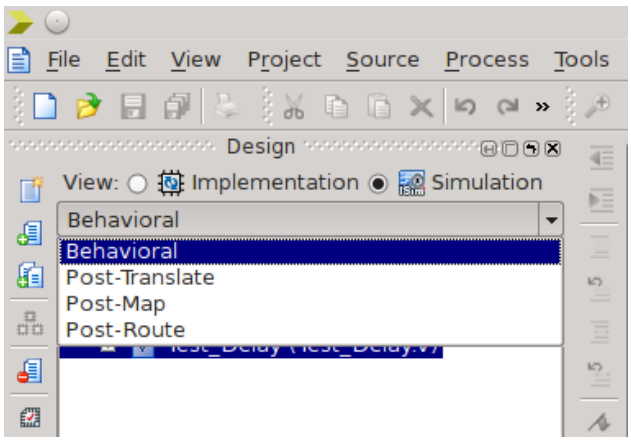
Glitches

AB \ CD	00	01	11	10
00	1	0	0	0
01	1	0	1	0
11	0	0	1	0
10	0	0	0	0

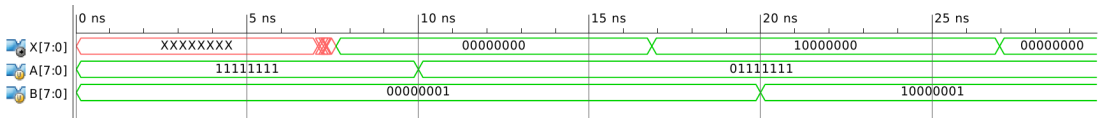
Fix Glitches

A \ BC	00	01	11	10
0	0	1	0	0
1	0	1	1	1

Post-Route Simulation



Post-Route Simulation



Settling Time