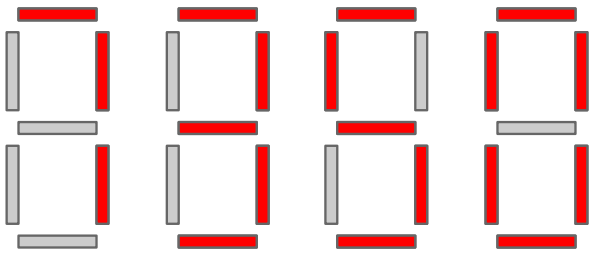
Project 8 - Stopwatch

Nexys3 7 Segment LED

7 Segment LED

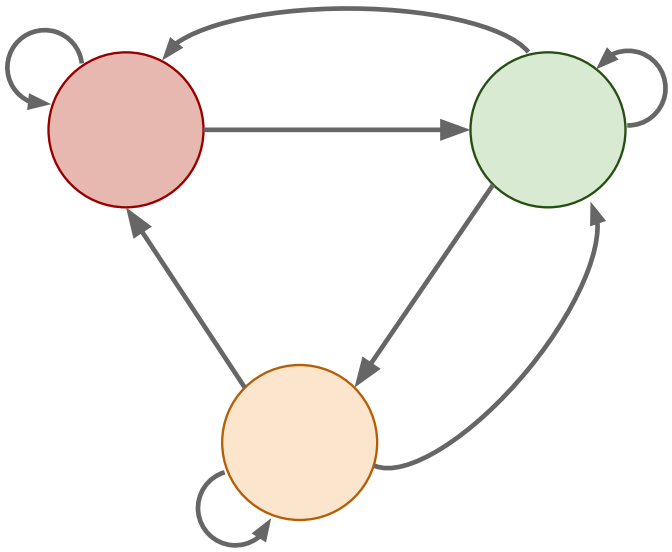


7 Segment LED

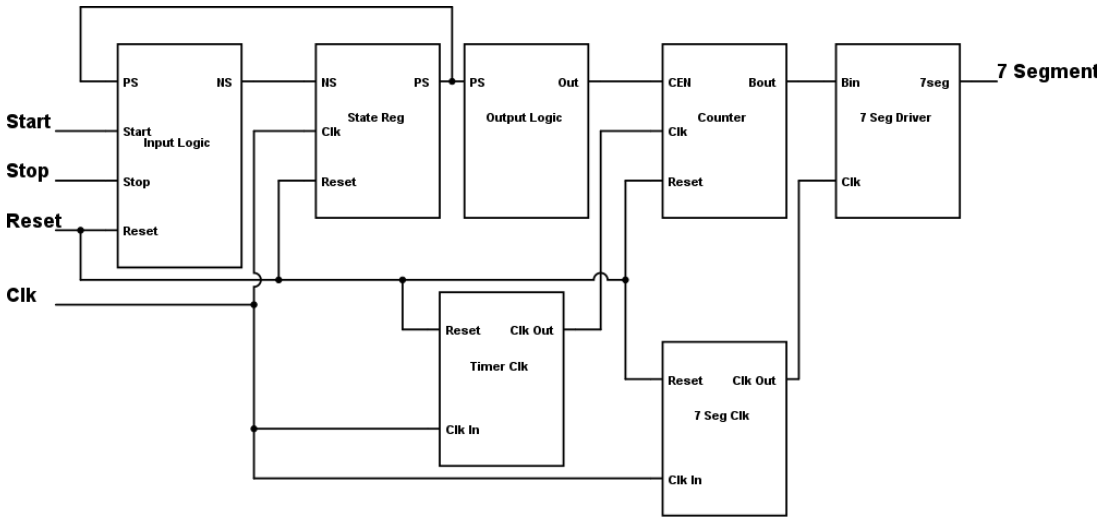
7 Segment Display

```
reg [1:0] digit  // only 2 bits, initialize to 2'b00

always @( Refresh_Rate )   // 240+ Hz input
    begin
        case (digit)
            00: // display digit 0 of time (hundredths of a second)
            01: // display digit 1 of time (tenths of a second)
            10: // display digit 2 of time (seconds)
            11: // display digit 3 of time (tens of seconds)
        endcase
        digit = digit + 1;
    end
```

Stopwatch

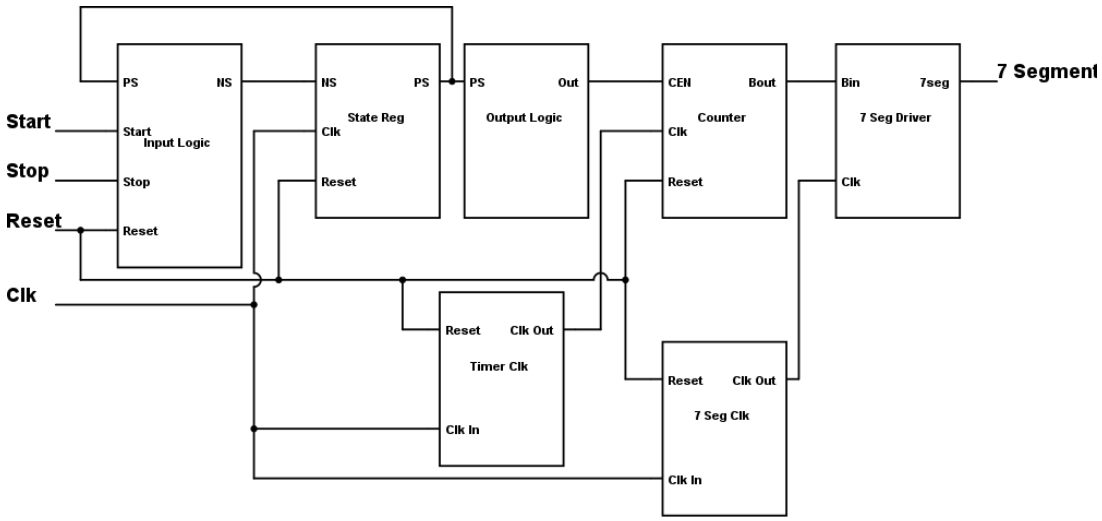


Stopwatch



Stopwatch Behavioral

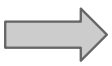
Stopwatch



WARNINGS!!!

Cannot change the same register from different always blocks

```
always @(A)
    begin
        X = 0;
    end

always @(B)
    begin
        X = 1;
    end
```



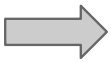
```
always @(A or B)
    begin


    end
```

WARNINGS!!!

Error Code:

Assignment under multiple single edges is not supported for synthesis

```
always @(posedge clk or posedge reset)
    begin
        if (reset == 1))
            B = 4'b0000;
        else if (enable == 1)
            B = B + 1;
        if ( B == 4'b1111)
            TC = 1;
        else
            TC = 0;
    end
```



```
else if (enable == 1)



end
```

WARNINGS!!!

Error Code:

A clock IOB / BUFGMUX clock component pair have been found that are not placed at an optimal clock IOB / BUFGMUX site pair. The clock IOB component <*Variable*> is placed at site <*Location*>

Fix:

Add line to the UCF file

NET "*Variable*" CLOCK_DEDICATED_ROUTE = FALSE;