Combinational Circuits

Multiplexer (MUX)

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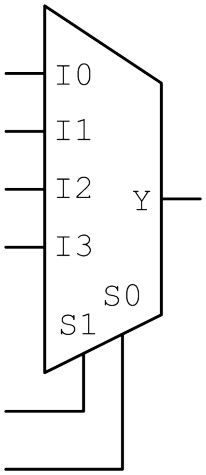


Multiplexer (MUX)

Behavioral Design

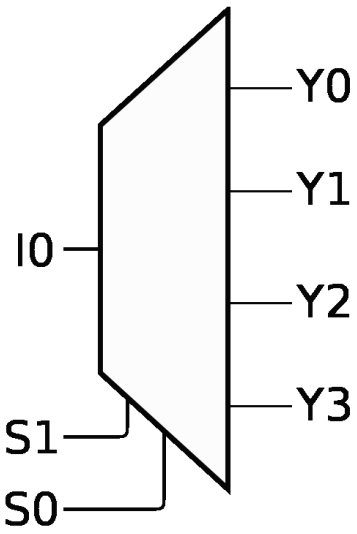
```
always @(I0,I1,I2,I3,S0,S1)
    begin
        case ({S1,S0})
            2'b00: Y = I0;
            2'b01: Y = I1;
            2'b10: Y = I2;
            2'b11: Y = I3;
        endcase
    end
```

Multiplexer (MUX)

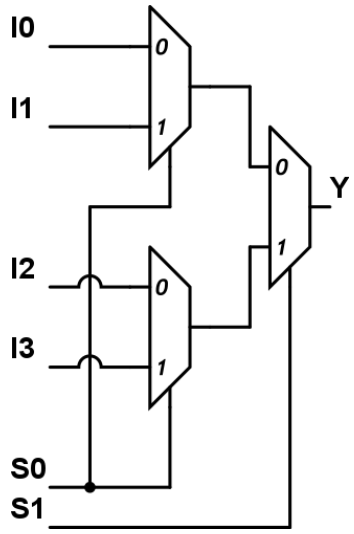
Structural Design

```
assign Y = (~S1 & ~S0 & I0) | (~S1 & S0 & I1) |
           (S1 & ~S0 & I2) | (S1 & S2 & I3);
```

Demultiplexer (DEMUX)

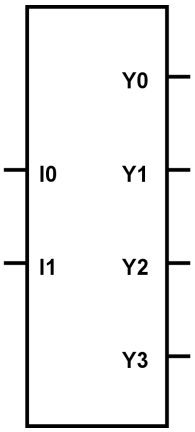


Multiplexer / Demultiplexer



Decoder

Binary Decoder



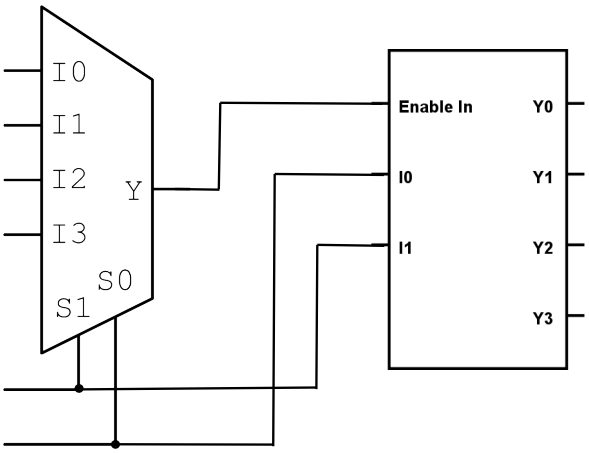
I1	I0	Y0	Y1	Y2	Y3
0	0				
0	1				
1	0				
1	1				

Binary Decoder (2:4)

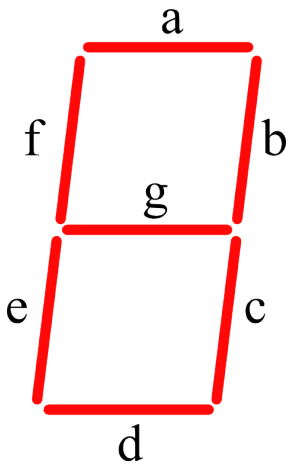
Behavioral Design

```
input [1:0] A
output reg [3:0] Y
always @(A)
    begin
        case (A)
            2'b00: Y = 4'b0001;
            2'b01: Y = 4'b0010;
            2'b10: Y = 4'b0100;
            2'b11: Y = 4'b1000;
        endcase
    end
```

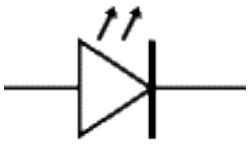
Enable In



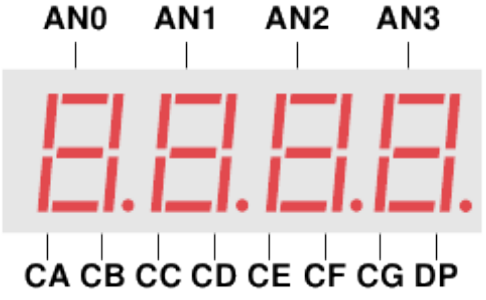
7 Segment Decoder



LED



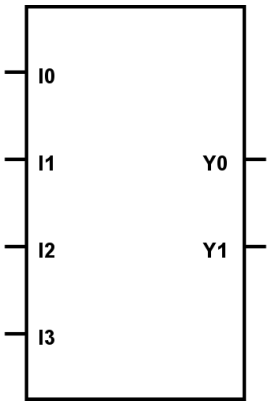
Nexys3 7 Segment LED



Nexys3 7 Segment LED

Priority Encoder

Priority Encoder



Priority Encoder

Priority Encoder