Project 3: Verilog Behavioral

I am submitting entirely my own work in this exercise, and I am aware of the penalties for cheating if I submit work that is not my own.

Name: _____ Date: _____

Demonstration

#	Demonstration	Pts	Score
2	Demo Circuit Design	10	
4	Demo Circuit Design	10	

Printouts

#	Submit	Pts	Score
1	Simulation	5	
3	Simulation	5	

Online Submission

#	Submit	Pts	Score
1	Verilog Module Source	5	
2	Verilog Module Source	5	
3	Verilog Module Source	5	
4	Verilog Module Source	5	

Problem 1. Create a *behavioral* Verilog module for a 4-input, 2-output logic system that behaves according to the two logic equations shown. Simulate your design to verify it behaves correctly. Print and submit your simulation plot. Submit your Verilog module file online.

$$X = \overline{A \cdot D \oplus B \cdot C \cdot D} + \overline{B} \cdot (A + C) \cdot D \oplus \overline{A \cdot D}$$

$$Y = \overline{A \cdot \overline{D}} + B \cdot (A \oplus D) \cdot B + C \cdot \left(\overline{A} + B\right)$$

Problem 2. Amy, Baker, Cathy, and David, the bean buyers for the "Overhead Coffee Company", have designed a more complex voting system to decide when to buy new beans. Design and implement a *behavioral* verilog module that they can use to indicate whether they should buy new beans. Use slide switches for vote entry (either "buy" or "not buy"), and an LED to indicate when beans should be purchased. A “buy” order is placed if:

Amy, Cathy, and David vote NO and Baker votes YES,
or Amy and Baker vote NO and the rest vote YES,
or Amy and David vote YES and the rest vote NO,
or David votes NO and the others vote YES,
or Cathy votes Yes and the others vote No,
or David and Cathy vote YES and Baker votes NO,
or Amy votes NO and the others vote YES,
or Baker and David votes NO and the others vote YES,
or Cathy vote YES and the others vote NO,
or they all vote YES.

After you have verified the circuit through simulation, download it to the Basys3 board, using four slide switches as inputs, and a single LED as output. Submit your Verilog module file online and demonstrate your Basys3 board in class.

For programming the Basys3 board use the following switches and LEDs

Amy: Switch 3 Output: LED 7
Baker: Switch 2
Cathy: Switch 1
David: Switch 0

Problem 3. Six judges are scoring a particular event, and they need a device to indicate particular judgments. Each judge can enter “pass” or “fail" with a single switch. Write a *behavioral* Verilog module that can indicate two separate conditions: The motion passed (4 or more “pass” votes), or the motion failed (3 or more “fail” votes). Simulate your design to verify it behaves correctly. Print and submit your simulation plot. Submit your Verilog module file online.

Problem 4. Create a *behavioral* Verilog module for a four-input, three-output circuit that behaves according to the truth table shown below.

A	B	C	D	F	G	H
0	0	0	0	1	1	0
0	0	0	1	1	0	0
0	0	1	0	0	0	1
0	0	1	1	0	0	0
0	1	0	0	1	1	1
0	1	0	1	0	1	0
0	1	1	0	0	0	0
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	1	0	1
1	0	1	0	0	1	1
1	0	1	1	1	0	1
1	1	0	0	1	1	1
1	1	0	1	0	0	1
1	1	1	0	0	1	0
1	1	1	1	1	0	1

After you have verified the circuit through simulation, download it to the Basys3 board, using four slide switches as inputs, and a three LEDs as outputs. Submit your Verilog module file online and demonstrate your Basys3 board in class.

For programming the Basys3 board use the following switches and LEDs

A: Switch 3
B: Switch 2
C: Switch 1
D: Switch 0

F: LED 0
G: LED 1
H: LED 2