TISE:

send: $[x \to dto\uparrow \square \neg x \to dfo\downarrow]; [di]; co\uparrow; [\neg ci]; dto\downarrow, dfo\downarrow; [\neg di]; co\downarrow; [ci]$

recieve: $[\quad \wedge dto \to x\uparrow \square \quad \wedge dfo \to x\downarrow]; [ci]; co\downarrow; [\neg dto \wedge \neg dfo]; do\downarrow; [\neg ci]; co\uparrow$

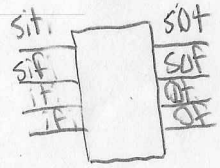
multibit:

send: $(|||i :: [x_i \to dto_i\uparrow \square \neg x_i \to dfo_i\downarrow)]; [di]; co\uparrow; [\neg ci]; (|||i :: dto_i\downarrow, dfo_i\downarrow); [\neg di]; co\downarrow; [ci]$

recieve: $(|||i :: [dto_i \to x_i\uparrow$ (updated) $\square\ dfo_i \to x_i\downarrow]$ (updated); $do\downarrow; [ci]; co\downarrow; [\neg(\neg dto_1 \wedge \neg dfo_1 \dots \neg dto_n \wedge \neg dfo_n)]; do\downarrow; [\neg ci]; co\uparrow$

$\widetilde{in}$: $(dto_1 \vee dfo_1) \wedge \dots (dto_n \vee dfo_n)$

$\neg\widetilde{in}$: $(\neg dto_1 \wedge \neg dfo_1) \vee \dots (\neg dto_n \wedge \neg dfo_n)$

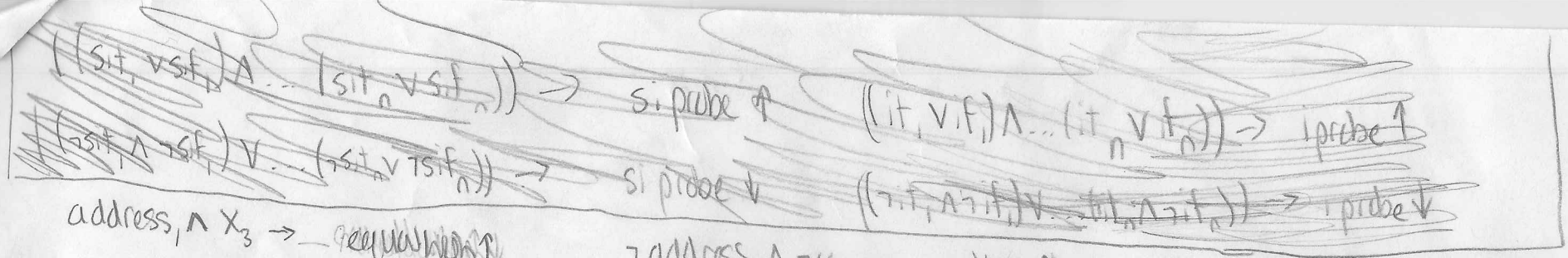


PRS:

$$\left[\begin{array}{l} \neg ci \wedge ((dto_1 \wedge x_1) \vee (dfo_1 \wedge \neg x_1)) \wedge \dots ((dto_n \wedge x_n) \vee (dfo_n \wedge \neg x_n)) \to do\uparrow, ready?\downarrow, si?\downarrow \\ \neg dto_1 \wedge \neg dfo_1 \dots \neg dto_n \wedge \neg dfo_n \to do\downarrow \end{array}\right.$$
$$\left.\begin{array}{l} \to co\downarrow \\ \neg ci \to co\uparrow \end{array}\right] \begin{array}{l} c \text{ is } i \\ d \text{ is } i \text{ or } si \text{ (same pos for both)} \\ si? \text{ goes up for } si \text{ and down for } i \end{array}$$

$$\left[\begin{array}{ll} di \to & co\uparrow \\ \neg di \to & co\downarrow, ready?\uparrow, \end{array}\right. \qquad \left.\begin{array}{l} \neg ci \to (|||i :: dto_i\downarrow, dfo_i\downarrow) \end{array}\right] \begin{array}{l} c \text{ is } o \\ d \text{ is } o \text{ or } so \end{array}$$

$$\left[\begin{array}{l} ((sit_1 \vee sif_1) \wedge \dots (sit_n \vee sif_n)) \wedge ((\neg it_1 \wedge \neg if_1) \vee \dots (\neg it_n \wedge \neg if_n)) \vee (((it_1 \vee if_1) \wedge \dots (it_n \vee if_n)) \wedge (\neg sit_1 \wedge \neg sif_1) \vee \dots (\neg sit_n \wedge \neg sit_n)) \\ \vee (((sit_1 \vee sif_1) \wedge \dots (sit_n \vee sif_n)) \wedge ((it_1 \vee if_1) \wedge \dots (it_n \vee if_n)) \wedge \\ \quad ((it_1 \wedge (((it_1 \vee if_1) \wedge \dots (it_n \vee if_n)) \wedge ((\neg sit_1 \wedge \neg sif_1) \vee \dots (\neg sit_n \wedge \neg sif_n))) \vee (((it_1 \vee if_1) \wedge \dots (it_n \vee if_n)) \wedge ((sit_1 \vee sif_1) \wedge \dots (sit_n \vee sif_n)) \\ \quad \text{two wire} \ \wedge \neg si?) \wedge ready?) \to \vee (sit_1 \wedge ((((sit_1 \vee sif_1) \wedge \dots (sit_n \vee sif_n)) \wedge ((\neg it_1 \wedge \neg if_1) \vee \dots (\neg it_n \wedge \neg if_n))) \vee (((sit_1 \vee sif_1) \wedge \dots (sit_n \vee sif_n)) \\ \quad \wedge (((it_1 \vee if_1) \dots (it_n \vee if_n)) \wedge ((si?_0 \wedge si?_1) \vee (\neg si?_0 \wedge \neg si?_1))))) \wedge ready? \to x_i\uparrow \\ (((if_1 \wedge \text{'' '' '' same as above '' '' ''}) \vee (sif_1 \wedge \text{'' '' '' same as above '' '' ''})) \wedge ready? \to x_i\downarrow \\ (i0) \wedge \neg ready? \wedge x_0 \wedge x_1 \wedge (((address_1 \wedge x_3) \vee (\neg address_1 \wedge \neg x_3)) \wedge \dots ((address_m \wedge x_{m+2}) \vee (\neg address_m \wedge \neg x_{m+2}))) \to flag\uparrow \\ \wedge i0 \wedge \neg ready? \wedge x_0 \wedge x_1 \wedge (((\neg address_1 \wedge x_3) \vee (address_1 \wedge \neg x_3)) \wedge \dots ((address_m \wedge \neg x_{m+2}) \vee (\neg address_m \wedge x_{m+2}))) \to flag\downarrow \\ flag \to \wedge \ ready? \wedge \neg x_0 \wedge \neg x_1 \wedge i0 \to flag\to, \ si?\to \end{array}\right.$$



$address_1 \wedge X_3 \rightarrow$ equiv two ↑

$\neg address_1 \vee \neg X_3 \rightarrow$ equiv two ↓

$\neg address_1 \wedge \neg X_3 \rightarrow$ equiv two ↑

$X_3 \vee address_1 \rightarrow$ equiv two ↓

These are extended

$\neg address_1 \wedge X_3 \rightarrow$ not equiv one ↑

$address_1 \vee \neg X_3 \rightarrow$ not equiv one ↓

$address_1 \wedge \neg X_3 \rightarrow$ no equiv two ↑

$\neg address_1 \vee X_3 \rightarrow$ not equiv two ↓

These are extended

$si^2_1 \wedge si^2_0 \rightarrow s_i^2 s_i$ twinkle ↑

$\neg si^2_1 \vee \neg si^2_0 \rightarrow s_i^2 s_i$ ↓

$\neg si^2_1 \wedge \neg si^2_0 \rightarrow s_i^2$ idle ↑

$si^2_1 \vee si^2_0 \rightarrow s_i^2$ idle ↓

$X_0 \wedge \neg X_1 \wedge flag \rightarrow$ not og two ↓

$\neg X_0 \vee X_1 \vee \neg flag \rightarrow$ not og two ↑

$\neg X_0 \wedge \neg X_1 \wedge \rightarrow$ not og three ↓

$X_0 \vee X_1 \rightarrow$ not og three ↑

$\neg ready^2_0 \wedge X_0 \wedge X_1 \wedge ((\neg$ not equiv high$_0 \vee \neg$ not equiv low$_0) \wedge \ldots (\neg$ not equiv high$_m \wedge \neg$ not equiv two$_m$)) $\rightarrow flag_1 \uparrow$

$X_1 \wedge \neg ready^2_0 \wedge flag_1 \wedge flag_0 \wedge (\ldots) \rightarrow ot_1 \uparrow$

$\neg X_1 \wedge \neg ready^2_0 \wedge flag_1 \wedge flag_0 \wedge (\ldots) \rightarrow of_1 \uparrow$

$X_1 \wedge \neg ready^2_0 \wedge \neg flag_0 \wedge flag_1 \wedge (\ldots) \rightarrow sot_1 \uparrow$

$\neg X_1 \wedge \neg ready^2_0 \wedge \neg flag_0 \wedge flag_1 \wedge (\ldots) \rightarrow sof_1 \uparrow$

$(\neg si t_1 \wedge \neg si f_1) \vee \ldots (i t_n \wedge (\neg i f_1 \vee i t_1) \wedge \ldots (\neg i f_n \vee i t_n)) \wedge si^2_1 \wedge \neg si^2_0 \rightarrow i ready_1 \uparrow$

$(si t_1 \vee si f_1) \wedge \ldots (si t_n \wedge ((\neg i f_1 \wedge i t_1) \vee \ldots (\neg i f_n \wedge \neg i t_n)) \vee si^2_1 \vee si^2_0 \rightarrow i ready_1 \downarrow$

$(si t_1 \vee si f_1) \wedge \ldots (si t_n \vee si f_n)) \wedge ((i t_1 \vee i f_1) \wedge \ldots (i t_n \vee i f_n)) \rightarrow$ both up ↑

$(\neg si t_1 \wedge \neg si f_1) \vee \ldots (\neg si t_n \vee \neg si f_n)) \rightarrow$ both up ↓

$(si t_1 \vee si f_1) \wedge \ldots (si t_n \vee si f_n)) \rightarrow s_i$ probe ↑

$(\neg si t_1 \wedge \neg si f_1) \vee \ldots (\neg si t_n \vee \neg si f_n)) \rightarrow s_i$ probe ↓

$((i t_1 \vee i f_1) \wedge \ldots (i t_n \vee i f_n)) \rightarrow i$ probe ↑

$((\neg i f_1 \wedge \neg i f_1) \vee \ldots (\neg i t_n \wedge \neg i t_n)) \rightarrow i$ probe ↓

$cIU \wedge ready^2_0 \rightarrow xcoeff \uparrow$

$\neg cIU \vee \neg ready^2_0 \rightarrow xcoeff \downarrow$

$xcoeff \wedge ((i t_1 \wedge$ ready$) \vee (si t_1 \wedge (si$ ready$)) \vee (si t_1 \wedge ready^2_0 \wedge ((i f_1 \vee i t_1) \wedge \ldots (i t_n \vee i f_n)) \wedge si^2_1 \wedge \neg si^2_0) \vee (si f_1 \wedge ((si f_1 \vee si t_1) \wedge \ldots (si f_n \vee si t_n)) \wedge (si^2 si \vee si^2$ idle$))) \rightarrow X_1 \downarrow$

$sit_i \wedge x_i \rightarrow situpdatedhigh_i \uparrow$ $\quad sif_i \wedge \neg x_i \rightarrow situpdatedlow_i \uparrow$ $\quad it_i \wedge x_i \rightarrow itupdatedhigh_i \uparrow$ $\quad if_i \wedge \neg x_i \rightarrow itupdatedlow_i \uparrow$

$\neg sit_i \vee \neg x_i \rightarrow situpdatedhigh_i \downarrow$ $\quad \neg sif_i \vee x_i \rightarrow situpdatedlow_i \downarrow$ $\quad \neg it_i \vee \neg x_i \rightarrow itupdatedhigh_i \downarrow$ $\quad \neg if_i \vee x_i \rightarrow itupdatedlow_i \downarrow$

$\neg c_{i_1} \wedge ((situpdatedhigh_1 \vee situpdatedlow_1) \wedge \dots (situpdatedhigh_n \vee situpdatedlow_n)) \rightarrow s_i o \uparrow, ready^2 \downarrow, si^2_{i_1} \uparrow, si^2_{i_0} \uparrow$

$\neg sit_1 \wedge \neg sif_1 \wedge \dots \neg sit_n \wedge \neg sif_n \rightarrow s_i o \downarrow$

$\neg c_{i_1} \wedge ((itupdatedhigh_1 \vee ifupdatedlow_1) \wedge \dots (itupdatedhigh_n \vee ifupdatedlow_n)) \rightarrow i o \uparrow, ready^2 \downarrow, s_{i_1} \uparrow$

$\neg it_1 \wedge \neg if_1 \wedge \dots \neg it_n \wedge \neg if_n \rightarrow i o \downarrow$

$\neg ready^2 \wedge si^2_{i_1} \wedge c_{i_1} \rightarrow c_i o \downarrow$

$\neg c_{i_1} \rightarrow c_i o \uparrow$

$s o_i \vee o_i \rightarrow c o c \uparrow$

$\neg s o_i \vee \neg o_i \rightarrow c o o \downarrow$

$(\neg c o_i \rightarrow sot_i \downarrow, suf_i \downarrow, ot_i \downarrow, of_i \downarrow)$ $\quad \neg c o_i \wedge (\neg s o_i \vee \neg o_i) \rightarrow ready^2 \uparrow$

$\neg iuponly \wedge (\neg bothup \vee \neg si^2_{i_1} \vee si^2_{i_0}) \rightarrow \_ix high \uparrow$

$iuponly \vee (bothup \wedge si^2_{i_1} \wedge \neg si^2_{i_0}) \rightarrow \_ix high \downarrow$

$ready^2 \vee \neg x_0 \vee \neg x_1 \rightarrow \_flagcoeff \uparrow$

$si^2_{i_1} \wedge o_i \wedge \neg ready^2 \wedge x_0 \wedge x_1 \rightarrow \_flagcoeff \downarrow$

$siuponly \vee (bothup \wedge (si^2\_si \vee si^2\_idle)) \rightarrow \_six high \downarrow$

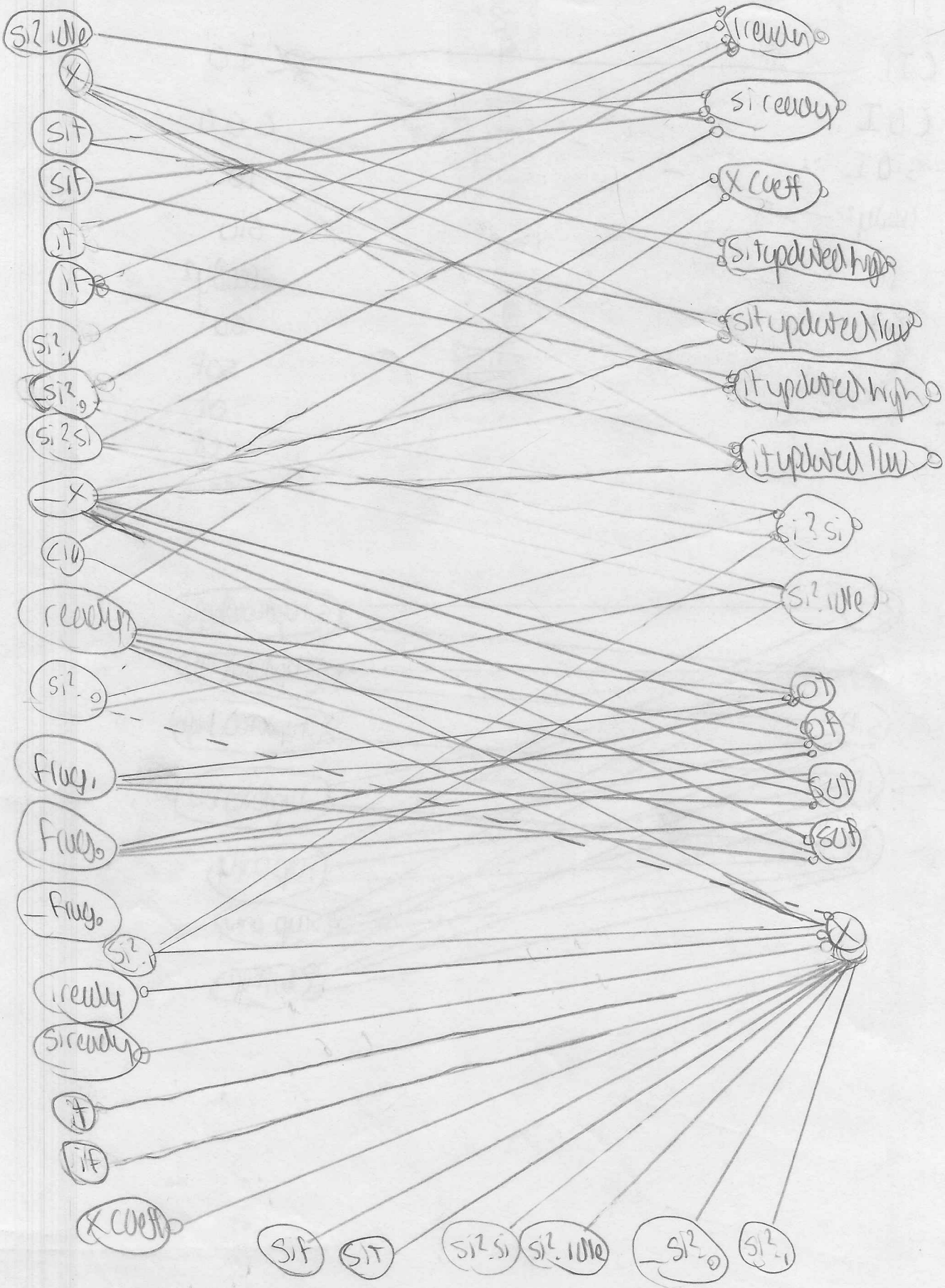
$\neg siuponly \wedge (\neg bothup \vee (\neg si^2\_si \wedge \neg si^2\_idle)) \rightarrow \_six high \uparrow$

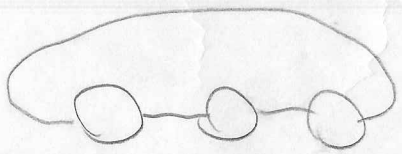
$\neg ready^2 \rightarrow \_ready^2 \uparrow$ $\quad \neg c o_i \rightarrow \_co_i \uparrow$

$ready^2 \rightarrow \_ready^2 \downarrow$ $\quad c o_i \rightarrow \_co_i \downarrow$

$ready^2 \wedge \neg x_0 \wedge \neg x_1 \rightarrow flag_1 \downarrow, flag_0 \downarrow, si^2_{i_1} \downarrow, si^2_{i_0} \downarrow$

$\neg ready^2 \wedge x_0 \wedge x_1 \rightarrow flag_1 \uparrow$ $\quad \neg ready^2 \wedge ((equalhigh_1 \vee equallow_1) \wedge \dots (equalhigh_m \vee equallow_m)) \rightarrow flag_0 \uparrow$


Si2_idle
X
Sit
Sit
it
it
Si2_1
Si2_0
Si_2_Si
_X
CIO
ready
Si2_0
Flag1
Flag0
_Flag0
Si2_1
iready
Siready
it
it
X coeff
Sit
Sit
Si2_Si
Si2_idle
_Si2_0
Si2_1
iready
Si ready
X coeff
Si_updated high
Sit updated low
it updated high
it updated low
Si_2_Si
Si2_idle
OT
Of
SUT
SUf
X

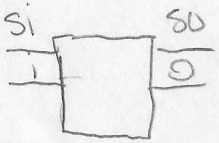


Header phits and Data phits — phit is n bits and type is one bit
(11) (10)
address length m

end phit is 00 with data

if there is a waiting phit at internal and external node input, route the one that has started or the internal input first

one direction and checking node address against destination address - two bit flag



$[\overline{s_i} \wedge \neg \overline{i} \rightarrow$ ready$_i$; $s_i?x$; $[x_0 \wedge x_1 \rightarrow [$address$_{node}$ == $x_{address} \rightarrow$ flag$\uparrow$; $s_i?\uparrow$; ready$\uparrow$; $o!x$ $[]$ address$_{node}$!= $x_{address} \rightarrow$ flag$\uparrow$; $s_i?\uparrow$; $so!x$; ready$\uparrow$; $]$ $[]$

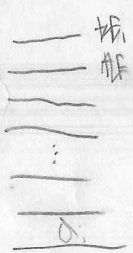
$x_0 \wedge \neg x_1 \rightarrow [$ flag $\rightarrow$ $o!x$ $[]$ $\neg$ flag $\rightarrow$ $so!x$ $]$ $[]$

$\neg x_0 \wedge \neg x_1 \rightarrow [$ flag $\rightarrow$ $o!x$; flag $\rightarrow$ $s_i?\rightarrow$; $]$ $[]$ $\neg$ flag $\rightarrow$ $so!x$; flag $\rightarrow$ $s_i?\rightarrow$; $]$ $]$ $[]$

$\neg \overline{s_i} \wedge \overline{i} \rightarrow$ $i?x$; "x" $\wedge$ "i" $[]$ %(except $s_i?$ goes down for a header before getting reset)

$\overline{s_i} \wedge \overline{i} \rightarrow [s_i? \rightarrow s_i?x$; "i" "$s_i$" in protocol" " $[]$
$\neg s_i? \rightarrow i?x$; "" ; in protocol"" $[]$
$(s_i? \rightarrow) \rightarrow s_i?x$; "" "$s_i$ in protocol"" $]]$ ← combine

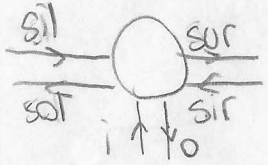
Handshake protocol:



control:
$co\uparrow$; $[c_i]$; $co\downarrow$; $[\neg c_i]$

data:
$[dti \vee dfi]$; $do\uparrow$; $[\neg dti \vee \neg dfi]$; $do\downarrow$; $sen: [x \rightarrow dti\uparrow [] \neg x \rightarrow dfi\uparrow]; [c_i]$;

interleaved:
$rel: [dti \vee dfi]$; $co\uparrow$; $[c_i \wedge dti \rightarrow x\uparrow [] c_i \wedge dfi \rightarrow x\downarrow]$, $do\uparrow$; $[\neg dti \vee \neg dfi]$; $co\downarrow$; $[\neg c_i]$; $do\downarrow$



x_0x_1 - header
x_3 - direction

$[\overline{sil} \wedge \neg\overline{sir} \wedge \neg\overline{i} \rightarrow sil?.x;\ ready?.\downarrow;\ [x_0 \wedge x_1 \rightarrow [address_{node} == x_{address} \rightarrow flag\uparrow;\ sil?._1\uparrow;\ sil?._0\uparrow;\ 0!x;\ ready\uparrow\ []$
$address_{node} != x_{address} \rightarrow flag\downarrow;\ sil?._1\uparrow,\ sil?._0\uparrow;\ sor!x;\ ready\uparrow]\ []$

$x_0 \wedge \neg x_1 \rightarrow [flag \rightarrow 0!x;\ ready?\uparrow\ []$
$\neg flag \rightarrow sor!x;\ ready?\uparrow][]$

$\neg x_0 \wedge \neg x_1 \rightarrow [flag \rightarrow 0!x;\ flag \rightarrow;\ si? \rightarrow;\ ready?\uparrow\ []$
$\neg flag \rightarrow sor!x;\ flag \rightarrow;\ si? \rightarrow;\ ready?\uparrow]]\ []$

$\overline{sir} \wedge \neg\overline{sil} \wedge \overline{i} \rightarrow$ """""" same as above but receive from sir, $sil?._1$ only goes up """""" []
$i \wedge \overline{sir} \wedge \overline{sil} \rightarrow [x_3 \rightarrow$ ' ' ' ' '

[' ' ' ' ' '
$address_{node} != x_{address} \rightarrow flag\downarrow;\ sil?._1\downarrow;\ sil?._0\uparrow;\ [x_3 \rightarrow sor!x;$ ready
$\neg x_3 \rightarrow sol!x;$ ' ' ' ' '
$[flag \wedge x_3 \rightarrow 0!x;\ ready?\uparrow\ []$
$\neg flag \wedge x_3 \rightarrow sor!x;\ ready?\uparrow\ []$
$\neg flag \wedge \neg x_3 \rightarrow sol!x;\ ready?\uparrow][]$
$[flag \rightarrow 0!x;\ flag \rightarrow;\ si? \rightarrow;\ ready?\uparrow\ []$
$\neg flag \wedge x_3 \rightarrow sor!x;\ flag \rightarrow;\ si? \rightarrow;\ ready?\uparrow\uparrow[]$
$\neg flag \wedge \neg x_3 \rightarrow sol!x;\ flag \rightarrow;\ si? \rightarrow;\ ready?\uparrow][]$

$\overline{i} \wedge \overline{sil} \wedge \neg\overline{sir} \rightarrow [sil?._1 \wedge sil?._0 \rightarrow sil?.x\ []$
$sil?._0 \wedge \neg sil?._1 \rightarrow i?.x\ []$
$\neg sil?._0 \wedge \neg sil?._1 \rightarrow sil?.x\ ]$

$\overline{i} \wedge \overline{sir} \wedge \neg\overline{sil} \rightarrow [sil?._1 \wedge \neg sil?._0 \rightarrow sir?.x\ []$
$\neg sil?._1 \wedge sil?._0 \rightarrow i?.x\ []$
$\neg sil?._1 \wedge \neg sil?._0 \rightarrow sir?.x\ ]$

!!!!! rest is the same !!!!!

$sil?._1 \wedge \neg sil?._0 \rightarrow sil?.x\ []$
$sil?._0 \wedge \neg sil?._1 \rightarrow i?.x\ []$

rest is the same