Digital Systems

Physics 5430

Wiatrowski Chapter 2

Homework

New homework assignment:

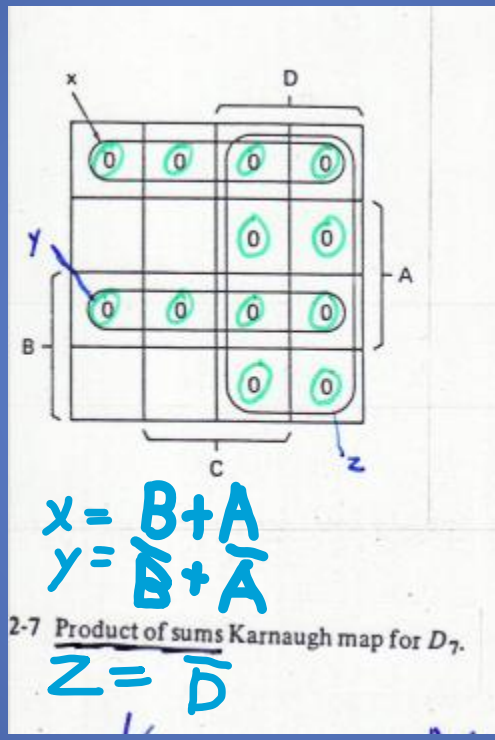
Chapter 2, Problem #10-a.

Chapter 2 Review

Reference pg 60

If your design has more 0's than 1's, it may be easier to use Product Of Sums (POS) Kmaps instead of Sum Of Products (SOP).

The x circle is where A = 0 and B = 0, so it should be zero when both of them are zero. The y circle is where A = 1 and B = 1, it should be zero when both of them are 1. The z circle should be zero when D = 1.



2-7 Product of sums Karnaugh map for D_7.

Table 2-4 Product of sums for D_7

D	C	B	A	D_7	OR function
0	0	0	0	0	$D+C+B+A$
0	0	0	1	1	
0	0	1	0	1	
0	0	1	1	0	$D+C+\overline{B}+\overline{A}$
0	1	0	0	0	$D+\overline{C}+B+A$
0	1	0	1	1	
0	1	1	0	1	
0	1	1	1	0	$D+\overline{C}+\overline{B}+\overline{A}$
1	0	0	0	0	$\overline{D}+C+B+A$
1	0	0	1	0	$\overline{D}+C+B+\overline{A}$
1	0	1	0	0	$\overline{D}+C+\overline{B}+A$
1	0	1	1	0	$\overline{D}+C+\overline{B}+\overline{A}$
1	1	0	0	0	$\overline{D}+\overline{C}+B+A$
1	1	0	1	0	$\overline{D}+\overline{C}+B+\overline{A}$
1	1	1	0	0	$\overline{D}+\overline{C}+\overline{B}+A$
1	1	1	1	0	$\overline{D}+\overline{C}+\overline{B}+\overline{A}$

$D_7 = (D+C+B+A)(D+C+\overline{B}+\overline{A})(D+\overline{C}+B+A)(D+\overline{C}+\overline{B}+\overline{A})$
$(\overline{D}+C+B+A)(\overline{D}+C+B+\overline{A})(\overline{D}+C+\overline{B}+A)(\overline{D}+C+\overline{B}+\overline{A})$
$(\overline{D}+\overline{C}+B+A)(\overline{D}+\overline{C}+B+\overline{A})(\overline{D}+\overline{C}+\overline{B}+A)(\overline{D}+\overline{C}+\overline{B}+\overline{A})$

$D_7 = (B+A)(B'+A')(D')$

Wired Logic Functions

Reference pg 73.

The “Wired OR” function works with emitter-coupled logic (**ECL**) – it is **obsolete** now.

The “Wired AND” function works with transistor-transistor logic (TTL)… but the chips must have open collector outputs!

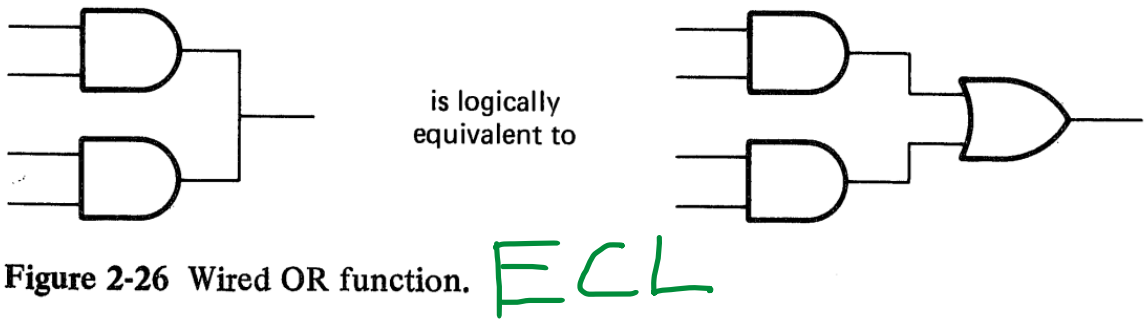


Figure 2-26 Wired OR function. ECL

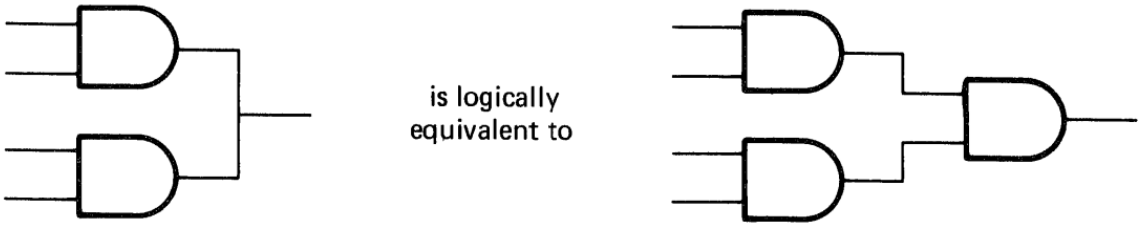
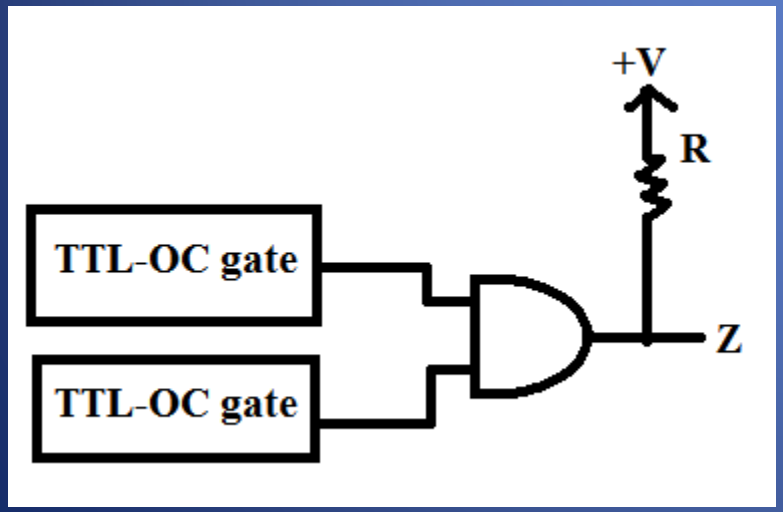


Figure 2-27 Wired AND function. TTL

Must know type of gate (ECL or TTL) to know if Wired-Or Wired-AND

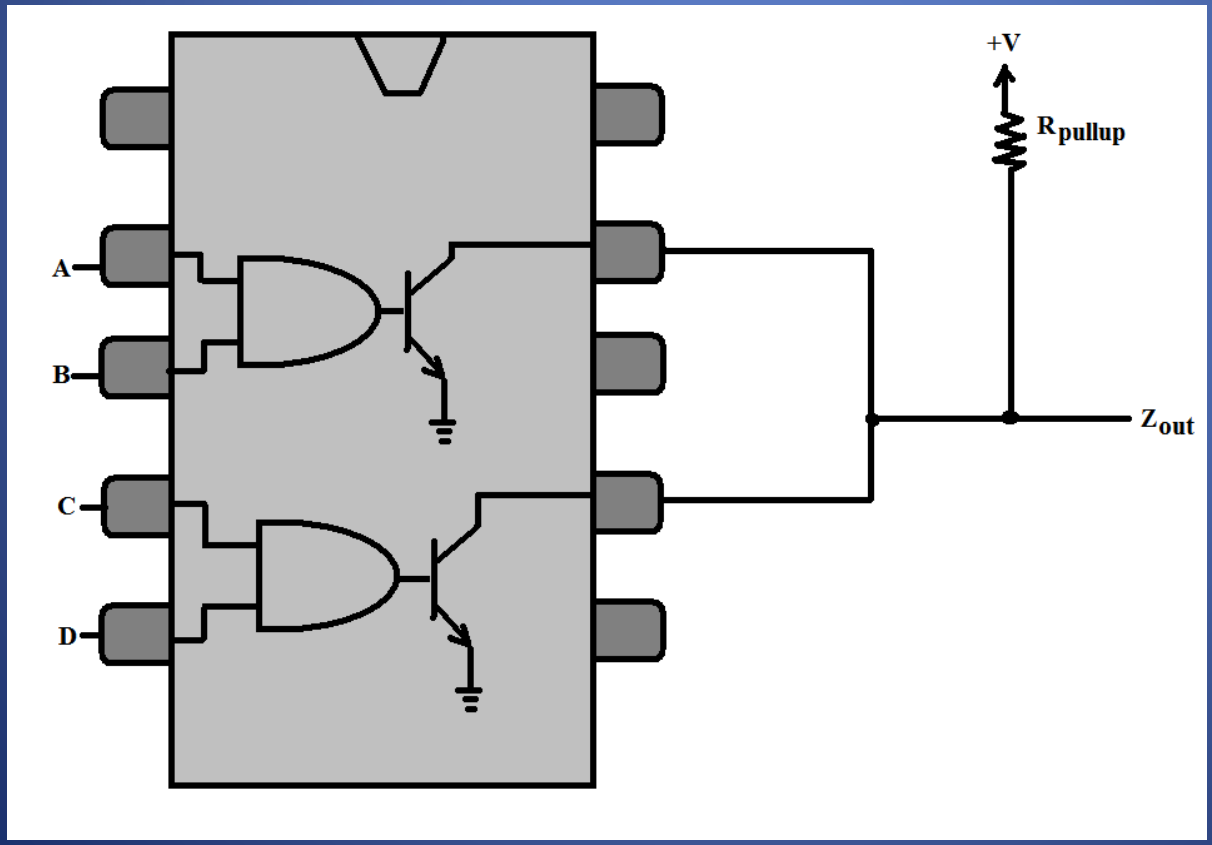
TTL Wired Logic

TTL-OC (open collector) yields a wired AND function **if** an external pull-up resistor is added. **Any** type of TTL-OC gate, NAND, NOR, AND, etc. will give a wired AND because the gate's output can pull the output line low.



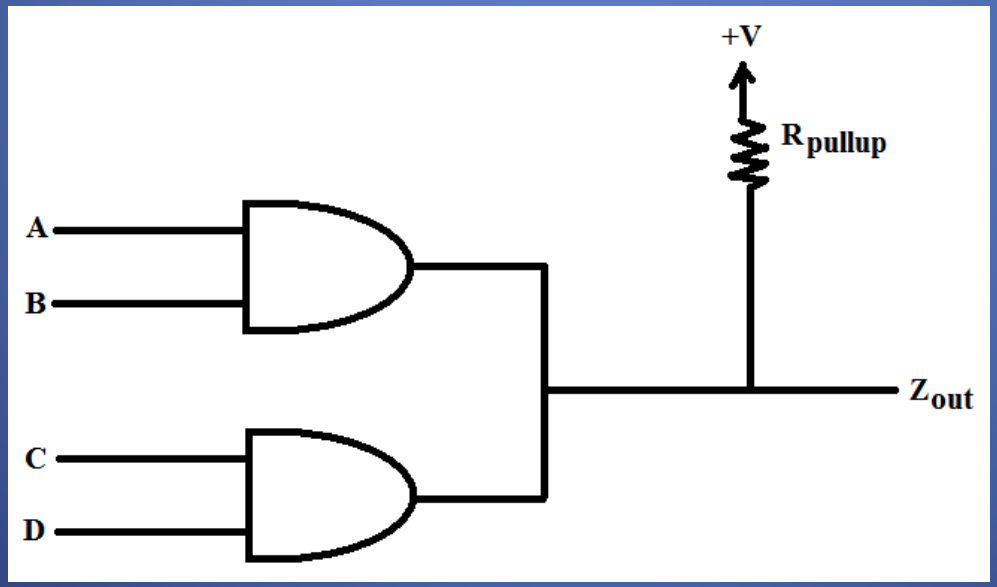
Simple Wired AND Example

Notice that the “open collectors” on the output transistors can not make the output high by themselves. The pull-up resistor must be used.



TTL Wired Logic

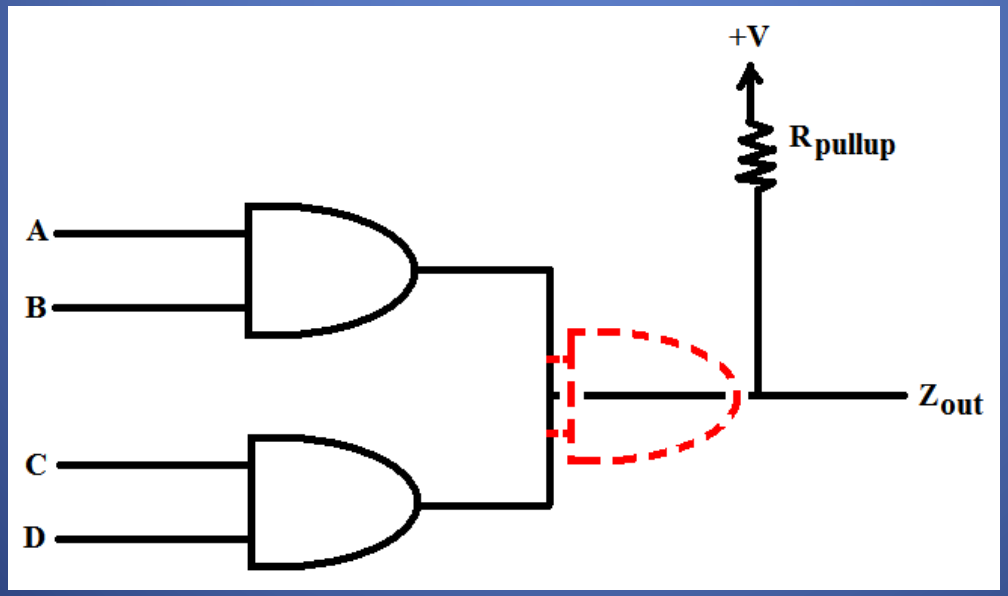
Although you have been taught to never tie outputs together, the following circuit is valid... as long as the outputs are open collector!



TTL Wired Logic

The connection simulates the AND function.

How???



Simple Wired AND Example

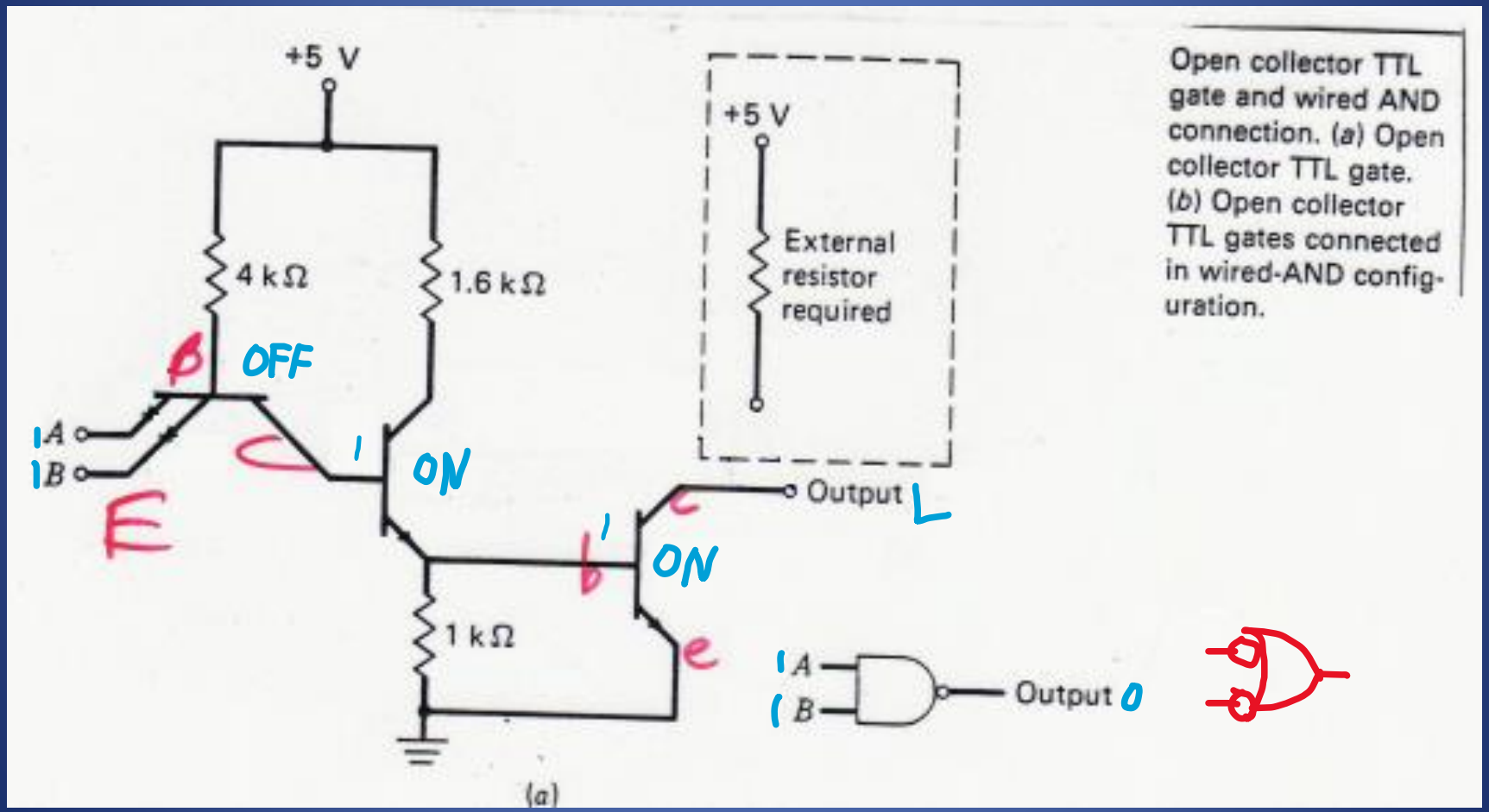
Advantages

- Use as a communication line, e.g., IEEE-488 bus.
- Being able to use different voltage values (handy to communicate between different logic families)
- Getting a free gate.

Disadvantages

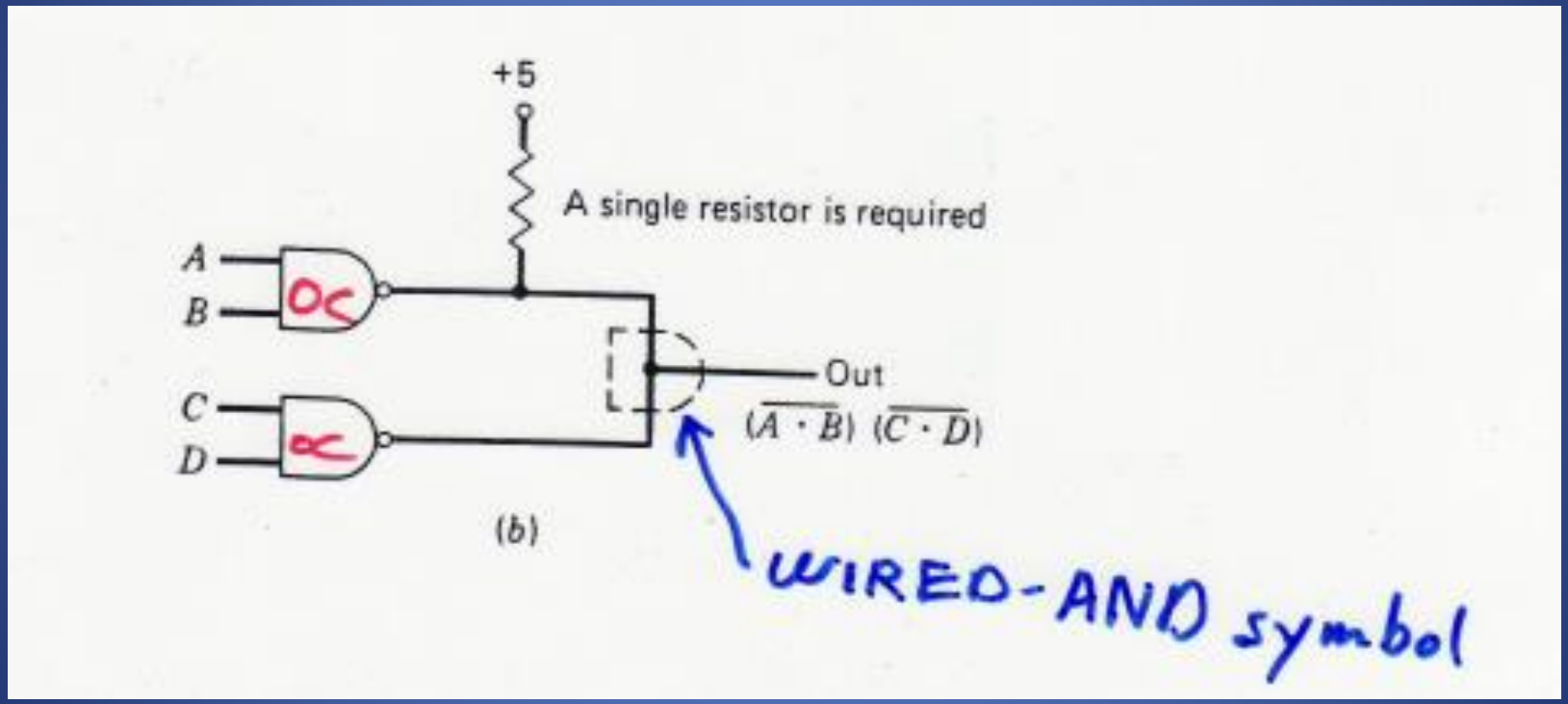
- Slows the signal propagation through the output gate
- Needing Open Collector versions of chips (might not be available for all types of gates).

OC NAND Internal TTL Transistors



Open collector TTL gate and wired AND connection. (*a*) Open collector TTL gate. (*b*) Open collector TTL gates connected in wired-AND configuration.

Boolean Equation



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