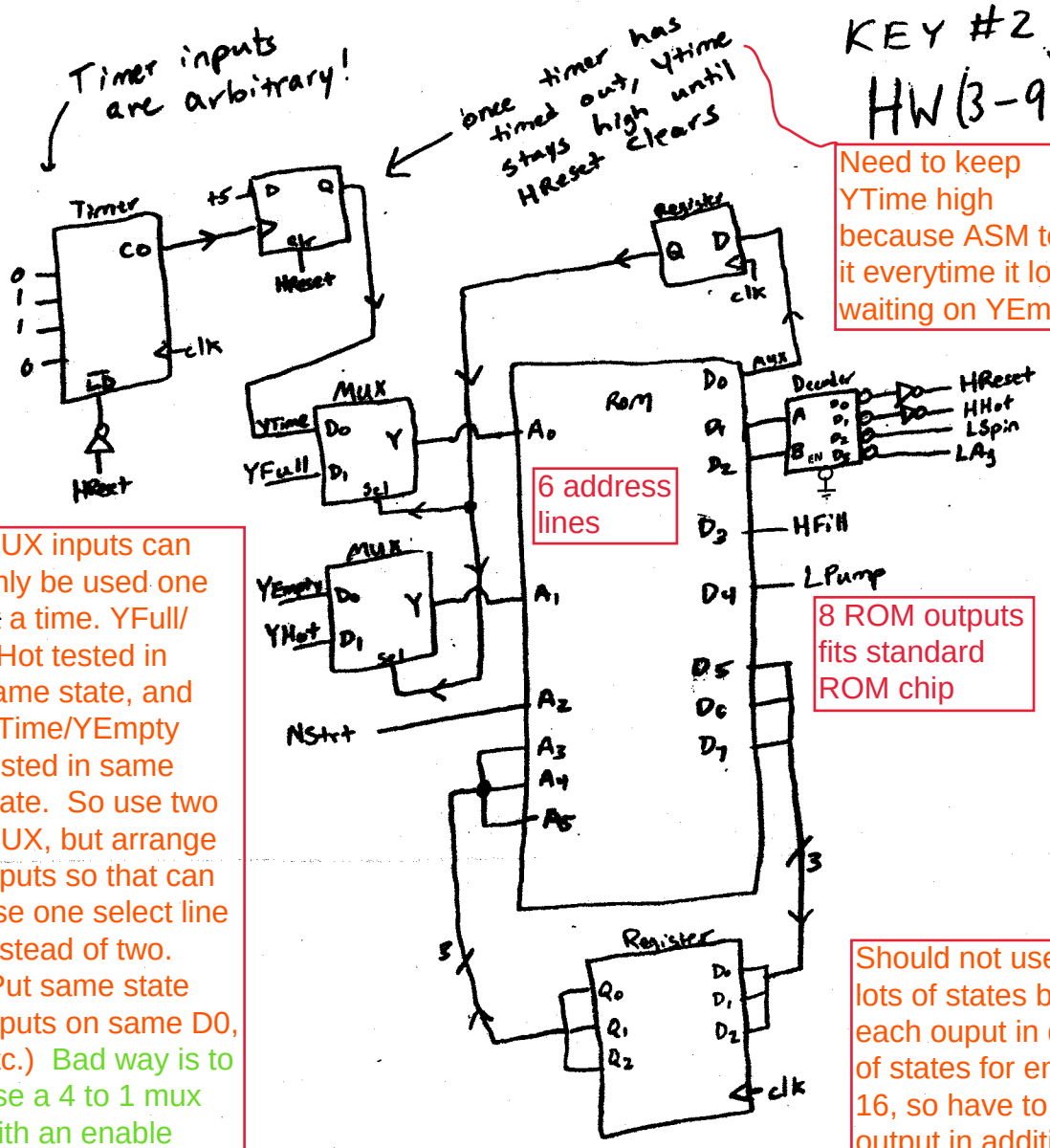
KEY #2 (best)

HW (3-9)



Need to keep YTime high because ASM tests it everytime it loops waiting on YEmpty.

Note: CO goes to FF clock, +5 to D, HRESET to async clear.

Decoder outputs are mutually exclusive. Decoder has ALL outputs active low, so need inverters on active high outputs. Can keep decoder enabled because can turn on HHot or HReset when other outputs need to be off. (HHot does nothing without LPump on.)

MUX inputs can only be used one at a time. YFull/ YHot tested in same state, and YTime/YEmpty tested in same state. So use two MUX, but arrange inputs so that can use one select line instead of two. (Put same state inputs on same D0, etc.) Bad way is to use a 4 to 1 mux with an enable register in front. Adds extra states and the enable register.

Should not use state counter. It adds lots of states because you have to load each ouput in different state. Number of states for entire ASM is greater than 16, so have to add another ROM output in addition to LLNS. Also huge slowdown of ASM. Don't need to load timer with different values. Don't need an output register. You need them to justify it.

TRICK * Could make the state register be a counter by having a signal go to an enable and having $\overline{CO}$ connect to the load line. This works because each state either goes to itself or the next sequential state. (We don't go from state 2 to 5

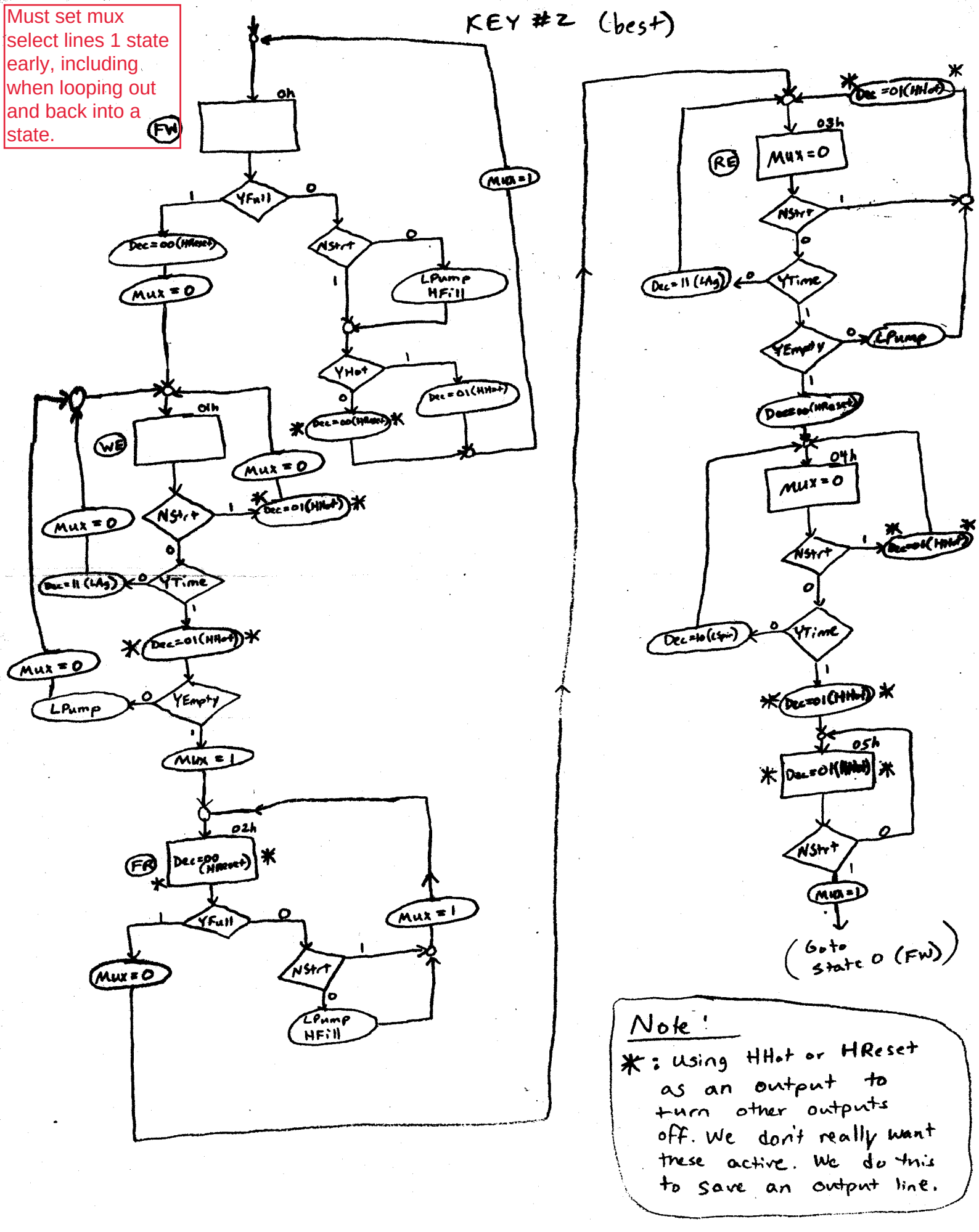
2 → 2 or

2 → 3

– Saves 2 lines.

Must set mux select lines 1 state early, including when looping out and back into a state.

KEY #2 (best)



Note:

*: using HHot or HReset as an output to turn other outputs off. We don't really want these active. We do this to save an output line.

Grad Digital – HW Ch3-9 ROM Table

KEY #2

Dec=00 – HReset
Dec=01 – HHot
Dec=10 – LSpin
Dec=11 – LAg

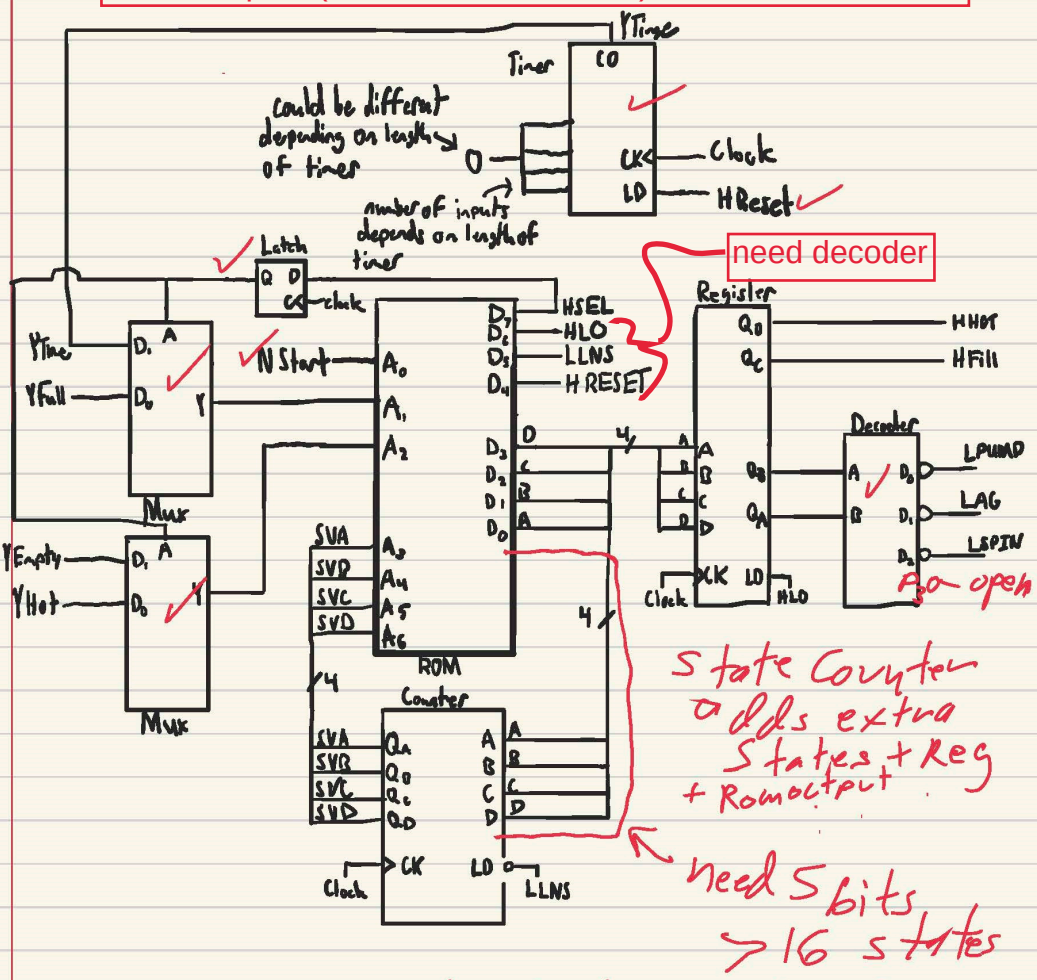
CS			NStrt	YHot/ YEmpty	YFull/ YTime	NS			LPump	HFill	Decoder		MUX
A_5	A_4	A_3	A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
000			X	X	1	010			1	0	00		0
000			0	0	0	000			0	1	00		1
000			0	1	0	000			0	1	01		1
000			1	0	0	000			1	0	00		1
000			1	1	0	000			1	0	01		1
001			1	X	X	001			1	0	01		0
001			0	X	0	001			1	0	11		0
001			0	0	1	001			0	0	01		0
001			0	1	1	010			1	0	01		1
010			X	X	1	011			1	0	00		0
010			0	X	0	010			0	1	00		1
010			1	X	0	010			1	0	00		1
011			1	X	X	011			1	0	01		0
011			0	X	0	011			1	0	11		0
011			0	0	1	011			0	0	01		0
011			0	1	1	100			1	0	00		0
100			1	X	X	100			1	0	01		0
100			0	X	0	100			1	0	10		0
100			0	X	1	101			1	0	01		0
101			0	X	X	101			1	0	01		1
101			1	X	X	000			1	0	01		1

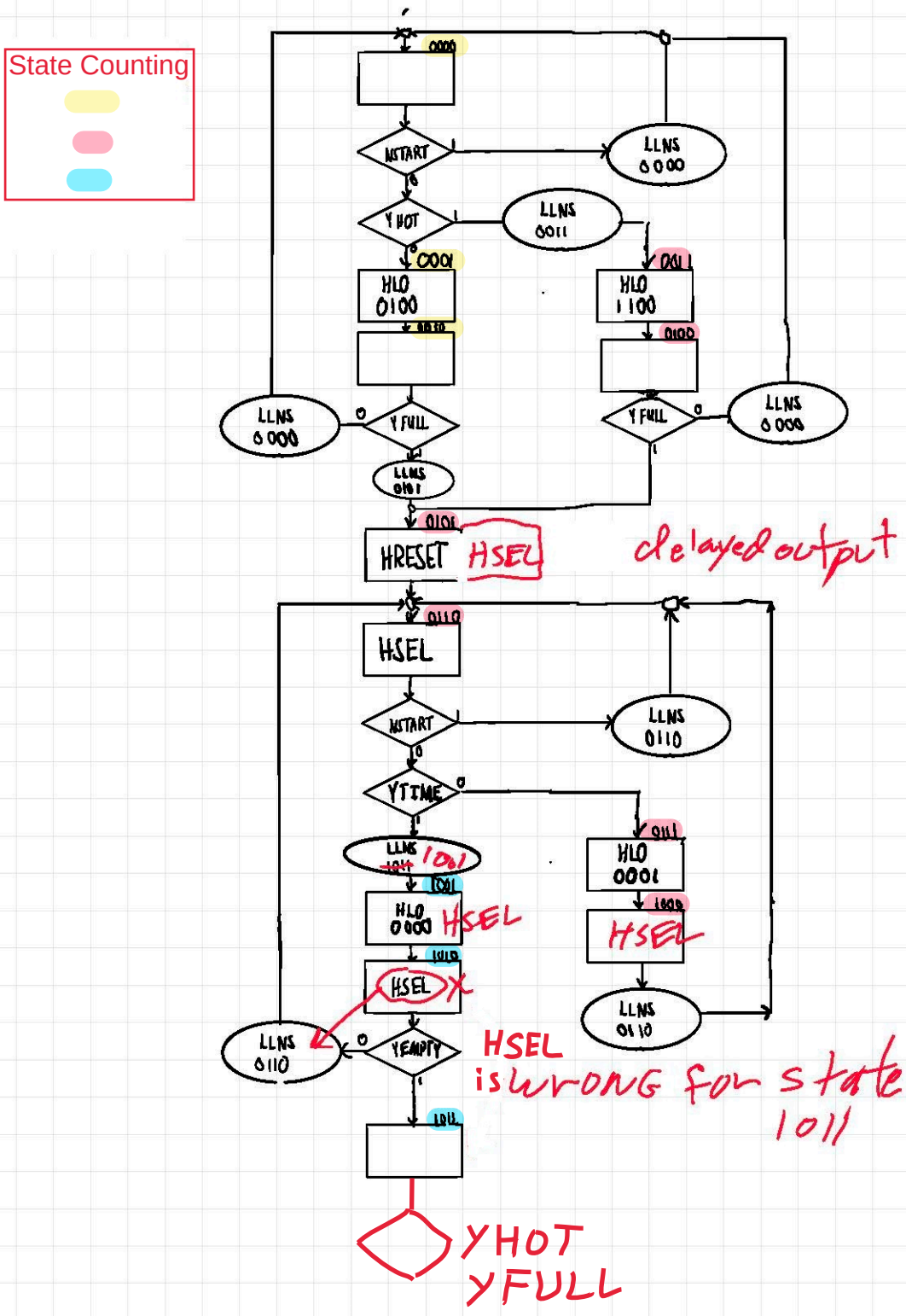
Solution with State Counter (circuit is more complicated and needs many more states (slower operation).

Chapter 3

3-9 Repeat Prob. 1-7. Use MSI parts as needed. Be sure to use a multiplexer for inputs. Add a separate counter to perform the cycle timing function (which was just assumed to exist in Prob. 1-7).

Don't need to latch Timer CO because YTIME is not in the YEMPTY path (it is in a different state)




State Counting
0000
MSTART
LLNS 0000
YHOT
LLNS 0011
0001
HLO 0100
0011
HLO 1100
0010
0100
YFULL
LLNS 0000
YFULL
LLNS 0000
LLNS 0001
0101
HRESET
HSEL
delayed output
0110
HSEL
MSTART
LLNS 0110
YTIME
LLNS 1011
1001
HLO 0000
HSEL
1011
HSEL
1010
0111
HLO 0001
1000
HSEL
LLNS 0110
LLNS 0110
YEMPTY
HSEL is wrong for state 1011
1011
YHOT
YFULL