Digital Systems

Physics 5430

State Counter and

“The Traffic Light ASM from Hell”

State Sequencing with Counter

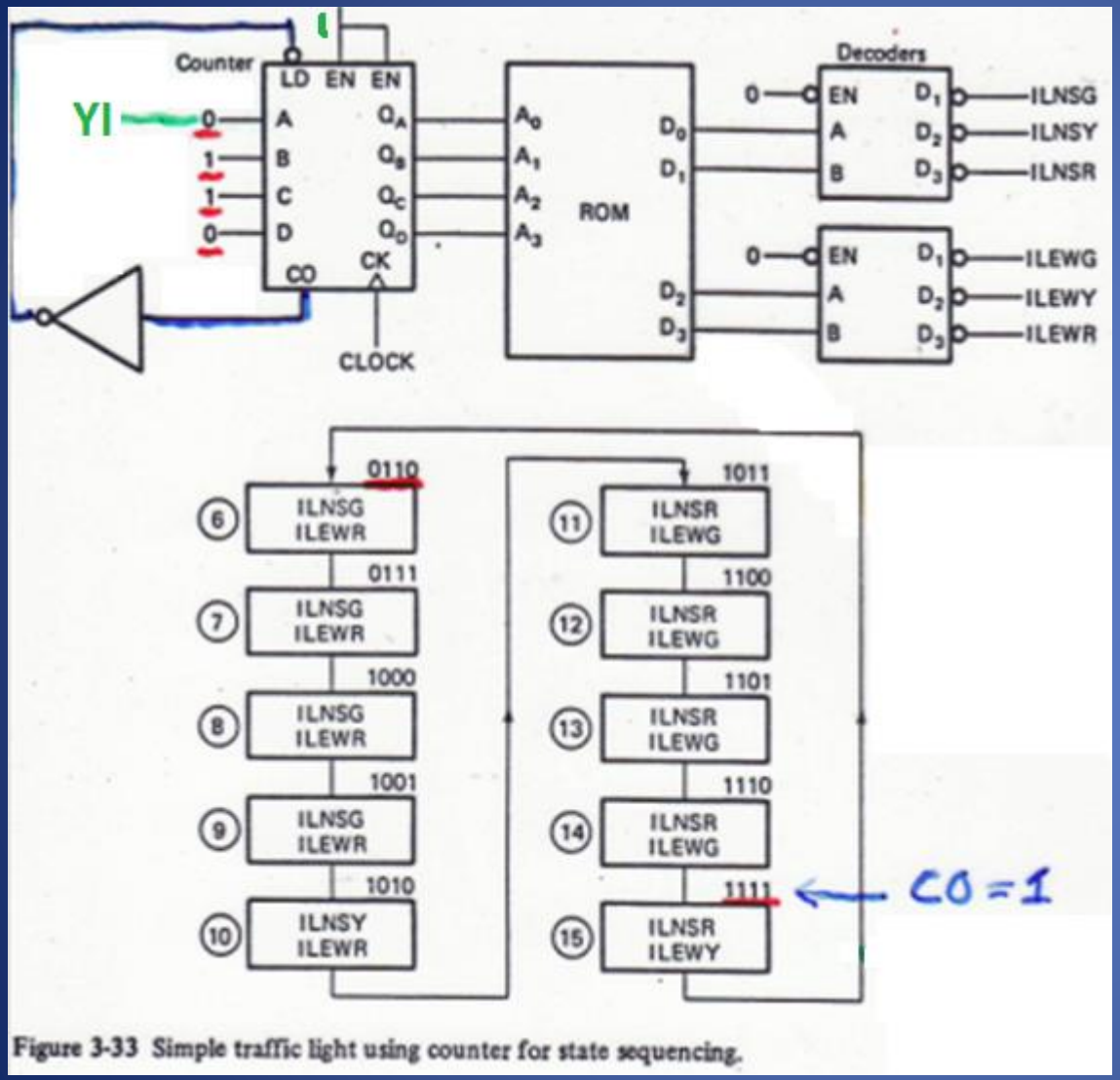


Figure 3-33 Simple traffic light using counter for state sequencing.

Replace state reg with state counter.

Counter sequences ASM through states in order.

4-bit counter matches 16 States, but we only have 10. So must load counter with 6 every time it tries to roll over to count 0.

Tie active-high CO to active-low LD through an Inverter.

For LIMITED branching (out of state 15 only) to either state 6 or state 7, can connect input YI to counter load line A. Or other inputs to other load lines.

Flexible Branching with State Counter

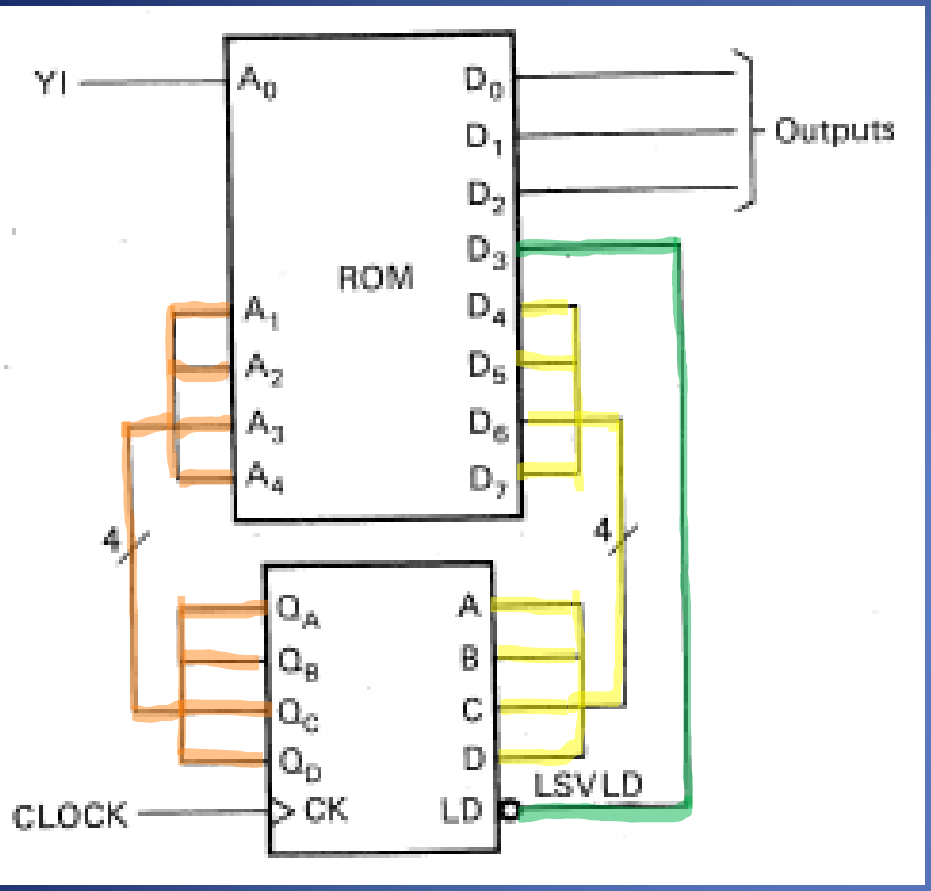


Figure 3-34 Loading an arbitrary next state when using a counter for the state register.

Connect counter outputs to ROM address lines as before.

Connect 4 ROM outputs to the 4 counter inputs.

Connect a ROM output to the counter load pin (LD).

LSVLD is a NEXT STATE output, so acts like delayed output.

Flexible Branching ASM Chart

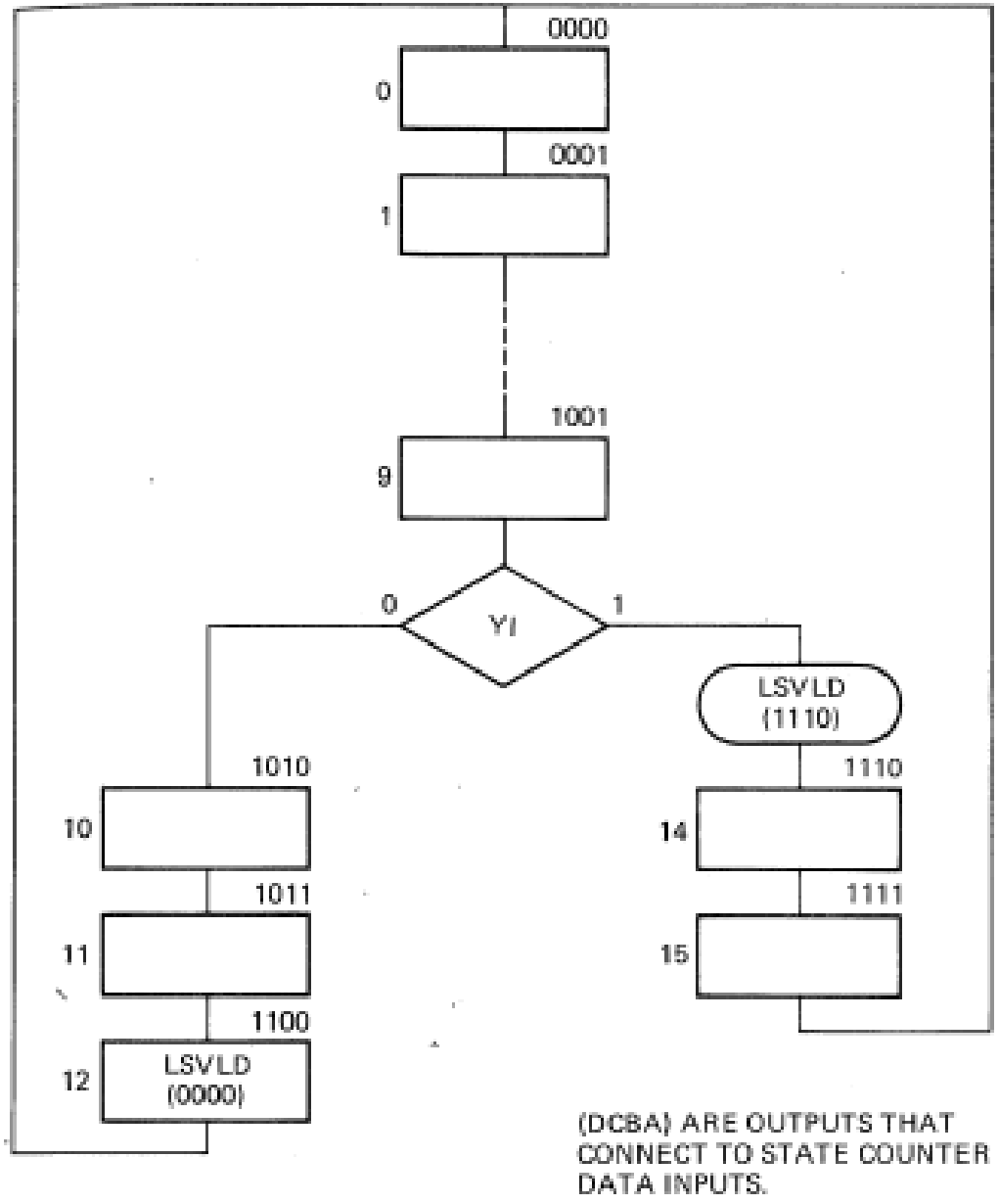


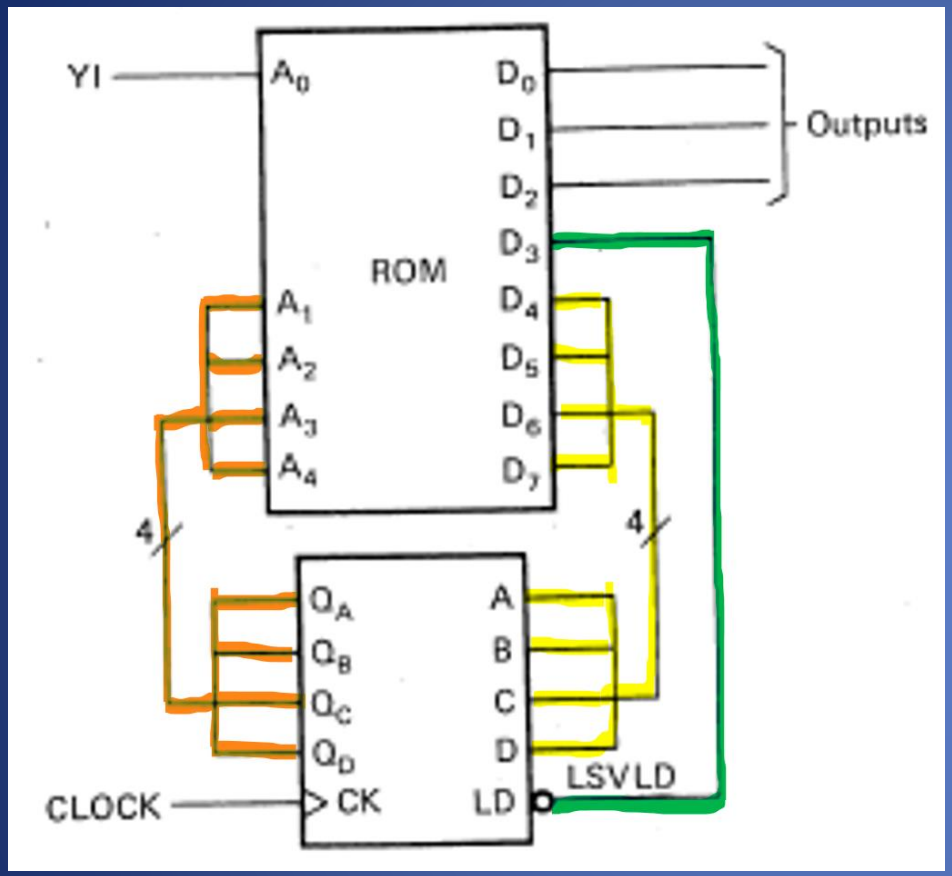
Figure 3-35 ASM chart that loads arbitrary next state into state variable counter.

Counter sequences through states 0 to 9.

State 9 has an input YI. If YI = 0, counter keeps sequencing to states 10, 11, 12. In state 12, ROM loads 0 into the counter, so goes to state 0 next.

If YI = 1, ROM loads 14 into the counter, so goes to 14 next. Then counts to 15 and rollsover to 0.

Flexible Branching Circuit



Using a state counter is much more difficult than a state register.

More importantly, this design uses 5 ROM outputs for the ASM next state instead of 4 without a state counter!

Why would we ever use a state counter?

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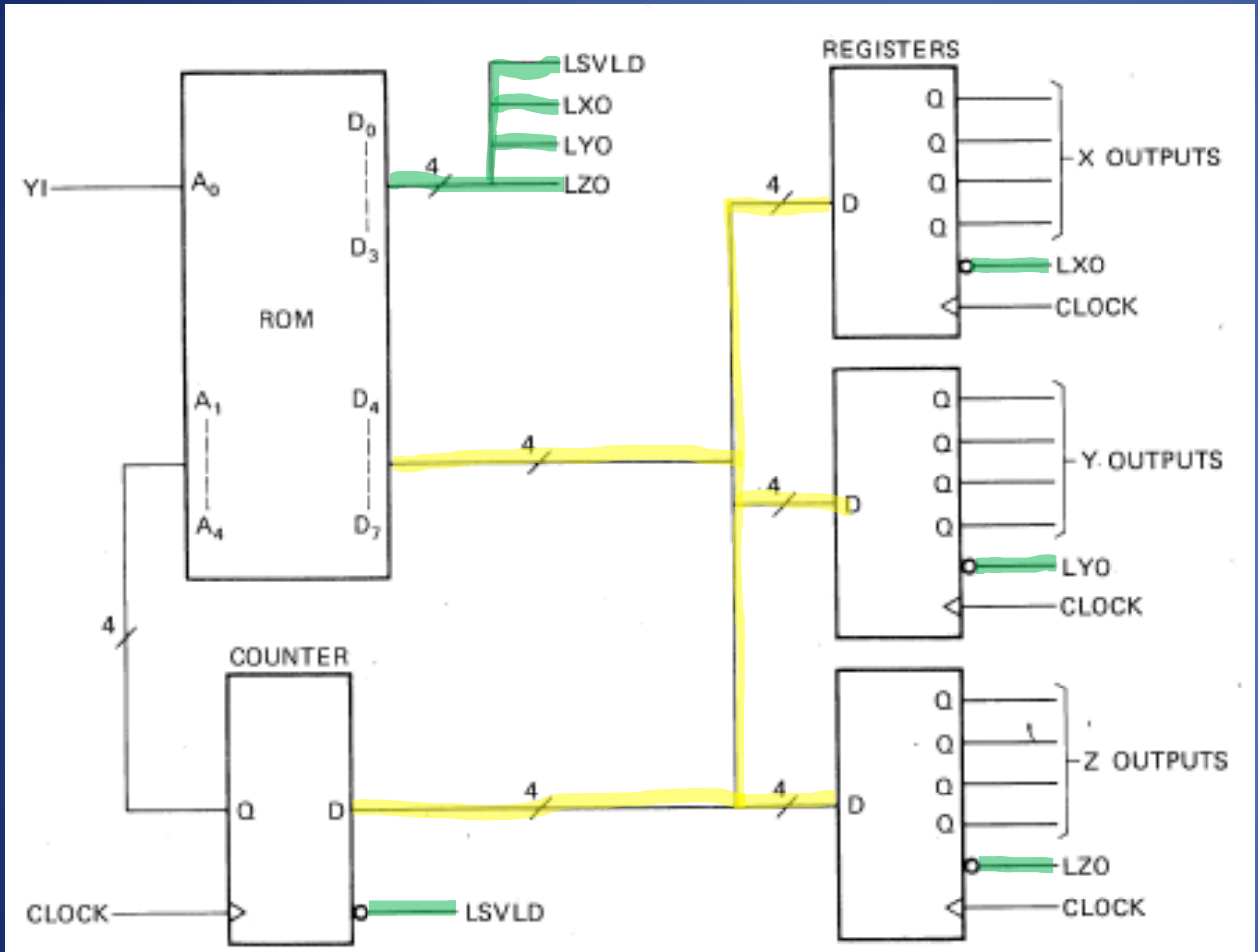


Figure 3-36. Sharing output and next state ROM outputs.

Answer

It makes sense if you also use the group of 4 state counter ROM outputs for other things. For example, output registers.

You can think of them as a data bus.

LSVLD, LXO, LYO, and LZO are load signals.

State Counter with Shared Data Bus

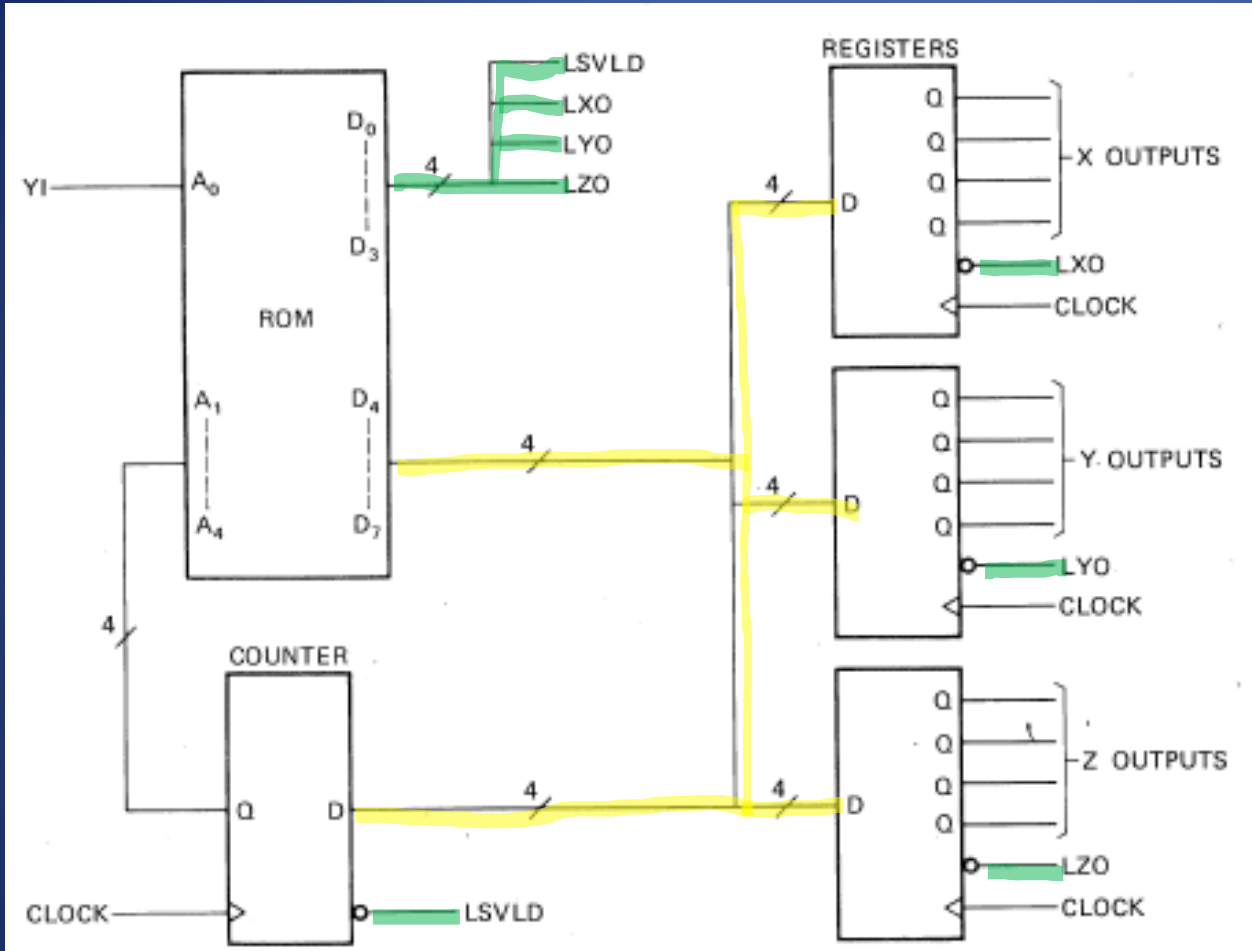


Figure 3-36. Sharing output and next state ROM outputs.

Use data bus and the load signals to load the registers or state counter one at a time.

Requires extra states to load registers.

ASM chart branching may require extra states. (Can't change states and load outputs at same time.)

State Counter with Shared Data Bus

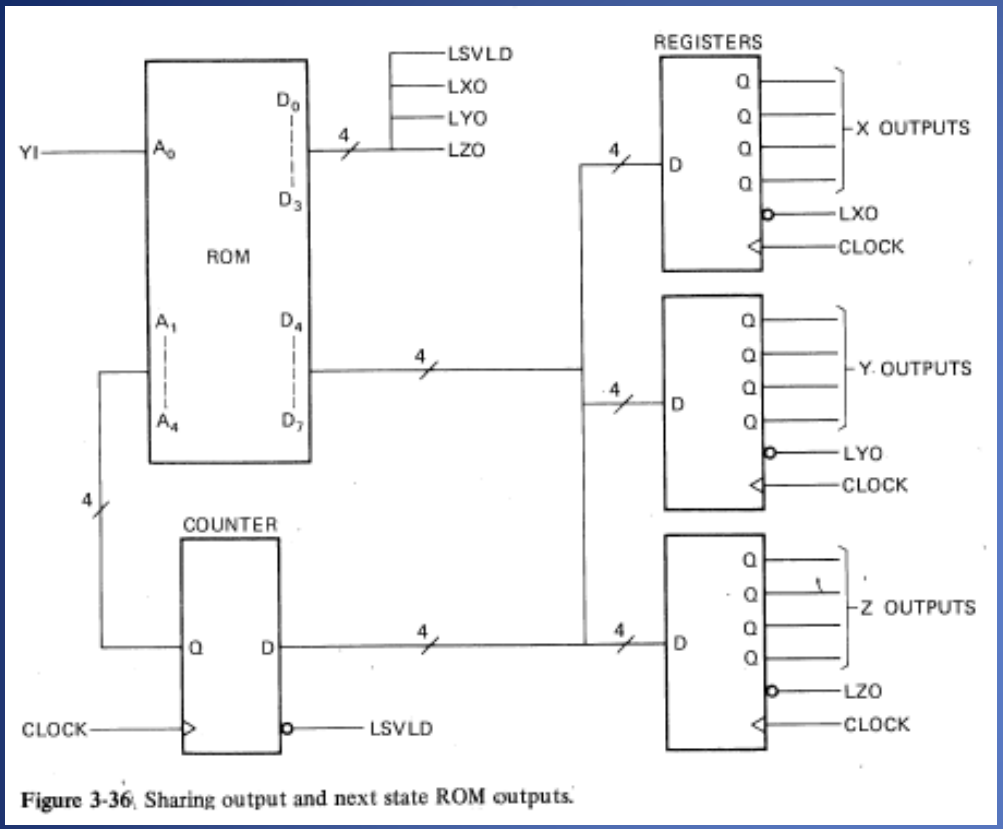


Figure 3-36. Sharing output and next state ROM outputs.

ASM has 8-bit ROM, 12 outputs and up to 16 states.

Standard ASM with 8-bit ROM would only have 4 outputs with up to 16 states.
It would need a 16-bit ROM to have12 outputs.

How many ROM outputs does the state counter save (not counting the ones the registers save)?

ANSWER: It saves 4 - 1 = 3.
D4-D7 minus LSVLD

How many ROM outputs would using a 1 to 4 decoder for the load signals save?

ANSWER: It saves 4 - 3 = 1,
or 4 – 2 = 2 if tie EN to gnd. But don't need to save any more (8-bit ROM)

“Traffic Light ASM from Hell”

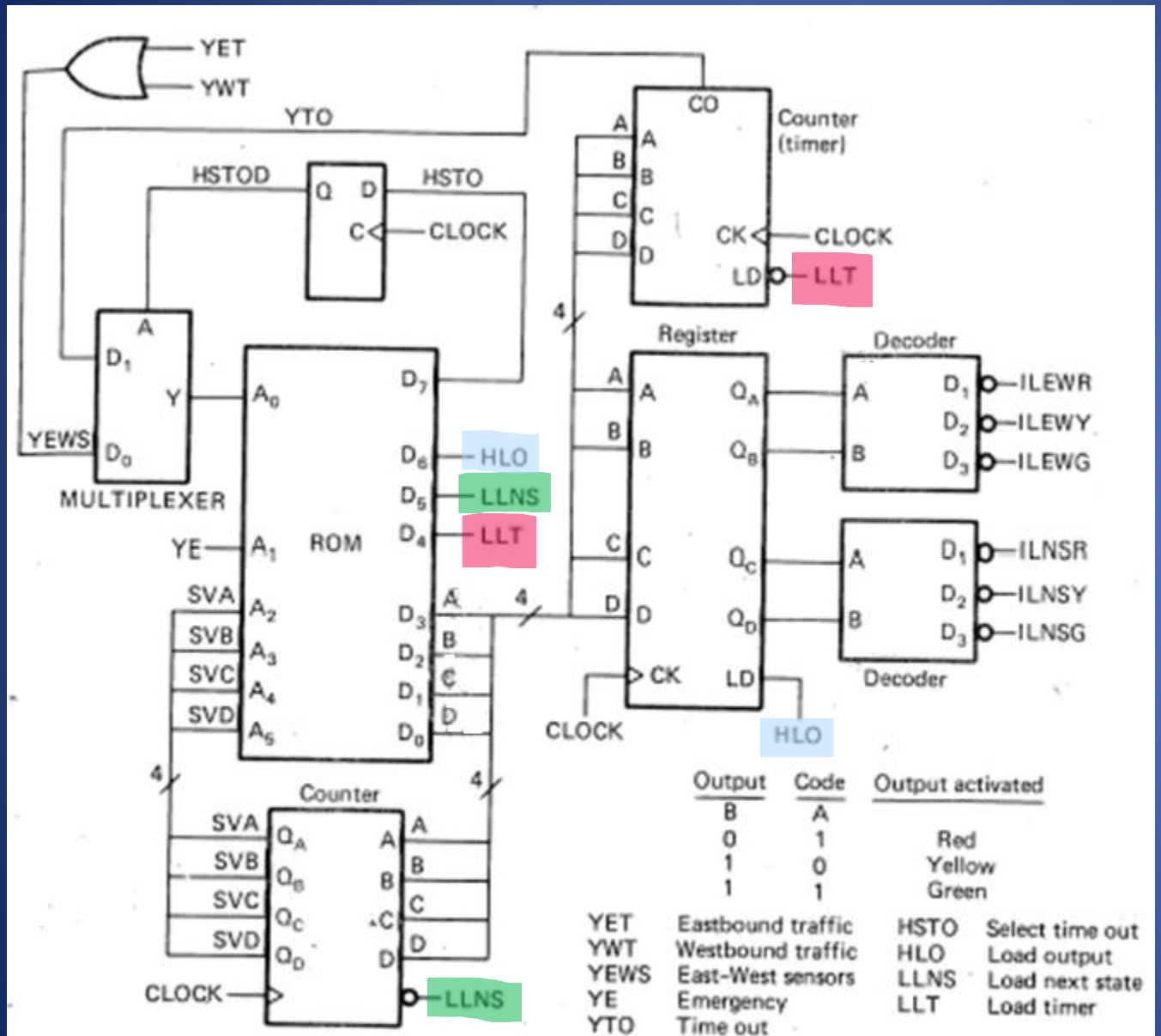


Figure 3-41 Traffic-light controller circuit.

1.25 s clock

Traffic Light Controller Design Features

This design uses:

MUX inputs, and a direct input.

Decoders on the outputs.

A timer,

A state counter,

Registers on the outputs.

Does not show registers on the inputs (no need to take a “snapshot” of the lines as discussed previously.) However, all inputs are assumed to be synchronized with the clock (using a FF).

“Traffic Light ASM from Hell”

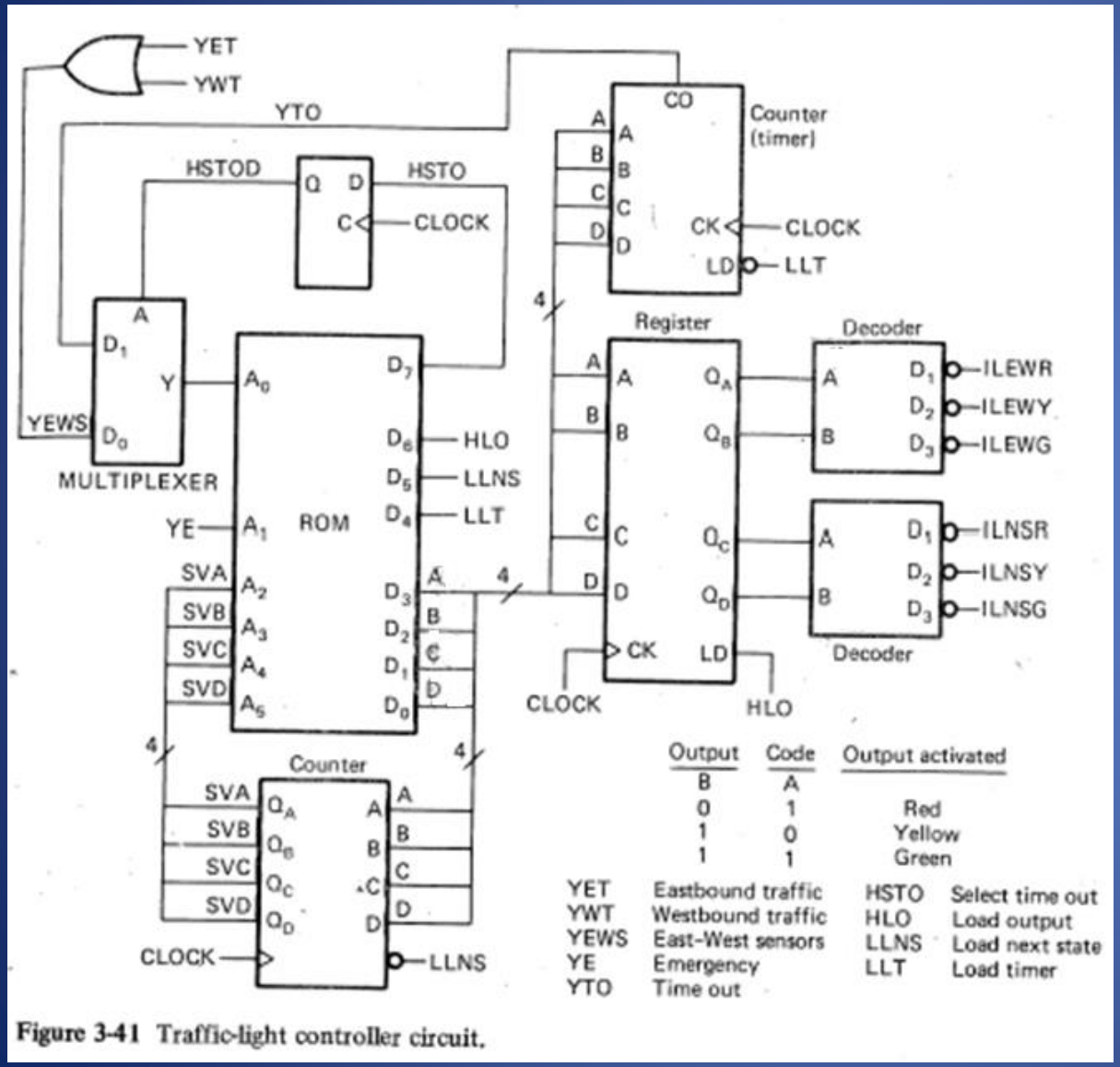


Figure 3-41 Traffic-light controller circuit.

NS is busy street.
EW has traffic sensors.

Has emergency input.
Goes to NSG/EWR
when over.

Timer has adjustable
delay times.

Traffic Light Controller (cont'd)

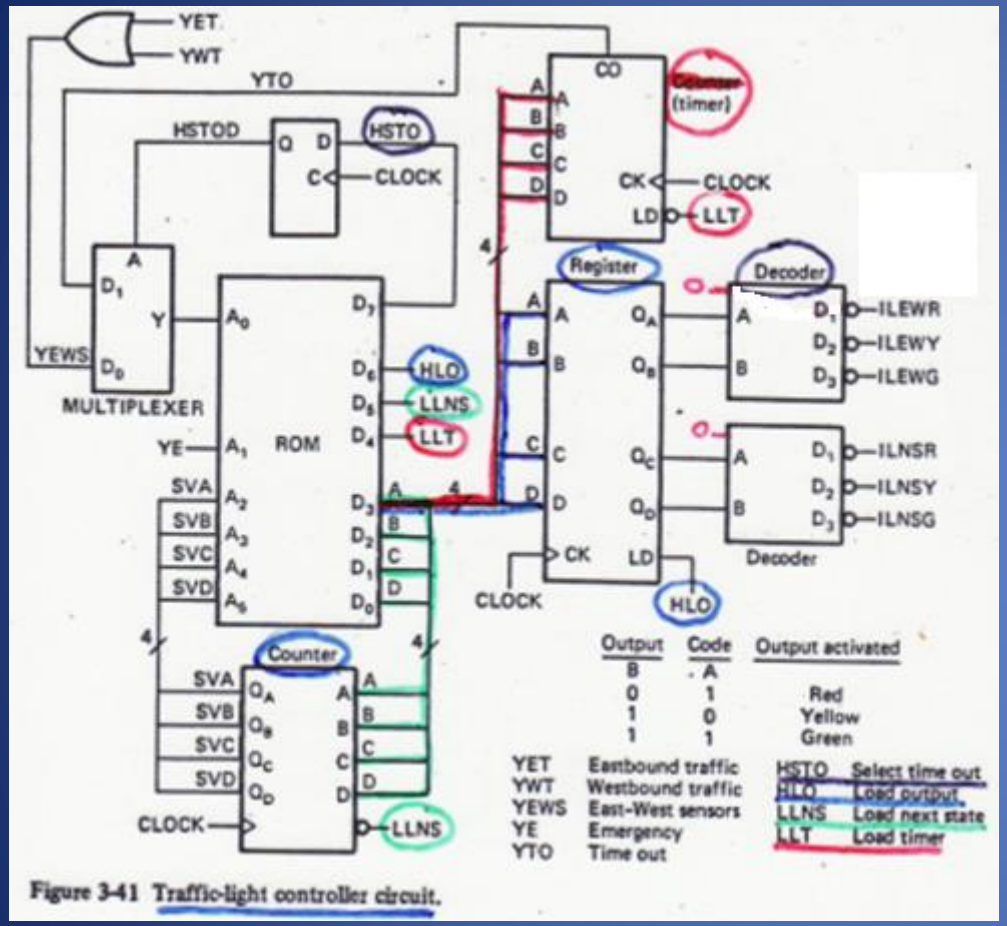


Figure 3-41 Traffic-light controller circuit.

Data bus connected to state counter, timer, and output register. Load signals are: LLNS, LLT, and HLO.

So extra states will be needed to use the data bus for 3 things.

ASM chart branching by loading state counter.

E/W sensor (YEWS) and timer output (YTO) are multiplexed.
HSTO = 0 selects YEWS
HSTO = 1 selects YTO.

Active-low decoders allow 4 ROM outputs to control six lights.

Yemer is not multiplexed.

More Traffic Light Controller Specs

East/West inputs are OR'ed together.

The MUX select line (HSTO) must be asserted early.

Note that LOAD's are color-coordinated in the previous figures.

Decoders are always enabled. (Notice the unused output D0 on the decoders.)

Uses 1.25 second clock: 16 states = 20 s; 4 states = 5 s

Register stores both decoder's binary select values.

Traffic Light Controller ASM Chart

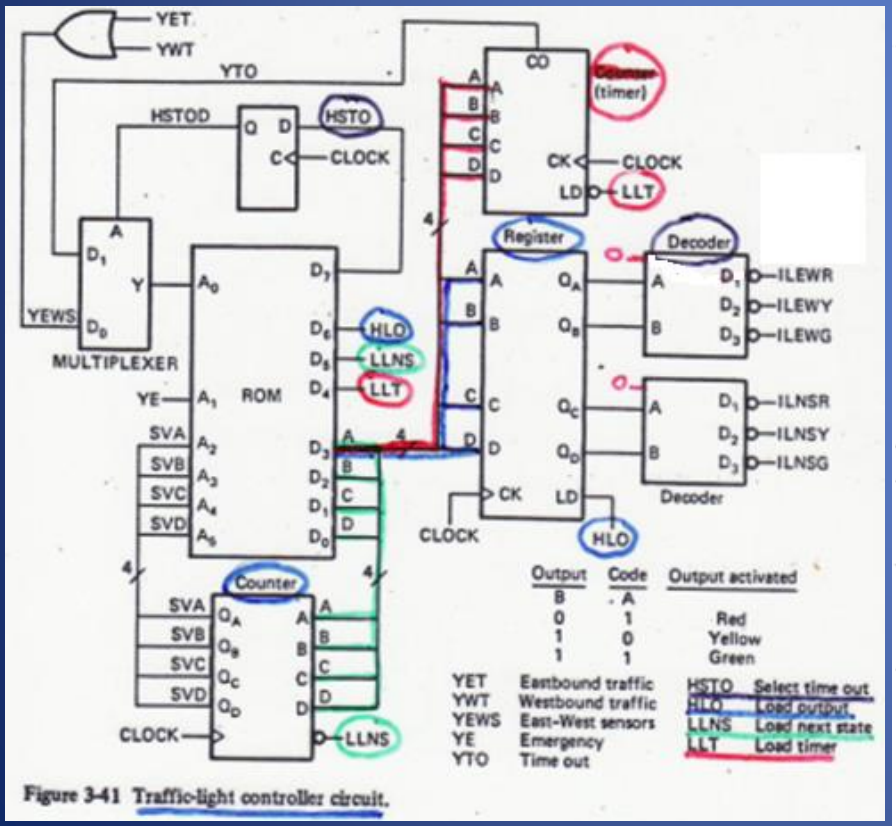
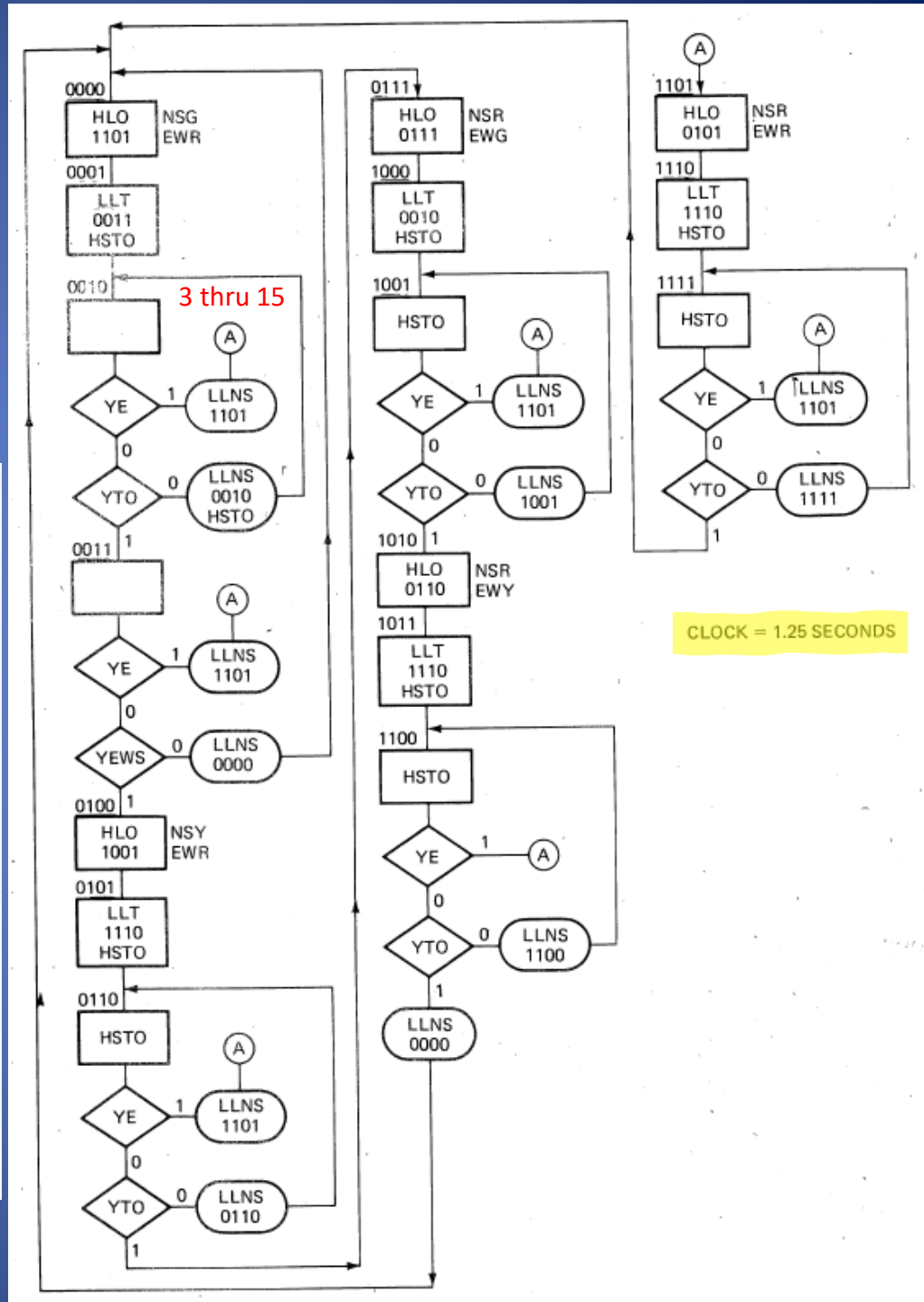


Figure 3-41 Traffic-light controller circuit.



Traffic Light Controller ROM Table

Table 3-5 Traffic light control ROM contents

Current state				YE	YEWS YTO	HSTO	HLO	LLNS	LLT	D	C	B	A
A_5	A_4	A_3	A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	X	X	0	1	1	1	1	1	0	1
0	0	0	1	X	X	1	0	1	0	0	0	1	1
0	0	1	0	1	X	0	0	0	1	1	1	0	1
0	0	1	0	0	0	1	0	0	1	0	0	1	0
0	0	1	0	0	1	0	0	1	1	X	X	X	X
0	0	1	1	1	X	0	0	0	1	1	1	0	1
0	0	1	1	0	0	0	0	0	1	0	0	0	0
0	0	1	1	0	1	0	0	1	1	X	X	X	X
0	1	0	0	X	X	0	1	1	1	1	0	0	1
0	1	0	1	X	X	1	0	1	0	1	1	1	0
0	1	1	0	1	X	1	0	0	1	1	1	0	1
0	1	1	0	0	0	1	0	0	1	0	1	1	0
0	1	1	0	0	1	1	0	1	1	X	X	X	X
0	1	1	1	X	X	0	1	1	1	0	1	1	1
1	0	0	0	X	X	1	0	1	0	0	0	1	0
1	0	0	1	1	X	1	0	0	1	1	1	0	1
1	0	0	1	0	0	1	0	0	1	1	0	0	1
1	0	0	1	0	1	1	0	1	1	X	X	X	X
1	0	1	0	X	X	0	1	1	1	0	1	1	0
1	0	1	1	X	X	1	0	1	0	1	1	1	0
1	1	0	0	1	X	1	0	1	1	X	X	X	X
1	1	0	0	0	0	1	0	0	1	1	1	0	0
1	1	0	0	0	1	1	0	0	1	0	0	0	0
1	1	0	1	X	X	0	1	1	1	0	1	0	1
1	1	1	0	X	X	1	0	1	0	1	1	1	0
1	1	1	1	1	X	1	0	0	1	1	1	0	1
1	1	1	1	0	0	1	0	0	1	1	1	1	1
1	1	1	1	0	1	1	0	1	1	X	X	X	X