



Explanation of States

- FW** - Fill and ~~Start Wash~~ ^{reset timer} - This state fills the washer with water of the proper temperature. When the washer is full, signal ~~LAG~~ ^{reset} is asserted as a conditional output to assure that YTIME will be a 0 when first tested in state WE. Remember that LAG is a delayed action output.
- WE** - Wash and Empty - This state agitates until the timer indicates done and then empties the wash water. When the washer is empty, state FR is entered.
- FR** - Fill and ~~Start Rinse~~ ^{reset timer} - This state is exactly analogous to state FW. Only cold water need be used.
- RE** - Rinse and Empty - This state is exactly analogous to state WE. When the washer is empty, delayed action output ~~LSPIN~~ ^{reset} is asserted as a conditional output to assure that YTIME will be a 0 when first tested in state D.
- D** - Dry - This state simply asserts LSPIN and waits for the timer done signal. It also waits for NSRT to become false so that the washer doesn't cycle continuously as long as the start switch is left on. The switch must first be turned off to enter state W.
- W** - Wait - This state simply waits for the start switch to be asserted.

Note that NSRT can disable the current action in each state. When NSRT is again asserted, the washer continues from where it was stopped (assuming NSRT disables the timer also). Note that no re-start signal is provided so each wash/rinse/dry cycle must be completed before another is initiated.

Problem 1-8

Draw an ASM chart with correct input and output mnemonics to implement an ordinary traffic light with an emergency input. The emergency input sets both EW and NS lights to red as before. However, when the emergency button is released, the traffic lights continue sequencing from the state in which they were when the emergency button was pressed. The easiest way to accomplish this is to use conditional outputs.