Brett Shook

EDA/CAD Software Engineer with expertise in analog and digital design flows and Machine Learning applications.

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WORK HISTORY

Motivo — *Principal Software Engineer*

Jan. 2022 - Jan. 2024

- Accelerated signal timing estimations (delays, transitions, power) by developing **predictive machine learning models**.
- Interfaced estimation models with **PrimeTime** to provide estimates on critical timing paths which **reduced analysis time by >100x.**
- Leveraged a combination of timing path data and physical design data (**Fusion Compiler**) to yield faster timing corrections.
- Worked with customers to understand project requirements and constraints to provide low friction user experience.

Intel — *Software Engineer*

Apr. 2014 - Jan. 2022

- Wrote and maintained software which enables faster more efficient integrated circuit design.
- Lead developer of **MLParest**, a machine learning based electrical parasitic estimation tool which reduced pre-layout simulation errors from **39% to 8% on average**.
- Managed two interns to help develop tool and model pipeline.
- Program used widely across design teams (>1000 engineers) and deployed for many semiconductor technologies. **See publications for more info.**
- Lead developer of **PLParest**, a placement based electrical parasitic estimation tool to help analog-mixed signal circuit floorplanning through a quick drag and drop style GUI integrated with Virtuoso Schematic Editor.
- Extensive experience with custom scripting for Cadence Virtuoso and Synopsys design tools and many other EDA and simulation tools.
- Worked with Splunk and datamining to highlight and fix simulation performance issues.

Intel — *Graduate Intern*

May 2013 - Sept. 2013

- Created a behavioral modeling library in SystemVerilog for high level architectural exploration for mixed signal systems.
- **Improved** simulation performance by **>1000x w.r.t SPICE simulations**.
- Library successfully used in production environments to model high speed serial I/O interfaces such as PCI Express.

SKILLS

VLSI & Analog Automation

Static Timing Analysis & Timing Closure

Mixed Signal Simulation

SPICE Simulation

HDL Behavioral Modeling

Machine Learning

Reinforcement Learning

Multi-Objective Optimization

Parser Development (ANTLR)

General Linux Usage

Docker

EDA SOFTWARE EXPERIENCE

Cadence Virtuoso, Spectre, AMS, QRC Extraction, Liberate-AMS

PrimeTime, Fusion Compiler, Synopsys VCS, VCS-XA, StarRC

OpenROAD, SiliconCompiler

Mentor Calibre

PROGRAMMING LANGUAGES

Python, C++, SKILL, TCL, SystemVerilog, VHDL, Verilog-AMS, SQL, TypeScript

SOFTWARE LIB. / FRAMEWORKS

Jupyter, Pandas, PyTorch, TorchRL, SciKit-Learn, NetworkX, Plotly, Django, Node.JS, QT, ANTLR

University of Arkansas — *Graduate Research Assistant*

Jan. 2011 - Apr. 2014

- Conducted research on electronic design automation tools for power electronics modules.
- Lead developer of **PowerSynth**, a power module design synthesis tool. Created the initial software architecture and framework which has been leveraged for many years by successive researchers.
- This project is highly multidisciplinary involving concepts ranging from multi-objective optimization, finite element analysis, and GUI development (Qt).

https://grapes.uapower.group/
https://e3da.csce.uark.edu/release/PowerSynth/

FlipFire LLC. — *Software Developer*

June 2008 - June 2009

- Wrote a distributed video encoding system for this startup company (Java, FFMPEG, Java Server Faces).

Wal-Mart Information Systems Division — *Programming Intern (High School)*

May 2005 - Aug. 2005

- Wrote and modified programs for replenishment and buyer scheduling (C++, Visual Basic)
- Gained experience with code repositories and group projects.

EDUCATION

University of Arkansas — *M.S. Electrical Engineering*

Jan. 2011 - Apr. 2014

Thesis: Multi-Chip Power Module Layout Synthesis and Optimization

University of Arkansas — *B.S. Electrical Engineering*

2006 - 2010

Senior Project: Sun tracking solar panel; Embedded electronics design

PUBLICATIONS

"**MLParest: Machine Learning based Parasitic Estimation for Custom Circuit Design**," 2020 57th ACM/IEEE Design Automation Conference (DAC), 2020, pp. 1-6, doi: 10.1109/DAC18072.2020.9218495.

"**Multi-chip power module fast thermal modeling for layout optimization**," Computer-Aided Design & Applications, 9(6), pp. 837-846, 2012.

"**Multi-objective layout optimization for multi-chip power modules considering electrical parasitics and thermal performance**," 2013 IEEE 14th Workshop on Control and Modeling for Power Electronics (COMPEL), Preprint, 2013.