4) TTL = Transistor-Transistor Logic

		Min [V]	Nominal [V]	Max [V]
VS		4.75	5.00	5.25
Input:	High	2.00		5.25
	Low	0.00		0.80
Output	High	2.40	3.40	
	Low		0.20	0.40

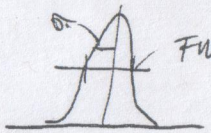
2 marks

at least nominal is required.

Delay: Cable lengths introduce (different) timing 1 mark
create gate with 1st pulse delay 2nd pulse

coincidence: Logic AND | distance of detectors from source 1 mark

5) resolution ~ $\sqrt{\text{variance}}$
~ how well



2 marks

$$f(x) = \frac{N}{S\sqrt{2\pi}} \exp\left(-\frac{(x-\mu)^2}{2\sigma^2}\right)$$

FWHM $\Rightarrow f(x) = S/2 \Rightarrow \log\frac{1}{2} = -\frac{(x-\mu)^2}{2\sigma^2}$ $\mu = 0$

$\Rightarrow x^2 = 2\sigma^2 \log 2$

$x = \sqrt{2\log 2}\,\sigma$, FWHM $= 2x$ 1 mark

$\Rightarrow$ FWHM $= \sqrt{2\log 2}\cdot 2\sigma$

DAH quiz

1) Range $R = 2^n$ (n = # of bit)

$\log_2 R = n \cdot \log 2$ $\Rightarrow R = \frac{2\,\text{keV}}{40\,\text{meV}} = 50000$ 1 mark

$n = \log R / \log 2 = \frac{\log(50000)}{0.693} = 15.61$

$\Rightarrow$ 16 bits are needed 1 mark

2) • slave address = 0 1 1 1 A2 A1 A0 (SA)
A2 = A1 = A0 = 1 all at 3 V

$\Rightarrow$ SA = 0111111 = 63 (decimal) = 0x3F (hex)

• 3 address lines $\Rightarrow$ 3 bits 1 mark
$\Rightarrow 2^n = 8$ different addresses possible 1 mark

3) • v = 1 cm/ns
t = 6.5 ns
σ_x = 200 μm

$x = vt = 6.5$ cm ✓
$x/\delta x = 325 =$
$\delta t = \delta x / v = 20$ ns ✓ or 50 MHz
1 mark

• measuring time requires a TDC ✓ 2 marks
charge signal needs to be amplified and discriminated to produce logical signal ✓ 3 GHz TDC

• R (Range ratio) $\Rightarrow$ 9 bit TDC ✓ $2^8 = 512 > 325$
(actually 8 bit, as $\sigma = \delta t/\sqrt{12}$, but not required) 1 mark

~~3 GHz TDC~~