INTEGRATED CIRCUITS

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT854-bit magnitude comparator

Product specification
File under Integrated Circuits, IC06

December 1990





74HC/HCT85

FEATURES

- · Serial or parallel expansion without extra gating
- Magnitude comparison of any binary words
- · Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT85 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT85 are 4-bit magnitude comparators that can be expanded to almost any length. They perform comparison of two 4-bit binary, BCD or other monotonic codes and present the three possible magnitude results at the outputs ($Q_{A>B}$, $Q_{A=B}$ and $Q_{A<B}$). The 4-bit inputs are

weighted (A_0 to A_3 and B_0 to B_3), where A_3 and B_3 are the most significant bits.

The operation of the "85" is described in the function table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed forward conditions that exist in the parallel expansion scheme.

For proper compare operation the expander inputs ($I_{A>B}$, $I_{A=B}$ and $I_{A<B}$) to the least significant position must be connected as follows: $I_{A<B} = I_{A>B} = LOW$ and $I_{A=B} = HIGH$.

For words greater than 4-bits, units can be cascaded by connecting outputs $Q_{A < B}$, $Q_{A > B}$ and $Q_{A = B}$ to the corresponding inputs of the significant comparator.

QUICK REFERENCE DATA

 $GND = 0 \text{ V}; T_{amb} = 25 \, ^{\circ}\text{C}; t_r = t_f = 6 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYP	LINUT	
STWIBUL	PARAMETER	CONDITIONS	нс	22 20 15 15 3.5 20	UNIT
t _{PHL} / t _{PLH}	propagation delay	C _L = 15 pF; V _{CC} = 5 V			
	A_n , B_n to $Q_{A>B}$, Q_{A		20	22	ns
	A_n , B_n to $Q_{A=B}$		18	20	ns
	$I_{A < B,}$ $I_{A=B}$, $I_{A > B}$ to $Q_{A < B}$, $Q_{A > B}$		15	15	ns
	$I_{A=B}$ to $Q_{A=B}$		11	15	ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	18	20	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:

f_i = input frequency in MHz

fo = output frequency in MHz

 $\sum (C_1 \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = GND$ to V_{CC} For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5$ V

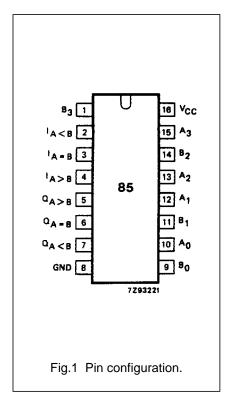
ORDERING INFORMATION

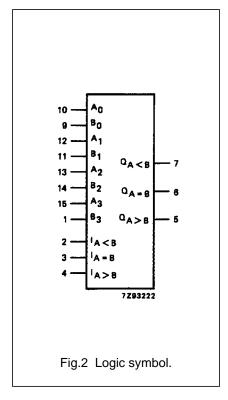
See "74HC/HCT/HCU/HCMOS Logic Package Information".

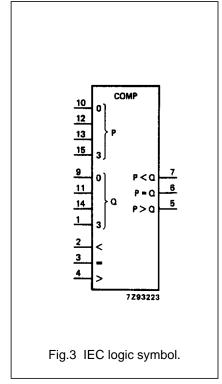
74HC/HCT85

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2	I _{A<b< sub=""></b<>}	A < B expansion input
3	I _{A=B}	A = B expansion input
4	I _{A>B}	A > B expansion input
5	Q _{A>B}	A > B output
6	$Q_{A=B}$	A = B output
7	$Q_{A < B}$	A < B output
8	GND	ground (0 V)
9, 11, 14, 1,	B ₀ to B ₃	word B inputs
10, 12, 13, 15	A ₀ to A ₃	word A inputs
16	V _{CC}	positive supply voltage

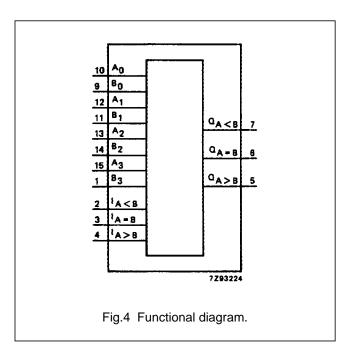






4-bit magnitude comparator

74HC/HCT85



APPLICATIONS

- Process controllers
- Servo-motor control

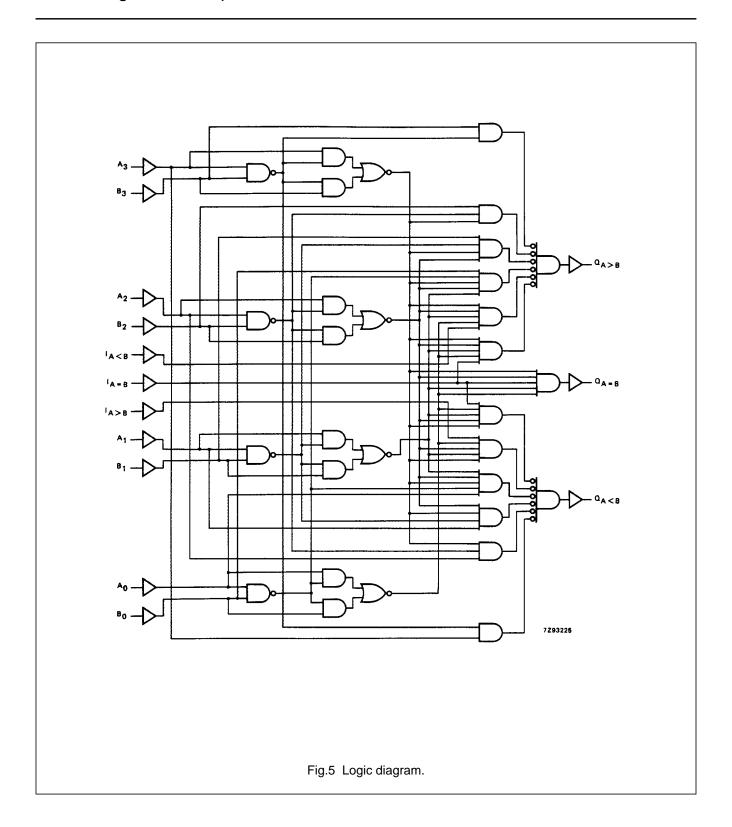
FUNCTION TABLE

COMPARING INPUTS				C	ASCADING	INPUTS		OUTPUTS			
A ₃ , B ₃	A ₂ , B ₂	A ₁ , B ₁	A ₀ , B ₀	I _{A>B}	I _{A<b< sub=""></b<>}	I _{A=B}	Q _{A>B}	Q _{A<b< sub=""></b<>}	Q _{A=B}		
A ₃ >B ₃	X	Х	Х	X	Х	Х	Н	L	L		
$A_3 < B_3$	X	X	X	X	X	X	L	H	L		
A ₃ =B ₃	A ₂ >B ₂	X	X	X	X	X	H	L	L		
$A_3=B_3$	$A_2 < B_2$	X	X	X	X	X	L	H	L		
A ₃ =B ₃	A ₂ =B ₂	A ₁ >B ₁	X	X	X	X	Н	L	L		
A ₃ =B ₃	$A_2=B_2$	A ₁ <b<sub>1</b<sub>	X	X	X	X	L	Н	L		
A ₃ =B ₃	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	Н	L	L		
A ₃ =B ₃	A ₂ =B ₂	A ₁ =B ₁	$A_0 < B_0$	X	X	X	L	H	L		
A ₃ =B ₃	A ₂ =B ₂	A ₁ =B ₁	$A_0 = B_0$	Н	L	L	Н	L	L		
A ₃ =B ₃	A ₂ =B ₂	A ₁ =B ₁	$A_0 = B_0$	L	Н	L	L	Н	L		
A ₃ =B ₃	A ₂ =B ₂	A ₁ =B ₁	$A_0 = B_0$	L	L	Н	L	L	Н		
A ₃ =B ₃	A ₂ =B ₂	A ₁ =B ₁	A ₀ =B ₀	Х	Х	Н	L	L	Н		
A ₃ =B ₃	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	Н	Н	L	L	L	L		
A ₃ =B ₃	A ₂ =B ₂	A ₁ =B ₁	$A_0 = B_0$	L	L	L	Н	Н	L		

Notes

- 1. H = HIGH voltage level
 - L = LOW voltage level
 - X = don't care

74HC/HCT85



4-bit magnitude comparator

74HC/HCT85

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

		T _{amb} (°C)								TES	T CONDITIONS
CVMDOL	PARAMETER	74HC									
SYMBOL		+25		-40 to +85		-40 to +125		UNIT	V _{CC} (V)	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.		(',	
t _{PHL} / t _{PLH}	propagation delay A _n , B _n to Q _{A>B} or Q _{A<b< sub=""></b<>}		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay A _n , B _n to Q _{A=B}		58 21 17	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay $I_{A < B}, I_{A = B}, I_{A > B} \text{ to}$ $Q_{A < B}, Q_{A > B}$		50 18 14	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay I _{A=B} to Q _{A=B}		39 14 11	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig.6
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6

4-bit magnitude comparator

74HC/HCT85

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
I _{A<b< sub=""></b<>}	1.00
$I_{A>B}$	1.00
$I_{A=B}$	1.50
A_{n}, B_{n}	1.50

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	T _{amb} (°C)							TEST CONDITIONS				
SYMBOL	PARAMETER	74HCT										
		+25		-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS		
		min.	typ.	max.	min.	max.	min.	max.		(-,		
t _{PHL} / t _{PLH}	propagation delay A_n , B_n to $Q_{A>B}$ or Q_{A		26	44		55		66	ns	4.5	Fig.6	
t _{PHL} / t _{PLH}	propagation delay A _n , B _n to Q _{A=B}		24	40		50		60	ns	4.5	Fig.6	
t _{PHL} / t _{PLH}	propagation delay $I_{A < B}$, $I_{A = B}$, $I_{A > B}$ to $Q_{A < B}$, $Q_{A > B}$		18	31		39		47	ns	4.5	Fig.6	
t _{PHL} / t _{PLH}	propagation delay I _{A=B} to Q _{A=B}		18	31		39		47	ns	4.5	Fig.6	
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6	

74HC/HCT85

AC WAVEFORMS

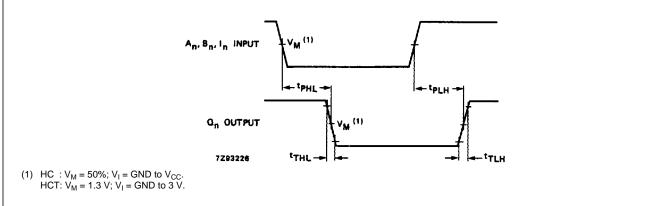
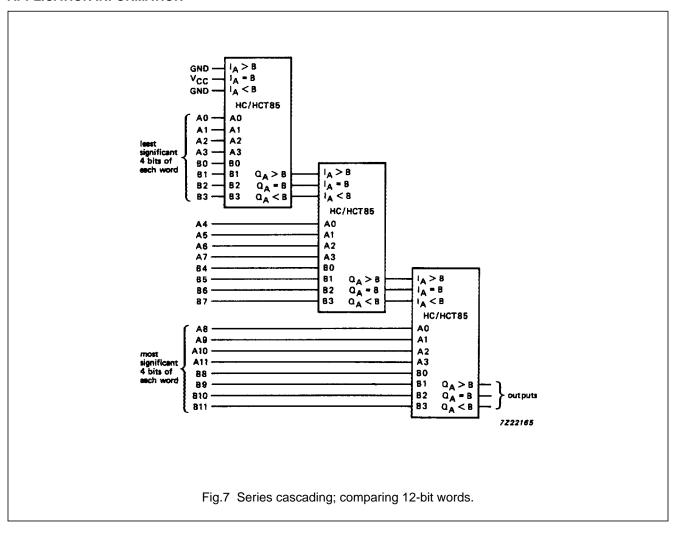


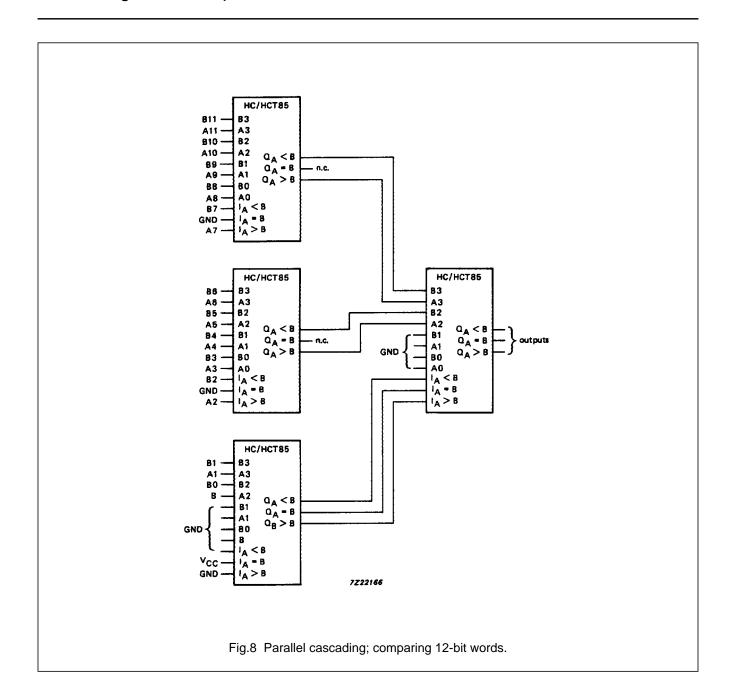
Fig.6 Waveforms showing the word A inputs (A_n) , word B inputs (B_n) and expansion inputs (I_n) to the outputs (Q_n) propagation delays and the output transition times.

APPLICATION INFORMATION



4-bit magnitude comparator

74HC/HCT85



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".