Description of the Hi3516A/Hi3516D Power Consumption, PCB Design, and Tailoring Design

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HiSilicon Technologies Co., Ltd.

Address: Huawei Industrial Base
Bantian, Longgang
Shenzhen 518129
People's Republic of China

Website: http://www.hisilicon.com

Email: support@hisilicon.com

About This Document

Purpose

This document describes the Hi3516A/Hi3516D chip and Internet Protocol camera (IPC) power design solution, printed circuit board (PCB) layer design, and tailoring design, and serves as a reference for customers on the hardware design of products developed based on the Hi3516A/Hi3516D.

NOTE

This document uses the Hi3516A as an example. Unless otherwise specified, this document applies to the Hi3516D and Hi3516A.

Related Versions

The following table lists the product versions related to this document.

Product Name	Version
Hi3516A	V100
Hi3516D	V100

Intended Audience

This document is intended for:

- Technical support engineers
- Board hardware development engineers

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 01 (2015-05-18)

This issue is the first official release.

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1 Background

To reduce power consumption, the core power supplies of the Hi3516A are divided into four parts. The Hi3516A implements selective voltage binging (SVB) voltage control by using four pulse-width modulation (PWM) outputs to reduce power consumption. During actual hardware circuit design, factors including the cost and design complexity must be taken into consideration.

The corresponding hardware solutions are recommended for typical application scenarios based on the Hi3516A core/system power consumption, PCB layer design, and tailoring design. The recommended solutions can be evaluated and referenced based on the actual application scenario during product design.

2 Solution and Design

2.1 Hi3516A Core Power Design Solution

The Hi3516A core power supplies include VDD_Core, CPU_Core, DDR_Core, and MEDIA_Core. According to the test results, MEDIA_Core has the largest current in all the application scenarios. The power combination solutions are evaluated from two perspectives.

- Power consumption
  - The power consumption of the master chip is the lowest when the four power supplies independently supply power (through SVB control).
  - The chip power consumption of the three-power combination solution (VDD_Core and DDR_Core are combined into one power supply, and CPU_Core and MEDIA_Core each supplies power independently) is about 70 mW higher than that of the four-power solution.
  - The chip power consumption of the two-power combination solution (VDD_Core, CPU_Core, and DDR_Core are combined into one power supply, and MEDIA_Core supplies power independently) is about 120 mW higher than that of the four-power solution.
  - The chip power consumption of the one-power combination solution (the four core power supplies are combined into one power supply) is about 400 mW higher than that of the four-power solution. The one-power combination solution is not recommended.
- Design complexity and cost
  - The design complexity is the highest when the four core power supplies independently supply power. In addition, the PMU efficiency is low. Therefore, the system power efficiency is low. When the DC-DC components with high conversion efficiency are used, the IPC power consumption is the lowest, whereas the design complexity and cost are the highest.
  - The power consumption of the three-power combination solution is higher than that of the four-power solution. In addition, the three-power combination solution has no obvious advantages over the four-power solution in design complexity and cost.
  - If the output DC-DC component with high conversion efficiency (for example, MPS2122) is used for the two power supplies respectively in the two-power combination solution, the design complexity is low, the occupied PCB area is small, and the cost is appropriate. You are advised to adopt the two-power combination solution.

- When the four core power supplies are combined into one power supply, the design complexity is the lowest, whereas the power consumption is high. You are strongly advised not to use this solution.

2.2 Chip Low Power Description

2.2.1 Power Consumption Reduction Measures

For the Hi3516A, power consumption can be reduced by improving the power conversion efficiency. In addition, there are other power consumption reduction measures.

The test scenario is as follows:

- HiSilicon reference design board (version: Hi3516AREFB VER.D)
- Service scenario and configurations
  - Two 16-bit DDR3L SDRAMs with 2 Gbits capacity
  - CPU: 600 MHz; DDR: 500 MHz, MIPI-VICAP-ISP: 250 MHz; VGS: 300 MHz; VPSS: 250 MHz; VEDU (H.265): 297 MHz; AVC (H.264): 297 MHz (disabled); SYS-AXI: 198 MHz; MDA1-AXI: 250 MHz; MDA0-AXI: 250 MHz
- Composite video broadcast signal (CVBS) automatic detection, audio single input and output, and disabled USB and secure digital input/output (SDIO)
- IMX178 sensor
- 5 Megapixels@25 fps+VGA@25 fps encoding performance, one-channel large stream network on demand at 12 Mbit/s

The power consumption measures and comparison are as follows:

- Integrate the V100R001C01SPC030 power consumption reduction software version to adjust the voltage of the core power supply. The power consumption is reduced by about 300 mW.
- Use the 1.35 V DDR3L component. The power consumption is reduced by 87.47 mW.
- Configure the unused pins as inputs.
- Disable the unused functions and modules such as Wi-Fi.

2.2.2 Software Power Consumption Reduction in SPC030

The dynamic voltage and frequency scaling (DVFS) and adaptive voltage scaling (AVS) functions for reducing power consumption are added in V100R001C01SPC030. To use the functions, the related registers need to be configured and the .ko file for power consumption reduction (**hi3516a_pm.ko**) is required. For details, see the *Low-Power Solution User Guide*.

The DVFS and AVS functions can be considered as the upgraded SVB function, and they are implemented by software. Therefore, the SVB circuit is required for implementing DVFS, AVS, and SVB. The Hi3516A SVB circuit parameters must be configured by strictly following the circuit parameters in table 2-1 "Recommended impedance and capacitance of mainstream DC-DC peripheral resistors and capacitors" in the *Hi3516A/Hi3516D SVB Circuit Design Guide*.

Table 2-1 describes the power combination solutions and corresponding software control.

Table 2-1 Power combination solutions and corresponding software control

	MEDIA	VDD	DDR	CPU	Description
Two-power combination solution	AVS+SVB circuit	SVB voltage scaling			This solution is recommended when the low-frequency CPU is used.
Three-power combination solution	AVS+SVB circuit	SVB voltage scaling		DVFS+SVB circuit	This solution is recommended when the high-frequency CPU is used.
Four-power solution	AVS+SVB circuit	SVB voltage scaling	SVB voltage scaling	DVFS+SVB circuit	This solution can be used but is not recommended when the high-frequency CPU is used because the design complexity is high.
One-power combination solution	SVB voltage scaling				This solution is not recommended because the power consumption is high.

Note the following:

- The DVFS function applies only to the CPU. If DVFS is used, the CPU power must supply power independently based on the hardware design, and the maximum voltage is 1.3 V. For details, see the DC-DC design circuit in the schematic diagram of the Hi3516ADMEB board.
- The 1.1 V DDR power can be controlled only through SVB voltage scaling. To be specific, if any power is combined with the 1.1 V DDR power, the AVS and DVFS functions cannot be used.
- The power consumption of the VDD power is low, and the power consumption reduction is not obvious when AVS is used. Therefore, the AVS function is not required.

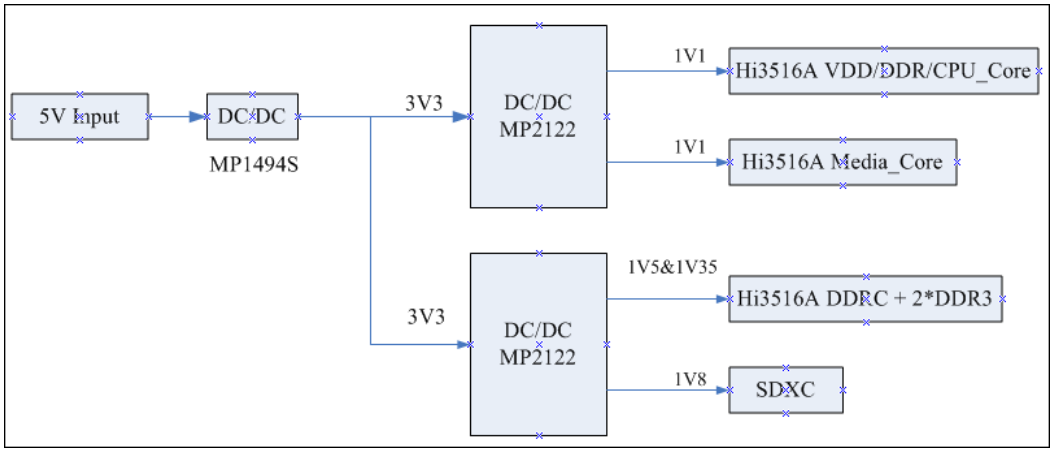
2.3 Recommendations on IPC System Power Design

During system power design, the power supply of the small system and the overall system power efficiency must both be considered. During actual system power design, mainly the system power efficiency and cost are taken into account. When 1-level DC-DC power conversion is used, the IPC efficiency is higher, but the cost of the DC-DC components and peripheral inductors is increased. When 2-level DC-DC power conversion is used, the system power conversion efficiency is lower, whereas the cost is reduced. Customers can choose the mode as required.

Among the four core power supplies of the Hi3516A, Media_Core has the largest current, and the currents of the other three power supplies are relatively small. When the load is low, the conversion efficiency of the DC-DC components is only about 80%. Note that the conversion efficiency of the DC-DC components differs according to the load current. When some of the four core power supplies are combined, the power conversion efficiency of the IPC is improved to a certain extent. As a result, the IPC power consumption is reduced. The following takes the recommended two-power combination solution as an example (Media_Core supplies power independently, and the other three power supplies are combined into one power supply).

The theoretical IPC efficiency is high and the cost is low when the IPC input voltage is 5 V and MP1494S and MP2122 are used for 2-level conversion, as shown in Figure 2-1. The conversion efficiency of the DC-DC components when the input voltage is 5 V is higher than that when the input voltage is 12 V. When the input voltage is 12 V, the conversion efficiency of level-1 DC-DC is considered.

Figure 2-1 Power conversion tree diagram for the master chip part in the Hi3516A IPC power structure



NOTE

If customers use 2-level DC-DC power conversion during actual product design, it is recommended that DC-DC components with high conversion efficiency be used to minimize efficiency loss.

During the IPC design, peripherals with low I/O voltages can be used to lower the IPC power consumption. For example, according to the power consumption test result for the network port PHY part on the HiSilicon demo board, the power consumption of the network port module (including MAC and PHY) when the network port PHY with 1.8 V I/O voltage is used is about 110 mW lower than that when the network port PHY with 3.3 V I/O voltage is used.

2.4 Board Capacitor Quantity Decrease

The quantity of capacitors on the entire Hi3516AREFB VER.D board is decreased to reduce the solution cost. The capacitor simplification measures are as follows:

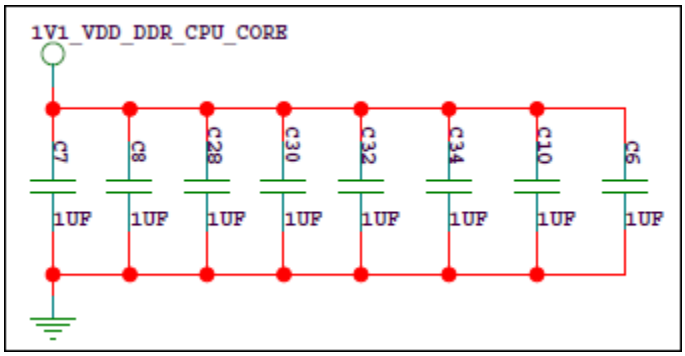
- The original two 22 μF or 47 μF output capacitors for the DC-DC components are reduced to one 22 μF output capacitor. The power noise is still within the acceptable range.

NOTE

This measure is directly related to the DC-DC components and PCB layout, and it cannot be taken if the quality of the DC-DC components is low or the PCB layout is inappropriate. According to the test result, this measure is supported for the MP2122 and MP1494S components used on the Hi3516AREFB VER.D board.

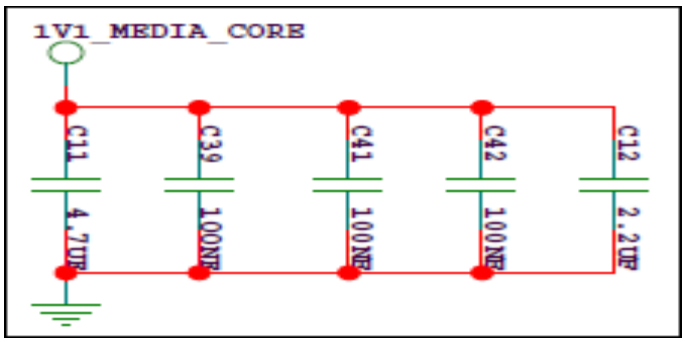
- The capacitance of the capacitors for the core power supplies of the master chip is changed from 100 nF to 1 μF, and the capacitor quantity is decreased. According to the test result, the power noise differs slightly before and after capacitor simplification.

Figure 2-2 Filter circuit for the combined 1.1 V power at the master chip side on the Hi3516AREFB VER.D board



The load of the MEDIA core power is high. The power noise becomes more obvious after capacitor simplification. Therefore, the capacitors for the MEDIA core power remain unchanged.

Figure 2-3 Filter circuit for the MEDIA core power on the Hi3516AREFB VER.D board



- For the DDR power, the noise of the DDR I/O power (Vpp) must be less than or equal to 150 mV, and the Vref noise must be 50 mV lower than the Vpp noise. The training window and stability meet the requirements. According to the test result, the power noise becomes more obvious but does not exceed the restrictions after capacitor simplification (the capacitance is changed from 0.1 μF to 1 μF, and the capacitor quantity is decreased), as shown in Figure 2-4 and Figure 2-5.

Figure 2-4 Filter capacitors for the 1.35 V power at the Hi3516A end

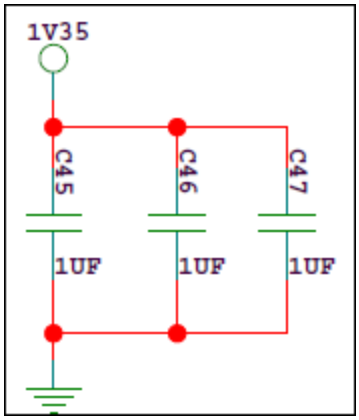
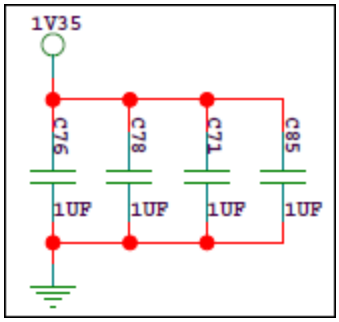


Figure 2-5 Filter capacitors at the DDR3L SDRAM end



For details about the simplified circuits, see the schematic diagram of the Hi3516AREFB VER.D board. Compared with the earlier version, the cost is reduced by RMB 3.66 yuan when the capacitor quantity is decreased.

NOTE

You are advised not to decrease the quantity of capacitors for the PLL and analog parts.

2.5 Hi3516A PCB Layer Design and Tailoring Design

The Hi3516A uses different PCB layer designs based on the application scenarios.

For the traditional box cameras, the PCB area is relatively large and the space is sufficient. Therefore, the 4-layer PCB can be used. For the DDR design, if two DDR SDRAMs are used, you are advised to mount the two DDR SDRAMs to the front and back of the PCB respectively to facilitate routing. Note that the DDR traces cannot be routed across plane splits, the spacing between adjacent traces complies with the 3W rule, and the trace is as short as possible.

For the products that are developed based on the Hi3516A, the PCB area is relatively small. The cost of the 4-layer PCB differs slightly from that of the 6-layer PCB. If customers can accept the cost and consider that the risk of designing their own 4-layer PCB is high, the 6-layer PCB design described in the released HiSilicon design documents is recommended.

2.5.1 Design Restrictions on the 38 mm x 38 mm Board

When the board size is 38 mm x 38 mm (1.50 in. x 1.50 in.), the Hi3516A can use the 4-layer PCB design under the conditions where a single DDR SDRAM is used, only the flash, DDR, network port PHY, and transformer are on the core board, the power supply DC-DC module and other peripheral modules are on another board, and the sensor board is independent.

When the board size is 38 mm x 38 mm and two DDR SDRAMs are used, the 4-layer PCB design cannot be implemented or the risk is too high. Therefore, you are advised not to use the 4-layer PCB design in this condition.

When the board size is 38 mm x 38 mm and the 6-layer PCB is used, the single DDR SDRAM, power module, and all peripherals are on the same board, and the sensor board is independent. This design is acceptable, but needs to be used with caution.

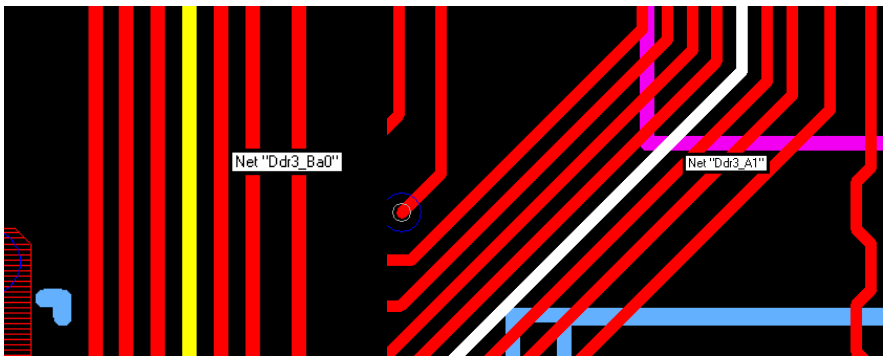
When the board size is 38 mm x 38 mm and the 6-layer PCB is used, the two DDR SDRAMs, power module, flash, and network port are on the same board, and the sensor board is independent. The heat dissipation may become a bottleneck when services are running at 5 Mbit/s. Perhaps this issue cannot be solved. Therefore, this design is not recommended.

When the board size is 38 mm x 38 mm, the DDR3 SDRAM(s) and the sensor cannot be on the same board regardless of the number of board layers.

2.5.2 Decrease in the DDR Trace Routing Area and Attempt on the 2W Trace Spacing

The DDR trace spacing should comply with the 3W rule. However, during product design, due to restrictions such as the structure, some DDR signal traces may not comply with the 3W rule. This is risky theoretically, and the test results also prove that. Given such conditions, the address and command signal traces on the Hi3516AREFB VER.D board uses the 2W trace spacing (the CS, CKE, and ODT signal traces must be routed by strictly following the 3W rule. For details, see the design documents of the Hi3516AREFB VER.D PCB), which challenges the 3W rule.

Figure 2-6 DDR3 trace routing on the Hi3516AREFB VER.D board that challenges the 3W rule



The test result shows that there is obvious crosstalk among A1, A7M, BA0, DQ0, and DQ6. No crash issue occurs during the sampling test. However, we still consider that the risk is high.

During actual design, if the spacing between some signal traces cannot meet the 3W rule due to restrictions such as the structure, customers can reference the design of Hi3516AREFB VER.D and assess the risks themselves. For details about the design circuits, see the Hi3516AREFB VER.D PCB design.

3 Summary

This document briefly describes the Hi3516A power consumption, capacitor simplification, and PCB tailoring design in the typical application scenarios. The power consumption reduction test, cost reduction test, and stability test are conducted on the Hi3516AREFB VER.D board. We have made it clear that it is risky to challenge the 3W rule when routing the DDR traces. Customers can use the routing design for reference, but they need to assess whether the risk is controllable themselves. HiSilicon assumes no responsibility for the board risks caused by the 2W trace spacing design of customers.