Low-Power Solution

User Guide

Issue 06

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About This Document

Purpose

This document describes the power consumption reduction policies and implementation of the recommended power supply solutions in the *Hi3516A/Hi3516D/Hi3519 V100/Hi3519 V101 Core Power Combination Solutions and Power Consumption Comparison*. It also describes the software development kit (SDK) debugging tool.

NOTE

This document uses the Hi3516A as an example. Unless otherwise specified, the contents of the Hi3516A also apply to the Hi3516D, and the contents of the Hi3516A are similar to those of other chips.

Related Versions

The following table lists the product versions related to this document.

Product Name	Version
Hi3516A	V100
Hi3516D	V100
Hi3519	V100
Hi3519	V101

Intended Audience

This document is intended for:

- Technical support engineers
- Software development engineers

Change History

Issue 06 (2016-11-25)

This issue is the sixth official release, which incorporates the following changes:

The description about Hi3519 V100 is added.

Issue 05 (2016-06-15)

This issue is the fifth official release, which incorporates the following changes:

Chapter 2 Debugging the SDK

In section 2.2.2, table 2-1 is modified.

Issue 04 (2016-02-25)

This issue is the fourth official release, which incorporates the following changes:

Chapter 1 Overview

The description in chapter 1 is modified.

Chapter 2 Debugging the SDK

The descriptions in section 2.1 and section 2.2.2 are modified.

Issue 03 (2015-05-29)

This issue is the third official release, which incorporates the following changes:

Chapter 1 Overview

The descriptions of the 2-power domain solution and 3-power domain solution are modified.

Table 1-2 is deleted.

Chapter 2 Debugging the SDK

The description in section 2.2.2 is modified.

Chapter 3 Appendix

Chapter 3 is added.

Issue 02 (2015-02-10)

This issue is the second official release, which incorporates the following changes:

Chapter 1 Overview

Table 1-1 and table 1-2 are added.

Chapter 2 Debugging the SDK

The descriptions in sections 2.1.3 and 2.1.4 are modified.

Issue 01 (2014-12-18)

This issue is the first official release.

Contents

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Tables

1 Overview

The power domain supplies power to the logic modules with similar voltage requirements. By using the power domain, a dedicated voltage is provided for the logic modules and the voltage as well as frequency of each logic module can be dynamically adjusted based on the defined algorithm, which significantly reduces power consumption of the chip. The Hi3516A/Hi3519 V100/Hi3519 V101 is divided into four power domains: core, DDR, MEDIA, and CPU. The CPU domain of Hi3519 V100/Hi3519 V101 indicates the power supply domain for the A17 core. You can select the power domain solution as required. The following describes the power consumption reduction technologies:

- The dynamic voltage and frequency scaling (DVFS) technology indicates that the voltage and frequency are dynamically configured based on the application scenario to meet the requirements on the current circuit timings and performance. It minimizes power consumption by quickly switching the voltage and frequency based on the CPU usage for running services.
- The adaptive voltage scaling (AVS) technology further reduces the chip power consumption on the basis of the DVFS by dynamically adjusting the voltage based on the chip manufacturing process, temperature, and circuit timings.
- The selective voltage binning (SVB) technology reduces chip power consumption by fine-tuning the initial voltage that meets scenario requirements based on the chip manufacturing process during power-on.
- DVFS/AVS reduces the power consumption of a running chip while the chip performance remains unchanged. As shown in Figure 1-2, the hardware power controller (HPC) controls the external power management unit (PMU)/DC-DC over the PMU interface to dynamically adjust the CPU, DDR, MEDIA, and core voltages based on preset AVS and DVFS algorithms and the feedback data from the speed monitor, performance monitor, and T-sensor. This reduces the average power consumption of the chip.

hi35xxx_pm.ko is a kernel driver for low-power adjustment. It is used to adjust the power consumption of the MEDIA and CPU. You can choose the compilation options of the MEDIA or CPU as required based on the power domain division and power consumption adjustment. When **hi3516a_pm.ko** is loaded, if the MEDIA is compiled, you can enable the MEDIA AVS and configure the AVS profile and MEDIA AVS detection interval by setting the module parameters **media_avs_en**, **media_avs_profile**, and **media_avs_inter**. If the CPU is complied, the DVFS function of the CPU is enabled automatically. You can enable the CPU AVS and configure the AVS adjustment interval by setting the module parameters **cpu_avs_en** and **cpu_avs_inter**. Table 1-1 describes the module parameters.

Table 1-1 Parameters of the low-power modules

Chip	media_avs_en	media_avs_profile	media_avs_inter	cpu_avs_en	cpu_avs_inter
Hi3516A	AVS enable for the MEDIA domain Value range: [0, 1] Default value: 1	Profile of the MEDIA domain Value range: [0, 3] Default value: 3 • 0: 1080p@30 fps • 1: 3 megapixels@30 fps • 2: 1080p@60 fps • 3: 5 megapixels@30 fps	Interval of the AVS detection for the MEDIA domain Default value: 20 ms	AVS enable for the CPU domain Value range: [0, 1] Default value: 1	Interval of the AVS detection for the CPU domain Default value: 20 ms
Hi3519 V100/Hi3519 V101	AVS enable for the MEDIA domain Value range: [0, 1] Default value: 1	Not supported	Interval of the AVS detection for the MEDIA domain Default value: 20 ms	AVS enable for the CPU domain Value range: [0, 1] Default value: 1	Interval of the AVS detection for the CPU domain Default value: 20 ms

Figure 1-2 Schematic diagram of DVFS and AVS

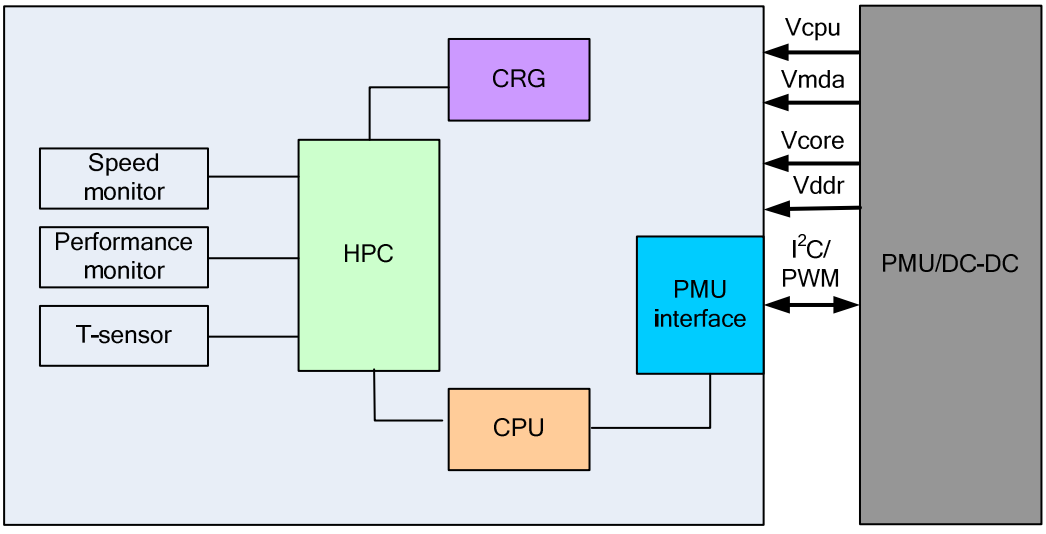


Table 1-2 lists the default working voltages and frequencies for the CPU domain (supplying power independently) after each chip is powered on.

Table 1-2 Default working voltages and frequencies for the CPU domain

Chip	Voltage	Frequency
Hi3516A	1.1 V	600 MHz
Hi3519 V100	0.94 V (The A17 frequency is less than or equal to 880 MHz.) 1.0 V (The A17 frequency is greater than 880 MHz.)	880 MHz
Hi3519 V101	0.94 V (The A17 frequency is less than or equal to 880 MHz.) 1.0 V (The A17 frequency is less than or equal to 1000 MHz.) 1.07 V (The A17 frequency is greater than 1000 MHz.)	930 MHz

Table 1-3 lists the power domains supported by each chip.

Table 1-3 Power domains supported by each chip

Chip	1-Power Domain	2-Power Domain (the MEDIA Domain Supplies Power Independently)	2-Power Domain (the CPU Domain Supplies Power Independently)	3-Power Domain	4-Power Domain
Hi3516A	Supported	Supported	Supported	Supported	Supported
Hi3519 V100	Not supported	Supported	Not supported	Supported	Supported
Hi3519 V101	Not supported	Not supported	Not supported	Supported	Not supported

The following describes power domain solutions:

1. 1-power domain solution

   The low power consumption of the 1-power domain solution is implemented by adopting the SVB technology. When the default maximum processing performance of the chip is specified, power consumption can be reduced during startup.

   - Configure the related Hi3516A registers as follows. For details, see Table 1-4.
     1) Set the power domain mode to 1-power domain mode by setting bit[3:0] of the U-boot table register (address: 0x2005015C) to 0x0.
     2) Set the default working voltage of the chip to 1.1 V by setting bit[7:4] of the U-boot table register (address: 0x2005015C) to 0x0.

3) Set the default working frequency of the CPU to 600 MHz by setting bit[0:4] of the U-boot table registers (addresses: 0x20030000 and 0x20030004) to 0x12000000 and 0x01501032 respectively.

- Hi3519 V100/Hi3519 V101 does not support the 1-power domain solution.

2. 2-power domain solution

Two power supplies are provided in this solution. In this case, the combined power supplies use the SVB technology to reduce power consumption, and the independent power domains such as the CPU or MEDIA use other technologies (for example, AVS or DVFS) to reduce power consumption. Hi3519 V100 supports only the solution in which the MEDIA supplies power separately.

The two 2-power domain solutions are described as follows:

- If the CPU, VDD, and DDR power supplies are combined, and the MEDIA domain supplies power independently:

  Configure the related Hi3516A registers as follows. For details, see Table 1-4.

  1) Set the power domain mode to 2-power domain mode (the MEDIA domain supplies power independently) by setting bit[3:0] of the U-boot table register (address: 0x2005015C) to 0x1.
  2) Set the default working voltage of the chip to 1.1 V by setting bit[7:4] of the U-boot table register (address: 0x2005015C) to 0x0.
  3) Set the default working frequency of the CPU to 600 MHz by setting bit[0:4] of the U-boot table registers (addresses: 0x20030000 and 0x20030004) to 0x12000000 and 0x01501032 respectively.

     After the preceding settings, the two power domains of the Hi3516A can use the SVB technology to reduce power consumption during power-on.

  Configure the related Hi3519 V100 registers as follows:

  1) Set the power domain mode to 2-power domain mode (the MEDIA domain supplies power independently) by setting bit[1:0] of the U-boot table register (address: 0x1202015C) to 0x2.
  2) Set the working voltage of the MEDIA domain to 1.0 V by setting the U-boot table register (address: 0x120A000C) to 0x4800c7.
  3) Set the default working frequency of the A17 core to 880 MHz by setting the U-boot table register (address: 0x12010004) to 0x0b118370 and bit[6:4] of the U-boot table register (address: 0x12010034) to 0x1.

     Hi3519 V100 does not perform the SVB operation on the combined power domains in the 2-power domain solution.

- The MEDIA, VDD, and DDR power supplies are combined, and the CPU domain supplies power independently:

  Configure the related Hi3516A registers as follows. For details, see Table 1-4.

  1) Set the power domain mode to 2-power domain mode (the CPU domain supplies power independently) by setting bit[3:0] of the U-boot table register (address: 0x2005015C) to 0x2.
  2) Set the default working voltage of the chip to 1.1 V by setting bit[7:4] of the U-boot table register (address: 0x2005015C) to 0x0.
  3) Set the default working frequency of the CPU to 600 MHz by setting bit[0:4] of the U-boot table registers (addresses: 0x20030000 and 0x20030004) to 0x12000000 and 0x01501032 respectively.

     To set the CPU frequency to another value, the maximum working voltage needs to be set to the voltage corresponding to the new frequency synchronously. After

the setting, the default voltage of the CPU is adjusted to the configured voltage, whereas the combined MEDIA, VDD, and DDR power uses the default 1.1 V voltage. See Table 1-4.

Hi3519 V100 does not support this power domain solution.

- Hi3519 V101 does not support the 2-power domain solution.

3. 3-power domain solution

   The 3-power domain solution indicates that the VDD and DDR power supplies are combined, and the MEDIA and CPU domains supply power independently. In this solution, the combined power supplies can use only the SVB technology under the U-boot to reduce power consumption. The power consumption of the two independent power domains can be further reduced.

   - Configure the related Hi3516A registers as follows. For details, see Table 1-4.
     1) Set the power domain mode to 3-power domain mode by setting bit[3:0] of the U-boot table register (address: 0x2005015C) to 0x3.
     2) Set the default maximum working voltage of the Hi3516A to 1.1 V by setting bit[7:4] of the U-boot table register (address: 0x2005015C) to 0x0.
     3) Set the default working frequency of the CPU to 600 MHz by setting the U-boot table registers (addresses: 0x20030000 and 0x20030004) to 0x12000000 and 0x01501032 respectively.
   - Configure the related Hi3519 V100 registers as follows:
     1) Set the power domain mode to 3-power domain mode by setting bit[1:0] of the U-boot table register (address: 0x1202015C) to 0x1.
     2) Set the working voltage of the MEDIA domain to 1.0 V by setting the U-boot table register (address: 0x120A000C) to 0x4800c7.
     3) Set the working voltage of the CPU (A17 core) to 0.92 V by setting the U-boot table register (address: 0x120A0004) to 0x6500c7. To set the voltage to 1.0 V, set this register to 0x4800c7.
     4) Set the default working frequency of the A17 core to 880 MHz by setting the U-boot table register (address: 0x12010004) to 0x0b118370 and bit[6:4] of the U-boot table register (address: 0x12010034) to 0x1.

        After the preceding settings, the three power domains of the chip can use the SVB technology to reduce power consumption during power-on.
   - Configure the related Hi3519 V101 registers as follows:
     1) Set the power domain mode to 3-power domain mode by setting bit[1:0] of the U-boot table register (address: 0x1202015C) to 0x1 or 0x0.
     2) Set the working voltage of the MEDIA domain to 1.0 V by setting the U-boot table register (address: 0x120A000C) to 0x4800c7.
     3) Set the working voltage of the CPU (A17 core) to 0.92 V by setting the U-boot table register (address: 0x120A0004) to 0x6500c7. To set the voltage to 1.0 V, set this register to 0x4800c7.
     4) Set the default working frequency of the A17 core to 930 MHz by setting the U-boot table register (address: 0x12010004) to 0x0b1183a2 and bit[6:4] of the U-boot table register (address: 0x12010034) to 0x1.

        After the preceding settings, the three power domains of the chip can use the SVB technology to reduce power consumption during power-on.

4. 4-power domain solution

The 4-power domain solution indicates that each power domain supplies power independently. The VDD and DDR domains can use only the SVB technology under the U-boot to reduce power consumption.

- Configure the related Hi3516A registers as follows. For details, see Table 1-4.
  1) Set the power domain mode to 4-power domain mode by setting bit[3:0] of the U-boot table register (address: 0x2005015C) to 0x4.
  2) Set the default maximum working voltage of the Hi3516A to 1.1 V by setting bit[7:4] of the U-boot table register (address: 0x2005015C) to 0x0.
  3) Set the default working frequency of the CPU to 600 MHz by setting the U-boot table registers (addresses: 0x20030000 and 0x20030004) to 0x12000000 and 0x01501032 respectively.
- Configure the related Hi3519 V100 registers as follows:
  1) Set the power domain mode to 4-power domain mode by setting the bit[1:0] of the U-boot table register (address: 0x1202015C) to 0x0.
  2) Set the working voltage of the MEDIA domain to 1.0 V by setting the U-boot table register (address: 0x120A000C) to 0x4800c7.
  3) Set the working voltage of the CPU (A17 core) to 0.92 V by setting the U-boot table register (address: 0x120A0004) to 0x6500c7. To set the voltage to 1.0 V, set this register to 0x4800c7.
  4) Set the default working frequency of the A17 core to 880 MHz by setting the U-boot table register (address: 0x12010004) to 0x0b118370 and bit[6:4] of the U-boot table register (address: 0x12010034) to 0x1.
- Hi3519 V101 does not support the 4-power domain solution.

If the CPU and MEDIA domains are independent, you can load the power consumption reduction ko (**hi35xx_pm.ko**) to further reduce power consumption and configure the supported module parameters (see Table 1-1) to adjust the behavior of the power consumption reduction module. The default adjustment solution of the CPU DVFS is on-demand. The frequency and voltage are dynamically adjusted based on the CPU load in this solution. You can change the power consumption policy by following section 2.2 "Setting Low-Power Parameters."

CAUTION

- The default frequency of the A17 core for Hi3519 V100 is 880 MHz. You can set the frequency of the A17 core. When the frequency is greater than 880 MHz, the voltage of the corresponding CPU (A17 core) domain needs to be set to 1.0 V. Otherwise, the voltage needs to be set to 0.92 V.
- The default frequency of the A17 core for Hi3519 V101 is 930 MHz. You can set the frequency of the A17 core. For details about the voltage corresponding to a specific frequency, see Table 1-2.

Table 1-4 Hi3516A Register configuration for the power domain solutions at different CPU frequencies

Frequency	Register	1-Power Domain Solution	2-Power Domain Solution (the Media Domain Supplies Power Independently)	2-Power Domain Solution (the CPU Domain Supplies Power Independently)	3-Power Domain Solution	4-Power Domain Solution
600 MHz (1.1 V)	SYSBOOT11 (0x2005015C)	bit[3:0] = 0x0 bit[7:4] = 0x0	bit[3:0] = 0x1 bit[7:4] = 0x0	bit[3:0] = 0x2 bit[7:4] = 0x0	bit[3:0] = 0x3 bit[7:4] = 0x0	bit[3:0] = 0x4 bit[7:4] = 0x0
	PERI_CFG0 (0x20030000)	0x12000000				
	PERI_CFG1 (0x20030004)	0x01501032				
732 MHz (1.2 V)	SYSBOOT11 (0x2005015C)	bit[3:0] = 0x0 bit[7:4] = 0x1	bit[3:0] = 0x1 bit[7:4] = 0x1	bit[3:0] = 0x2 bit[7:4] = 0x1	bit[3:0] = 0x3 bit[7:4] = 0x1	bit[3:0] = 0x4 bit[7:4] = 0x1
	PERI_CFG0 (0x20030000)	0x11000000				
	PERI_CFG1 (0x20030004)	0x015182dc				
850 MHz (1.3 V)	SYSBOOT11 (0x2005015C)	bit[3:0] = 0x0 bit[7:4] = 0x2	bit[3:0] = 0x1 bit[7:4] = 0x2	bit[3:0] = 0x2 bit[7:4] = 0x2	bit[3:0] = 0x3 bit[7:4] = 0x2	bit[3:0] = 0x4 bit[7:4] = 0x2
	PERI_CFG0 (0x20030000)	0x11000000				
	PERI_CFG1 (0x20030004)	0x01518352				

2 Debugging the SDK

After **hi35XXX_pm.ko** is loaded, you can use the methods described in this chapter to query or debug information on low power consumption.

2.1 Viewing Information on Low Power Consumption

The Hi3516A CPU has only one core, and therefore the related information is regarded as that of CPU0. Hi3519 V100/Hi3519 V101 adopts the big-little architecture. Only the big core is used for low-power adjustment, and the related information is regarded as that of CPU1.

2.1.1 Viewing the CPU Frequency and Voltage

Run the following command over the serial port:

```
cat /sys/devices/system/cpu/cpu0/cpufreq/cpuinfo_cur_freq
```

If the following information is displayed through the serial port:

```
600
```

The CPU frequency is 600 MHz.

Run the following command over the serial port (the number in **regulator.1** varies according to the number of loading times):

```
cat /sys/class/regulator/regulator.1/name
```

If the following information is displayed through the serial port:

```
regulator_cpu
```

Run the following command:

```
cat /sys/class/regulator/regulator.1/microvolts
```

- For Hi3516A, if the following information is displayed through the serial port:

  1029

  The CPU voltage is 1029 mV.
- For Hi3519 V100 and Hi3519 V101, if the following information is displayed through the serial port:

  878159

The CPU voltage is 0.878189 V.

2.1.2 Viewing the Media Voltage

Run the following command over the serial port:

```
cat /sys/class/regulator/regulator.2/name
```

If the following information is displayed through the serial port:

```
regulator_media
```

Run the following command:

```
cat /sys/class/regulator/regulator.2/microvolts
```

- For Hi3516A, if the following information is displayed through the serial port:

  983

  The MEDIA voltage is 983 mV.
- For Hi3519 V100 and Hi3519 V101, if the following information is displayed through the serial port:

  880448

  The MEDIA voltage is 0.880448 V.

2.1.3 Viewing the Low-Power Policies Supported by the CPU

Run the following command over the serial port:

```
cat /sys/devices/system/cpu/cpu0/cpufreq/scaling_available_governors
```

The following information may be displayed over the serial port:

```
conservative ondemand userspace powersave interactive performance
```

The preceding policies are described as follows:

- conservative: The frequency and voltage are adjusted by step.
- ondemand: The frequency and voltage are dynamically adjusted based on the CPU load. It is slower than the interactive policy. This policy is used by default.
- userspace: The voltage and frequency are set by the user. The SDK does not automatically adjust them.
- powersave: The frequency is always set to the lowest to ensure low power consumption.
- interactive: The frequency and voltage are dynamically adjusted based on the CPU load.
- performance: The frequency is always set to the highest to ensure high performance.

2.1.4 Viewing the Low-Power Policy Used by the CPU

Run the following command over the serial port:

```
cat /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor
```

If the following information is displayed through the serial port:

```
ondemand
```

The interactive low-power policy is used.

2.2 Setting Low-Power Parameters

2.2.1 Setting the CPU Low-Power Policy

- Run the following command over the serial port (*xxx* is the policy name):

  ```
  echo xxx > /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor
  ```

- To disable dynamic CPU frequency and voltage scaling, set the low-power policy to userspace.

  ```
  echo userspace >
  /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor
  ```

- To enable dynamic CPU frequency and voltage scaling, set the low-power policy to ondemand.

  ```
  echo ondemand > /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor
  ```

2.2.2 Setting the CPU Frequency

Table 2-1 lists the frequencies supported by the CPU of each chip.

Table 2-1 Frequencies supported by the CPU of each chip

Chip	Frequency
Hi3516A/Hi3516D	Unit: MHz Frequency: 400, 500, 600, 732, or 850
Hi3519 V100 (big core)	Unit: kHz Frequency: 594000, 792000, 880000, 1000000, or 1150000
Hi3519 V101 (big core)	Unit: kHz Frequency: 594000, 792000, 930000, 1000000, 1150000, or 1250000

NOTE

Due to differences between the Linux versions, the frequency unit of Hi3519 V100 differs from that of the Hi3516A/Hi3516D.

To manually set the CPU frequency, disable dynamic CPU frequency and voltage scaling by running the following command:

```
echo userspace > /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor
```

Then set the CPU frequency by running the following command:

```
echo 600 > /sys/devices/system/cpu/cpu0/cpufreq/scaling_setspeed
```

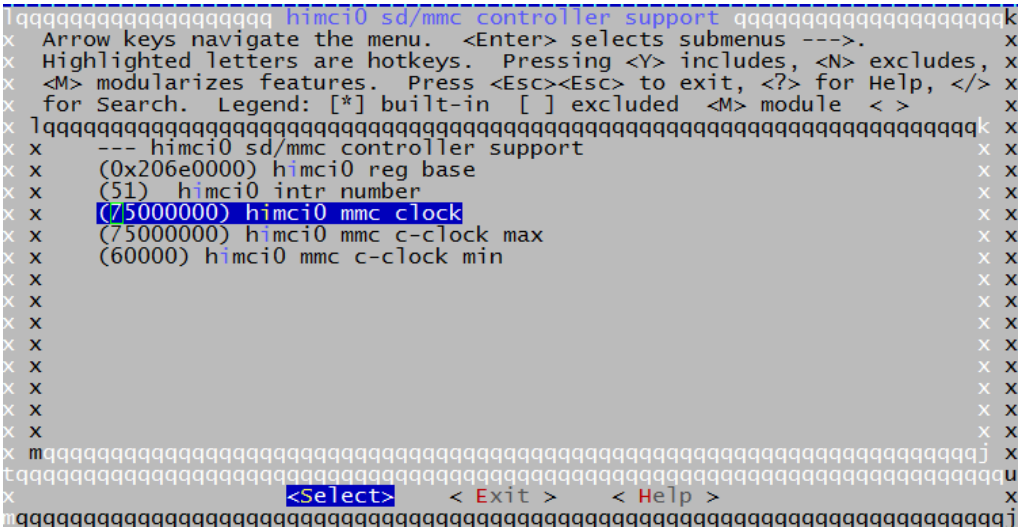
The value 600 indicates that the CPU frequency is set to 600 MHz. Note that the CPU voltage is also synchronized to the preset stable voltage that supports this frequency.

3 Appendix

3.1 Precautions

The Hi3516A secure digital input/output (SDIO) controller is in the MEDIA domain. When the voltage and frequency of the MEDIA domain is dynamically scaled, the SDIO controller cannot work stably at the 100 MHz clock frequency. Therefore, the frequency of the reference clock for the SDIO controller needs to be decreased to 75 MHz when the DVFS or AVS function is enabled. Figure 3-1 shows the configuration method.

Figure 3-1 Configuration of the clock for the SDIO controller



In addition, if the default clock frequency of the SDIO controller is 75 MHz and the frequency of the interface clock supported by the SDIO card is lower than 75 MHz, frequency division is required during interface clock adaption. For example, when the frequency of the clock supported by the SDIO card ranges from 50 MHz to 75 MHz, the interface clock frequency is changed from 75 MHz to 37.5 MHz (instead of 50 MHz) after the clock is divided by 2. To improve the read and write performance, frequency division is not required in this case. The frequency of the SDIO controller clock can be directly set to 50 MHz. The code modification is as follows:

In the hi_mci_set_cclk() function, when the range of the card clock frequency (cclk) is [50 MHz, 75 MHz), the controller clock frequency is reconfigured to 50 MHz and the frequency divider **reg_value** is set to **0**. See the red text.

```
    /*
     * set card clk divider value,
     * clk_divider = Fmmcclk/(Fmmc_cclk * 2)
     */
    if (0 == host->id) {
#ifdef CONFIG_HIMCI0
        if (CONFIG_MMC0_CLK <= cclk)
            reg_value = 0;
        else {
            reg_value = CONFIG_MMC0_CLK / (cclk * 2);
            if (CONFIG_MMC0_CLK % (cclk * 2))
                reg_value++;
            if ((50000000 <= cclk) && (75000000 > cclk)) {
                crg_value = himci_readl(PERI_CRG49);
                crg_value &= ~(SDIO0_CLK_BIT_HIGH);
                crg_value &= ~(SDIO0_CLK_BIT_LOW);
                crg_value |= SDIO0_CLK_SEL_50M;
                crg_value |= SDIO0_CKEN;
                himci_writel(crg_value, PERI_CRG49);
                reg_value = 0;
            }
        }
#endif
    } else if (1 == host->id) {
#ifdef CONFIG_HIMCI1
        if (CONFIG_MMC1_CLK <= cclk)
            reg_value = 0;
        else {
            reg_value = CONFIG_MMC1_CLK / (cclk * 2);
            if (CONFIG_MMC1_CLK % (cclk * 2))
                reg_value++;
            if ((50000000 <= cclk) && (75000000 > cclk)) {
                crg_value = himci_readl(PERI_CRG49);
                crg_value &= ~(SDIO1_CLK_BIT_HIGH);
                crg_value &= ~(SDIO1_CLK_BIT_LOW);
                crg_value |= SDIO1_CLK_SEL_50M;
                crg_value |= SDIO1_CKEN;
                himci_writel(crg_value, PERI_CRG49);
                reg_value = 0;
            }
        }
```

```
#endif
    } else {
        himci_error("himci host id error!");
        return;
    }
```