Hi3516A/Hi3516D 4-Layer PCB Reference Design Guide

Issue 02

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About This Document

Purpose

This document describes the design key points, requirements, and recommendations for the Hi3516A/Hi3516D 4-layer printed circuit board (PCB).

Related Versions

The following table lists the product versions related to this document.

Product Name	Version
Hi3516A	V100
Hi3516D	V100

Intended Audience

This document is intended for hardware engineers.

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 02 (2014-12-19)

This issue is the second official release, which incorporates the following changes:

The contents related to the Hi3516D are added.

Issue 01 (2014-09-05)

This issue is the first official release.

Contents

1 Power Supply

NOTE

This document uses the Hi3516A as an example. Unless otherwise stated, Hi3516D and Hi3516A contents are consistent.

You are advised to design the power splits and capacitor layout for the 4-layer PCB by following the reference design of HiSilicon.

1. The Hi3516A has four core power supplies: VDD, VDD_CPU, VDD_MEDIA, and VDD_DDR. You are advised to use independent power supply modules to supply power to the four core power supplies and reserve the selective voltage bing (SVB) voltage adjustment circuit for each core power supply. Power supplies AVDD_DDRPLL, AVDD11_PLL, and AVDD33_PLL use π-shape filtering and must be isolated from the I/O power and core power for the Hi3516A by using an EMI bead whose specifications are 100 MHz@1 kΩ. A 100 nF capacitor and a 2.2 μF capacitor must be placed at the two sides of the EMI bead. The100 nF capacitor is placed close to the chip pins and the 2.2 μF capacitor is placed close to the EMI bead.
2. The power must be supplied to the power pins of modules that are not used.
3. AVDD_EFUSE must be connected to GND.

2 DDR

You are advised to design the DDR for the 4-layer PCB by following the reference design of HiSilicon.

A 33 Ω resistor is not connected to the T point on the DDR address trace and command trace in series for the HiSilicon reference board. It is recommended that the design of connecting a 33 Ω resistor in series be reserved.

3 Reset

You are advised to use the internal power on reset (POR) to reset the Hi3516A, SYS_RSTN_OUT to reset the flash memories, GPIO0_0 (pin number: Y1) to reset the sensor, and GPIO0_1 (pin number: D20) to reset the ETH PHY.

4 Sensor

The sensors with differential data interfaces are recommended.

Differential signal traces must be routed by referring to the GND plane, and the plane must be complete.

You are advised to use Sensor_CLK (pin number: AA1) as the working clock of the sensor. This spares a crystal oscillator.

The recommended sensor configuration pin is SPI0/I^2C0.

5 SDIO

The Hi3516A provides two SDIO interfaces and you can select one for facilitating PCB routing as required. SDIO1 is used in the HiSilicon reference design.

6 Analog Audio

You are advised to place a 4.7 μF capacitor close to the AC_MICBIAS pin.

The AC_LINE analog audio input (AI) signal must connect to a 4.7 μF DC blocking capacitor close to the Hi3516A.

The AC_OUT audio output signal must connect to a 470 kΩ pull-down resistor close to the Hi3516A.

Ensure that the signal traces of AC_OUT and AC_LINE are surrounded by GND traces, and the GND vias are evenly distributed on the adjacent GND copper foils.

7 Network Port

It is recommended that a 33 Ω resistor connect to TXCK, RXCK, and MDCK in series at the source end.

You are advised to use EPHY_CLK (pin number: E19) as the working clock of ETH PHY.

8 Configuration Pins

The configuration pins for the Hi3516A have default pull-up and pull-down resistors in the chip. The following table describes the default pin status after power-on when these pins are floated. If the configuration status required by the Hi3516A is the same as the default status, the pin can be floated.

Pin Name	Default Status	Default Function
JTAG_EN	0	Disable JTAG
TEST_MODE	0	Normal mode
POR_SEL	0	Enable POR
SFC_BOOT _MODE	0	The boot mode of the SPI flash is 3-byte mode. It is recommended that the pull-up and pull-down resistors of this pin be reserved so that it is compatible with various flash memories.
BOOT_SEL	0	Boot from the SPI flash
BOOTROM_SEL	0	Disable BOOTROM

Pin Name	Default Status	Default Function
SFC_DEVICE_MODE	0	The SPI NOR flash is selected.
SFC_NAND_BOOT[1:0]	01	SPI NAND flash 8-bit ECC
SFC_NAND_BOOT2	0	SPI NAND flash 2 KB page size

9 Risks

1. The DDR address trace and control trace are not connected to matched resistors in series for the 4-layer PCB in HiSilicon reference design, and therefore the signal quality risk exists. You are advised to connect these traces to matched resistors in series.
2. The TX and RX data traces of the gigabit media independent interface (RGMII) are not connected to matched resistors in series for the 4-layer PCB in HiSilicon reference design, and therefore the signal quality risk exists. You are advised to connect these data traces to matched resistors in series if these data traces are long.
3. One 4.7 µF capacitor and one 100 nF capacitor are connected to the AC_VREF pin for the 4-layer PCB in HiSilicon reference design. You are advised to change the 4.7 µF capacitor to a 10 µF capacitor to ensure the audio quality.
4. Some GPIO and PWM signal traces for the 4-layer PCB in HiSilicon reference design are routed across plane splits. However, the risk is relatively low because these are low-speed signals.