Hi3516A/Hi3516D DDR Configuration Guide

Issue 02

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About This Document

Purpose

This document describes the methods for modifying the commonly used DDR configuration for the Hi3516A/Hi3516D.

Related Versions

The following table lists the product versions related to this document.

Product Name	Version
Hi3516A	V100
Hi3516D	V100

Intended Audience

This document is intended for:

- Field application engineers
- Hardware engineers

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 02 (2015-06-23)

This issue is the second official release, which incorporates the following changes:

Section 1.3 is added.

Issue 01 (2015-03-12)

This issue is the first official release.

1 Changes

CAUTION

For the Hi3516A, the double data rate (DDR) parameters in the software development kit (SDK) are configured based on the 32-bit DDR SDRAM (on the demo board) with the capacity of 4 Gbits by default. For the Hi3516D, the DDR parameters in the SDK are configured based on the 16-bit DDR SDRAM (on the demo board) with the capacity of 4 Gbits by default. Therefore, the following modifications are required if you need to connect the 16-bit DDR SDRAM with the capacity of 2 Gbits to the double data rate controller (DDRC). If you need to change only the bit width or the capacity of the DDR SDRAM, see the following sections. You are advised to pay attention to the modified bits in the following sections (for details about other bits, see the data in the SDK) and not change the bit values. For details, see the chapters related to the DDR in the chip data sheet. If you need to change the capacity of the 32-bit DDR SDRAM to 2 Gbits, make modifications by following the Hi3516A U-boot table. If you need to change the capacity of the 16-bit DDR SDRAM to 2 Gbits, make modifications by following the Hi3516D U-boot table.

1.1 Changing the Bit Width of the 16-bit DDR SDRRM

Perform the following steps:

Step 1 Change the bit width to 16 bits by configuring bit[5:4] of the register with the address of 0x2011_1050 on the **mddrc_dmc1** sheet.

DDRC_CFG_DDRMODE	0x50	0x16	0	write	31	0	0x0000000FD

Step 2 Set the bank bit width to 2 kbits by setting bit[3:0] of the AXI_CONFIG register to **0xb** on the **mddrc_dmc2** sheet.

Register	Offset Address	Value Written to or Read from Register	Delay	Read or Write	Bits to Be Read or Written	Start Bit to Be Read or Written	Register Attribute
AXI_CONFIG	0x0	0x2000b	0	write	31	0	0x0000000FD
PHYINITCTRL	0x8004	0x1429	0	write	31	0	0x0000000FD

NOTE

The value 0x2000c is changed to 0x2000b.

Step 3 Mask the data of the upper 16 bits to be written on the **mddrc_phy** sheet.

PLLCTRL	0x18	0x7	0	write	31	0	0x0000000FD
DXNCTRL2	0x308	0x3	0	write	31	0	0x0000000FD
DXNCTRL3	0x388	0x3	0	write	31	0	0x0000000FD
PLLCTRL	0x18	0x0	0	write	31	0	0x0000000FD

----End

1.2 Changing the Capacity to 2 Gbits

To change the capacity of the DDR SDRAM to 2 Gbits, perform the following steps:

Step 1 Change the value of the DDRC_CFG_RNKVOL register from 0x142 to 0x132 on the **mddrc_dmc1** sheet.

DDRC_CFG_RNKVOL	0x60	0x142	0	write	31	0	0x0000000FD

Step 2 Change the value of bit[7:0] of the DDRC_CFG_TIMING1 register from 0x4126804c to 0x41268028 on the **mddrc_dmc1** sheet. The default DDR bus frequency of the U-boot is 250 MHz. Therefore, the clock cycle is 4 ns. The default refresh cycle for the DDR with the capacity of 2 Gbits is 160 ns. The value 0x28 is calculated as follows: 0x28 (40 in decimal) = DDR refresh cycle/clock cycle (160/4).

DDRC_CFG_TIMING1	0x84	0x4126804c	0	write	31	0	0x0000000FD

Step 3 Change the value of bit[24:16] of the DRAMTIMER1 register from 0x089726c4 to 0x085026c4 on the mddrc_phy sheet. The DDR bus frequency of the U-boot is 500 MHz.

Therefore, the clock cycle is 2 ns. The default refresh cycle for the DDR with the capacity of 2 Gbits is 160 ns. The value 0x50 is calculated as follows: 0x50 (80 in decimal) = DDR refresh cycle/clock cycle (160/2).

DRAMTIMER1	0x34	0x089726c4	0	write	31	0	0x0000000FD

----End

1.3 Changing the Capacity to 1 Gbits

To change the capacity of the DDR SDRAM to 1 Gbits, perform the following steps:

Step 1 Change the value of the DDRC_CFG_RNKVOL register from 0x142 to 0x122 on the **mddrc_dmc1** sheet.

DDRC_CFG_RNKVOL	0x60	0x142	0	write	31	0	0x0000000FD

Step 2 Change the value of bit[7:0] of the DDRC_CFG_TIMING1 register from 0x4126804c to 0x4126801c on the **mddrc_dmc1** sheet. The default DDRC bus frequency of the U-boot is 250 MHz. The frequency of the DDR PHY clock is 500 MHz. Therefore, the clock cycle is 4 ns. The default refresh cycle for the DDR with the capacity of 1 Gbits is 110 ns. The value 0x1c is calculated as follows: 0x1c (27.5 in decimal; rounded up to 28) = DDR refresh cycle/clock cycle (110/4).

DDRC_CFG_TIMING1	0x84	0x4126804c	0	write	31	0	0x0000000FD

Step 3 Change the value of bit[24:16] of the DRAMTIMER1 register from 0x089726c4 to 0x083826c4 on the mddrc_phy sheet. The frequency of the DDR PHY clock is twice that of the DDRC bus. Therefore, the configured value of the PHY should be twice that of the DDRC. The value 0x38 is obtained after 0x1c is multiplied by 2.

DRAMTIMER1	0x34	0x089726c4	0	write	31	0	0x0000000FD

----End