IMX185 Sensor Design Reference

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HiSilicon Technologies Co., Ltd.

Address: Huawei Industrial Base
Bantian, Longgang
Shenzhen 518129
People's Republic of China

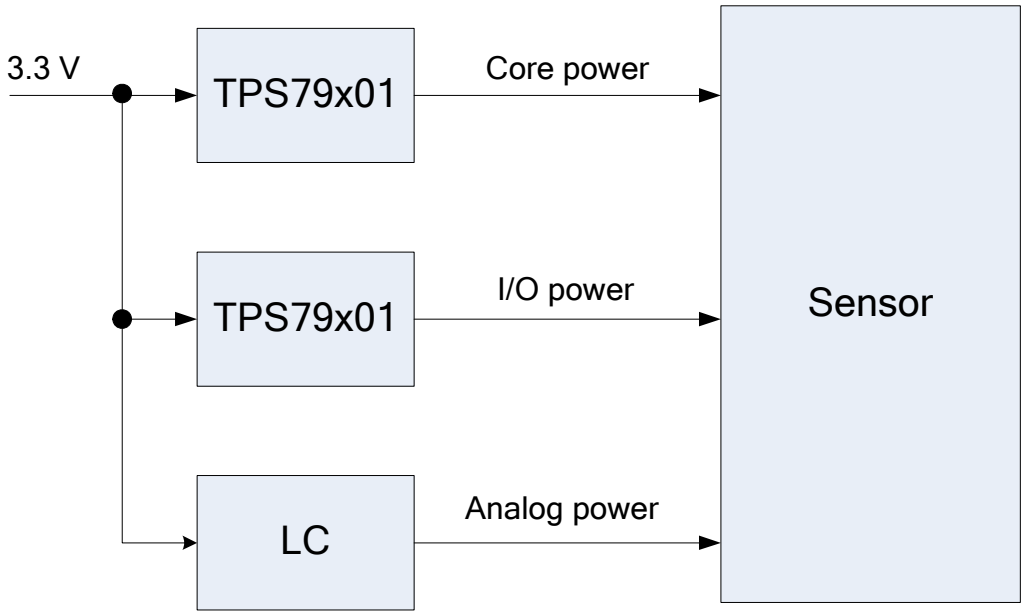
Website: http://www.hisilicon.com

Email: support@hisilicon.com

1.1 Schematic Diagram

1. The IMX185 sensor analog power supply is susceptible to interference. This section describes the recommended power supply design.

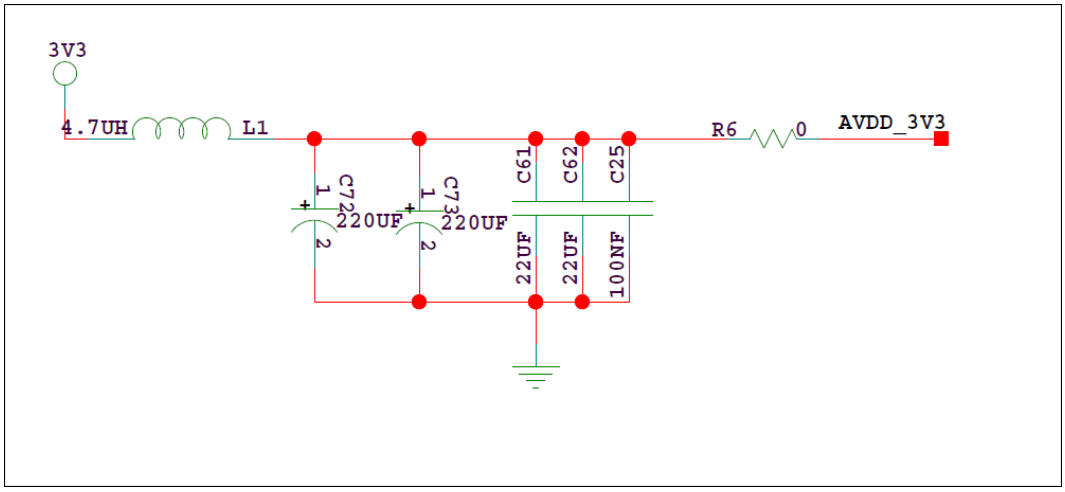
Figure 1-1 Power tree



The recommended power chip is the low-noise low dropout regulator (LDO) such as the TPS79X01 series. Figure 1-1 shows the power tree.

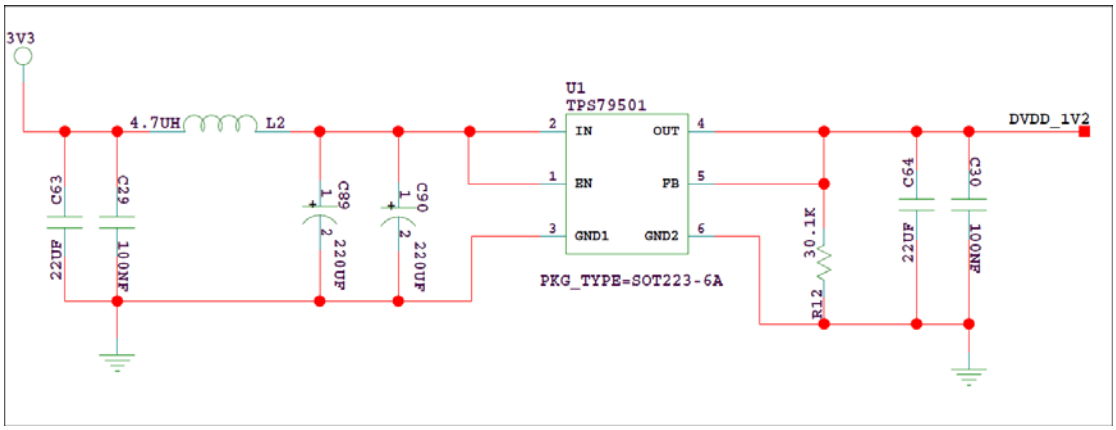
The 3.3 V analog power supply AVDD_3V3 directly obtains power from the image signal processor (ISP) end. An LC filter circuit must be placed before the 3.3 V analog power supply to reduce the noise. A 4.7 µH inductor with shielding and two 220 µF capacitors are used, as shown in Figure 1-2. If there is an available 5 V power supply, it is recommended that the LDO convert the 5 V power supply into 3.3 V power supply and the 3.3 V power be supplied to AVDD_3V3. If horizontal stripes appear on sensor pictures, reduce the noise of the 3.3 V analog power supply.

Figure 1-2 AVDD_3V3 power processing



The AVDD_3V3 analog power supply is easily affected by the noise of the DVDD_1V2 power supply through the crosstalk between them. It is recommended that an LC filter circuit be added to the LDO input end (AVDD_3V3) of DVDD_1V2. A 4.7 µH inductor with shielding and two 220 µF capacitors are used, as shown in Figure 1-3.

Figure 1-3 DVDD_1V2 power processing



2. During the design of filter capacitors for the power pins, ensure that one large filter capacitor and one small one connect to the power pins of AVDD_3V3 and DVDD_1V2, as shown in Figure 1-5.

   A 4.7 µF capacitor and a 100 nF capacitor connects to each power pin of AVDD_3V3 and DVDD_1V2.

3. For other power pins that are sensitive to the power noise, ensure that a capacitor connects to each power pin of VCP, VRL, and VCAP, as shown in Figure 1-4. The recommended capacitance is 4.7 µF. If scroll horizontal stripes appear on sensor picture, enlarge the capacitance of the filter capacitor at each pin of VCP, VRL, and VCAP.

Figure 1-4 Capacitor design for other power pins that are sensitive to the power noise

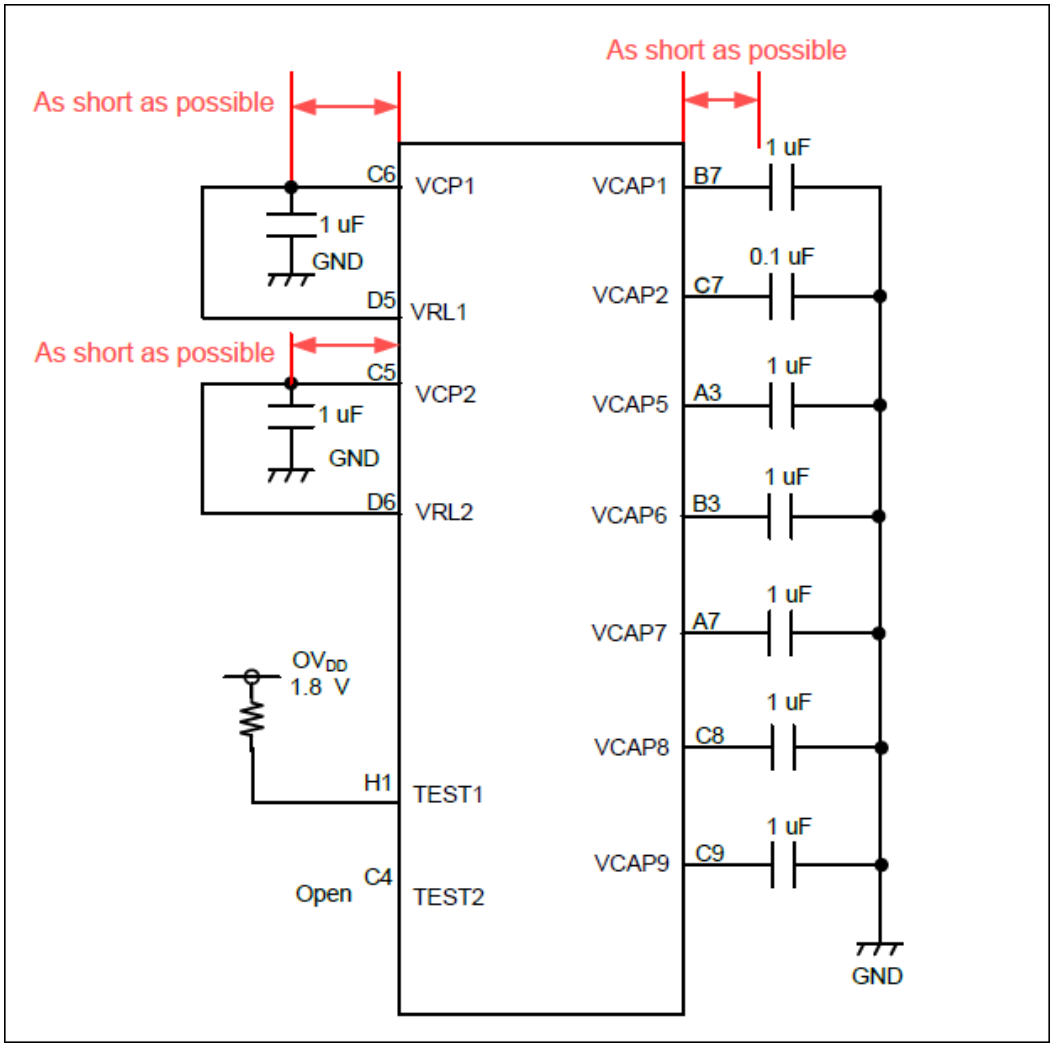
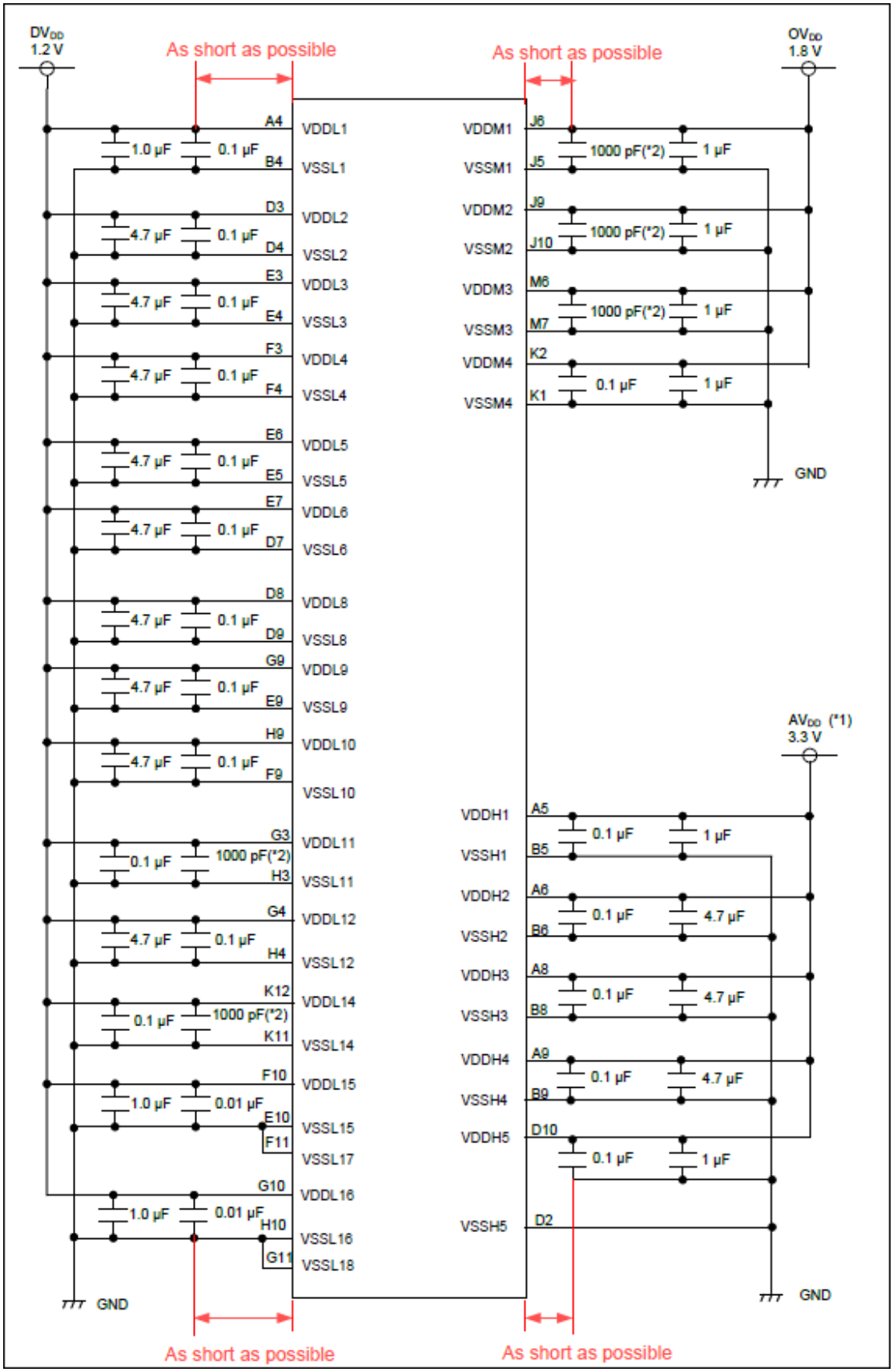


Figure 1-5 Filter capacitor design for power pins

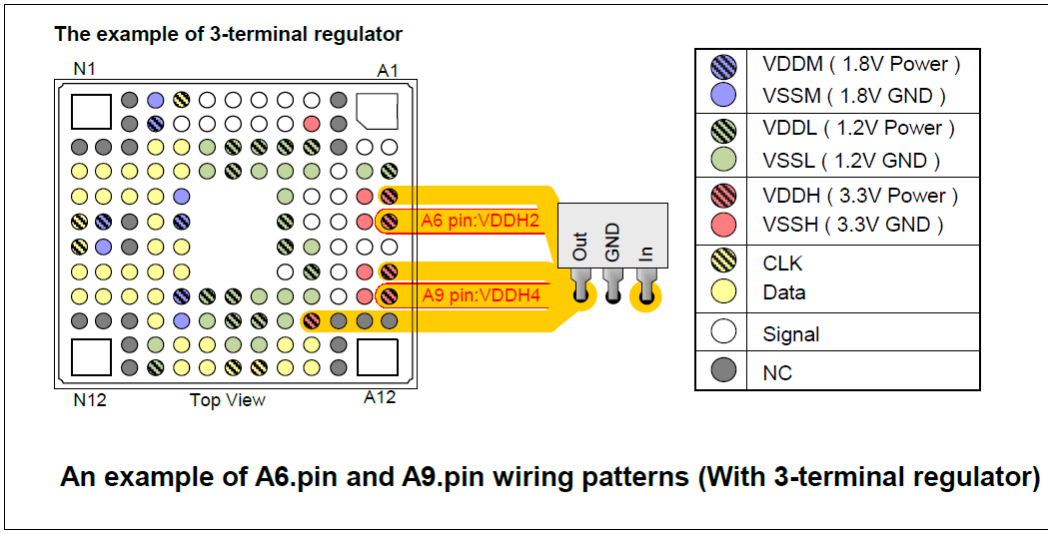


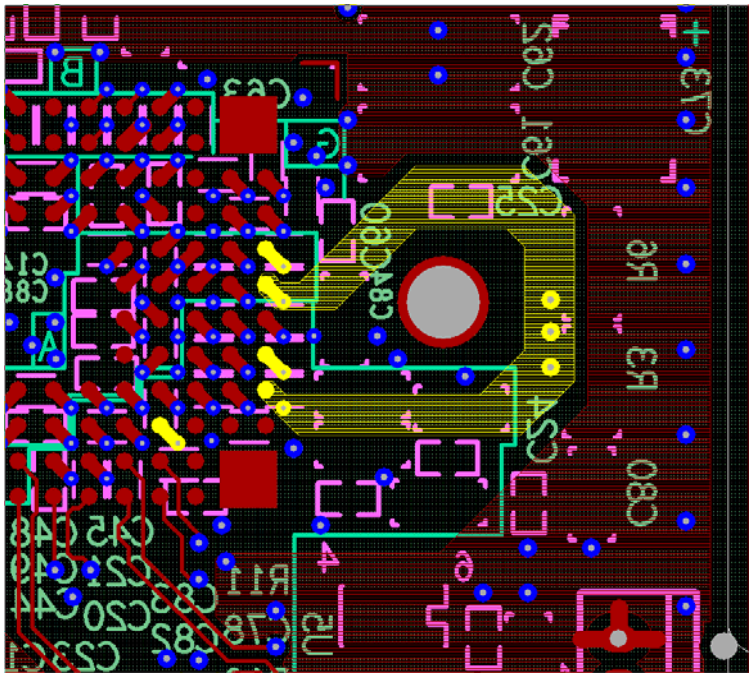
1.2 PCB Design

1. Design of the AVDD_3V3 analog power supply

   For the analog power supply, the power is separately supplied to each analog power pin and the traces are routed as wide as possible. The yellow part in Figure 1-6 shows the separate trace from the AVDD_3V3 analog power supply to the VDDH pin.

Figure 1-6 Design of the AVDD_3V3 analog power supply





2. Capacitor layout

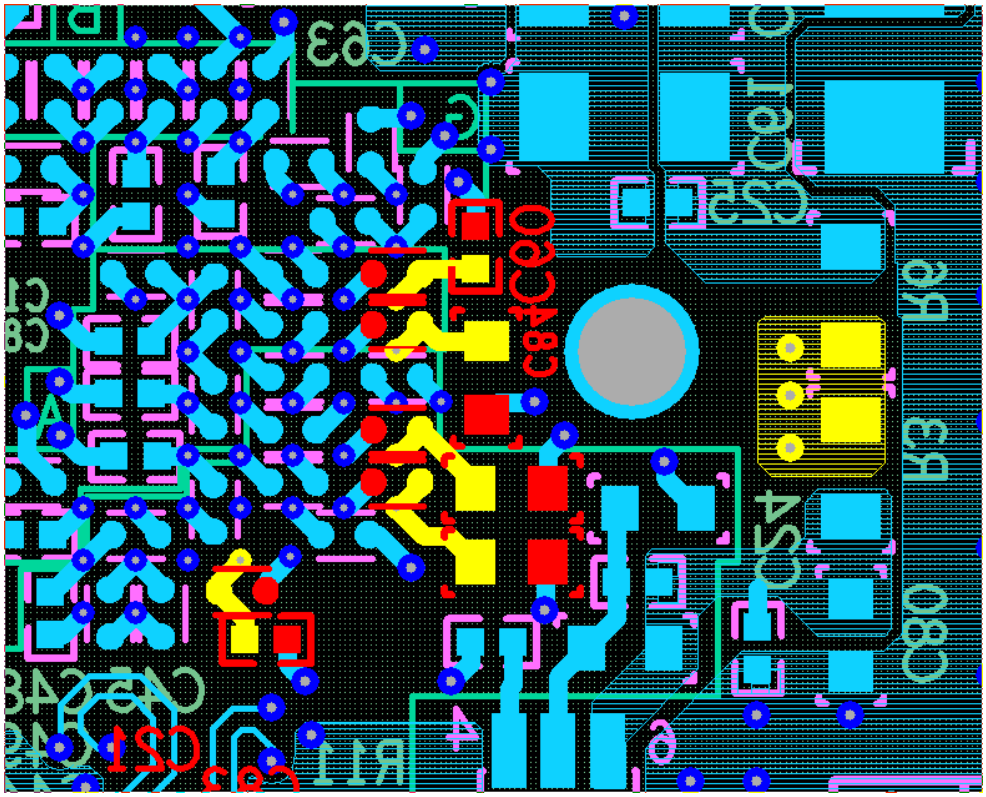
   Ensure that a 100 nF capacitor and a 4.7 µF capacitor (0402 package) is closely placed at each power pin. If the space is limited, choose the 100 nF capacitor.

   The filter capacitors for pins of the analog power supply must be connected to power and GND planes through separate vias and cannot be connected to components on the

surrounding electrical network on the bottom side. Figure 1-7 shows the capacitor layout and via processing method for the AVDD_3V3. The yellow part indicates the AVDD_3V3 analog power supply and the red part indicates capacitors.

The filter capacitors at each pin of VCP, VRL, and VCAP must be connected to GND through separate vias and cannot be connected to components on the surrounding electrical network on the bottom side.

Figure 1-7 Capacitor layout

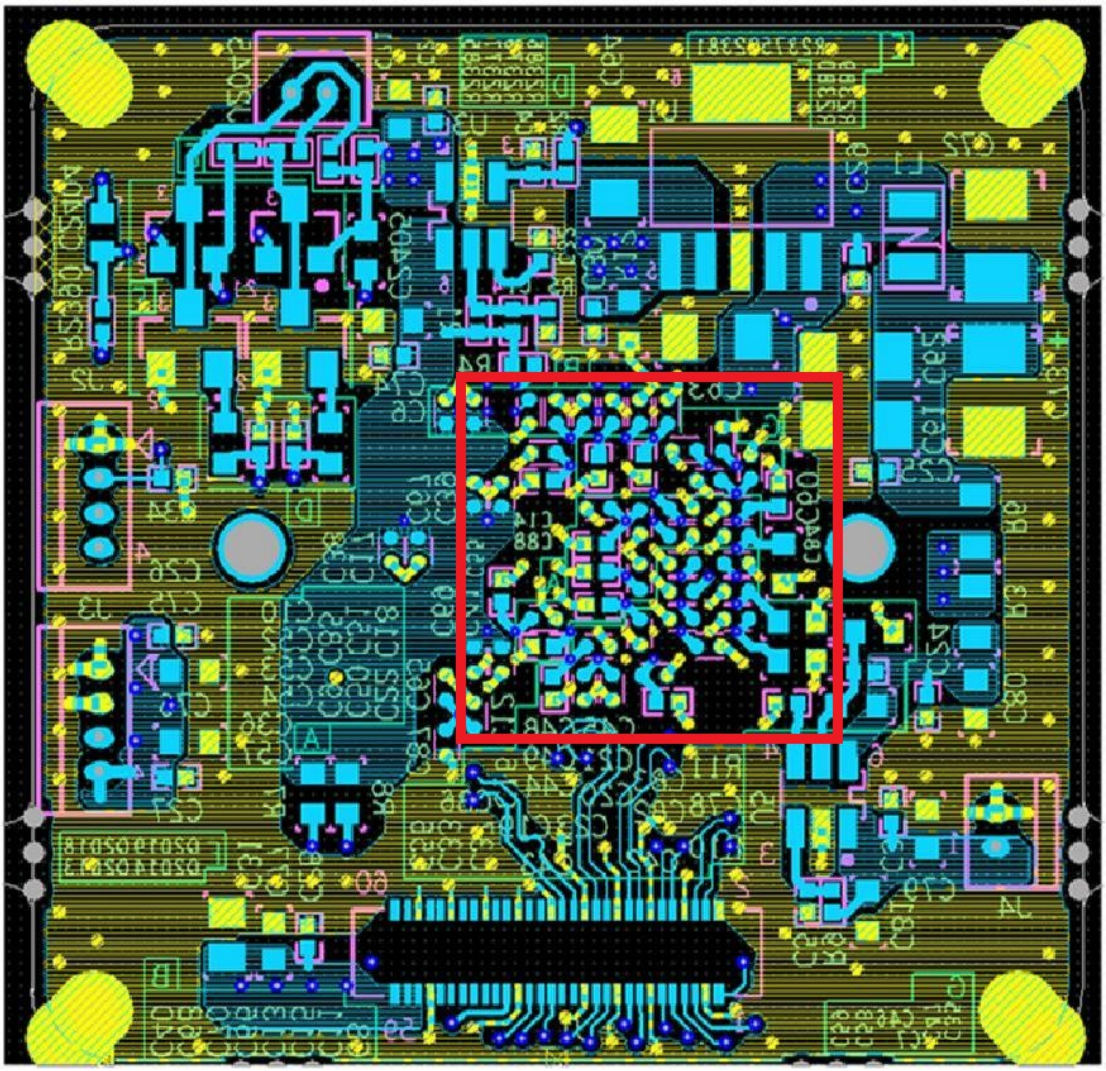


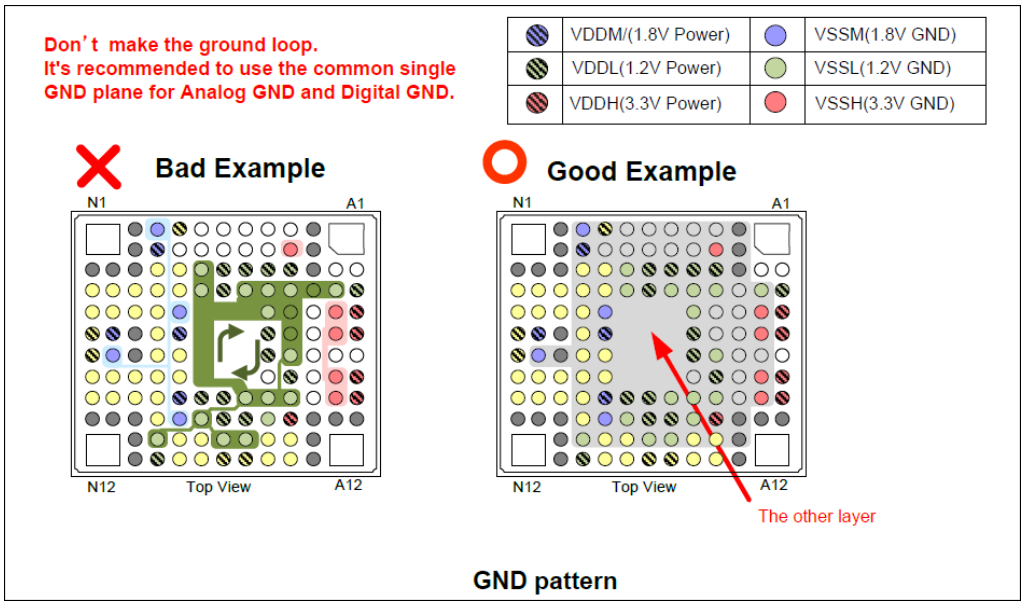
3. Connecting to the GND

   It is recommended that the filter capacitors for sensor power pins be connected to GND through separate vias. The red rectangle region in Figure 1-8 indicates the filter capacitors for the power pins, which need to be connected to GND through separate vias.

   Minimize the return path and avoid the loop.

Figure 1-8 Connecting to the GND





4. The digital signal traces should be routed far from the analog power supply.

   In Figure 1-9, the yellow region indicates the AVDD_3V3 analog power supply and the red region indicates the signal traces

Figure 1-9 Digital signal processing