IPC Correction-free AI

Application Notes

Issue 07

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About This Document

Purpose

This document describes the software and hardware design key points for the Internet Protocol camera (IPC) correction-free automatic iris (AI) circuit.

Related Versions

The following table lists the product versions related to this document.

Product Name	Version
Hi3518A	V100
Hi3518C	V100
Hi3518E	V100
Hi3516C	V100
Hi3516A	V100
Hi3516D	V100
Hi3518E	V200
Hi3518E	V201
Hi3516C	V200
Hi3519	V100
Hi3519	V101
Hi3516C	V300

Intended Audience

This document is intended for:

- Field application engineers

- Hardware engineers

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 07 (2016-08-24)

This issue is the seventh official release, which incorporates the following change:

The contents related to the Hi3519 V101 and Hi3516C V300 are added.

Issue 06 (2016-03-14)

This issue is the sixth official release, which incorporates the following change:

Chapter 1 Description

Section 1.1 is modified.

Issue 05 (2015-11-09)

This issue is the fifth official release, which incorporates the following change:

The content related to the Hi3519 V100 is added.

Issue 04 (2015-09-28)

This issue is the fourth official release, which incorporates the following changes:

The contents related to the Hi3518E V200, Hi3518E V201, and Hi3516C V200 are added.

Issue 03 (2015-03-30)

This issue is the third official release, which incorporates the following change:

Chapter 3 is added.

Contents

1 Description

1.1 Introduction

You can control the amount of light entering an AI lens by increasing or decreasing the aperture based on image signal processor (ISP) outputs.

AI lenses include video-driven lenses and DC-driven lenses.

- Video-driven lens: The lens converts video amplitude signals received from a camera into iris motor control signals by using a built-in amplifier circuit. Generally, three pins are used for a video-driven AI interface, including the power supply pin (+), video pin, and ground pin.
- DC-driven lens: The lens controls the iris by using the DC voltage on a camera. It drives the built-in iris motor by using DC voltage transferred over the built-in iris motor driver circuit. Four pins are used for a DC-driven AI interface, including DRV+, DRV–, CONT+, and CONT–.

DC-driven lenses are widely used in the security and protection field. Descriptions of the DC-driven lenses are as follows:

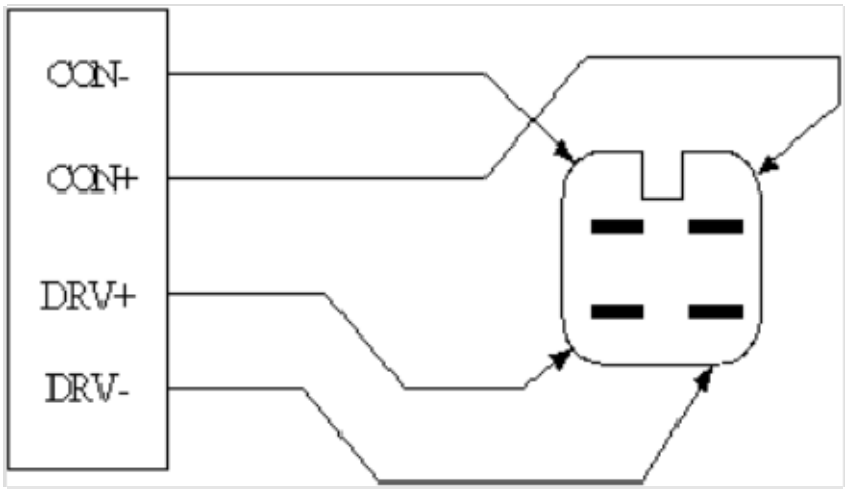
The iris is an optical curtain driven by a fixed drive coil and a rotational magnetic core. A feedback coil (also called a damping coil or braking coil) is assembled with the fixed drive coil.

When the light is weak, a camera increases the positive voltage transferred from the totem-pole drive optional amplifier to the drive coil. The drive coil is driven by positive voltage, and the optical curtain moves towards the opening direction. In addition, the feedback coil cuts the magnetic lines of the rotor, generating electromotive force. The electromotive force increases as the rotational speed of the rotor increases and is coupled to the negative feedback terminal of the operational amplifier. The operational amplifier then decreases the voltage output to the drive coil for controlling the opening speed of the optical curtain.

When the light is strong, the camera transfers negative voltage to the circuit. The drive coil is driven by negative voltage, and the optical curtain moves towards the closing direction. In addition, the negative feedback terminal of the feedback coil responds to reduce the closing speed of the optical curtain. Based on continuous adjustment by the camera, the optical curtain is in a dynamic balancing state, which indicates the opening size of the optical curtain.

Figure 1-1 shows the AI control signal interfaces and AI motor interfaces.

Figure 1-1 AI control signal interfaces and AI motor interfaces



Before verifying the AI function, ensure that the drive voltage of the AI control circuit changes linearly within a certain range according to the PWM duty cycle. Table 1-1 describes the mapping between the drive voltage of the AI control circuit and the duty cycle of the PWM signal (no load and lens). Table 1-2 describes the mapping between the drive voltage of the AI control circuit and the duty cycle of the PWM signal duty cycle (with loads and lenses).

Table 1-1 Mapping between the drive voltage of the AI control circuit and the duty cycle of the PWM signal (no load and lens)

Duty Cycle of the PWM Signal	DRV (V)
79%	3.45
78%	3.42
77%	3.32
76%	3.22
75%	3.12
74%	3.02
73%	2.92
72%	2.82
71%	2.72
70%	2.62
69%	2.52
68%	2.42
67%	2.32
66%	2.22

Duty Cycle of the PWM Signal	DRV (V)
65%	2.12
64%	2.02
63%	1.92
62%	1.82
61%	1.72
60%	1.62
59%	1.52
58%	1.42
57%	1.32
56%	1.22
55%	1.12
54%	1.02
53%	0.92
52%	0.82
51%	0.72
50%	0.62
49%	0.52
48%	0.42
47%	0.32
46%	0.22
45%	0.12
44%	0.02
43%	0.01
42%	0.01
41%	0.01
40%	0.01
39%	0.01

Table 1-2 Mapping between the drive voltage of the AI control circuit and the duty cycle of the PWM signal duty cycle (with loads and lenses)

Duty Cycle of the PWM Signal	DRV (V)
79%	2.88
78%	2.88
77%	2.88
76%	2.88
75%	2.88
74%	2.88
73%	2.88
72%	2.88
71%	2.88
70%	2.87
69%	2.87
68%	2.85
67%	2.8
66%	2.72
65%	2.62
64%	2.53
63%	2.43
62%	2.34
61%	2.24
60%	2.15
59%	2.06
58%	1.96
57%	1.87
56%	1.77
55%	1.68
54%	1.59
53%	1.5
52%	1.4
51%	1.31
50%	1.22

Duty Cycle of the PWM Signal	DRV (V)
49%	1.12
48%	1.03
47%	0.94
46%	0.85
45%	0.76
44%	0.66
43%	0.57
42%	0.48
41%	0.39

The recommended operational amplifier models are ST LM358 and TI TLV2372.

The AI operational amplifier chip must be selected based on the following test data of actual circuits:

- When there are no loads and lenses, and the duty cycle of the PWM output signal is 60%, the output amplitude of the DRV+ signal ranges from 1.6 V to 2 V.
- When there are loads and lenses, and the duty cycle of the PWM output signal is 50%, the output amplitude of the DRV+ signal is less than 1.6 V.
- When there are loads and lenses, and the duty cycle of the PWM output signal is 80%, the output amplitude of the DRV+ signal is greater than 2.8 V.

Note that the preceding test data is obtained from the tests based on the HiSilicon demo board and lenses, and only serves as references. During application, when the duty cycle of the PWM output signal is 10%, the lenses can be disabled. When the duty cycle of the PWM output signal is 90%, the lenses can be enabled. When there are loads, each time the duty cycle of the PWM output signal in the linear region is incremented by 1%, the output amplitude of the DRV+ signal is incremented by about 0.1 V accordingly.

2 AI Hardware Implementation Circuit

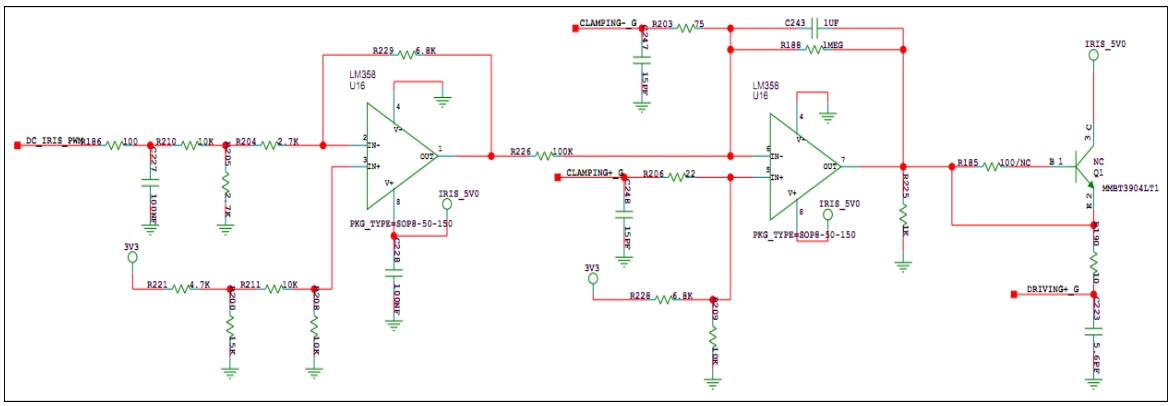
2.1 AI Analysis

When the drive voltage is greater than the damping coil voltage, the iris is opened. The current luminance information is collected by algorithms based on the histograms in the ISP.

- When the automatic exposure (AE) is set to the minimum value and the luminance shown in the histogram is higher than the normal value, decrease the aperture and the amount of light until the luminance of the image becomes normal.
- When the AE is set to the maximum value and the luminance shown in the histogram is lower than the normal value, increase the aperture and the amount of light until the luminance of the image becomes normal.

To slowly open and close the iris, the system outputs the PWM duty cycle based on the collected luminance information, converts the PWM signal into DC voltage over the RC circuit, and controls the drive voltage by using the amplifier circuit.

Figure 2-1 AI control circuit



2.2 Preferable Hardware Implementation Circuit

- You must design the circuit by completely following the HiSilicon circuit for the IP camera. For details, see the circuit diagram of the DC_IRIS I part in the schematic diagram of the ai_circuit_verb board, as shown in Figure 2-1.
- It is required that 1% resistors and 5% capacitors be used in the circuit to ensure precision control.
- During the product design, you cannot use resistors and capacitors whose specifications are close to those of the required resistors and capacitors, and you cannot use 5% resistors and 10% capacitors to replace the required resistors and capacitors. The iris precision control may be affected due to the consistency variance of components from different lots. You cannot reduce the number of resistors through equivalence. You must choose the operational amplifier models recommended by HiSilicon.
- In the D-IRIS circuit, the quality of the 5 V power supply is important, which directly affects the iris precision control. The iris may oscillate if the ripples and noises of the power supply are too large. Theoretically the smaller the ripples and noises of the 5 V power supply are, the more precise the iris control is. It is recommended that the ripples and noises of the 5 V power supply be less than 30 mV (the smaller, the better). For details about the 5 V power supply, see the circuit diagram of the DC_IRIS I part in the schematic diagram of the ai_circuit_verb board, as shown in Figure 2-1.

3 AI Algorithm

Note the following when using the AI algorithm:

- Before testing the lens by using the AI algorithm, you are advised to check whether the AI circuit characteristics meet the preceding circuit design requirements.
- For the DC iris, the correction-free AI algorithm adjusts the iris based on the environment luminance. When the minimum exposure time and gain are reached, the AI algorithm starts iris control. If the iris control meets the requirements of the target luminance, the AE exits directly and the exposure time and gain remain unchanged. After the picture luminance becomes stable and the PWM duty cycle retains the value when the iris is opened for a while, the AI algorithms consider that the iris has been opened to the maximum size, end the iris control, and hand over the control to the AE algorithm. During iris control, if AE algorithm parameters that need to take effect immediately (for example, the maximum/minimum exposure time, maximum/minimum gain, and anti-flicker parameter) are changed, the AE algorithm responds instantaneously. Then the AI algorithm determines whether to start iris control based on the configured parameters and ambient luminance. Starting or ending iris control takes a short period of time. Therefore, you are advised to disable AI when the non-DC iris is used; otherwise, the AE adjustment speed will be affected. It is recommended that AI be always enabled for the DC iris because disabling and enabling AI may result in iris control exceptions.
- When the DC iris is tested on the HiSilicon demo board or reference board, you must specify the PWM number when loading the .ko driver of the ISP. For the Hi3518 series chips, PWM0 is used by default in the SDK. You can change the PWM number from PWM0 to PWM1 by running **insmod hi3518_isp.ko pwm_num=1**. For the Hi3516A, PWM4 and PWM5 are used for the HiSilicon demo board and reference board respectively. However, PWM5 is used by default in the SDK. You need to change the PWM number to PWM4 by running **insmod hi3516a_isp.ko pwm_num=4** when the HiSilicon demo board is used. Note that the corresponding pin multiplexing registers need to be modified when different PWMs are used. You can change the PWM number of the AI control circuit for chips of later versions by running **insmod hi35*XX*_isp.ko pwm_num=*X*** (**hi35*XX*** indicates the chip model, and **pwm_num=*X*** indicates that PWM*X* is used).
- For details about the AI MPIs, see the *HiISP Development Reference*.