SDK Differences Between the Hi3516A/Hi3516D and the Hi3518A

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About This Document

Purpose

The Hi3516A is a high-performance system-on-chip (SoC) launched by HiSilicon for high definition Internet Protocol camera (HD-IPC) applications. The software development kit (SDK) of the Hi3516A is basically the same as that of Hi3518A and is optimized for better performance. This document describes the differences between the Hi3516A and the Hi3518A from the aspects of specifications, SDK components, and application programming interfaces (APIs).

Related Versions

The following table lists the product versions related to this document.

Product Name	Version
Hi3516A	V100
Hi3516D	V100

Intended Audience

This document is intended for:

- Technical support engineers
- Software development engineers

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 01 (2014-12-20)

This issue is the first official release, which incorporates the following changes:

Chapter 4 "Differences Between the Hi3516D and Hi3516A" is added.

Issue 00B02 (2014-09-14)

This issue is the second draft release, which incorporates the following changes:

Chapter 1 Differences on Specifications

In Table 1-1, the differences of the VGS and TDE are added, the audio differences are deleted, and the differences of the ISP, audio output, video pre-processing, and network are modified.

Issue 00B01 (2014-07-25)

This issue is the first draft release.

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1 Differences on Specifications

Table 1-1 lists the IPC specification differences between the Hi3516A and the Hi3518A. For details about the specifications of the Hi3516A, see the *Hi3516A Full-HD IP Camera SoC Brief Data Sheet*.

Table 1-1 Differences on specifications

Key Specifications	Hi3516A	Hi3518A
Processor	A7@ 600 MHz	ARM 9@Max. 440 MHz
Image signal processor (ISP)	• Noise reduction in fixed pattern noise (FPN) mode • Digital anti-jitter • Digital wide dynamic range (WDR), frame base/line base WDR, and tone mapping • ISP tuning tools for the PC • 5-megapixel picture inputs	• Defog and anti-false color • 2-megapixel picture inputs
Video input (VI)	• 8-/10-/12-/14-bit RGB Bayer input, a maximum of 150 MHz clock frequency • BT.601, BT.656 and BT.1120 progressive input • Mobile industry processor interface (MIPI), low-voltage differential signaling (LVDS)/sub-LVDS, and high-speed serial pixel interface (HiSPI) • Compatibility with mainstream HD CMOS sensors provided by Sony, Aptina, OmniVision, and Panasonic • Various sensor levels supported • Programmable sensor clock output • Maximum input resolution of 5 megapixels	• One VI interface that provides the ISP function • 8-/10-/12-bit RGB Bayer input, a maximum of 74.25 MHz clock frequency • BT.601 and BT.656 • 1080p@30 fps or 720p@30 fps • Lens distortion correction • Picture rotation by 90° or 270°

Key Specifications	Hi3516A	Hi3518A
Video output (VO)	• One CVBS/BT656, 960H@50, or 960H@60 output • One BT.1120 VO interface for connecting to the external high-definition multimedia interface (HDMI) or serial digital interface (SDI), maximum performance of 1080p@60 fps • CVBS/BT.656 output or BT.1120 output	• One composite video broadcast signal (CVBS) output • One BT.1120 VO interface for connecting to the external HDMI or SDI interface, maximum performance of 1080p@30 fps • CVBS output or BT.1120 output
Video pre-processing (VPP)	• 3D denoising, picture enhancement, and dynamic contrast enhancement • 1/15x video zoom-out (zoom-in not supported) • Cover overlay pre-processing for eight regions	• One input and multiple outputs. That is, after an input picture is processed, several pictures can be output for subsequent processing. • Scaling on pictures in channels
Video graphics subsystem (VGS)	• 1/2x to 2x graphics scaling • Anti-flicker for output videos and graphics • Rotation and lens distortion correction (LDC)	None
Two-dimensional engine (TDE)	YUV domain processing not supported	YUV domain processing
Video encoding/decoding performance	• A maximum of 5-megapixel resolution for H.264/H.265 encoding • Real-time H.264/H.265 encoding of multiple streams: – 1080p@30 fps+720p@30 fps+VGA@30 fps – 1080p@60 fps+VGA@30 fps – 5-megapixel@30 fps+VGA@30 fps • JPEG snapshot at 5-megapixel@8 fps	• H.264 BP/MP encoding • 720p@30 fps+VGA@30 fps+QVGA@30 fps+720p@1 fps JPEG snapshot
DDR	• DDR3/3L synchronous dynamic random access memory (SDRAM) interface • 32-bit DDR3/3L@600 MHz • Maximum capacity of 4 Gbits	DDR2/DDR3 SDRAM interface, 16-bit data width, 440 MHz, a maximum of 2 Gbits capacity for the Hi3518A or 1 Gbit for the Hi3518C

Key Specifications	Hi3516A	Hi3518A
Network	• Reduced gigabit media independent interface (RGMII) and reduced media independent interface (RMII) modes, 100/1000 Mbit/s full-duplex or half-duplex mode, physical (PHY) clock output • Media independent interface (MII) mode (half duplex not supported in MII mode)	• Media access control (MAC) interface • RMII and MII modes, 10/100 Mbit/s full-duplex or half-duplex mode, PHY clock output
Secure digital input/output (SDIO)	Two SDIO 3.0 interfaces, supporting secure digital extended capacity (SDXC)	One SDIO 2.0 interface, supporting a maximum of 32 GB secure digital high capacity (SDHC)
Analog-to-digital converter (ADC)	One integrated low-speed ADC with dual channels	One integrated low-speed ADC with dual channels

2 Differences on SDK Components

Table 2-1 describes the SDK component differences between the Hi3518A and the Hi3516A.

Table 2-1 Differences on SDK components

SDK Component	Hi3516A	Hi3518A
lib	uClibc-0.9. 33.2 glibc-2.16-2012.09	uClibc-0.9.32.1 glibc-2.11.1
Tool chain	arm-hisiv300-linux- arm-hisiv400-linux- gcc 4.8	arm-hisiv100nptl-linux- arm-hisiv200-linux- gcc 4.4.1
Linux Kernel	linux-3.4.y, supporting A7, neon, and VFP	linux-3.0.y, supporting ARM9
File System	busybox-1.20.2.tgz	busybox-1.16.1.tgz

3 Differences on APIs

Table 3-1 describes API differences between the Hi3516A and the Hi3518A. For details, see the *HiMPP V2.0 Media Processing Software Development Reference*.

Table 3-1 Differences on MPIs

Module	Change Extent of the Hi3516A Compared with the Hi3518A	Change Description
System control	Same	-
ISP	Partially new	• 2-to-1 WDR (frame/line mode) • ACM function • DIS function • FPN (frame/line mode, configurable) • Defog • **IspDev** added for MPIs for supporting multiple ISPs
VI	Partially modified	Added the online VI-VPSS mode, in which picture data of VI channels is not written into the memory. Parameters in script load are used to control whether to enable the online mode. • Implemented the cover function in the VPSS. • Implemented invocation of the VGS to provide the CoverEx/OSD/LDC/Rotate/extended channel in the VPSS in online mode. • Canceled the user picture function in online mode. • Improved the Bayer dump function. • Added the RAW data read function for debugging. • Added the DCI function. • Added the function of outputting compressed picture data in offline mode. • Added the WDR buffer control function for interoperation with the ISP WDR. • Added the BT.1120 progressive input.

Module	Change Extent of the Hi3516A Compared with the Hi3518A	Change Description
VPP	Partially new	Added the online VI-VPSS mode, that is, the VPSS only supports one group. • Supported the 1 to 4 VPSS. The 3D NR processing can be enabled or disabled for pictures of one channel. • Added the LDC/Rotate/CoverEx/OSD function in subsequent processing. • Added arbitrary quadrilateral solid covers (8 in total), which can be enabled or disabled for a channel independently. • Supported statistics collection on region luminance sums. • Supported selection of major-stream channel data or 3D NR reconstructed frames as the 3D NR reference source. • Added the function of outputting compressed picture data. • Supported configuration of the enable status of 3D NR reference frame compression (controlled by module parameters). • Provided a low-delay scheme.
Video encoding	Partially new	• Deleted the group concept. An encoding channel can be directly created. • Modified the scheme of using the color-to-gray function. • Added H.265 functions. • Supported control of the ROI background frame rate. • Added the policy of evenly discarding frames when the transient bit rate crosses the threshold. Discarded frames can be arranged into PSKIP frames. • Supported channel priorities for working with the low-delay scheme. • Supported SVC-T of H.264.
VO	Partially modified	• Added the direct VO scheme. For a single channel, the display buffer is reduced.
FrameBuffer	Same	-
Motion detection (MD)	Partially new	• Added detection of input user pictures. • Supported 960x960-resolution pictures.
TDE	Partially simplified	• Added a VGS module dedicated to video graphics/picture processing. • Deleted video picture-related functions in TDE. Only graphics processing is supported (in the RGB area).
Region	Newly added function	Modified the OSD usage scheme. • Added a scheme of using the canvas. • Added selection of the field picture overlay.

Module	Change Extent of the Hi3516A Compared with the Hi3518A	Change Description
VGS	Newly added module	• Added the decompression, scaling, rotation, and LDC functions for video pictures. • Supported OSD overlay. • Supported single-component scaling and rotation. • Added arbitrary quadrilateral solid/void covers (supporting point/line drawing).
Audio	Newly added function	• Added setting of the input and output track modes. • Supported the output muting function and the fade-in/fade-out function. • Added the function of controlling the output volume.
Intelligent video engine (IVE)	Newly added function	• Added 28 operators for supporting boundary security and video diagnosis.

4 Differences Between the Hi3516D and Hi3516A

Table 4-1 describes the differences between the Hi3516D and Hi3516A. Unless otherwise specified, the specifications of the Hi3516D are the same as those of the Hi3516A.

Table 4-1 Differences between the Hi3516D and Hi3516A

Module	Specifications	Difference
Chip	DDRC	The Hi3516D supports only the 16-bit DDR3/3L SDRAM.
	Performance	The maximum encoding performance of the Hi3516D is 3-megapixel@30 fps+VGA@30 fps.