Hi3516A DMEB DDR3 Test Report

System History

Date	Contents	Remarks
2015-01-27	The test is performed based on DDR3 1333 MHz AC150.	

Note: All test data in this report is obtained based on the samples tested by HiSilicon. It is provided for reference only, and cannot replace the related tests that should be conducted by customers.

Information

Chipset	HI3516A
Board Name	Hi3516A DMEB VER.A
DRAM PartNumber	Micron MT41K256H16HA
Oscilloscope	DSA72004C DPX
Temperature	25ºC
DRAM Operating Frequency	600MHz(DDR3)
VDD/Vref-CA/Vref-DQ/Vcore	1.5 V/0.75 V/0.75 V/1.1 V
DRAM_RODT	ODT OFF
SOC_RODT	ODT OFF
DRAM_RON	40ohm
SOC_RON	CLK:34 ohm AC 2T:48 ohm AC 1T:48 ohm DQS:40 ohm DQ:40 ohm

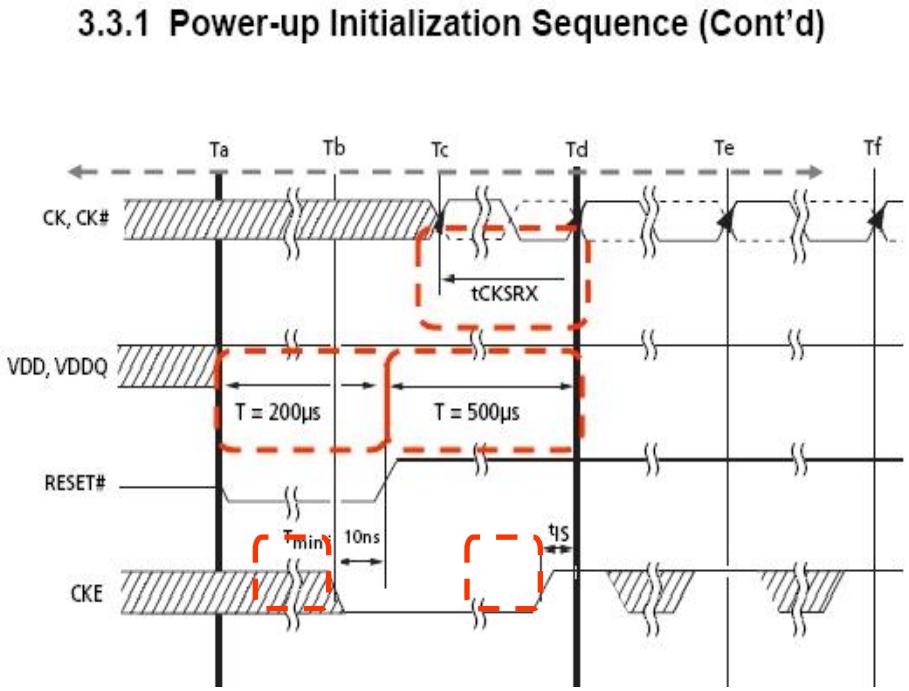
Signal Integrity Summary & Conclusion

Judgment&Summary
The margin for the CLK0 jitter (per) of the differential clock is insufficient. The jitter defined in the SPEC standard is ± 85 ps, whereas the test result is –82.57 ps to +79.38 ps. 1. A sufficient margin of the setup hold time is recommended according to the tested AC signal timing. 2. The timing margin of the DQ Training window is sufficient. 3. The result of the 7 x 24-hour high- and low-temperature environment test is normal. Comprehensive assessment: the margin for the CLK0 jitter (per) is insufficient, and the risk is controllable.

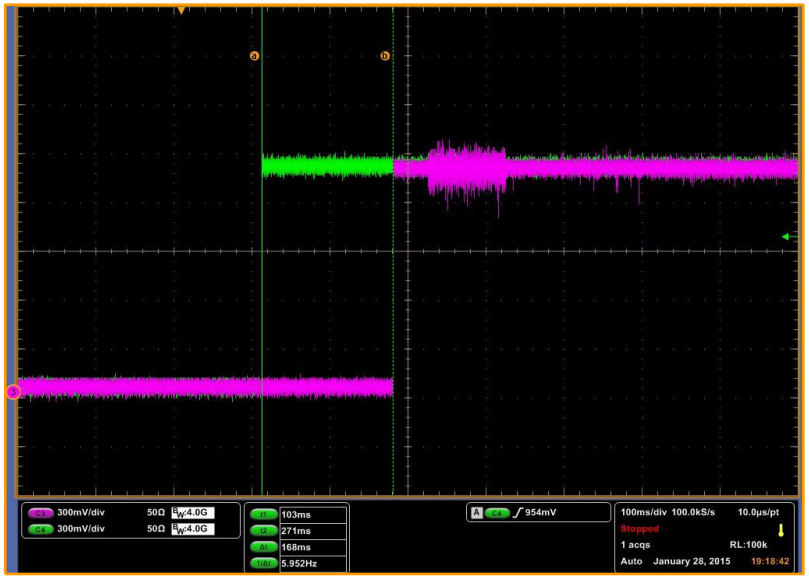
Measurement Item	Result	Remark
Sequence Check	**PASS**	
Power Check	**PASS**	
Signal Integrity Check	**Fail**	Insufficient margin for the CLK0 Jitter (per)

Power Up Initialization Sequence Check Result

- **SPEC**



- **Stable VDD to /Reset Up**

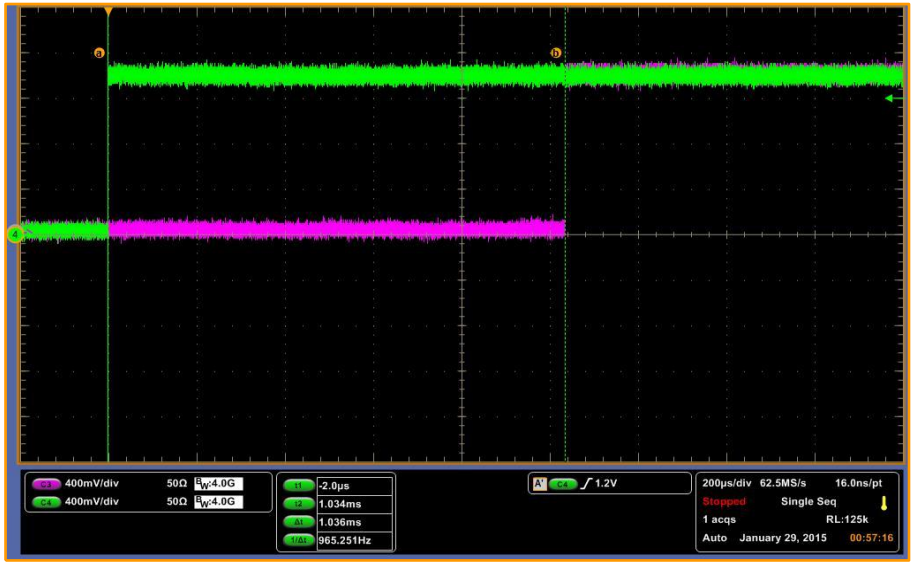


CH3:Reset
CH4:VDD

Parameter	Time	Spec	Result	Remark
Stable VDD to /Reset Up	168ms	Min:200us	PASS	/RESET needs to be maintained for minimum 200us with stable power. (JEDEC spec.)

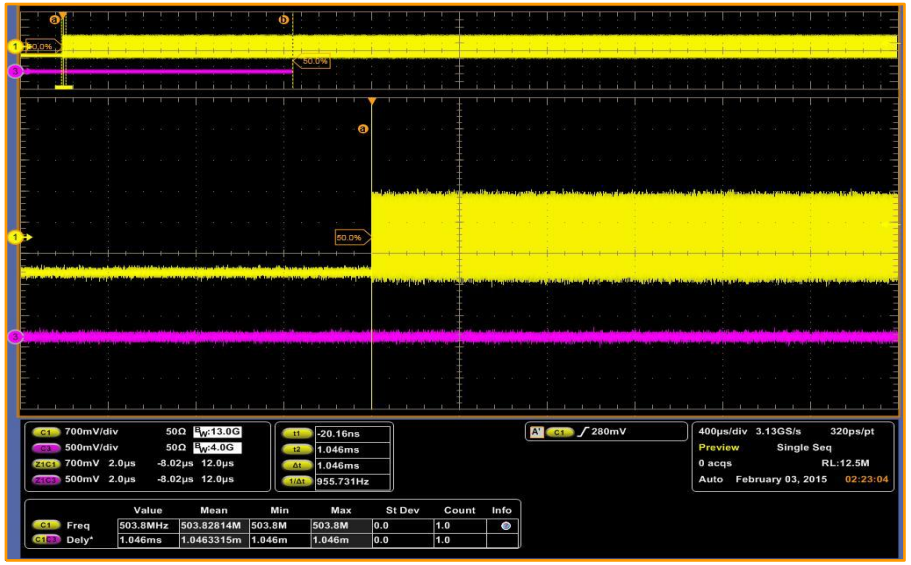
Power Up Initialization Sequence Check Result

- /Reset Up To CKE Up



CH3:CKE
CH4:Reset

- tCKSRX

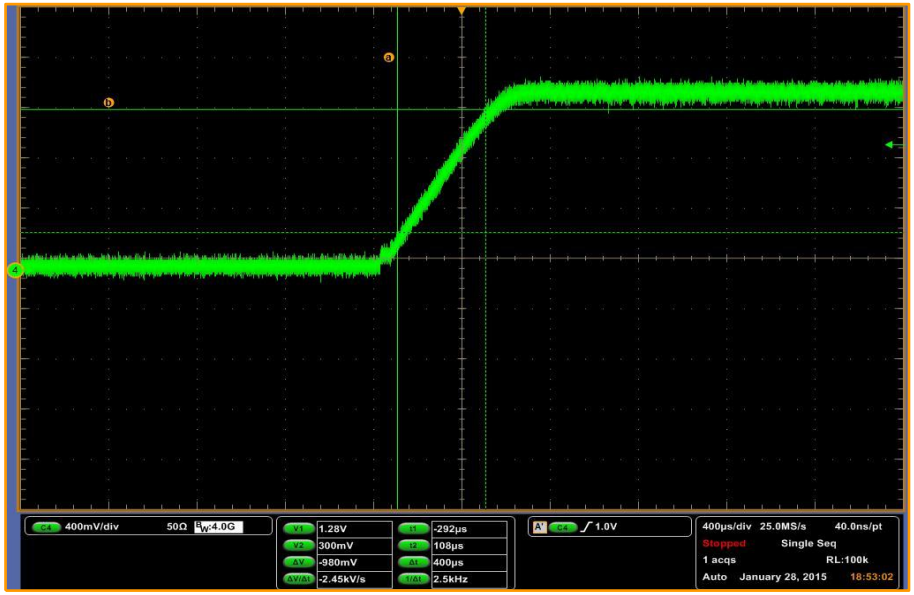


CH1:CLK
CH3:CKE

Parameter	Time	Spec	Result	Remark
/Reset Up To CKE Up	1.036ms	Min:500us	PASS	After /RESET is de-asserted. Wait for another 500us until CKE becomes active.(JEDEC spec.)
tCKSRX	1.046ms	Min:Max(5 tCK,10ns)	PASS	Clocks (CK, CK#) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active.(JEDEC spec.)

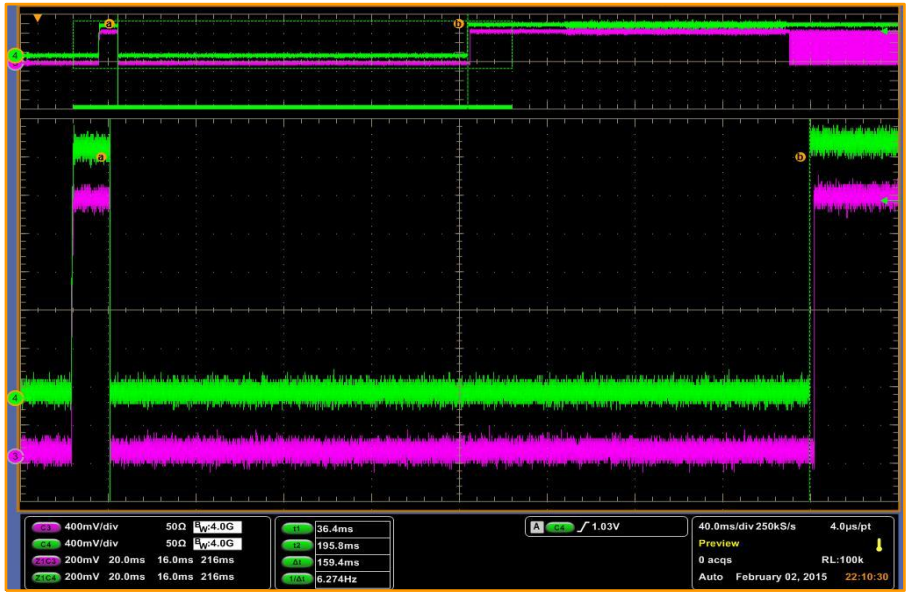
Power Up Initialization Sequence Check Result

- **VDD Rising Time**



CH4:VDD

- **CKE Falling Edge To Reset Rising Edge**

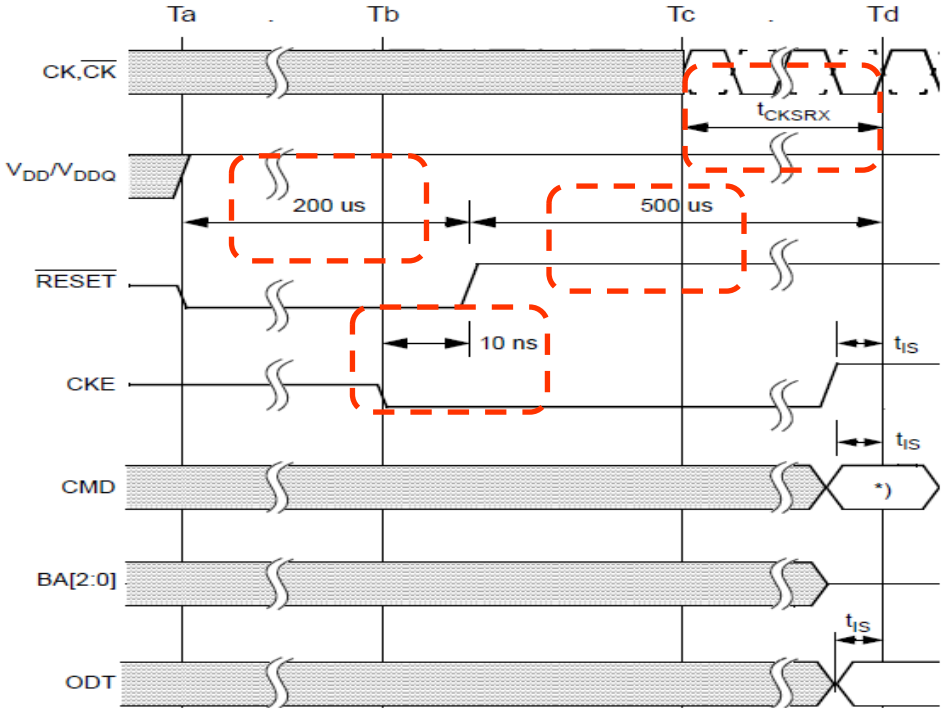


CH3:CKE
CH4:Reset

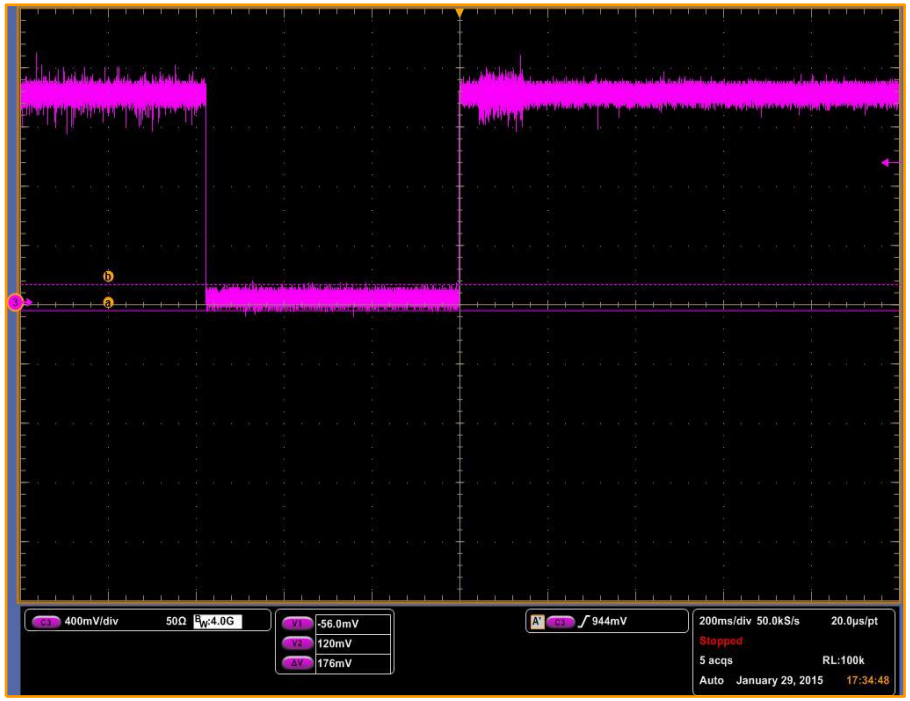
Parameter	Time	Spec	Result	Remark
VDD Rising Time	400us	Max:200ms	PASS	The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms.(JEDEC spec.)
CKE Falling Edge to Reset Rising Edge	159.4ms	Min:10ns	PASS	CKE is pulled “Low” anytime before RESET# being de-asserted (min. time 10 ns).

Reset Initialization Sequence Check Result

SPEC



Reset Low Level Voltage

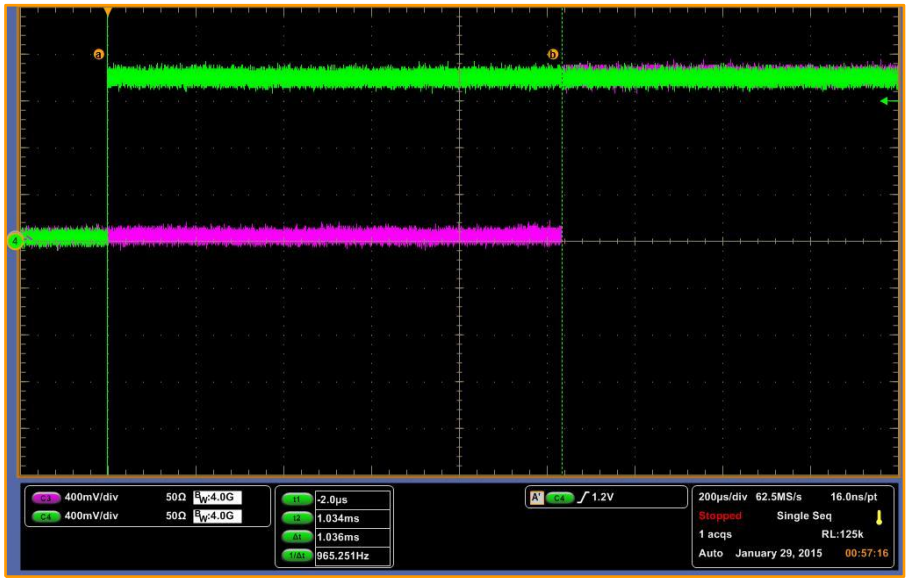


CH3: Reset

Parameter	Voltage	Spec	Result	Remark
Reset Low Level Voltage	175mV	Max:300mV	PASS	Reset Low Level Voltage must be within 300 mV.

Reset Initialization Sequence Check Result

▣ /Reset Up To CKE Up



CH3:CKE
CH4:Reset

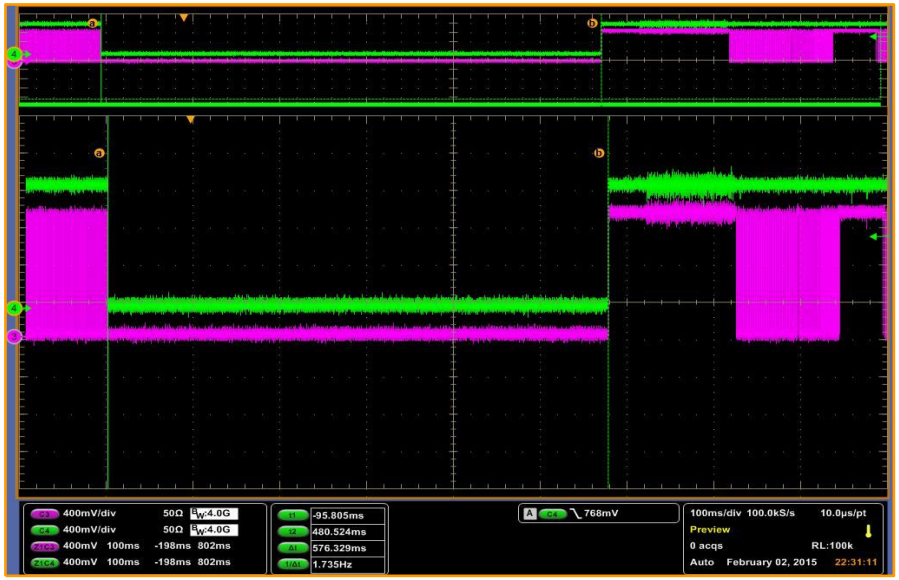
▣tCKSRX

CH1:CLK
CH3:CKE

Parameter	Time	Spec	Result	Remark
/Reset Up To CKE Up	1.036ms	Min:500us	PASS	After /RESET is de-asserted. Wait for another 500us until CKE becomes active.(JEDEC spec.)
tCKSRX	1.048ms	Min:Max(5 tCK,10ns)	PASS	Clocks (CK, CK#) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active.(JEDEC spec.)

Reset Initialization Sequence Check Result

- **CKE Falling Edge To Reset Rising Edge**



CH3:CKE
CH4:Reset

Parameter	Time	Spec	Result	Remark
CKE Falling Edge To Reset Rising Edge	576.3ms	Min:10ns	PASS	CKE is pulled “Low” anytime before RESET# being de-asserted (min. time 10 ns).

Average Periodic Refresh Interval Check Result

SPEC

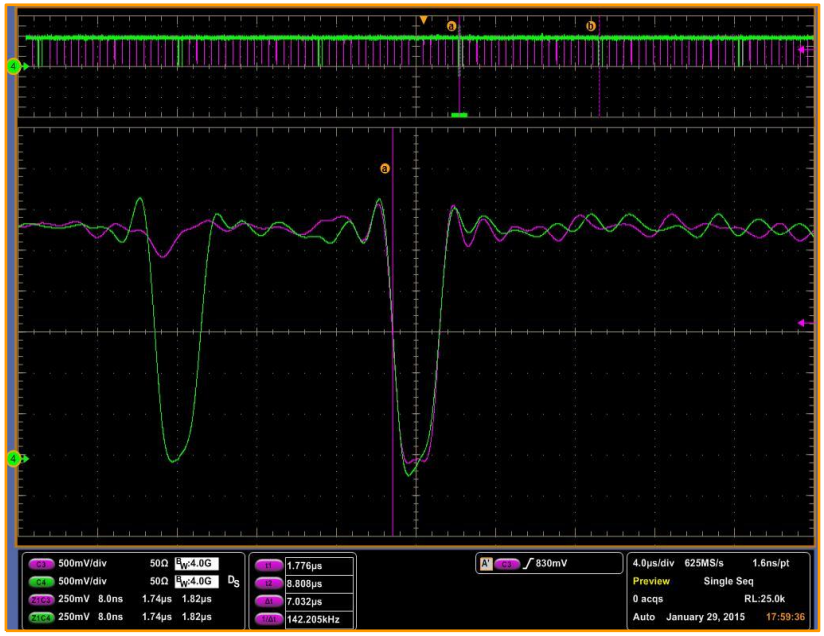
12.2 Refresh parameters by device density

Table 61 — Refresh parameters by device density

Parameter	Symbol		512Mb	1Gb	2Gb	4Gb	8Gb	Units	Notes
REF command to ACT or REF command time	tRFC		90	110	160	300	350	ns	
Average periodic refresh interval	tREFI	0 °C ≤ T_{CASE} ≤ 85 °C	7.8	7.8	7.8	7.8	7.8	µs	
		85 °C < T_{CASE} ≤ 95 °C	3.9	3.9	3.9	3.9	3.9	µs	1

NOTE 1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material.

Average Periodic Refresh Interval



CH3:CAS#
CH4:RAS#

Parameter	Time	Spec	Result	Remark
tREFI	7.03us	Max: 7.8us	PASS	

Power Check Result

Power Noise Check Result

Parameter	Spec（mV）Vpp	Value（mV）Vpp	Result	Position	Test Point
VDD_DDR	60*	16.8	-	Hi3516A	C11
VDDIO_DDR	75*	41.6	-	Hi3516A	C42
		44.8	-	Hi3516A	C51
Vref-CA	30	24.32	PASS	DDR1	C87
		13.76	PASS	DDR2	C90
Vref-DQ	30	18.24	PASS	DDR1	C88
		15.36	PASS	DDR2	C89

*** Note: The SPEC for VDD_DDR and VDDIO_DDR in the preceding table indicates the power supply requirement for Hi3516A board design.**

VDDIO Supply Voltage

Parameter	Spec	Value	Result	Position	Test Point
VDDIO	1.425V~ 1.575V	1.490 V	PASS	Hi3516A	C108
		1.488 V	PASS	DDR1	C135
		1.489 V	PASS	DDR2	C134

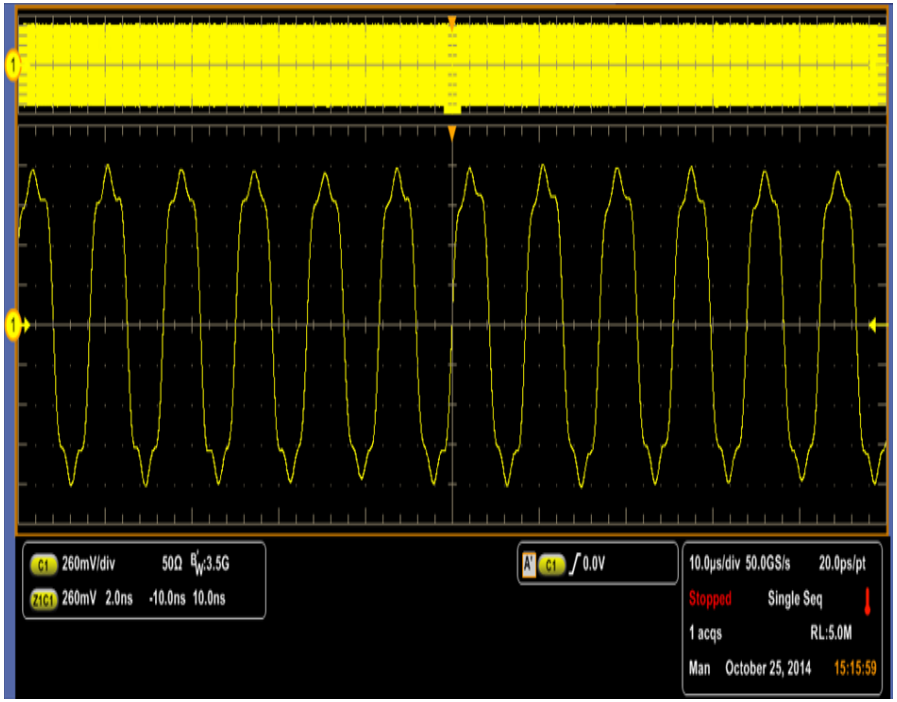
Signal Integrity Test Result (Clock)

Clock0 Signal Integrity Test Result

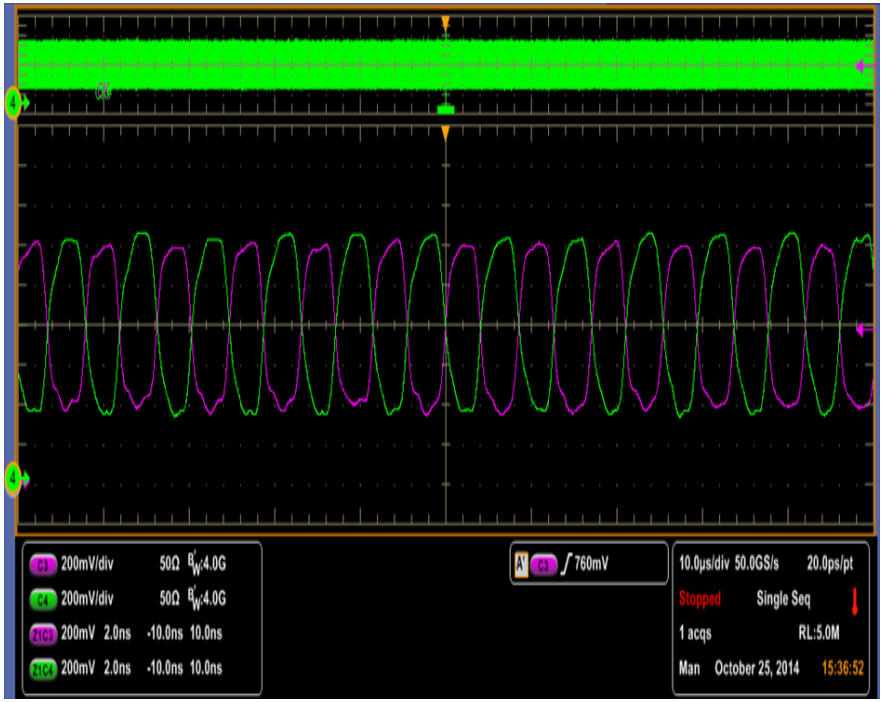
Parameter	Spec(Min)	Spec(Max)	Measurement data(Min)	Measurement data(Max)	Unit	Result
Vix	-150	150	-67.33	90.94	mV	PASS
tCK(avg)	1.64	1.8	1.6827	1.6842	Ns	PASS
tCH(avg)	470	530	511.80	513.27	mtCK(avg)	PASS
tCL(avg)	470	530	486.73	488.20	mtCK(avg)	PASS
tJIT(per)	-85	85	-82.57	79.38	ps	Marginal value The margin of the timing windows is sufficient, and no exception occurs in the reliability test. Risks are controllable.
tJIT(cc)	-170	170	-79.58	79.43	ps	PASS

Signal Integrity Test Result (Clock)

- CLK0 With Differential Measurement



- CLK0 Vix With High Voltage Trigger



Signal Integrity Test Result (Clock)

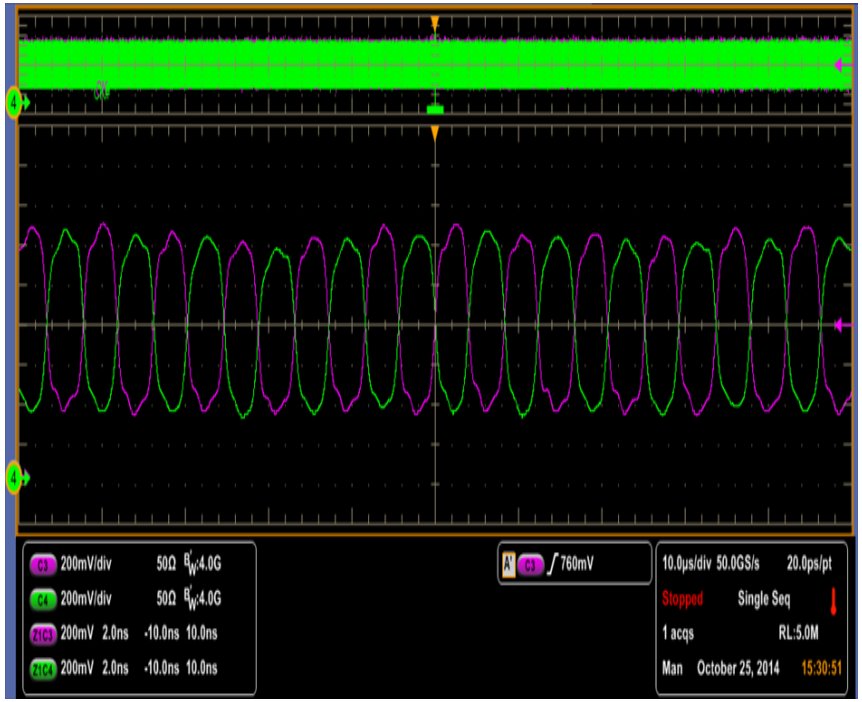
Clock1 Signal Integrity Test Result

Parameter	Spec(Min)	Spec(Max)	Measurement data(Min)	Measurement data(Max)	Unit	Result
Vix	-150	150	-75.33	138	mV	PASS
tCK(avg)	1.64	1.8	1.6829	1.6842	ns	PASS
tCH(avg)	470	530	478.34	480.33	mtCK(avg)	PASS
tCL(avg)	470	530	519.63	521.66	mtCK(avg)	PASS
tJIT(per)	-85	85	-76.23	75.07	ps	PASS
tJIT(cc)	-170	170	-79.25	78.48	ps	PASS

Signal Integrity Test Result (Clock)

- CLK1 With Differential Measurement

- CLK1 Vix With High Voltage Trigger



Signal Integrity Test Result (CMD&ADDR)

- **SPEC**

Table 70 — ADD/CMD Setup and Hold Base-Values for 1V/ns

Symbol	Reference	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Units
tIS(base) AC175	$V_{IH/L(ac)}$	200	125	65	45	-	-	ps
tIS(base) AC150	$V_{IH/L(ac)}$	350	275	190	170	-	-	ps
tIS(base) AC135	$V_{IH/L(ac)}$	-	-	-	-	65	60	ps
tIS(base) AC125	$V_{IH/L(ac)}$	-	-	-	-	150	135	ps
tIH(base) DC100	$V_{IH/L(dc)}$	275	200	140	120	100	95	ps

ΔtIS, ΔtIH derating in [ps] AC/DC based
Alternate AC150 Threshold -> VIH(ac)=VREF(dc)+150mV, VIL(ac)=VREF(dc)-150mV

		CK,CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ ADD Slew rate V/ns	2.0	75	50	75	50	75	50	83	58	91	66	99	74	107	84	115	100
	1.5	50	34	50	34	50	34	58	42	66	50	74	58	82	68	90	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	0	-4	0	-4	0	-4	8	4	16	12	24	20	32	30	40	46
	0.8	0	-10	0	-10	0	-10	8	-2	16	6	24	14	32	24	40	40
	0.7	0	-16	0	-16	0	-16	8	-8	16	0	24	8	32	18	40	34
	0.6	-1	-26	-1	-26	-1	-26	7	-18	15	-10	23	-2	31	8	39	24
	0.5	-10	-40	-10	-40	-10	-40	-2	-32	6	-24	14	-16	22	-6	30	10
	0.4	-25	-60	-25	-60	-25	-60	-17	-52	-9	-44	-1	-36	7	-26	15	-10

Signal Integrity Test Result (CMD&ADDR)

- **1T Command Signal Integrity Test Result**

CMD /ADD	Input SetupTime (tIS)@AC150 tIS(min)	Input Hold Time (tIH)@DC100 tIH(min)	Units	Remaik
Spec	265	190	ps	
CLK0_CS0N	798.99	609.97	ps	PASS
CLK0_ODT0	871.24	635.77	ps	PASS
CLK0_CKE	761.09	693.22	ps	PASS
CLK1_CS1N	801.34	587.02	ps	PASS
CLK1_ODT1	784.91	635.06	ps	PASS
CLK1_CKE	791.11	647.22	ps	PASS

Signal Integrity Test Result (CMD&ADDR)

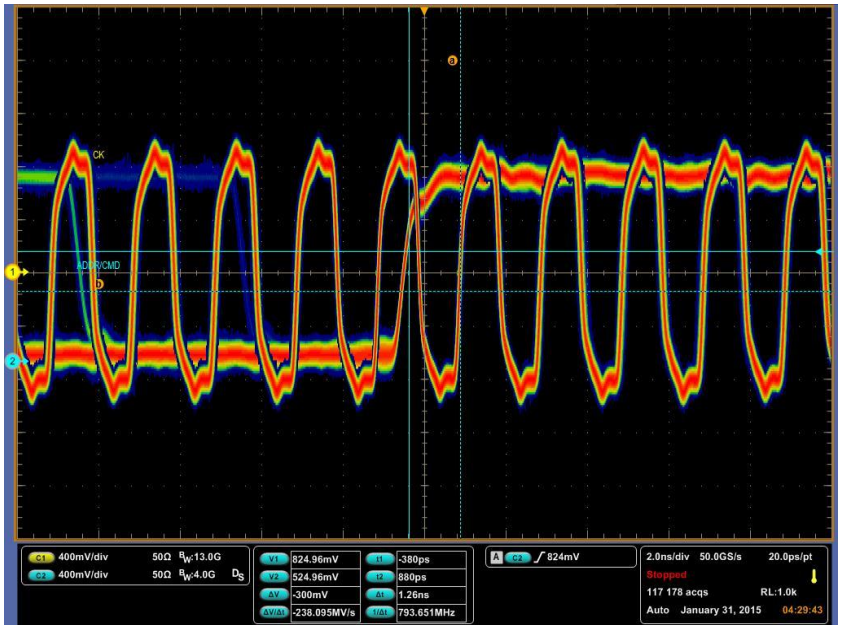
- **1T_CSN Wave**

CLK0_CS

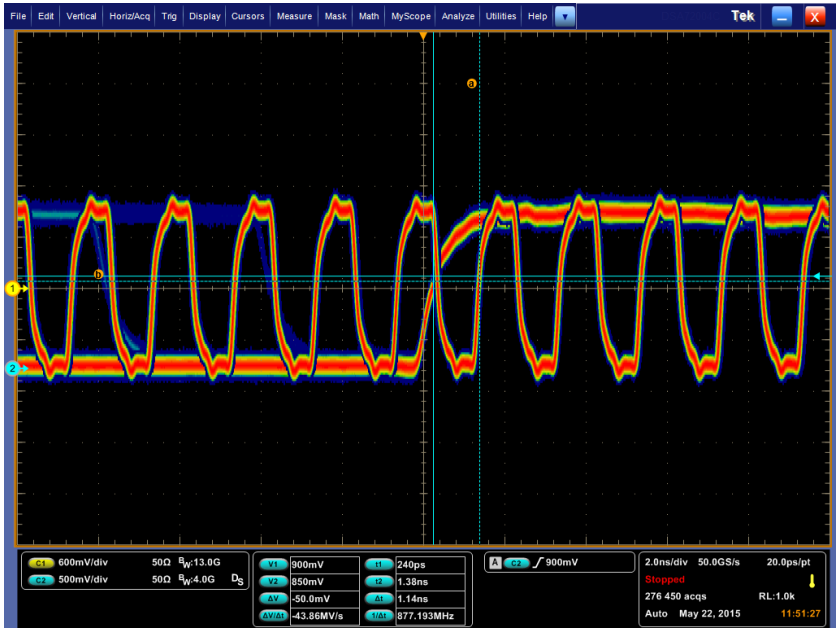
CLK1_CS

Signal Integrity Test Result (CMD&ADDR)

- **1T_ODT Wave**



CLK0_ODT

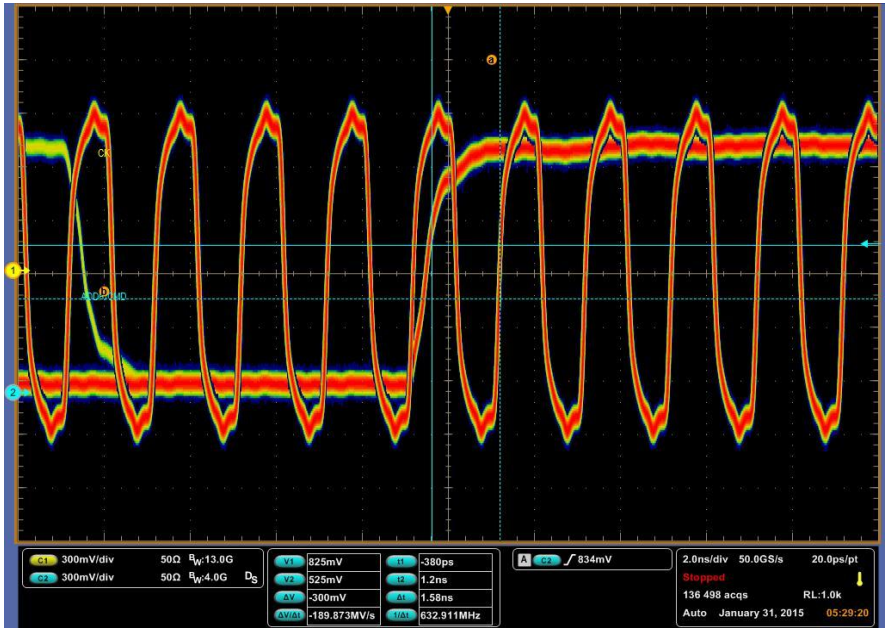


CLK1_ODT

Signal Integrity Test Result (CMD&ADDR)

- **1T_CKE Wave**

CLK0_CKE



CLK1_CKE

Signal Integrity Test Result (CMD&ADDR)

- 2T_A7 Wave

- 2T_CAS Wave

Signal Integrity Test Result (DATA)

- **SPEC**

Table 76 — Data Setup and Hold Base-Values

Symbol	Reference	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Units	Notes
tDS(base) AC175	$V_{IH/L(ac)}$ SR=1V/ns	75	25	-	-	-	-	ps	2
tDS(base) AC150	$V_{IH/L(ac)}$ SR=1V/ns	125	75	30	10	-	-	ps	2
tDS(base) AC135	$V_{IH/L(ac)}$ SR=1V/ns	165	115	60	40			ps	2, 3
tDS(base) AC135	$V_{IH/L(ac)}$ SR=2V/ns	-	-	-	-	68	53	ps	1
tDH(base) DC100	$V_{IH/L(dc)}$ SR=1V/ns	150	100	65	45	-	-	ps	2
tDH(base)DC100	$V_{IH/L(dc)}$ SR=2V/ns					70	55	ps	1

NOTE 1. (ac/dc referenced for 2V/ns DQ-slew rate and 4V/ns DQS slew rate)
NOTE 2. (ac/dc referenced for 1V/ns DQ-slew rate and 2V/ns DQS slew rate)
NOTE 3. Optional in DDR3 SDRAM

Table 78 — Derating values for DDR3-800/1066/1333/1600 tDS/tDH - (AC150)Derating

ΔtDS, ΔDH derating in [ps] AC/DC based[1]																	
		DQS, DQS# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	75	50	75	50	75	50	-	-	-	-	-	-	-	-	-	-
	1.5	50	34	50	34	50	34	58	42	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	0	-4	0	-4	8	4	16	12	24	20	-	-	-	-
	0.8	-	-	-	-	0	-10	8	-2	16	6	24	14	32	24	-	-
	0.7	-	-	-	-	-	-	8	-8	16	0	24	8	32	18	40	34
	0.6	-	-	-	-	-	-	-	-	15	-10	23	-2	31	8	39	24
	0.5	-	-	-	-	-	-	-	-	-	-	14	-16	22	-6	30	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	7	-26	15	-10

NOTE 1. Cell contents shaded in red are defined as ‘not supported’.

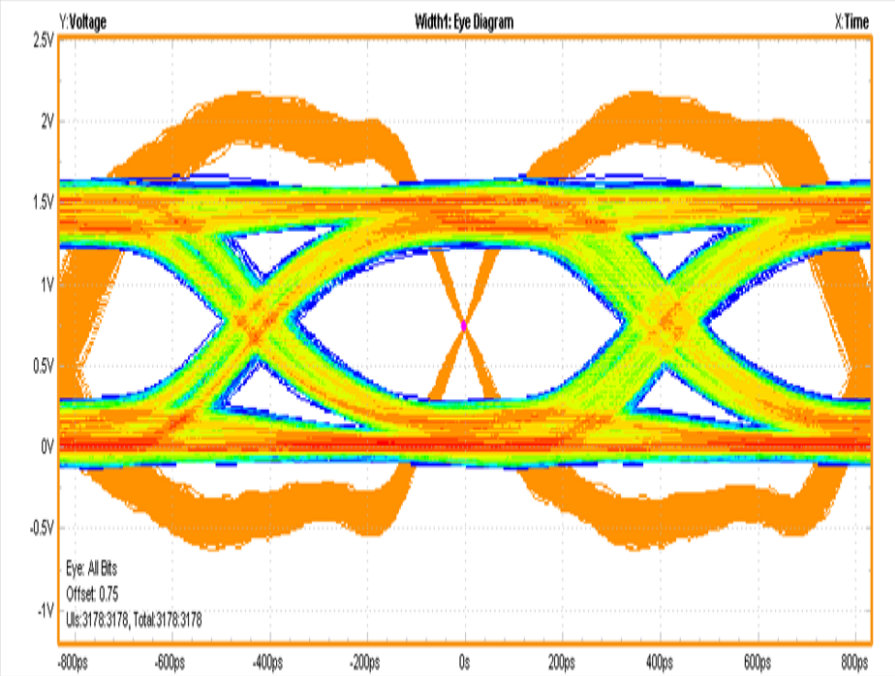
Signal Integrity Test Result (DATA)

Data Signal Integrity Test Result

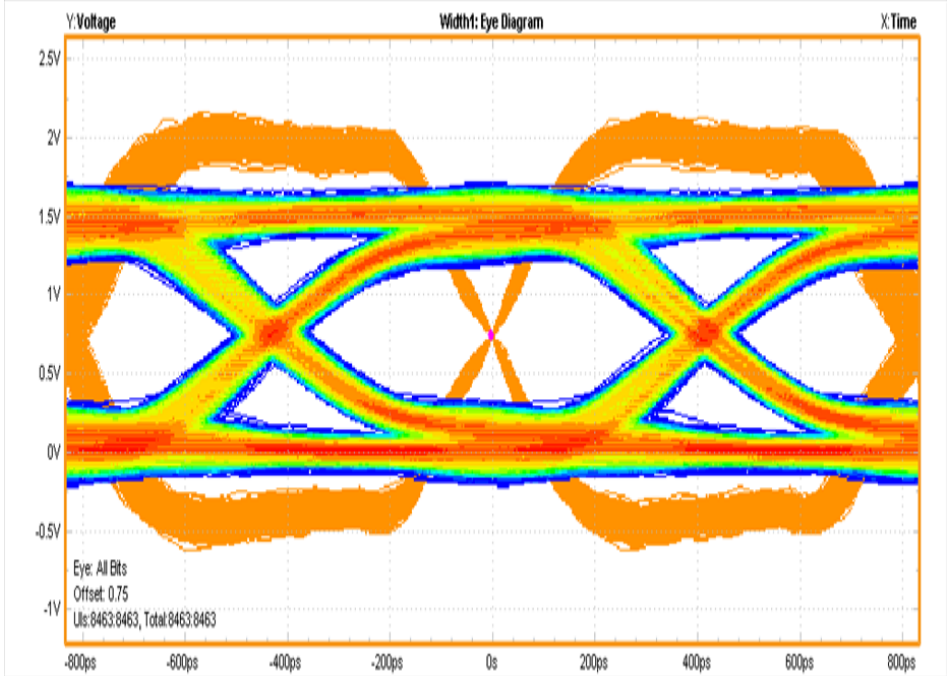
Parameter			Spec	DQ3	DQ10	DQ22	DQ28	Unit	Result
Data	Write	Input Setup-Time(tDS)@AC150 [tDS(base)=30ps]	min:105	273.71	290.84	248.22	226.51	ps	PASS
		Input Hold-Time(tDH)@DC100 [tDH(base)=65ps]	min:115	279.22	291.51	319.94	321.60	ps	PASS

Signal Integrity Test Result (DATA)

- DQ3_write

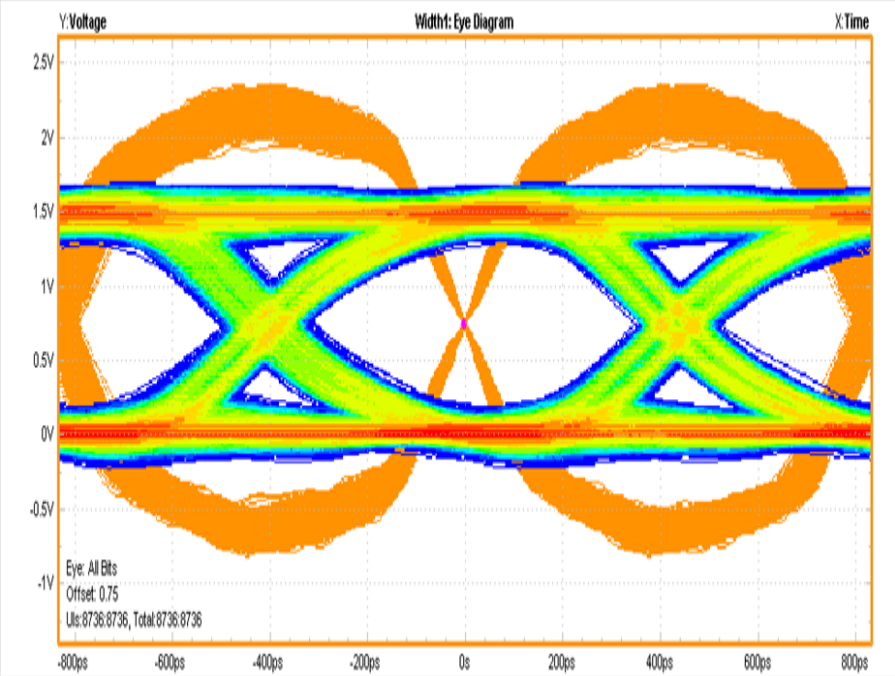


- DQ10_write

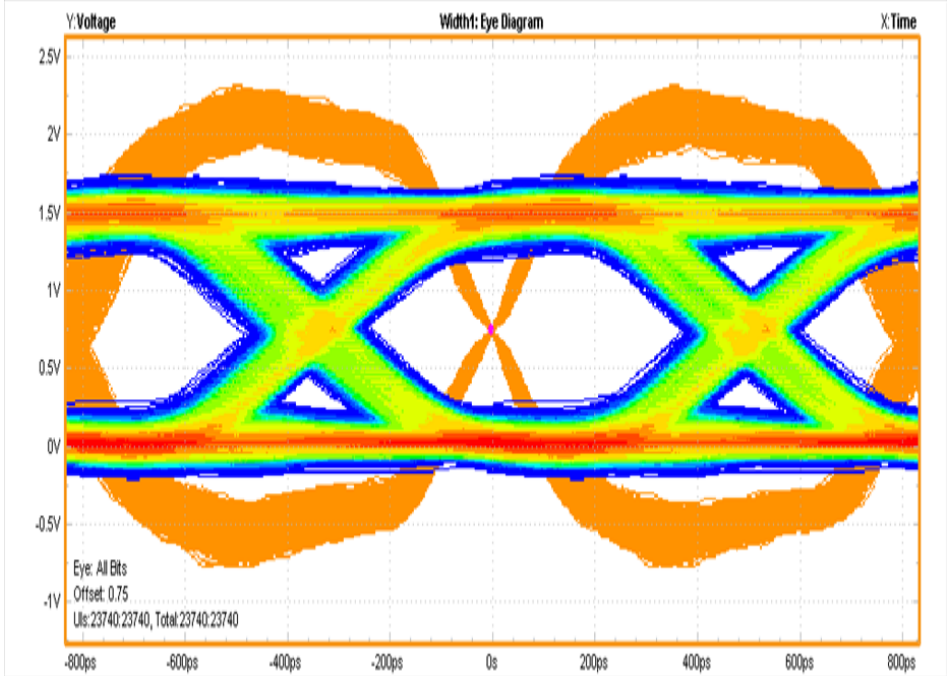


Signal Integrity Test Result (DATA)

- DQ22_write



- DQ28_write



DDR Training Window

- **DDR Training-write window**

```
## DDR training terminated.
Boot Training result. The write window of prebit-deskew
--------------------------------------------------------------------------------
DQ  0  1  2  3  4  5  6  7  8  9  10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31  HEX_VALUE     DQphDQ  WIN
0   X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  X  X   0x3ffffffe    11  15  29
1   X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xfffffffc    11  17  30
2   X  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  X  X   0x7ffffff8    11  17  28
3   X  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  X  X   0x7ffffff8    11  17  28
4   X  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  X  X   0x3ffffff8    11  16  27
5   X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  X  X   0x3ffffffc    11  16  28
6   X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  X   0x7ffffffe    11  16  30
7   X  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  X   0x7ffffff8    11  17  28
8   X  X  X  X  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xfffffffc0   10  19  26
9   X  X  X  X  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xfffffffc0   10  19  26
10  X  X  X  X  X  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xffffff80    10  19  25
11  X  X  X  X  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xfffffffc0   10  19  26
12  X  X  X  X  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xfffffffc0   10  19  26
13  X  X  X  X  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xfffffffc0   10  19  26
14  X  X  X  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xfffffffe0   10  18  27
15  X  X  X  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xfffffffe0   10  18  27
16  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xfffffffc    11  17  30
17  X  X  X  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xfffffffe0   11  18  27
18  X  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xfffffff8    11  17  29
19  X  X  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xfffffff0    11  18  28
20  X  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xfffffff8    11  17  29
21  X  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xfffffff8    11  17  29
22  X  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xfffffff8    11  17  29
23  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xfffffffc    11  17  30
24  X  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  X   0x7ffffff8    11  17  28
25  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xfffffffc    11  17  30
26  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  X   0x7ffffffe    11  16  30
27  X  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xfffffff8    11  17  29
28  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xfffffffc    11  17  30
29  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  X   0x7ffffffc    11  16  29
30  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xfffffffc    11  17  30
31  X  X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -   0xfffffffc    11  17  30
--------------------------------------------------------------------------------
```

DDR Training Window

- **DDR Training-read window**

Boot Training result.The read window of prebit-deskew

DQ	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	HEX_VALUE	DQS	DQ	WIN
0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	X	X	0x3ffffff	27	13	26
1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	0xfffffff	27	14	28
2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	0x1fffffff	27	14	29
3	X	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	0x7ffffffe	27	16	30
4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	0xfffffff	27	14	28
5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	X	0x7ffffff	27	13	27
6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	X	0x7ffffff	27	13	27
7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	0x1fffffff	27	14	29
8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	X	0x7ffffff	29	13	27
9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	X	X	X	0x1ffffff	29	12	25
10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	0xfffffff	29	14	28
11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	X	X	X	0x1ffffff	29	12	25
12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	X	X	X	0x1ffffff	29	12	25
13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	X	X	X	0x1ffffff	29	12	25
14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	X	X	0x3ffffff	29	13	26
15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	X	X	X	0x1ffffff	29	12	25
16	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	X	0x7ffffff	27	13	27
17	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	0xfffffff	27	14	28
18	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	0x1fffffff	27	14	29
19	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0xffffffff	27	16	32
20	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	X	0x7ffffff	27	13	27
21	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	X	0x7ffffff	27	13	27
22	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	0x1fffffff	27	14	29
23	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	0x1fffffff	27	14	29
24	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	X	X	X	0x1ffffff	28	12	25
25	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	X	0x7ffffff	28	13	27
26	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	X	X	X	0x1ffffff	28	12	25
27	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	X	0x7ffffff	28	13	27
28	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	0x1fffffff	28	14	29
29	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	0xfffffff	28	14	28
30	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	0x1fffffff	28	14	29
31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	0x1fffffff	28	14	29

Thank you